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Epitaxial graphene on SiC formed by the surface structure control technique

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The thermal decomposition of silicon carbide (SiC) is a promising method for producing wafer-scale single-crystal graphene. The optimal growth condition for high-mobility epitaxial graphene fabricated by infrared rapid thermal annealing is discussed in this paper. The surface structures, such as step-terrace and graphene coverage structures, on a non-off-axis SiC(0001) substrate were well controlled by varying the annealing time in a range below 10 min. The mobility of graphene grown at 1620 ºC for 5 min in 100 Torr Ar ambient had a maximum value of 2089 $cm^2V^{-1}s^{-1}$. We found that the causes of the mobility reduction were low graphene coverage, high sheet carrier density, and nonuniformity of the step structure.

1. Introduction

Graphene is a two-dimensional carbon crystal that has attracted considerable attention owing to its excellent electrical[1, 2] and mechanical properties.[3, 4] In particular, owing to its very high carrier mobility, which has been reported to exceed 200,000 $cm^2V^{-1}s^{-1}$,[5] it is expected to be applied as a post-silicon material. The most popular graphene fabrication method is mechanical exfoliation.[1, 2] Although the quality of exfoliated graphene is high, its sample size is very small for practical applications. The chemical vapor deposition (CVD) method[6-9] can be used to synthesize large-area graphene, but it yields polycrystal graphene, the grain size of which is similar to that of exfoliated graphene. In addition, these methods principally require complex film transfer processes in which the graphene quality markedly degrades.[10, 11] The thermal decomposition of SiC[12-17] is the most promising method of growing wafer-scale single-crystal graphene.[17] Furthermore, this method does not require the transfer processes when a semi-insulative substrate is used.[18] Graphene on a SiC substrate is expected to be applied as a platform of future electronic devices.[19-21)]

The growth mechanism of graphene grown by the thermal decomposition of SiC has been discussed in previous studies through analyses using scanning probe microscopy (SPM)[22-25] and low-energy electron microscopy (LEEM).[23-28] However, the detailed growth mechanism remains unclear. Surface structures continuously change in the SiC decomposition process because three bilayers of the SiC substrate are required to grow one atomic layer of graphene. Because step edges are a major source of carbon atoms,[29] the conformation of surface steps will be an important factor in epitaxial graphene growth. It is known that the graphene grown in Ar ambient exhibits an almost atomic layer thickness.[23] The graphene in the terrace region can be controlled to exhibit a monolayer thickness because of its self-limiting growth mechanism. On the other hand, additional graphene layers preferentially grow from the step edge.[25] This unintentional graphene growth at the step edge is the main cause of nonuniform growth. In this study, we attempt to prevent this unintentional growth to realize highly uniform epitaxial graphene with high mobility. To control the surface structure of graphene on a SiC substrate, the infrared rapid thermal annealing (RTA) method is used. To prevent step bunching before the graphene growth stage, the sample temperature is immediately increased to the target

temperature for the thermal decomposition of SiC. Initially, the SiC substrate surface is atomically flat because it is polished by chemical mechanical polishing (CMP). The surface morphology might be kept flat up to the SiC decomposition temperature for preventing the unintentional graphene growth. The infrared RTA method is found to be suitable for this purpose. The RTA system can precisely control the temperature by rapidly increasing the temperature. The surface structure and electrical properties were measured after graphene growth. Furthermore, we discuss the annealing conditions for obtaining uniform, high-quality graphene.

2. Experimental procedure

4H-SiC(0001) non-off-axis semi-insulating substrates (Cree) diced to square pieces with 10 mm^2 size were used. The sample was cleaned using a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). Then, the surface oxide layer was removed using dilute hydrofluoric acid (HF). The epitaxially grown graphene layers were annealed at high temperatures in an Ar environment (100 Torr) by using a super-RTA system, SR1800 (THERMO RIKO). Figure 1 shows the annealing procedure for this experiment. The samples were annealed from room temperature to 1200 ºC in 5 min. The temperature was kept for 1 min at 1200 ºC for degassing. The temperature of the samples was rapidly increased to the target temperature to prevent any change in surface morphology. The samples were maintained at the target temperature (1600 – 1700 ºC) for various annealing times of 0–10 min. The number of graphene layers was determined using SPM images taken using SPA400 (SII-NT). The mobilities and sheet carrier densities were measured by the van der Pauw method using a homemade device. The gold-plated spring loaded pins put on the four corners of the square sample. The applied magnetic field had a strength of 261 mT.

3. Results and discussion

3.1 Time dependence

Figures 2(a)-2(f) show SPM images of graphene on SiC annealed at 1600 ºC for various annealing times. Figures 2(a) and 2(b) show SPM images at 0 min. The topographic image

in Fig. 2(a) shows the surface structure. Bright domains (plateau-like structures) are observed on the terrace. The plateaus that correspond to the buffer layer ($6\sqrt{3} \times 6\sqrt{3}$ structure) are observed as the dark domains in the phase image [Fig. 2(b)]. The bright area in Fig. 2(b) is the monolayer-graphene region. Figures 2(c) and 2(d) show the topographic and phase images of the sample annealed at 5 min, respectively. The plateau structures on terraces are shown in Fig. 2(c). The phase image [Fig. 2(d)] shows that the sample surface is completely covered with monolayer graphene. The surface of the sample annealed at 10 min is shown in Figs. 2(e) and 2(f). A bilayer region was observed with a slightly dark contrast, as shown in Fig. 2(f). Because of the longer annealing time, the proceeding of step bunching results in bilayer regions.

Figure 3 shows the annealing time dependence of the effective graphene thickness of the sample annealed at 1600 ºC. The effective thickness was calculated using the area ratio of the contrast of SPM phase images. Monolayer and bilayer graphene and the buffer layer were easily identified by the phase contrast, as previously discussed. With an annealing time of 0 min, the effective thickness was 0.82 layers. This result indicates that 0.82 layers of graphene and a buffer monolayer were grown in a very short time (less than 1 min) in the temperature range of 1200 to 1600 ºC. The sample surface is not completely covered with graphene, because buffer layer domains, which are shown in Fig. 2(b) as dark contrasts, exist on the surface. The effective thickness monotonically increases with annealing time. At 5 min, the effective thickness reaches one monolayer. A longer annealing time of 10 min results in a slightly thicker graphene layer with a thickness of 1.03 layers. In this time range (1–10 min), the estimated graphene growth rate at 1600 ºC is 0.01 layer/min. The time dependence results show that the growth of the graphene layer started before reaching the target temperature of 1600 ºC. In the annealing procedure, the process temperature measured using the infrared thermometer was strictly controlled with an accuracy of 3 ºC, as shown in Fig. 1. With an annealing time of 0 min, the surface temperature of a sample should be slightly lower than the process temperature because the infrared thermometer can measure the temperature of a carbon susceptor. This is the main cause of the large amount of buffer layer in Figs. 2(a) and (b).

Figure 4 shows the annealing time dependences (0–10 min) of the mobility and sheet carrier density of epitaxial graphene annealed at 1600 ºC. The mobility of the sample grown with an annealing time of 0 min is 388 $cm^2V^{-1}s^{-1}$, and the mobility increases with

annealing time. The time dependence of the mobility has a maximum (1310 $cm^2V^{-1}s^{-1}$) at 3 min. The mobility decreases with further increase in annealing time. The sheet-carrier density shown in Fig. 3 monotonically increases with annealing time. In the short-annealing-time regime, the mobility is strongly affected by graphene coverage. With longer annealing times, a high carrier density reduces the carrier mobility.

3.2 Temperature dependence

Figure 5(a)-5(f) show SPM images of the sample annealed for 5 min at various temperatures. Figures 5(a) and 5(b) show the surface structure annealed at 1600 ºC. A step-terrace structure is observed in the topographic image [Fig. 5(a)]. The bright and dark regions are confirmed in the phase image [Fig. 5(b)]. Monolayer graphene and the buffer layer are shown as the bright and dark domains, respectively. The buffer layer exists locally on the terrace; therefore, it is not completely grown. Figures 5(c) and 5(d) show the topographic and phase images at 1620 ºC. Bright domains corresponding to the buffer layer disappeared from the terrace in the topographic image. The phase image [(Fig. 5(d))] shows that the entire surface is covered with monolayer graphene. Figures 5(e) and 5(f) show the sample surface for growth at 1650 ºC. In the phase image [Fig. 5(f)], the sample surface is covered with monolayer graphene, which is similar to the case of the sample grown at 1620 ºC. The difference between the two samples (annealed at 1620 and 1650 ºC) is in the average step height. The step bunching of SiC proceeded at a higher temperature, and terrace regions are divided by step edges, as shown in Fig. 5(f). The topographic and phase images of graphene on SiC for growth at 1700 ºC are shown in Figs. 5(g) and 5(h), respectively. Bilayer graphene is identified by the dark regions in the phase image [Fig. 5(h)]. The effective graphene thickness for annealing at 1700 ºC for 5 min is 1.01.

Figure 6 shows the dependence of electrical properties on the annealing temperature obtained using the van der Pauw method. The mobility and sheet carrier density have maxima at 1706 $cm^2V^{-1}s^{-1}$ and 1.98×10^{12} cm^{-2}, respectively, for annealing at 1620 ºC. It is well known that a low carrier density gives a high mobility. The relationship between mobility and carrier density will be discussed later. The surface structure affected the electrical properties of graphene on SiC because of the temperature dependence. Buffer

regions locally remained on the terrace when the annealing temperature was 1600 ºC. Because the effective thickness of the sample annealed at 1620 ºC was 1.03, an increase in effective thickness by 0.04 layers increased the mobility by 34 %. The surfaces of samples with growth temperatures ranging from 1620 to 1650 ºC were covered with monolayer graphene. The step bunching had a great impact on the mobility. The mobility was reduced by step-edge-divided terrace regions.[30] Epitaxial graphene was usually electron-doped[31, 32] because electrons were induced by Si atoms through the dangling bond of SiC.[33] The sheet carrier density of the sample annealed at 1620 ºC decreased by 41 % compared with that of the sample grown at 1600 ºC. We suppose that the mobility increased because the sheet carrier density was reduced by decreasing the dangling bond density under the optimal growth condition. Figure 7 shows the sheet carrier density as a function of the average step height. The sheet carrier density linearly increased with step height. Figure 8 shows the mobility as a function of the sheet carrier density. The theoretical curve was used as the Einstein relation in a previous study.[34] The measurement data correspond to this relationship. These results suggest that the carrier density of epitaxially grown graphene is dominated by the surface morphology of the SiC substrate. Then, the mobility of graphene on SiC is determined. The mobility of the sample grown at 1620 ºC for 5 min [Fig. 5(c) and 5(d)] has a maximum of 2089 $cm^2V^{-1}s^{-1}$. The high mobility could be realized by controlling the surface structure. Thus, we successfully established the optimal growth condition for high-quality, uniform monolayer graphene. After fabricating devices with graphene on SiC, a high mobility can be obtained by controlling sheet carrier density.[35] The fabrication of uniform, high-quality graphene can be expected to improve device properties.

4. Conclusions

We revealed that the surface structures of graphene on SiC can be precisely controlled under RTA conditions. To determine the time dependence, the annealing time was varied in the range of 0–10 min at 1600 ºC. The mobility showed a maximum at an annealing time of 3 min. The mobility decreased with further increase in annealing time. To determine the temperature dependence, the samples were annealed at 1600–1700 ºC with an annealing time of 5 min. The mobility showed a maximum at 1620 ºC. Under the

optimal annealing condition (1620 ºC, 5 min), monolayer graphene covered the entire sample surface, and the step-terrace structure was not divided. Thus, we successfully optimized the annealing conditions for obtaining high-quality single-crystal graphene. The proposed fabrication method will contribute to improving device properties.

Acknowledgment

This work was partially supported by JSPS KAKENHI Grant Numbers 26289107 and 15H03551.

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Figure Captions

Fig. 1. (Color online) Annealing procedure.

Fig. 2. (Color online) SPM images of graphene grown at 1600 ºC. Annealing time in (a) and (b) is 0 min. Annealing time in (c) and (d) is 5 min. Annealing time in (e) and (f) is 10 min.(a), (c), and (e) show topographic images. (b), (d), and (f) show phase images.

Fig. 3. (Color online) Effective thickness vs annealing time (annealing temperature: 1600 ºC).

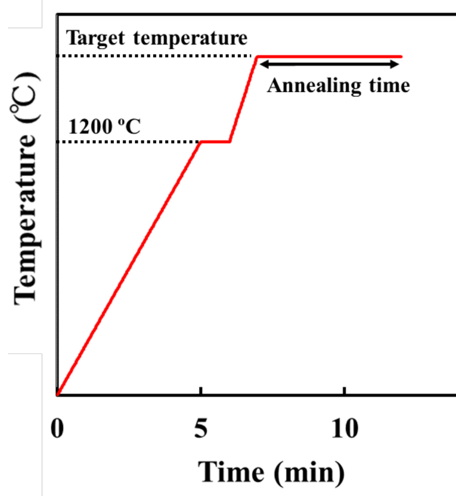
Fig. 4. (Color online) Annealing time dependences of mobility and sheet carrier density.

Fig. 5. (Color online) SPM images of graphene grown with annealing for 5 min. Annealing temperature in (a) and (b) is 1600 ºC. Annealing temperature in (c) and (d) is 1620 ºC. Annealing temperature in (e) and (f) is 1650 ºC. Annealing temperature in (g) and (h) is 1700 ºC. (a), (c), (e) and (g) show topographic images. (b), (d), (f) and (h) show phase images.

Fig. 6. (Color online) Annealing temperature dependences of mobility and sheet carrier density.

Fig. 7. (Color online) Sheet carrier density vs average step height.

Fig. 8. (Color online) Mobility vs sheet carrier density.



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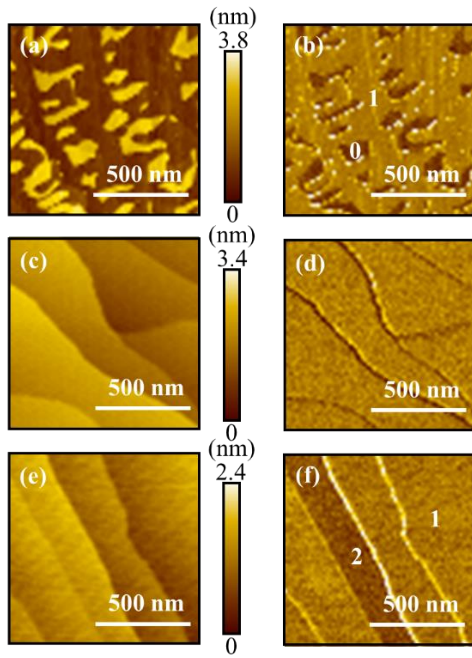

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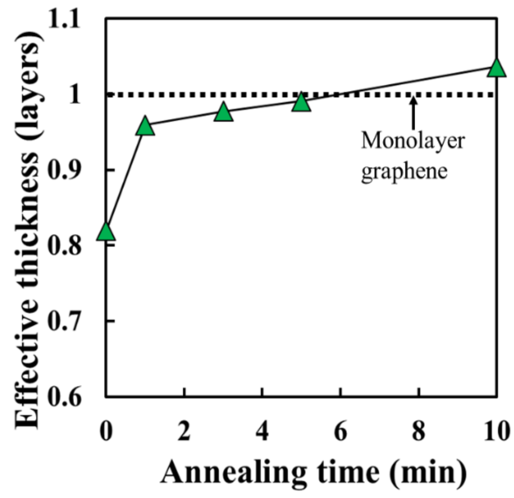

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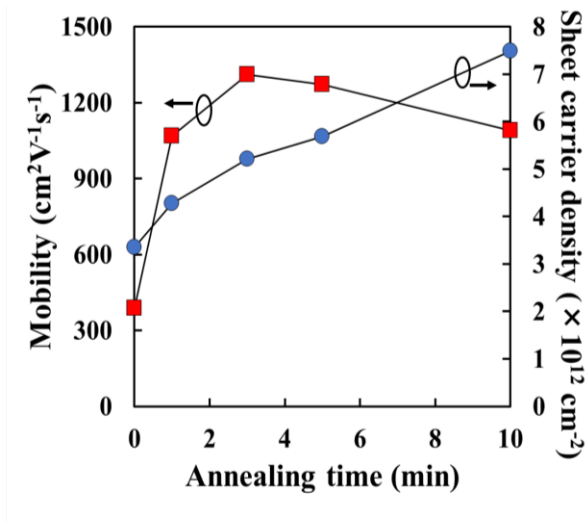

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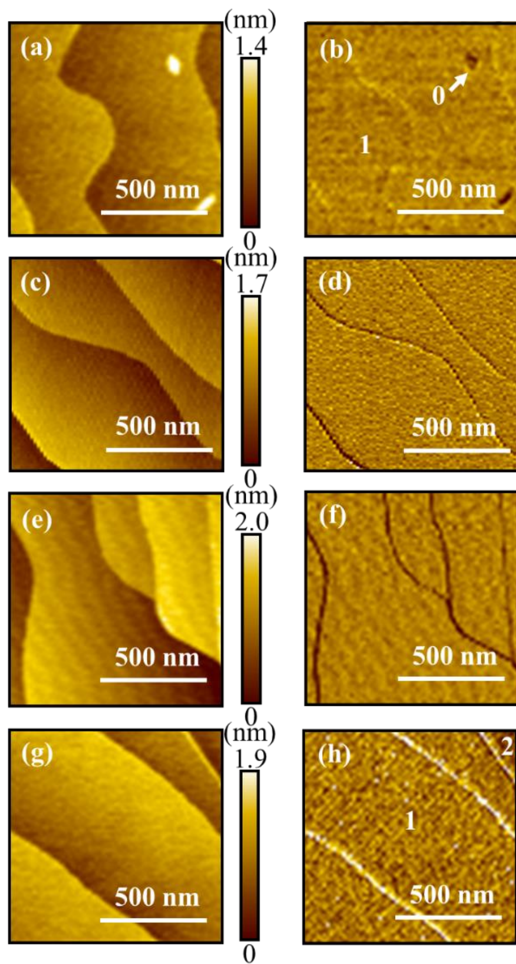

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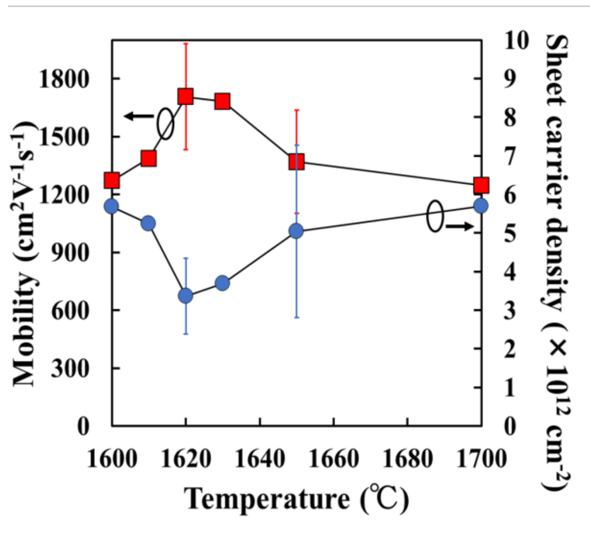

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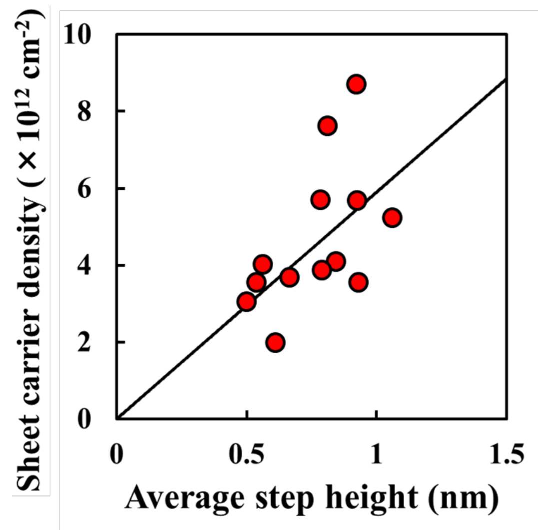

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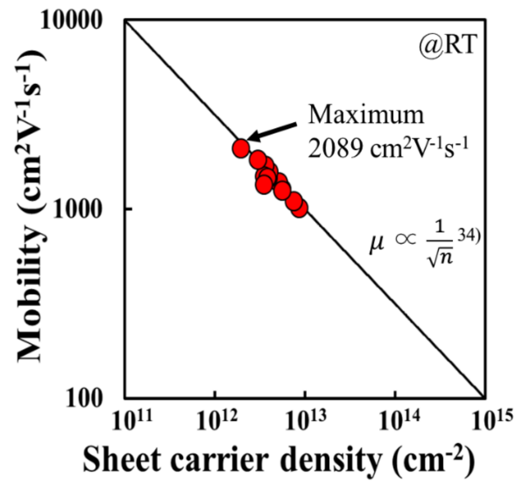

Fig. 8. (Color online)