論 文 の 内 容 の 要 旨

論文題目　Study on La_2O_3/InGaAs MOS interfaces and the application to InGaAs MOSFETs
(La_2O_3/InGaAs MOS界面とMOSFETへの応用に関する研究)

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InGaAs has been seen as one of promising III-V semiconductor material for fabricating high performance nMOSFET in the upcoming 5 nm node CMOS technology because of its light electron mass (0.0411 m_0) and high electron mobility (13800 cm^2/V-s). However, unlike conventional channel material Si, which can be easily passivated by SiO_2 to have good interface between channel and gate insulator, the sp^3 hybrid electron orbital of InGaAs make InGaAs difficult to be passivated such that there is always a large amount of interface states between InGaAs and gate insulator, which may degrade the subthreshold slope (*S. S.*) and the mobility in InGaAs MOSFET. The interface state density (D_{it}) of InGaAs MOS structures is usually larger than 10^{12} cm^{-2}-eV^{-1}, over an order larger than Si. Therefore, to reduce the interface state density is a critical issue to improve InGaAs MOSFET performance.

In this thesis, the improvement of InGaAs MOS interfaces by atomic-layer-deposited (ALD) La_2O_3 was studied. It is found that the La_2O_3 can have good passivation on InGaAs not only because it is a trivalent oxide, which has the same electron count with InGaAs, but the intermixing layer of As_2O_3 is formed between

La_2O_3 and InGaAs, which further reduces the D_{it}. The recorded-low D_{it} value on InGaAs of 3×10^{11} cm^{-2}-eV^{-1} was obtained in Au/ La_2O_3/InGaAs MOS capacitors.

In addition, in order to make use of the good interface of La_2O_3/InGaAs to fabricate InGaAs MOSFET, the impact of gate metal on La_2O_3/InGaAs MOS interfaces was also investigated. It is found that thinner capacitance equivalent thickness (CET) and less slow traps can be obtained by using W as gate metal on La_2O_3/InGaAs. The reaction of W on La_2O_3/InGaAs was analyzed by X-ray photoelectron spectroscopy (XPS). We found that the interfacial layer of As_2O_3 between La_2O_3 and InGaAs was reduced during PMA such that the CET was decreased but D_{it} was increased. The reaction is similar to the scavenging effect on high-k/Si MOS interfaces. For those advantages and process compatibility of W gate to La_2O_3/InGaAs, W can be seen as a good candidate for gate metal to fabricate La_2O_3/InGaAs MOSFET.

The energy distributions of slow traps density at W/La_2O_3/InGaAs MOS interfaces were also evaluated. By mearsuring the hysteresis with elaborately changing the range of V_g sweep in *C*-*V* measurement, we characterized the distributions of slow traps at W/La_2O_3/InGaAs MOS interfaces that more slow traps distributed from the midgap toward valence band and less distributed around conduction band edge in the InGaAs MOS band diagram. The distributions allow the performance of W/La_2O_3/InGaAs *n*MOSFET being less influenced by the slow traps because *n*MOSFET turns on while the position of Fermi lever is around conduction band edge.

Then the W/La_2O_3/InGaAs MOSFETs has been successfully fabricated. High-k/InGaAs MOSFET with small *S. S.* was realized by La_2O_3/InGaAs MOS interfaces due to its low D_{it}. Also, by the low D_{it} in La_2O_3/InGaAs MOS interfaces, the carriers transporting through the channel of La_2O_3/InGaAs MOSFET is more immune

from the carrier trapping, providing higher reliability of positive bias temperature instability (PBTI). The scattering effect on mobility of La_2O_3/InGaAs MOSFET was also elaborately analyzed by Hall mobility measurement. The overview of the applications of La_2O_3/InGaAs MOS interfaces to InGaAs MOSFET was given in this thesis.

In the end, we firstly found the ferroelectric-like characteristic in W/La_2O_3/InGaAs MOS structures. The ferroelectricity in W/La_2O_3/InGaAs MOS structures was examined by electrical analysis on the hysteresis in *C*-*V* measurement and *P*-*E* hysteresis loop. Due to the ferroelectric-like characteristic in W/La_2O_3/InGaAs MOS structures, W/La_2O_3/InGaAs MOSFET was found to be having negative capacitance FET (NCFET) properties. The prospects of utilizing W/La_2O_3/InGaAs MOSFET to realize steep slope transistor with subthreshold slope (*S. S.*) lower than 60 mV/dec were also discussed.

In this thesis, we clarified the physical origin of interface state on InGaAs and obtained the recorded-low D_{it} on InGaAs by ALD-La_2O_3. The InGaAs MOSFET with La_2O_3 as gate insulator has been successfully fabricated with elaborate analysis on the mobility, reliability and the slow traps distribution. On the other hand, a new functionality of ferroelectricity in W/La_2O_3/InGaAs MOS structures was firstly demonstrated. This research provides an insight into gate stacks technology on InGaAs for further improving the performance of InGaAs MOSFETs, and proposes a feasibility of realizing steep slope transistors by W/La_2O_3/InGaAs gate stacks we developed.