Study on Characterization and Application of Silicon Single Electron Devices

(シリコン単一電子素子の特性評価とその応用に関する研究)

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by

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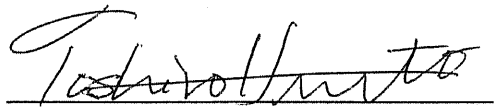

Professor Toshiro Hiramoto

Preface

This thesis describes a part of the research work carried out at the Institute of Industrial Science, University of Tokyo, under the direction of Professor Toshiro Hiramoto, while the author was a graduate student of the Department of Electronic Engineering, University of Tokyo, from April 1996 to March 1999.

The focus of this thesis is on the characterization of silicon single electron devices aiming at application to the future integrated circuits. For evaluation of device characteristics, single electron tunneling phenomena caused by silicon dots naturally formed in nano-scale narrow channel metal-oxide-semiconductor field-effect transistors (MOSFETs) are used. Fabrication of nano-scale silicon channels and investigation of the mechanisms of dot formation in the narrow channel are also matters treated in this study. From the consideration that silicon dots in single electron devices operating at high temperature get smaller than several nano-meter and quantum mechanical effects in such small system become prominent, much attentions are paid on the influences of the quantum mechanical effects on the device characteristics. Important roles of quantum confinement effects in device operation temperature and a method to utilize the effects are also investigated.

The introduction of Chapter 1 gives a brief overview of a progress and recent trend in the research field of single electron devices. Anomalous phenomena expected in the characteristics of single electron devices operating at high temperature are also mentioned. In Chapter 2, various features of the quantum mechanical effects which appear in the Coulomb blockade characteristics in the nano-size narrow channel MOSFETs are described. Comparisons between the measured device characteristics and theoretical characteristics calculated by semi-classical model are carried out. Chapter 3 gives a novel fabrication process of uniform nano-size point contact channels on silicon-on-insulator

substrates. The fabrication process was newly developed in this study to characterize the single electron tunneling phenomena in large number of devices. Relation between the quantum confinement effects and dot size is also discussed from experimental results and numerical calculations. In Chapter 4, the Coulomb blockade characteristics in electron and hole systems in the same channel are shown. Potential profiles of conduction band and valence band are estimated from the experimental results, and subsequently, origin of the tunnel barriers and dot structures naturally formed in the nano-scale channels are discussed. Chapter 5 provides a new device structure for adjustment of peak positions of Coulomb blockade oscillations in single electron devices. The adjustments of peak positions are experimentally demonstrated. Finally, concluding remarks are given in Chapter 6.

Acknowledgments

This work has been supported and contributed by several people, directly and indirectly. The author would like to take this opportunity to extend his thanks and appreciation for their contribution.

The author wishes to express his sincere gratitude for the guidance and the encouragement received from the dissertation supervisor Professor T. Hiramoto, Institute of Industrial Science, University of Tokyo. This work could not have been accomplished without his invaluable supports.

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Dr. T. Akiyama, Dr. G. Hashiguchi, Dr. S. N. Wang, Dr. H. Sakakibara, Y. Shimada, and Dr. K. Yamanaka taught the author the device fabrication process and measurements at low temperature from the beginning. Dr. T. Saito gave the author knowledge on the numerical calculation. The author is also indebted to T. Saraya, M. Ataka, T. Iizuka, and S. Ishida for their technical supports to maintain the apparatus for the device fabrication. He owed to S. Ishida and T. Saraya for nano-scale patterning by electron beam lithography.

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Contents

Chapter 1

Introduction

1.1 Backgrounds

From the beginning of the experimental discover[1)] of Coulomb blockade of single electron tunneling at mid 1980s, the devices using the phenomena have been thought as promising candidates for the component of future ultra low power consumption and high density LSIs. At 1986, Averin and Likarev had already discussed the characteristics of devices with switching operation by single electron[6,7)], and therefore called such devices as "single electron transistors".[7,8)] Application of the single electron transistors in the conventional CMOS-type logic has been proposed by Tucker[9)] and evaluated by many groups. Another way to apply the single electron devices to the integrated circuit based on cellar automata has also been proposed by Lent.[10-13)] Although the concept of the devices that control the individual electron attracts much interest, insufficient fabrication technology of ultra small structures has limited the idea only to theoretical discussion.

In the field of experimental studies, after the observation of Coulomb blockade phenomena in metal systems, periodic conductance oscillations caused by Coulomb blockade have been reported using silicon narrow channels formed by split gate technique.[14-16)] Because of the large size of dots and weak confinement of electron, the Coulomb blockade phenomena were observed only at low temperatures (typically lower than liquid helium temperature) and most of the later experiments were made on the GaAs systems[17)] from the interest of physics. [18-25)]

However recent progress in the fabrication technology of semiconductor devices, such as electron beam lithography with ultra fine resolution, makes the application of single electron devices practicable. Especially in the experiments using the silicon as a material, single electron tunneling phenomena observed at high temperature have been reported by many groups. Single electron memories[26,27] and single electron transistors,[28-31] which operate at room temperature, increase the possibility of the application of silicon single electron devices. Large barrier height of silicon-dioxide (SiO_2) makes it easier to realize strong confinement of electron in a small dot, resulting in the observation of Coulomb blockade phenomena at high temperature. In addition to the compatibility with the conventional LSIs, simple formation of SiO_2 by thermal oxidation becomes large advantage in using silicon as a material.

Compared with the steady progress in the operation temperature of single electron devices, transport properties in the single electron devices operating at high temperature are not well characterized. Many problems should be resolved before the application to the integrated devices. One of such issues is the influence of quantum mechanical effects on the device characteristics because the silicon single electron devices operating at room temperature consist of ultra fine structures whose size are less than 10 nm. From the standpoint that the quantum mechanical effects have complex dependences on the device geometry and it is difficult to predict their exact behavior, the quantum mechanical effects are regarded as disadvantages. On the other hand, the discrete energy levels by quantum confinement effects can be utilized to raise the operation temperature, which is one of the advantages of quantum mechanical effects.

1.2 Features of single electron devices operating at high temperature

As explained in many books,[32-34] the control of individual electron is based on the blockade of single electron tunneling by the repulsive force of the unit charge, which is called "Coulomb blockade of single electron tunneling". Let us consider a simple case of a single electron transistor as shown in the upper part of Figure 1.1. Adding one electron into the dot raise the dot potential by e/C_{dot}, where C_{dot} is the total capacitance of the dot. Under the condition of small drain to source voltage (V_{ds}), the single electron tunneling

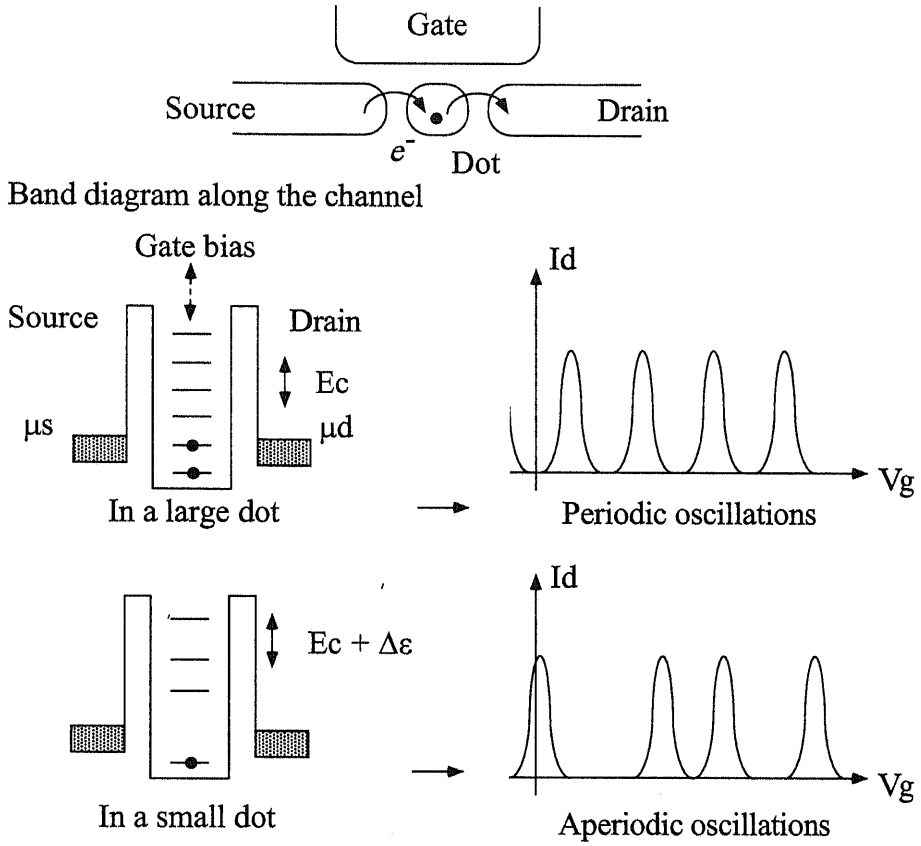

Figure 1.1: Comparison between the characteristic of single electron transistors with large dot and those with small dot.

into the dot may be allowed only if the potential of the dot after the tunneling would lies between the chemical potential of drain and source. Otherwise, the single electron tunneling into the dot may be forbidden by the repulsive force. Since the increasing gate voltage (ΔV_g) change the potential of the dot by $C_g \Delta V_g / C_{dot}$, where C_g is the dot to gate capacitance, the condition that the electron tunneling is allowed appear at the interval of e/C_g (by solving $e/C_{dot} = C_g \Delta V_g / C_{dot}$). As a result, the current from source to drain may oscillate periodically as a function of V_g (middle of Fig. 1.1). The reason why the word "may" was used in the previous sentence is that the Coulomb blockade of single electron tunneling occurs only on the condition that single electron charging energy ($e^2/2C_{dot}$) becomes much larger than the thermal fluctuation ($k_B T$) and V_{ds}. Otherwise, the Coulomb blockade oscillations are smeared out and the device does not operate correctly. This fact implies that the capacitance of the dot must be less than a few ato-farad, and therefore,

the dot in the single electron transistor must be smaller than a few nano-meter, if one wants to use the device at room temperature.

In nano-scale semiconductor dots, since the separation of single particle energy level by quantum confinement effects is much larger than that in the metal dots, the energy level separation becomes comparable or exceeds the single electron charging energy in the devices operating at high temperature. The typical influence of quantum confinement effects may appear in the change of peak positions of the devices as shown in the lower part of Fig. 1.1. Coulomb blockade characteristics will become completely different from the characteristics expected from the semi-classical model. Here, the last part of the previous section is repeated. Due to the complicated behavior of the quantum mechanical effects, it will be difficult to predict the device characteristics. In this sense, the quantum mechanical effects become a problem for the device application. From another point of view, the quantum mechanical effects can be advantage if one can utilize them. For instance, the suppressed region of the drain current remain at higher temperature if the energy level separation by quantum confinement effects is large at that point. In the lower part of Fig 1.1, the suppressed region of the drain current between first peak and second peak corresponds to the above explained case. Therefore, the single electron transistor operates at higher temperature if it is operated at the gate voltage where the energy level separation in the dot is large.

1.3 Objectives

Standing on the above mentioned backgrounds, the evaluation of transport properties of silicon single electron devices operating at high temperature become very important for their application. For the quantitative evaluation of the transport properties of the devices, fabrication process of nano-scale structures should be further progressed. After the evaluation of device characteristics, the methods to use the single electron devices in the integrated circuits must be developed.

This study was carried out focused on the following three themes.

- To develop novel fabrication techniques of silicon nano-scale narrow channels for the quantitative characterization of silicon single electron devices.

- To evaluate the transport properties of devices operating at high temperature, especially paying attention on the influences of quantum mechanical effects.
- To find new methods to utilize the quantum mechanical effects for the application of single electron devices.

1.4 Synopses of chapters

In chapter 2, the influence of the quantum mechanical effects on the characteristics of silicon single electron devices are described. The devices are fabricated on the SOI substrate using electron-beam lithography and anisotropic wet etching. Aperiodic Coulomb blockade oscillations are observed in the device operating at high temperature. Negative differential conductance and fine structures, which are caused by quantum mechanical effects, are also found at low temperature. Energy levels in the silicon dot are extracted from the obtained device characteristics.

Chapter 3 provides a newly developed fabrication process of nano-scale point contact channels on SOI substrate. In the developed fabrication technique, the width of nano-size point contact channels is determined only by the thickness of SOI layer. Therefore, wafer-scale uniform channels can be fabricated without using fine resolution lithography. The quantum confinement effects on the Coulomb blockade characteristics are discussed using the experimental results. For quantitative evaluation of the quantum confinement effects, numerical calculations are carried out using the finite element method. The effects of the anisotropic effective mass of carrier in silicon are also discussed.

In Chapter 4, Coulomb blockade characteristics in both electron channel and hole channel are indicated. The potential profiles of conduction band and valence band in the same point contact channels are evaluated, and subsequently, origin of the tunnel barriers and dot formation in narrow silicon channels are discussed.

Chapter 5 gives the method to adjust the peak positions of Coulomb blockade oscillations in single electron devices. In the experiments, charge injection into the silicon nano-crystals deposited on the single electron transistors are used for the peak adjustment.

The knowledge obtained in this study are summarized in Chapter 6.

Bibliography

[1] Although the charging effects of electrons have been already recognized in the early 1950s by Gorter[2] and several experiments which suggested the importance of charging effects have been carried out[3-5] using very thin metallic films, clear zero-bias anomalous caused by "Coulomb blockade of single electron tunneling" in a single dot system was first confirmed by T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. **59**, 109 (1987).

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Chapter 2

Coulomb blockade characteristics in a nano-size silicon dot system

2.1 Introduction

Since the experiment[1)] carried out by Field (1990), it has been well known that drain conductance oscillations caused by the Coulomb blockade of single electron tunneling were often observed in silicon narrow channels.[1-3)] In the experiments, the Si narrow channels were formed using split-gate structures and dot structures were thought to originate from the potential fluctuations by ionized impurities. Electron confinement by the potential barriers of split gate and impurity ions were very weak. Therefore, Coulomb blockade oscillations were observed only at very low temperature, typically at liquid helium temperature. In such devices, the Coulomb blockade oscillations are characterized by the semi-classical theory, which indicates that the energy levels are dense and the many body effects can be described by single electron charging energy of the dot with constant capacitance.

Recently, it becomes possible to fabricate silicon nano-size narrow channels surrounded by silicon-dioxide (SiO_2), using electron-beam lithography with nano-scale resolution and silicon-on-insulator (SOI) substrate. In such devices, Coulomb blockade oscillations are observed at high temperature[4-9)] and some of them remain even at room temperature because of the strong confinement by SiO_2 and large charging energy in

extremely small (less than 10 nm) silicon dots. As mentioned in Chapter 1, quantum mechanical effects, such as quantum confinement effects, are thought to have influence on the device characteristics in the high temperature operating devices. For the application of the single electron devices, it is inevitable to clarify the influence of quantum mechanical effects.

In this chapter, an experiment that has been carried out to investigate the single electron tunneling phenomena in Si nano-size channels is described. Coulomb blockade oscillations at room temperature have been observed in a device fabricated on the SOI substrate using electron beam lithography and anisotropic wet etching. The quantum mechanical effects, especially the quantum confinement effects, are studied based on the obtained experimental results. Comparison of the experimental results with numerical calculation is also made.

2.2 Fabrication of silicon nano-size channel MOSFETs

Figure 2.1 shows a schematic view of the fabrication process of point contact MOSFET. A (001) oriented, p-type SOI substrate prepared by the separation-by-implanted-oxygen (SIMOX) technique is employed. The resistivity of the wafer is 20 $\sim$ 30 Ωcm and the concentration of acceptor is 10^{15} cm^{-3}. Thicknesses of surface silicon layer and buried oxide layer are 165 nm and 105 nm, respectively. The point contact channel is defined by the EB lithography. An anisotropic wet etching technique is employed to smooth out the fluctuations caused by the EB lithography.[9] Tetramethylammonium-hydroxide (TMAH) which is fully compatible with the current VLSI process[8-10] is utilized for anisotropic wet etching.

First, the surface Si layer of the SIMOX wafer is thinned to 40 nm by thermal oxidation and subsequent wet etching. Then, 10 nm thermal oxide is formed as a mask for anisotropic etching. Point contact patterns are exposed in the poly-methyl-methacrylate (PMMA) resist by EB lithography (Fig. 2.1(a)). After the development of PMMA resist, the patterns are transferred to the SiO_2 mask by buffered HF. The edges of the PMMA resist patterns after the development and SiO_2 mask patterns are rounded as shown in Fig. 2.1(a) and (b). Then, anisotropic wet etching by TMAH (15 wt%) is performed at

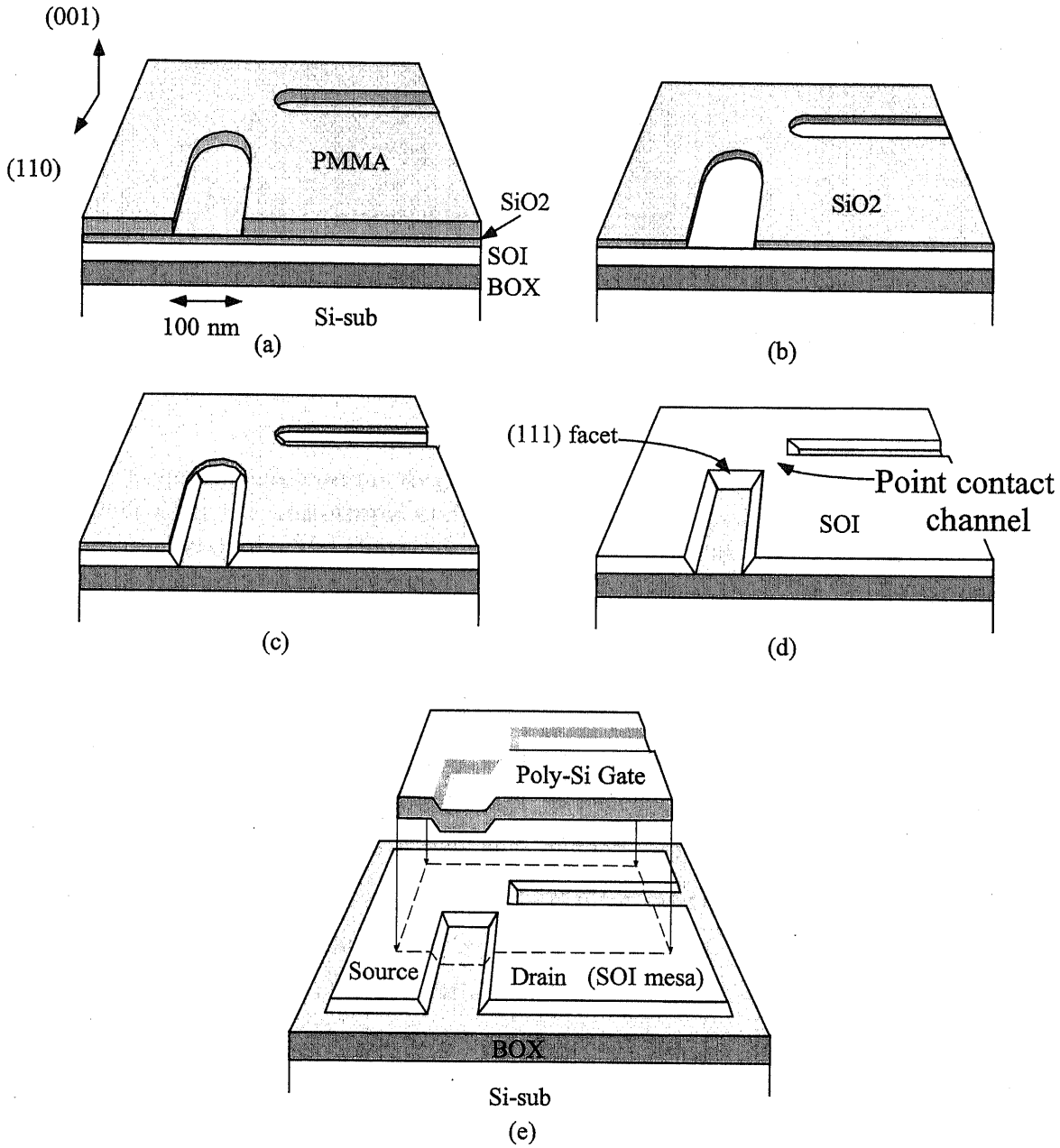
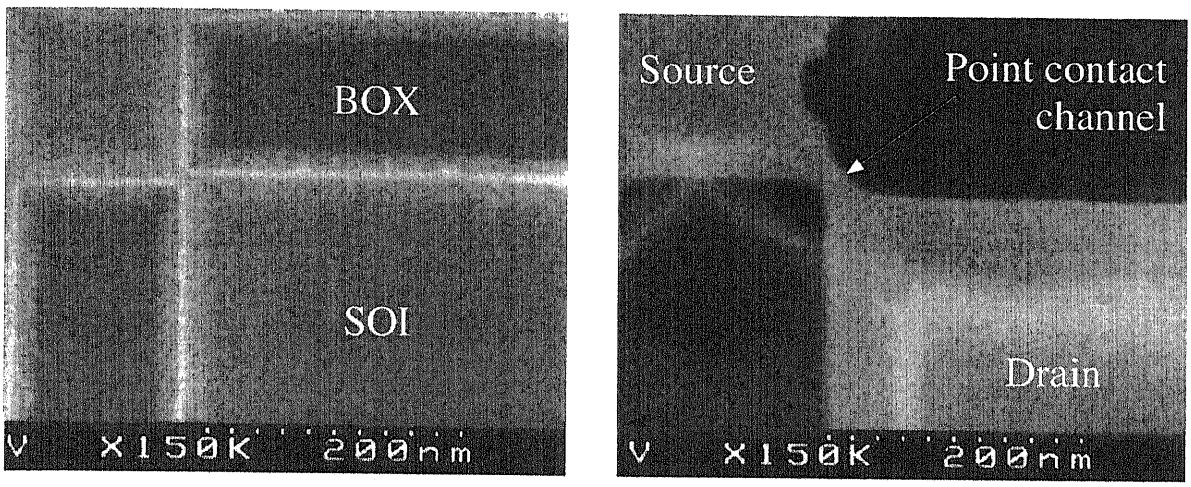


Figure 2.1: Schematic view of the fabrication process of Si point contact channel MOSFET. The devices are fabrication on a SIMOX wafer using EB lithography and anisotropic wet etching. The width of the point contact channel is changed by the condition at EB lithography.



(a) (b)

Figure 2.2: Scanning electron micro-graph images of the fabricated Si point contact channel. (a) Just after the anisotropic etching. (b) Passivation oxide, poly-Si gate, and gate oxide were removed after the characterization of the device at low temperature. Although the width of this point contact channel is narrower than 30 nm, this device operated as a normal MOSFET even at 4.2 K.

75 °C. By this anisotropic etching, the edges become sharpened as shown in Fig. 2.1(c). Therefore, the fluctuation of the resist pattern can be smoothed out. When the {111} facets appear at the edges of the SiO_2 mask, the anisotropic etching automatically stops and the point contact structure is precisely defined. The width of the point contact is controlled by the dose of electrons at EB lithography. After the removal of the SiO_2 mask (Fig. 2.1(d)), 50 nm-thick gate oxide is formed by thermal oxidation at 1000 °C, which squeezes the point contact channel. After the gate oxidation, usual MOSFET fabrication processes, that is, poly-Si gate formation, phosphorus ion (P^+) implantation, contact hole etching, and metalization by aluminum evaporation, are performed to complete the device (Fig. 2.1(e)).

Detailed conditions at each steps during the device fabrication are listed in Table 2.1

From the scanning electron micro-graph taken after the anisotropic etching (Figure 2.2 (a)), the point contact channel surrounded by {111} facets are successfully formed. It is noted that the point contact channel is further squeezed after the gate oxidation

(Fig. 2.2 (b)). In this experiment, the point contact MOSFETs with various channel widths are fabricated.

Table 2.1: Conditions of the fabrication process of point contact MOSFETs.

step	condition	temperature (°C)	time (min)	thickness (nm)	remark
Dicing	2cm×1.5cm (Low dose SIMOX)				
Wafer cleaning	$NH_4OH : H_2O_2 : H_2O = 1 : 2 : 8$ (SC1)	75	10		*1
SiO_2 remove	BHF				
RCA cleaning	DI water (DeIonized water)		3		
	$HF : H_2O = 1 : 100$		dip		
	DI water		3		
	$NH_4OH : H_2O_2 : H_2O = 1 : 1 : 4$ (SC1)	75	20		
	DI water		3		
	$HF : H_2O = 1 : 100$		1		
	DI water		3		
	$HCl : H_2O_2 : H_2O = 1 : 1 : 4$ (SC2)	75	20		
	DI water		3		
	$HF : H_2O = 1 : 100$		1		
	DI water		3		
Oxidation	O_2 : 1.0l/min	1100			*2
	N_2 : 1.0l/min (Annealing)	1100	5		
SiO_2 remove	BHF				
Oxidation	O_2 : 1.0l/min	950	10	12	
	N_2 : 1.0l/min (Annealing)	950	5		
EB lithography	OEBR1000(100cp):ECA=2:1 4000 rpm		40 sec	160	
(JEOL : JBX-5DII)	Prebake	170	30		
	Line 3.0 nC/cm Area 450 $\mu C/cm^{-2}$				
	50keV 600pA				
	MIBK:IPA =1:3 (develop)		1.5		
	IPA (rinse)		1		
	DI water (rinse)		3		
	Postbake	90	10		
Pattern transfer	BHF		10 sec		*3
Resist remove	Acetone				
Anisotropic etching	TMAH (15%)	75	20sec		
Photo lithography	AZ1350 4000rpm		40sec	400	
(mesa)					
	Prebake	90	30		
	Exposure,development,rinse				
	Postbake	125	30		
Pattern transfer	$HF:H_2O$=1:20		50 sec		
Resist remove	Acetone				
Anisotropic etching	TMAH (15%)	75	30sec		

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SPM cleaning	$H_2SO_4 : H_2O_2 = 3 : 1$	130	15		
RCA cleaning	Same as previous RCA cleaning				
Gate oxidation	$O_2 : 1.0l/min$	1000	50	49	
	$N_2 : 1.0l/min$ (Annealing)	1000	5		
Poly-Si deposition	SiH_4 200sccm 1.0Torr	600	30	195	
Photo lithography (gate)	AZ1350 4000rpm		40sec	400	
	Prebake	90	25		
	Exposure,development,rinse				
Gate RIE	SF_6 30sccm 0.013Torr 100W	0	1.5		
Resist remove	Acetone				
SPM cleaning	$H_2SO_4 : H_2O_2 = 3 : 1$	130	15		
Ion implantation source, drain, gate	P^+ 50keV $5\times10^{15}cm^{-2}$ $I_{beam} \sim 40\mu A$		~35		
SPM cleaning	$H_2SO_4 : H_2O_2 = 3 : 1$	130	15		
Annealing	$N_2 : 1.0l/min$	950	20		
Photo lithography (contact hole)	AZ1350 4000rpm		40sec	400	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	130	30		
Contact hole etching	HF:H_2O=1:10		70sec		
Resist remove	Acetone				
Photo lithography (Al electrode)	AZ1500 4000rpm		40sec	800	
	Prebake	90	25		
	Exposure,development,rinse				
Al evaporation				277	
Lift off	Acetone				
Wire bonding					

*1 To remove particles on the wafer.

*2 To reduce the thickness of SOI layer.

*3 Do not use diluted HF.

2.3 Quantum mechanical effects in a high temperature operating single electron transistor

After a wire bonding, the devices were mounted on a rotary pumped ^{4}He cryostat and dc-characteristics were measured using a high precision semiconductor parameter analyzer (HP4156A).

The characteristics of the point contact MOSFETs strongly depend on the channel width. The devices with large width have normal MOSFET characteristics. By the scanning electron microscopy observation, it was found that the device with 30 nm width (shown in Fig 2.2 (b)) shows the normal MOSFET operation even at 4.2 K. As the width decreases, the drain current decreases and, when the channel becomes extremely narrow (less than 10 nm), the device shows clear Coulomb blockade oscillations, which indicates that the channel is separated by tunnel barriers. When the width further decreases, the device has no drain current because the channel is cut by the thermal oxidation.

Several causes, such as localized states, Si nano-size particles in the transition layer between surface Si layer and buried oxide layer, thickness fluctuations of the surface Si layer, or pattern dependent oxidation[4-6] may become the origin of dot formation in nano-size narrow channel. But the reason of the dot formation in the devices used in this experiment is not clarified. An experiment to investigate the mechanism of dot formation in nano-size narrow channels is described and the origin of the tunnel barriers is discussed in Chapter 5.

In this chapter, since the interest is in the the influence of quantum mechanical effects on the device characteristics, experimental results of the device in which the Coulomb blockade oscillations are observed even at room temperature are focused on.

Figure 2.3 shows the drain current (I_d) as a function of gate voltage (V_g) in a device which shows Coulomb blockade oscillations even at room temperature. The device is characterized at temperature range from 15 K to room temperature. Drain voltage (V_{ds}) is kept at 1 mV which is smaller than the thermal energy of electron. In the figure, step like fluctuation of drain current is observed even at room temperature and it becomes clear oscillations at 77 K. It should be noticed that the intervals between the peaks are not constant. From the inset of Fig 2.3, in which the second peak at 15 K is fitted by two functions, the peaks of oscillations are well characterized by the derivative of the Fermi-

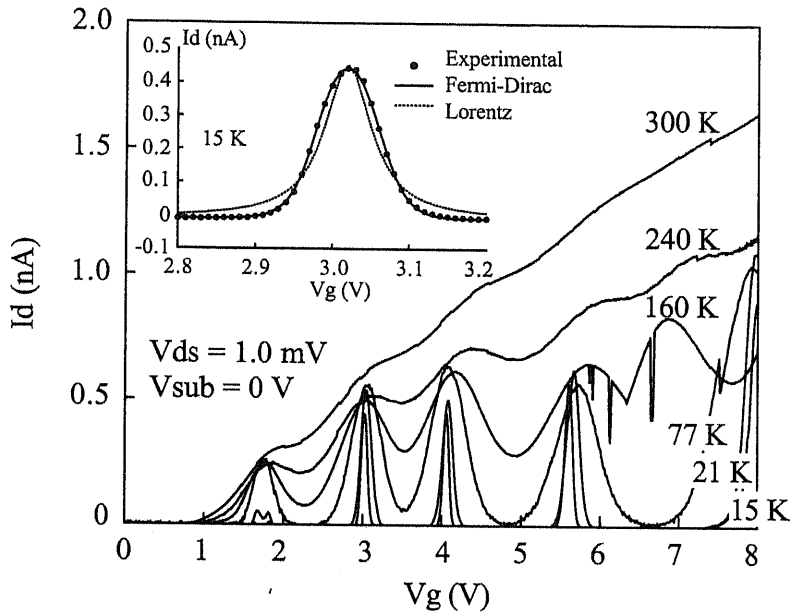


Figure 2.3: Dependence of the drain current (I_d) on the gate voltage (V_g) with the drain voltage (V_{ds}) of 1.0 mV. The temperature is changed from room temperature down to 15 K. The abrupt I_d changes at 160 K are the random telegraph noise. The inset shows the second peak at $V_g = 3$ V which is fitted by the derivative of the Fermi-Dirac distribution and Lorentzian resonance line shape.

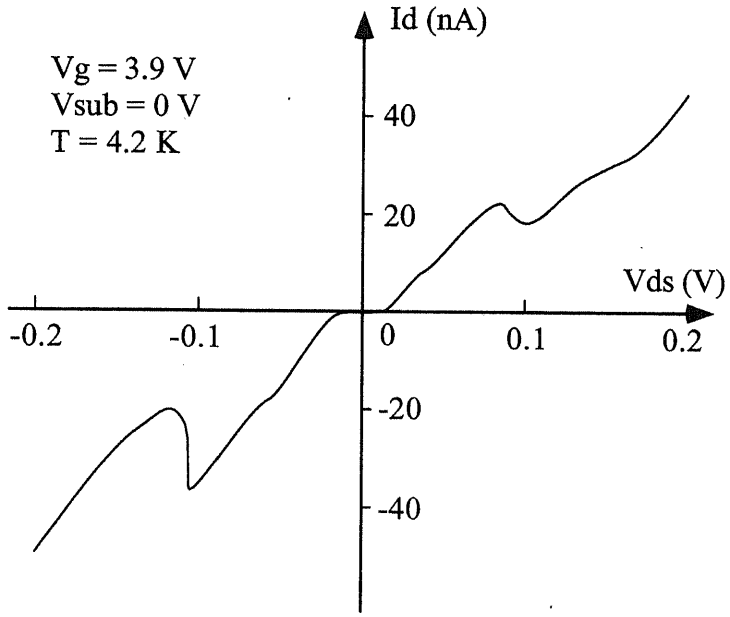


Figure 2.4: $I_d - V_{ds}$ characteristics near the third peak of Coulomb blockade oscillations at 4.2K. Negative differential conductances (NDCs) are observed at $V_{ds} \simeq \pm 100$ meV and fine structures appear at $V_{ds} \simeq +40, -50$ meV.

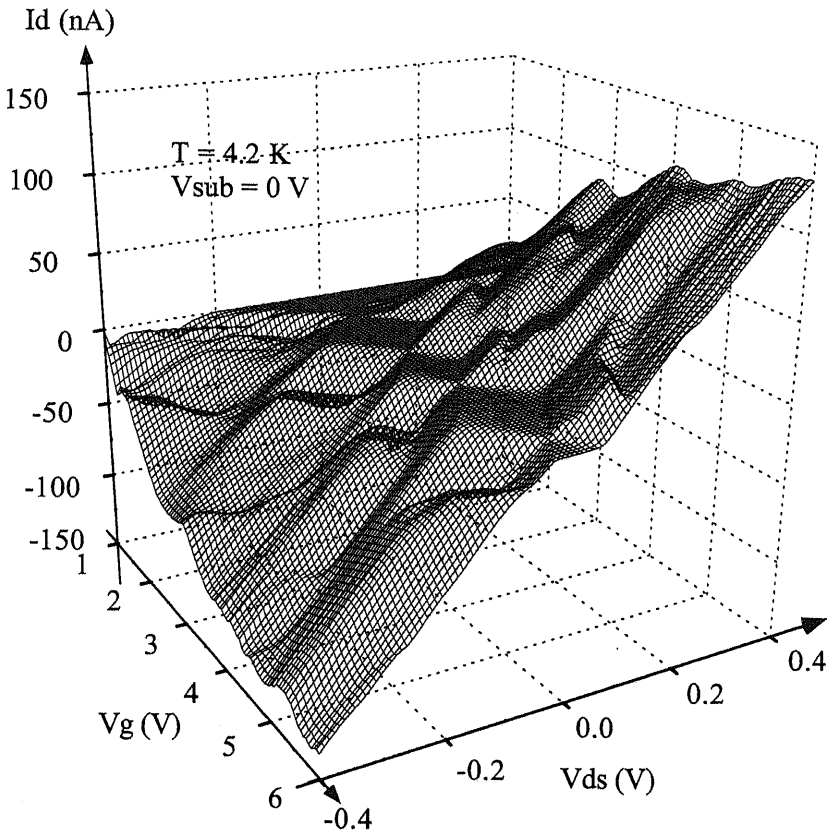


Figure 2.5: 3D plot of the I_d as a function of the V_g and V_{ds} at 4.2 K. Clear rhombus shapes caused by Coulomb blockade oscillations are observed. NDCs and fine structures appear in parallel with the sides of each rhombus shape.

Dirac distribution function. Incidentally, the abrupt changes of the drain current at 160 K from $V_g = 6$ V to 7 V are the random telegraph signal (RTS) noise which is caused by single electron capture into and emission from an interface state and often observed in narrow channels.[11-13] This RTS noise with large abrupt modulation in drain current also suggests the extremely narrow channel width (less than 10 nm). Figures 2.4 shows the V_{ds} dependence of the I_d near the Coulomb blockade oscillations peak at $V_g = 3.9$ V. The temperature is 4.2 K. Negative differential conductances (NDCs) (at $V_{ds} \simeq \pm 100$ meV) and fine structures (at $V_{ds} \simeq +40, -50$ meV) are clearly observed as well as suppressed drain current region by Coulomb blockade at low drain voltage region ($|V_{ds}| < 10$ meV).

The $I_d - V_g$ and $I_d - V_{ds}$ characteristics only show one aspect of the device properties. To grasp the entire property of the device, the I_d dependence on the V_{ds} and V_g at 4.2

K are measured and shown in Figure 2.5. Clear rhombus shapes which are caused by the Coulomb blockade of single electron tunneling are observed. Furthermore, the NDCs and fine structures appear in parallel with the sides of each rhombus shape. Then, the transport mechanisms in the point contact channel are considered in the next section.

2.4 Mechanism of electronic transport

In Fig. 2.3, except the first peak, the temperature dependence of the peak heights is not strong and the peaks do not split at low temperature as in the case of multiple-dot system.[8,14-16] In Fig. 2.5, where the V_g is fixed at oscillations peaks, the rhombus shapes of the current suppressed regions are closed and the $I_d - V_{ds}$ characteristics are perfectly linear at small V_{ds}. Therefore, the Coulomb blockade effects are caused by a single-dot system.

Different from the Coulomb blockade characteristics of the semi-classical model[17] which well describes the characteristics of metal system,[18] i) the interval between the oscillations peaks are not constant (Fig. 2.3), ii) NDCs and the fine structures are superposed on the $I_d - V_{ds}$ characteristics (Fig. 2.4 and 2.5). The cause of the anomalous characteristics is attributed to the quantum mechanical effects. In a small semiconductor dot, separation ($\Delta\varepsilon$) between the single particle energy levels becomes comparable to the single electron charging energy (E_C), which break the periodicity of the Coulomb blockade oscillations[17] as explained in the following.

The energy states in a single dot system, which is shown in the upper part of Figure 2.6, are considered. The ground-state energy ($E(N; V_g, V_{ds})$) in a dot of N electrons is approximated as the sum of the filled single particle energy states and the electrostatic energy of the dot. Therefore, it is written as

$$E(N; V_g, V_{ds}) = U(N; V_g, V_{ds}) + \sum_{i=0}^{N} \varepsilon_i, \tag{2.1}$$

where ε_i are the single particle energy levels of the dot. $U(N; V_g, V_{ds})$ is the electrostatic energy of the dot and written using a total capacitance of dot (C_{dot}) as

$$U(N; V_g, V_{ds}) = \frac{(Ne - C_g V_g - C_d V_{ds})^2}{2C_{dot}}. \tag{2.2}$$

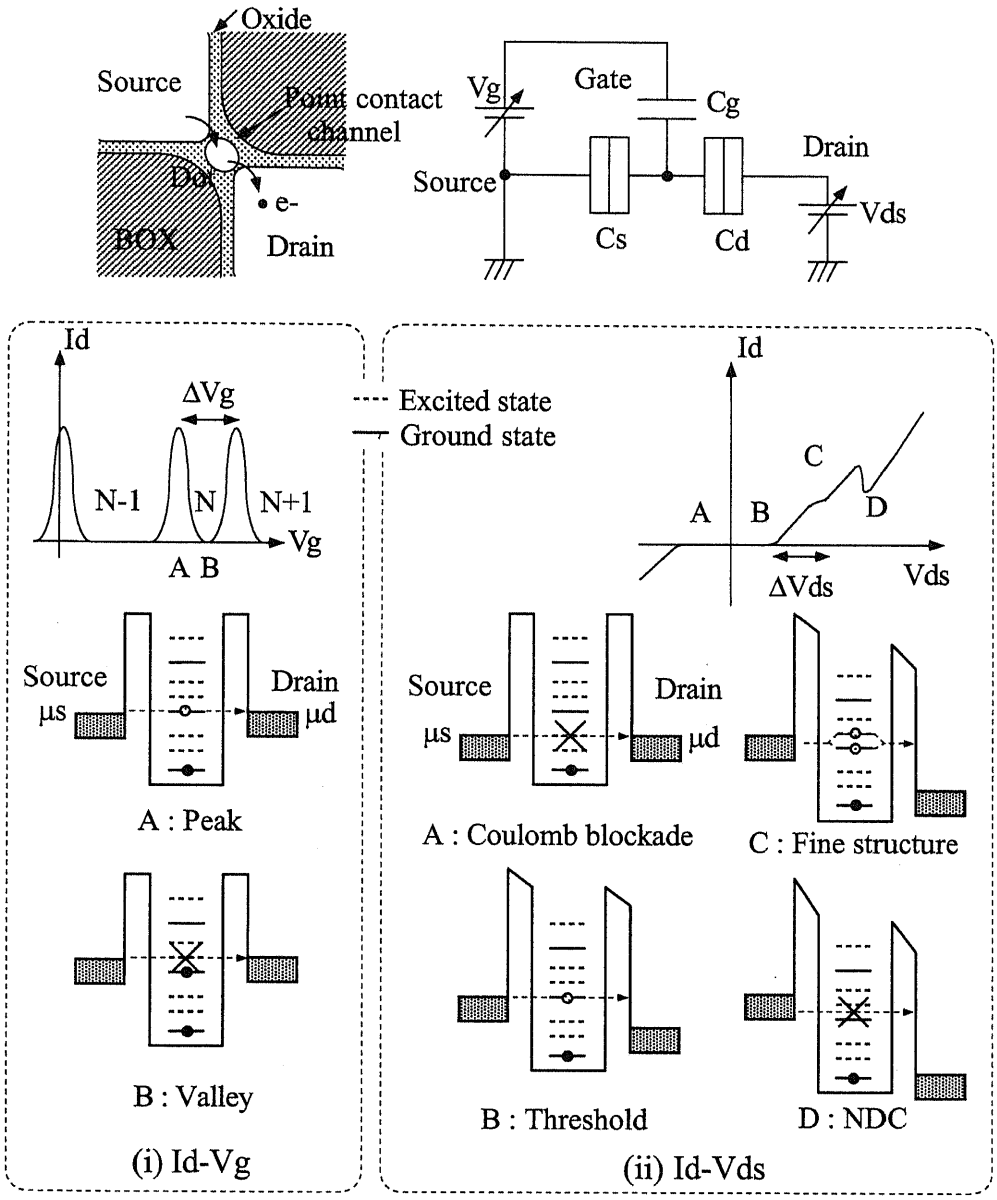


Figure 2.6: Mechanism of the transport in the single dot system naturally formed in Si nano-size channel. (i) $I_d - V_g$ characteristics with fixed small V_{ds}. (ii) $I_d - V_{ds}$ characteristics at fixed gate voltage.

Since the electrochemical potential in the dot with N electrons is defined as

$$\mu_{dot}(N; V_g, V_{ds}) = E(N; V_g, V_{ds}) - E(N-1; V_g, V_{ds}), \tag{2.3}$$

it is expressed as

$$\begin{aligned} \mu_{dot}(N; V_g, V_{ds}) &= \varepsilon_N + U(N; V_g, V_{ds}) - U(N-1; V_g, V_{ds}) & (2.4) \\ &= \varepsilon_N + \frac{e^2(N-\frac{1}{2})}{C_{dot}} - e\frac{C_g V_g}{C_{dot}} - e\frac{C_d V_{ds}}{C_{dot}}. & (2.5) \end{aligned}$$

First, let us consider the case in which the V_g is scanned while the V_{ds} is kept constant with small bias. The drain current peak appears at each time when the electrochemical potential in the dot, $\cdots, \mu_{dot}(N-1; V_g, V_{ds}), \mu_{dot}(N; V_g, V_{ds}), \mu_{dot}(N+1; V_g, V_{ds}), \cdots$, lies between the electrochemical potential in source (μ_s) and drain (μ_d) region, denoted as "A : Peak" in the left of Fig 2.6. For example, if $\mu_{dot}(N+1; V_g, V_{ds}) = \mu_s$, the electron can travel from source to drain via the $N+1$ electron and N electron states in the dot. Therefore, the interval ($\Delta V_g = V_g' - V_g$) between the peaks, when N electrons resides in the dot, is obtained by solving

$$\begin{aligned} \mu_{dot}(N+1; V_g', V_{ds}) &= \mu_{dot}(N; V_g, V_{ds}), & (2.6) \\ \varepsilon_{N+1} + \frac{e^2(N+\frac{1}{2})}{C_{dot}} - e\frac{C_g V_g}{C_{dot}} - e\frac{C_d V_{ds}}{C_{dot}} &= \varepsilon_N + \frac{e^2(N-\frac{1}{2})}{C_{dot}} - e\frac{C_g V_g'}{C_{dot}} - e\frac{C_d V_{ds}}{C_{dot}}. & (2.7) \end{aligned}$$

The result is

$$\Delta V_g = \frac{C_{dot}}{C_g}\left(\frac{\Delta\varepsilon}{e}\right) + \frac{e}{C_g}, \tag{2.8}$$

where $\Delta\varepsilon$ is the difference between ε_{N+1} and ε_N. In comparison to the interval between the conductance peaks in metal systems, which is simply described as $\Delta V_g = e/C_g$, there is an additional contribution due to the single particle energy level spacing by the quantum confinement effects.

On the other hand, in the $I_d - V_{ds}$ characteristics, the conductance ($\partial I_d/\partial V_{ds}$) increases for increased V_{ds} if during transport the dot can go either into the ground state or excited states of dot with N electron, which corresponds to the increased channel for electron[19-23]. Although the transport channel increases, the number of electron which can travel through the dot at same time is limited to one. This phenomenon is different from so called "Coulomb staircase" observed when the number of electron traveling through the

dot increases. The above mentioned situations are described as follows. When the ground states of the dot with N electron reaches to the electrochemical potential ($\mu^*_{dot}(N; V_g, V_{ds})$) of the source ($\mu_s$), electron begins to travel from source to drain via the ground state, which is denoted as "B : threshold" in the right part of Fig 2.6. As the first exited states of the dot ($\mu^*_{dot}(N; V_g, V'_{ds})$) get below the μ_s, the conductance increases due to the increased channel, which is shown as "C : fine structure" in the right part of Fig 2.6. Therefore, $\mu_{dot}(N; V_g, V_{ds}) = \mu_s$ defines the boundaries of the rhombus shapes of Coulomb blockade, while $\mu^*_{dot}(N; V_g, V'_{ds}) = \mu_s$ defines the fine structures in Fig 2.5. At fixed gate and source voltage, the difference between the V_{ds} where the drain current begins to flow and the V'_{ds} where the fine structures are observed can be calculated from

$$\mu_{dot}(N; V_g, V_{ds}) = \mu^*_{dot}(N; V_g, V'_{ds}). \tag{2.9}$$

In the case when the highest electron in the dot of the ground state is exited into the next state, the first excited state in the dot with N electrons are approximately expressed as

$$E^*(N; V_g, V'_{ds}) = U(N; V_g, V'_{ds}) + \sum_{i=0}^{N-1} \varepsilon_i + \varepsilon_{N+1}, \tag{2.10}$$

therefore,

$$\mu^*_{dot}(N; V_g, V'_{ds}) = \varepsilon_{N+1} + \frac{e^2(N - \frac{1}{2})}{C_{dot}} - e\frac{C_g V_g}{C_{dot}} - e\frac{C_d V'_{ds}}{C_{dot}}. \tag{2.11}$$

As a result, one can obtain from Equations (2.5), (2.9), and (2.11),

$$\Delta V_{ds} = \frac{C_{dot}}{C_d}\left(\frac{\Delta\varepsilon}{e}\right). \tag{2.12}$$

Thus, ground states of the dot can be obtained from the $I_d - V_g$ characteristics with small V_{ds}, and single particle energy level separations by quantum confinement effects can be extracted from the $I_d - V_{ds}$ characteristics at fixed V_g.[19-23] As for the NDCs, as denoted "D : NDC" in the right part of Fig 2.6, they should be observed when the conduction band edge of the source passes by the ground state level of the dot, which is same as the case in resonant tunneling diode.

The above discussion assume the constant capacitance model that the many body effects are put into the constant charging energy. For more precise investigation, the energy levels of many body systems must be considered. However, the influence of quantum confinement effects can be approximately evaluated using the above model.

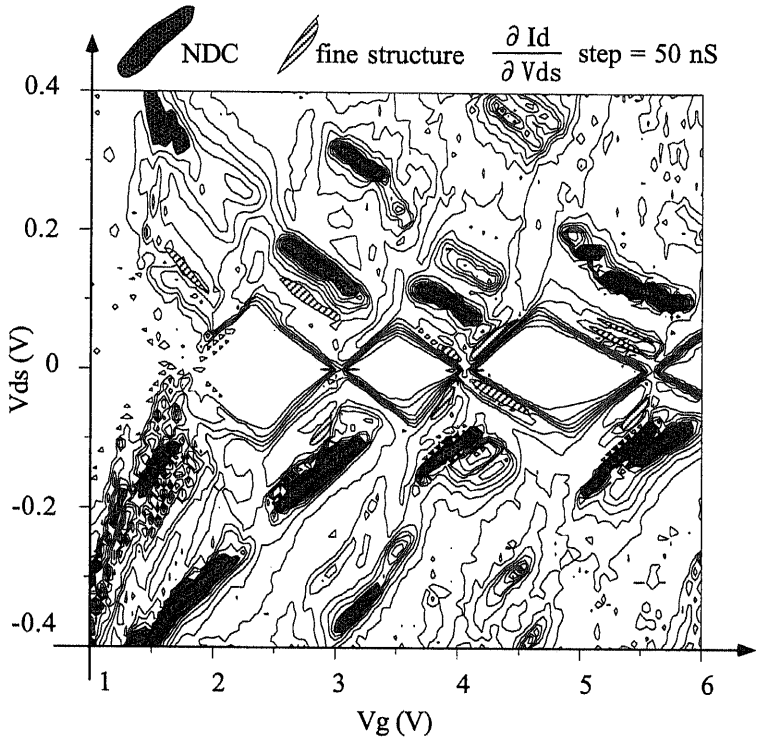


Figure 2.7: Contour plot of the differential conductance ($\partial I_d/\partial V_{ds}$) as a function of V_g and V_{ds} at 4.2 K. The hatched areas indicate the NDCs and dotted areas show the fine structures. One step corresponds to 50 nS.

2.5 Energy levels in nano-size silicon dot in a single electron transistor

To extract the electronic structure in silicon dot using Equations (2.8) and (2.12), the capacitance ratios between each electrode are required. For this purpose, a contour plot of the differential conductance ($\partial I_d/\partial V_{ds}$) as a function of V_g and V_{ds} are plotted in Figure 2.7. The hatched areas indicate the NDCs and dotted areas represent the fine structures. Single dot systems can be represented in the left part of Figure 2.8. From the slope of each side of the rhombus shapes ($\partial V_g/\partial V_{ds}$), one can calculate the ratio of the gate-dot (C_g), drain-dot (C_d), and source-dot (C_s) capacitance.[17] It is also possible to estimate the ratio of the substrate-dot capacitance (C_{sub}) and C_g from the shift of Coulomb blockade oscillations by the substrate bias (not shown here).

From the simple calculation, it is found that potential in the dot ($\phi_{dot}(N)$) is

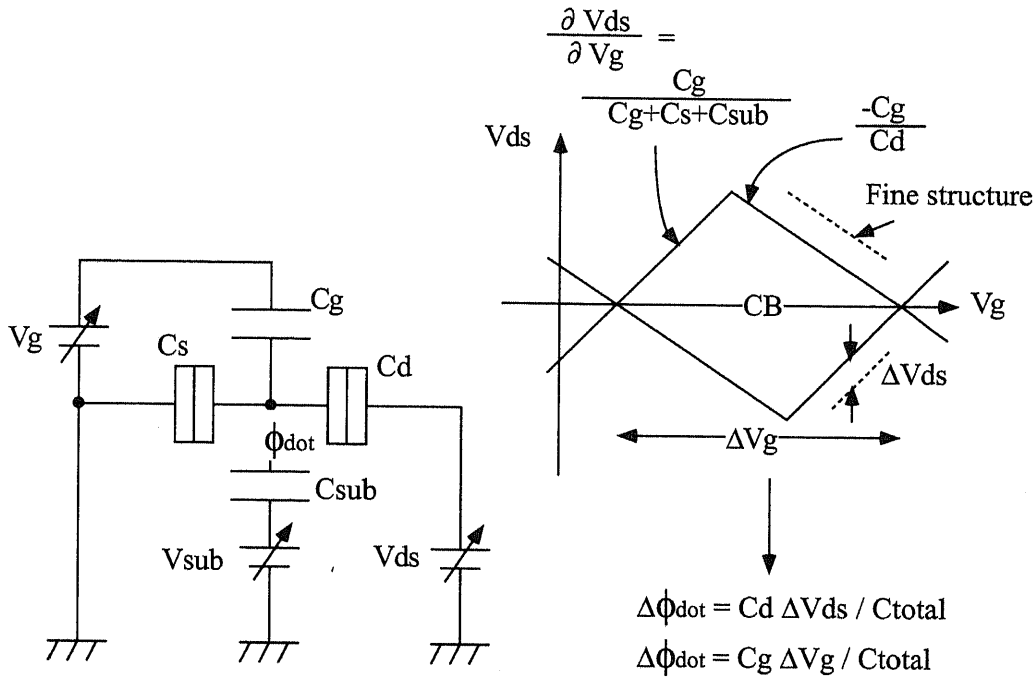


Figure 2.8: The relation used to extract the parameter of the capacitance.

described as

$$\phi_{dot}(N) = \frac{C_g V_g + C_d V_d + C_s V_s + C_{sub} V_{sub} - Ne}{C_{dot}}, \tag{2.13}$$

where $C_{dot} = C_g + C_d + C_s + C_{sub}$. The sign of the right term of Equation (2.13) is opposite to that of Equation (2.5), because the electron energy is considered as a basic in Eq. (2.5). The slope with positive gradient corresponds to the case that $\phi_{dot}(N)$ is kept constant with respect to drain voltage ($\phi_{dot}(N) - V_{ds} = \text{const.}$), and therefore, described as

$$\frac{\partial V_d}{\partial V_g} = \frac{C_g}{C_g + C_s + C_{sub}}. \tag{2.14}$$

On the other hand, the slope with negative gradient corresponds to the case that $\phi(N)$ is kept constant with respect to source voltage ($\phi(N) - V_s = \text{const.}$ in this case 0 V) and described as

$$\frac{\partial V_d}{\partial V_g} = -\frac{C_g}{C_d}. \tag{2.15}$$

Furthermore, the shift (ΔV_{peak}) of peak positions of Coulomb blockade oscillations in the $I_d - V_g$ characteristics when the substrate bias is changed by ΔV_{sub} is calculated from the

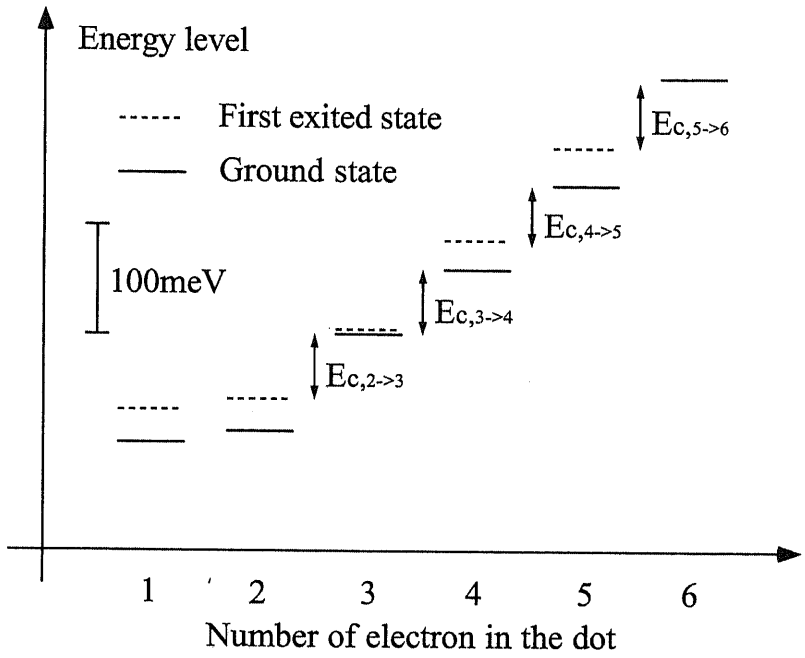


Figure 2.9: Energy levels of N electron state in the quantum dot extracted from the fine structure of Fig. 2.7. Horizontal axis indicates the number of electrons and vertical axis is the energy.

condition that $\phi(N) = \text{const.}$

$$\frac{\Delta V_{peak}}{\Delta V_{sub}} = -\frac{C_{sub}}{C_g}. \tag{2.16}$$

In this device, the relation is estimated as $C_g : C_d : C_s : C_{sub} = 1 : 5.9 : 9.4 : 0.01$. From these value, the potential in the quantum dot (ϕ_{dot}) is changed by $\Delta\phi_{dot} = C_g\Delta V_g/C_{total} = 0.061\Delta V_g$, when the gate voltage is changed by ΔV_g and the voltages of the other leads are fixed. In the same way, ϕ_{dot} are changed by $\Delta\phi_{dot} = C_d\Delta V_{ds}/C_{total} = 0.36\Delta V_{ds}$, when the drain voltage is changed by ΔV_{ds} and the voltages of the other leads are fixed.

Using the above relations, the energy levels in the silicon quantum dot in the single electron transistor are evaluated from the intervals between the peaks in Fig. 2.3 and fine structures in Fig. 2.7. It is very difficult to determine the number of electrons in the dot because there is a possibility that the threshold voltage of parasitic MOSFET is larger than the intrinsic threshold voltage of single electron transistors. However, in this device, the device threshold voltage locates at $V_g = 1.7$ V, which is much higher than the

threshold voltage of parasitic MOSFET ($V_{th} = -0.2$ V obtained from the other devices). Furthermore, no drain current peaks can be observed even when a positive substrate bias is applied to reduce the threshold voltage of parasitic MOSFET. Therefore, it is considered that no electron exists in the dot at the gate voltage lower than the first peak.

Figure 2.9 shows the corresponding energy of the ground states and excited states as a function of the number of electrons (N) in the quantum dot. The average single electron charging energy (E_C) is 58 meV and the quantized level separation at $N = 2$ is 30 meV. The barrier height of the tunnel junctions are no less than 340 meV which is estimated from the $I_d - V_{ds}$ characteristics. Therefore, the sum of the charging energy and quantized level spacing in the dot as well as tunnel barrier height are much larger than the thermal energy at 300 K. Once the E_C are obtained, the average capacitances are evaluated as $C_g = 0.085$ aF, $C_d = 0.50$ aF, $C_s = 0.80$ aF, $C_{sub} = 0.0009$ aF, and $C_{dot} = 1.4$ aF. From these values, the dot size is estimated to be 6 nm if a spherical dot shape is assumed.

The quantized level separation strongly depend on the number of electron, because it is strongly affected not only by the size but also by the shape of the dot. The dot would be irregular in shape in this system. Furthermore, the quantized level separation seems to increase as the number of electron increases which indicates that the confinement of the potential barrier of the dot is stronger than that of a harmonic potential well. On the other hand, the above mentioned capacitances and charging energy are not constant. It also weakly depends on the number of electrons. This is because, when the dot size and the electron number are extremely small, the charge distribution and the size of the dot are completely changed by the addition of only one electron.

Some explanations should be needed for the almost same energy levels of one electron and two electron states in the dot and weak temperature dependence of peak heights. In Fig 2.3, the temperature dependence of first peak is different from the other peaks. The height of first peak rapidly decreases as the temperature decreases. Furthermore, the peak split into two fine peaks below 50 K. This behavior of first peak is explained by the coupled double-dot system. As explained in Appendix A, the peak heights of the multiple-dot system show thermally activated behavior if the system is not symmetric and the peak split into fine peaks at low temperature. In this device, a single dot at high

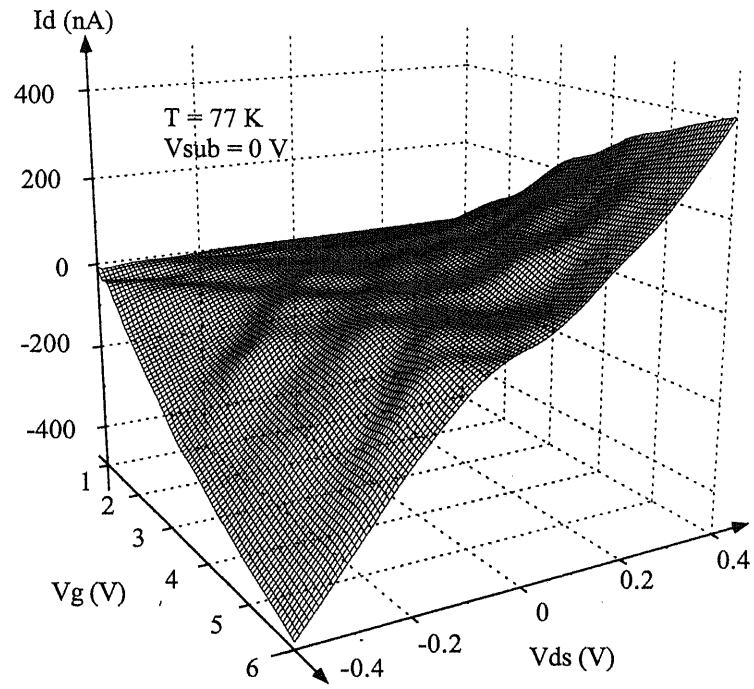
gate voltage range is divided into double dots as the gate voltage is decreased because the screening of potential fluctuation in the channel by the electron becomes week at low gate voltage. If the difference between the size of each dot is small, two electrons tunnel into the double-dots at similar gate voltage. As a result, the energy levels of one electron and two electrons are almost same.

As shown in the inset of Fig. 2.3, the peak shape of Coulomb blockade characteristics are well fitted not by the Lorentzian resonance line shape but by the derivative of the Fermi-Dirac distribution function of electron. This fact indicates that the thermal energy (k_BT) is much larger than the intrinsic level width ($h\Gamma$) in the dot. Since the separation of the single particle energy levels ($\Delta\varepsilon$) and the single electron charging energy (E_C) are larger than the thermal energy at several ten Kelvin ($h\Gamma < k_BT < \Delta\varepsilon, E_C$), the peak height must decrease as the temperature increases reflecting the broadening of the Fermi-Dirac distribution function. However, in the obtained results, the peak heights do not strongly depend on the temperature. This can be explained by the increased conductance of the parasitic MOSFET as the temperature increases.

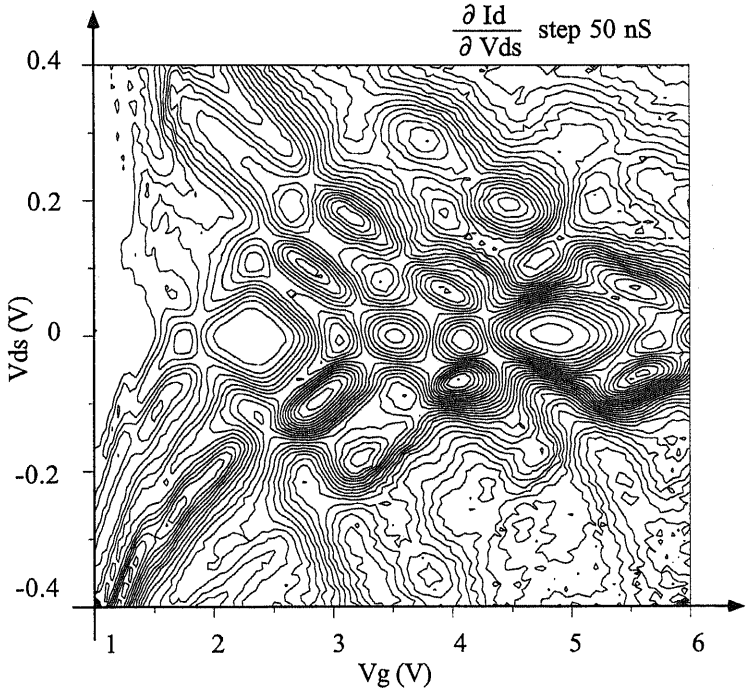
In this device, the NDCs and fine structures are smeared out at 77 K (Figure 2.10). Furthermore, the periodicity of the Coulomb blockade oscillations is improved as the temperature is increased (Fig 2.3). This can be explained as follows. At high temperature, some electron can travel from source to drain via the excited states in the dot even when the μ_s is lower than the excited states in the dot. As the number of the states in the dot used for electron transport increases, the characteristics becomes close to the semi-classical model. This becomes the cause of the smeared fine structure and improved periodicity of the Coulomb blockade oscillations at high temperature. Increased scattering rate of the electron in the dot at high temperature becomes the reason why the NDCs can not be observed as the temperature is increased.

2.6 Comparison with calculated characteristics by the orthodox theory.

For the comparison between the experimental results and the characteristics simulated by semi-classical model (orthodox theory), device characteristics of a single-dot system are simulated by solving the master equation. The single-dot system taking into account



(a)



(b)

Figure 2.10: (a) 3D plot of the I_d as a function of the V_g and V_{ds} at 77 K. The NDCs and fine structures observed at 4.2 K are smeared out by thermal fluctuation. (b) Contour plot of the differential conductance ($\partial I_d/\partial V_{ds}$) as a function of V_g and V_{ds} at 77 K. The device characteristics becomes close to the characteristics simulated by orthodox theory.

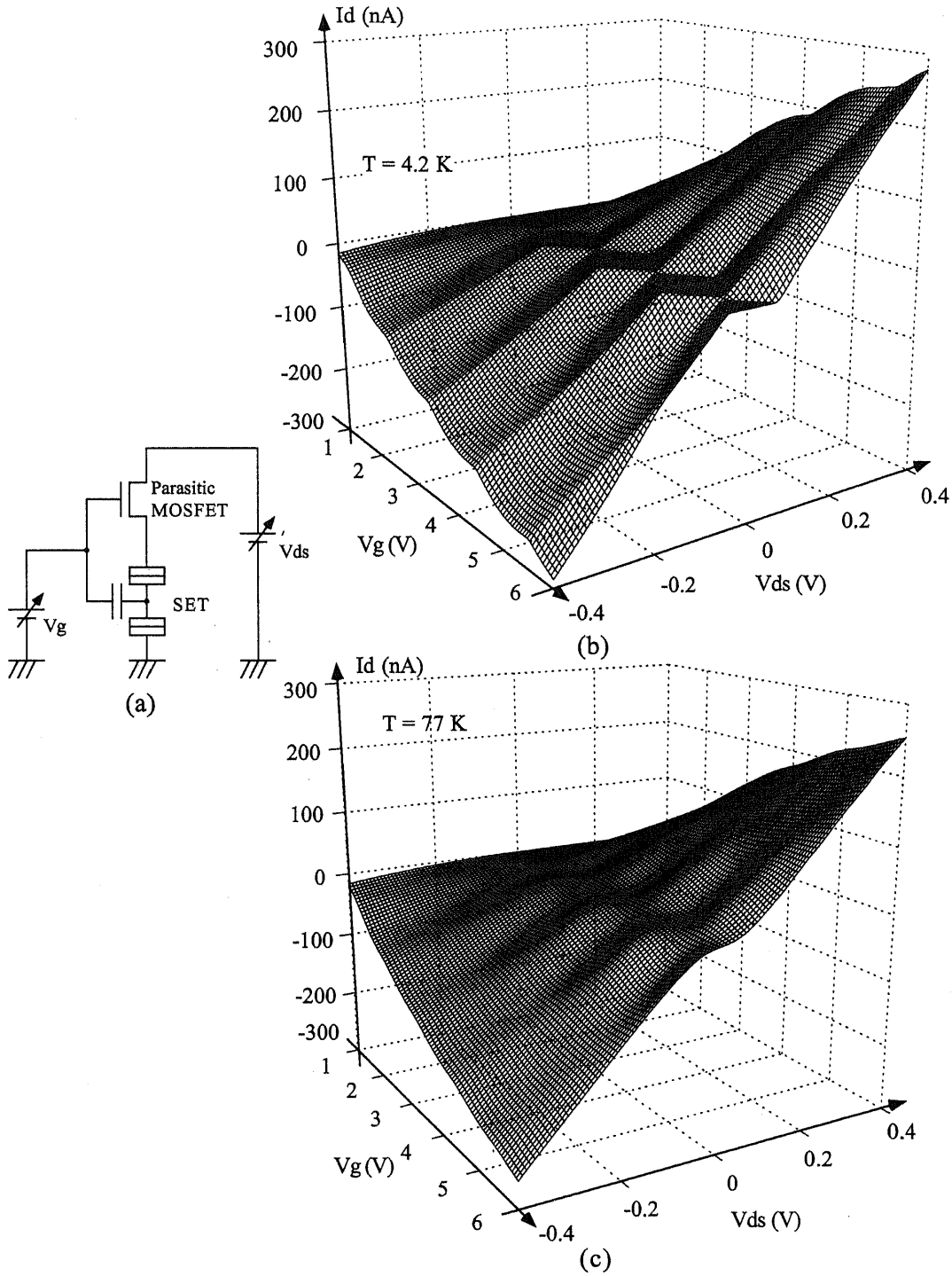


Figure 2.11: 3D plot of the I_d as a function of the V_g, and V_{ds} at (b) 4.2 K and (c) 77 K calculated by solving the master equation based on the orthodox theory. The effects of parasitic MOSFET are modeled in the equivalent circuit as shown in (a). At 4.2 K the characteristic is completely different from the experimental result whereas the characteristics look like each other at 77 K.

the effect of parasitic MOSFET is modeled as Figure 2.11(a). The parameters except the tunnel resistances of the single electron transistor are determined from the measured results.

Fig 2.11(b) and (c) show calculated device characteristics at 4.2 K and 77 K respectively. Since the effect of discreate energy levels is not taken into account in the orthodox theory, the oscillations become periodic. Furthermore, the fine structures and NDCs which is caused by the discreate energy levels are not obtained from the numerical calculations. Therefore, the measured device characteristics and simulated characteristics are completely different at low temperature where the quantum mechanical effects become significant. This result indicates that the evaluation of the device characteristics by orthodox theory becomes inaccurate when the dot size becomes small. Although there are slight difference between the measured characteristics and simulated characteristics even at 77 K, the difference becomes small because of the increased thermal energy compared with the energy level separation in this device. However, the quantum mechanical effects will become more prominent and have a significant influence on the device characteristics as the size of the quantum dots in the single electron devices further decreases.

2.7 Summary

In this chapter, the quantum mechanical effects observed in the silicon single electron transistor operating at high temperature have been described. The devices used for the experiment have been fabricated in the form of point contact MOSFETs using EB lithography and anisotropic wet etching technique. The discussion was based on the Coulomb blockade characteristics caused by the nano-size silicon dot in the extremely narrow (< 10 nm) channel. The aperiodic Coulomb blockade oscillations in $I_d - V_g$ characteristics, the NDCs, and fine structures in $I_d - V_{ds}$ characteristics are observed at low temperatures caused by the quantum mechanical effects. The energy levels in the nano-size silicon dot are extracted from the transport properties of the device. Since the measured characteristics are much different from the theoretical characteristics calculated by semi-classical model, the understanding of the influence of quantum mechanical effects becomes more important for the design of the extremely small single electron devices operating at room temperature.

Several problems are brought up by this experiment. The first one is the validity of the discussions, since the discussions stand on the experimental results of only one sample. Next one is about the mechanism of the dot formation in the nano-size silicon channel. The last one is the evaluation of the quantum mechanical effects from the point that whether it acts as advantage or disadvantage.

In relation to the above points, the following subjects,

1. How to fabricate many devices with uniform nano-size channel for quantitative characterization of single electron devices,

2. How to investigate the origin of the dot formation in silicon nano-size channel,

3. How to prevent or utilize the quantum mechanical effects for device applications,

should be studied.

To answer the first subject, a novel fabrication process for the uniform nano-size channel fabrication without using fine lithography is developed. The obtained results about the relation between the dot size and quantum confinement effects with supports by numerical calculations are described in the next chapter. For the second subject, devices to characterize single electron and single hole tunneling phenomena in the same channel are fabricated. Discussions on the origin of the tunnel barriers and dot formation in the nano-size silicon channel are mentioned in Chapter 4. To provide one of the solution for the final subject, peak adjustment of Coulomb blockade oscillations of single electron transistors using charge injection into the silicon nano-crystals on the device are proposed. The results are given in Chapter 5.

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Chapter 3

Relation between quantum confinement effects and silicon dot size

3.1 Introduction

Silicon new concept devices which utilize the single electron charging effects[1-3] have been intensively investigated. Such devices require nano-scale channels or dot structures for high temperature device operation. For application to integrated circuits or investigation of fundamental physics, uniform fabrication of nano structures is strongly desired. Even though fine lithography such as electron beam lithography has improved, it is not sufficient for fabricating uniformly nano structures with wafer-scale. Furthermore, it requires a great deal of cost and time.

Previously, the fabrication technique[4, 5] of silicon quantum wire without using fine lithography developed in our laboratory was reported. Although the width of the silicon wire was determined by the thickness of the surface Si layer and the nano-scale narrow channel could be easily formed, fine lithography had to be used to reduce the length of the channel in the process. Metal-oxide-semiconductor field-effect-transistors (MOSFETs) with wire channels showed Coulomb blockade oscillations even at room temperature.[5] However, it turned out that the channel was a multiple-dot system because the channel length was long even when a fine lithography was used.[5] Point contact structure

is the shortest limit of the channel length, where the single electron tunneling phenomena through a single dot are clearly observed[6] as described in the previous chapter. Since the point contact channels fabricated using electron beam lithography[6] result in large variations of channel width, a fabrication process for uniform point contact channels without using fine lithography is desired.

In this chapter, novel fabrication process of nano-scale point contact channel MOSFETs using only the usual lithography technique is proposed. The process utilizes SiO_2/Si_3N_4 double layer mask, anisotropic wet etching, and selective oxidation on the silicon-on-insulator (SOI) substrate. The width of the point contact channel is determined only by the thickness of the surface Si layer. Furthermore, the distance between the source and drain is extremely small because of its channel shape. The uniformity of the fabricated nano-scale channels has been evaluated from the experimental results. Based on the Coulomb blockade characteristics in the fabricated devices, relation between the quantum confinement effects and dot size is discussed. Numerical calculations are also carried out to support the experimental results.

3.2 Fabrication of nano-size point contact channel without using fine lithography

Fabrication process of the point contact structure is shown in Figure 3.1. The fabrication process is developed by modifying the fabrication technique of Si nano-size channel which is based on the combination of selective oxidation and anisotropic wet etching. The newly developed fabrication process is based on the combination of SiO_2/Si_3N_4 double layer mask, anisotropic wet etching, and selective oxidation. The technique makes it possible to form a nano-size point contact channel whose width is determined by the thickness of surface silicon layer, and therefore, does not require any fine resolution lithography apparatus. Wafer scale uniformity of the channel width can be obtained. Furthermore, the distance between the source and drain is extremely short, which is very appropriate for the experiments on single dot system.

In the same way of the device fabrication described in Chapter 2, SOI substrates prepared by the separation-by-implanted-oxygen (SIMOX) technique are employed. The substrates are (100) oriented, p-type with resistivity of 20 $\sim$ 30 Ωcm. The thicknesses

of the SOI and the buried oxide (BOX) layer are 168 nm and 106 nm, respectively. The anisotropic wet etching technique by Tetramethylammonium-hydroxide (TMAH)[4-6] is used for the formation of the point contact channel.

First, the surface Si layer of the SIMOX wafer is thinned by thermal oxidation and subsequent wet etching. To change the width of the point contact channel, several wafers with different thicknesses of the surface Si layer are prepared. Then, a 20 nm-thick Si_3N_4 film is deposited by low-pressure-chemical-vapor-deposition (LPCVD). The Si_3N_4 film is patterned in a rectangular shape using the usual photo-lithography and dry etching. The longer sides of the rectangle are parallel to the (110) direction. Then, a 20 nm-thick SiO_2 film is deposited by LPCVD, and again, patterned in a rectangular shape with the longer sides parallel to the $(\bar{1}10)$ direction by the usual photo lithography and chemical dry etching. The SiO_2 rectangular pattern is at right angles to the Si_3N_4 rectangular pattern. In this way, a SiO_2/Si_3N_4 double layer mask is formed (Fig. 3.1(a)). The SiO_2 single layer mask, Si_3N_4 single layer mask, and the region with bare Si surface are also formed as shown in Fig. 3.1(a).

Next, anisotropic wet etching of the surface Si layer is performed using TMAH at 75 °C. Only the bare Si region is etched and the etching automatically stops when the Si {111} facets appear at each side of the mask (Fig. 3.1(b)). Then, the Si_3N_4 film is removed by dry etching (Fig. 3.1(c)) followed by the removal of the SiO_2 film of the mask by buffered HF. Only the part of the Si_3N_4 film that had been covered by the SiO_2 film remains (Fig. 3.1(d)). Then, the surface Si region where the Si_3N_4 does not cover is thermally oxidized to 20 nm (Fig. 3.1(e)) and the Si_3N_4 film is removed by H_3PO_4 at 180 °C resulting in the exposure of the Si bare surface where the Si_3N_4 covered. After that, the second anisotropic etching by TMAH is performed. At this step, the point contact channels are formed at the intersection of each long side of the rectangles and the etching automatically stops (Fig. 3.1(f)).

Figures 3.2(a) and (b) show schematics of the enlargement and the cross-sectional view of the point contact channel, respectively. The cross section of the most constricted part of the point contact channel becomes a right-angled triangle. As shown in the figure, the width (W) of the point contact channel is just double of the surface Si layer thickness (t). Therefore, W depends only on t, and it does not require any fine lithography technique

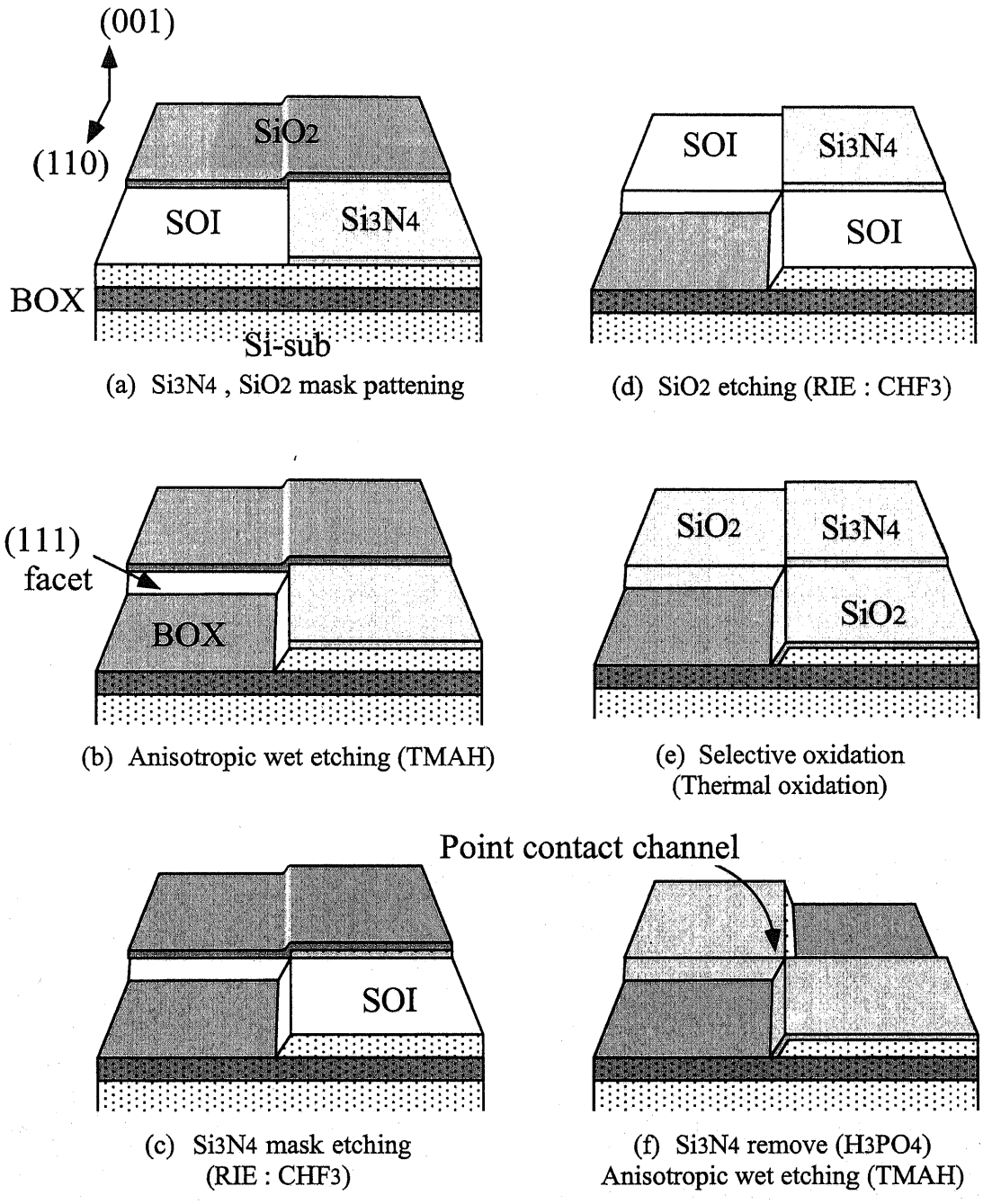

Figure 3.1: Fabrication process of the Si nano-scale point contact channel MOSFETs. It bases on the combination of SiO_2/Si_3N_4 double layer mask, anisotropic wet etching, and selective oxidation.

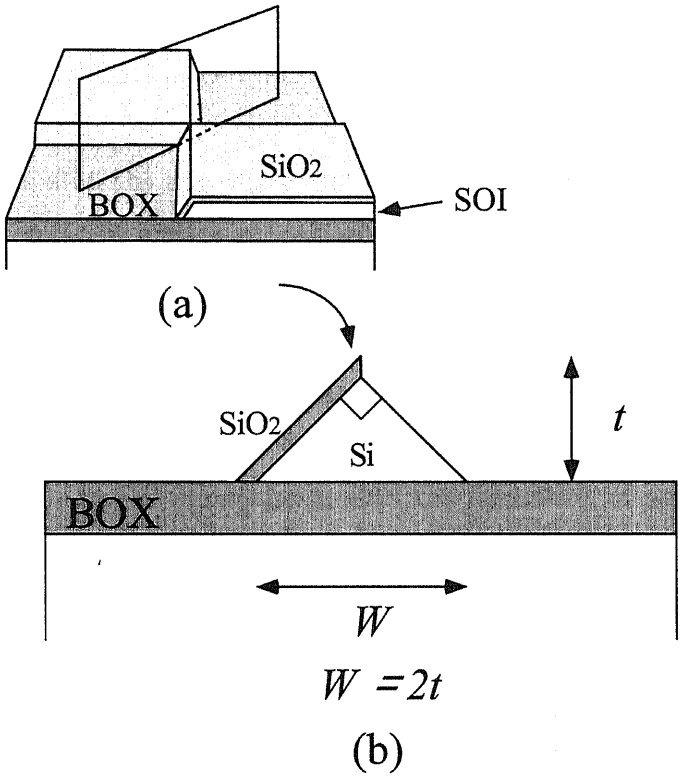

Figure 3.2: (a) Schematic view of a part of the point contact channel. (b) Cross-sectional view of the point contact channel.

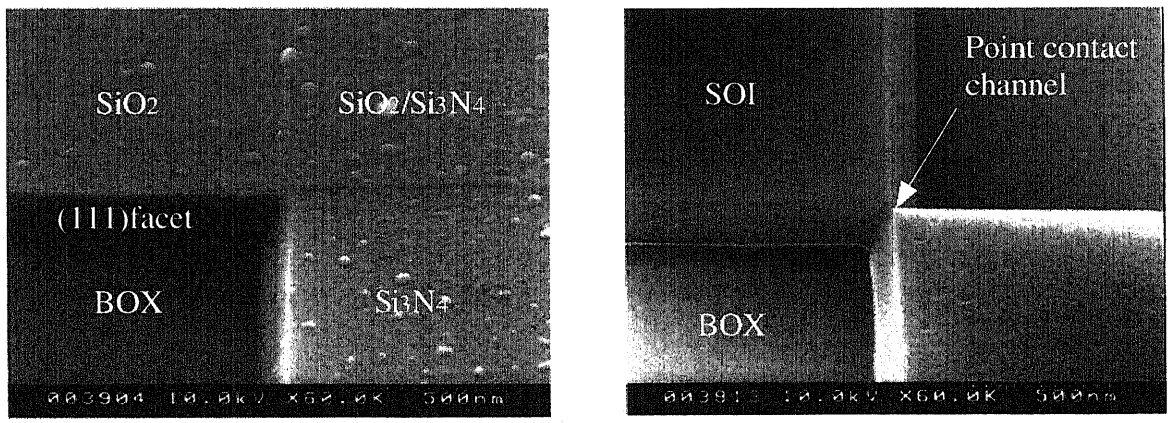

Figure 3.3: Scanning electron micro-graphs of the fabricated point contact channel. (a) A micro-graph taken after the step of Fig. 3.1(b). (b) Fabricated point contact structure.

such as electron beam lithography to fabricate nano-scale channels. Furthermore, this shape of the point contact is preferable for the investigation of the nano-scale channel because the distance between source and drain is extremely small.

Figure 3.3 shows the scanning electron micro-graphs of the fabricated point contact channel (just after the step (b) and (f) in Fig. 3.1). The thickness of the surface Si layer after the first oxidation is 100 nm. A very sharp point contact channel defined by Si {111} facets is successfully fabricated using only the usual photo lithography technique.

For the characterization of the nano-size point contact channel, MOSFET structures are formed. For this purpose, a cross shaped SiO_2/Si_3N_4 double layer mask is formed (Figure. 3.4(a)). In this case, four point contacts are formed at each cross point of double layer mask (Fig. 3.4(b)). In this experiment, after the formation of point contact channel, three types of ions (oxygen, phosphorus, and boron) are implanted into the channel with various amount of dose for the evaluation of the influence of impurity ions on the device characteristics. To characterize the four point contacts independently, four separate gate electrodes are formed (Fig. 3.4(c)) using the usual fabrication process for MOSFETs described as follows. The gate oxide is formed by thermal oxidation at 1000 °C. The oxide thickness of the (100) surface is 50 nm. The width of the point contact channel is further narrowed by thermal oxidation. Gate electrodes are formed by 200 nm poly-Si deposition and dry etching. Phosphorus ions (P^+) are implanted into the source, drain, and gate areas at an acceleration voltage of 45 keV and with a dose of $5 \times 10^{15} cm^{-2}$, before the annealing in dry N_2 atmosphere at 950 °C for 20 min. Contact holes are formed and the pad metal is evaporated. For more detail of the fabrication process of the point contact MOSFETs, see Table 3.1.

SEM images of completed point contact MOSFET are shown in Figure 3.5. From the enlargement of the part of point contact channel, it can be seen that a nano-size point contact channel is successfully formed.

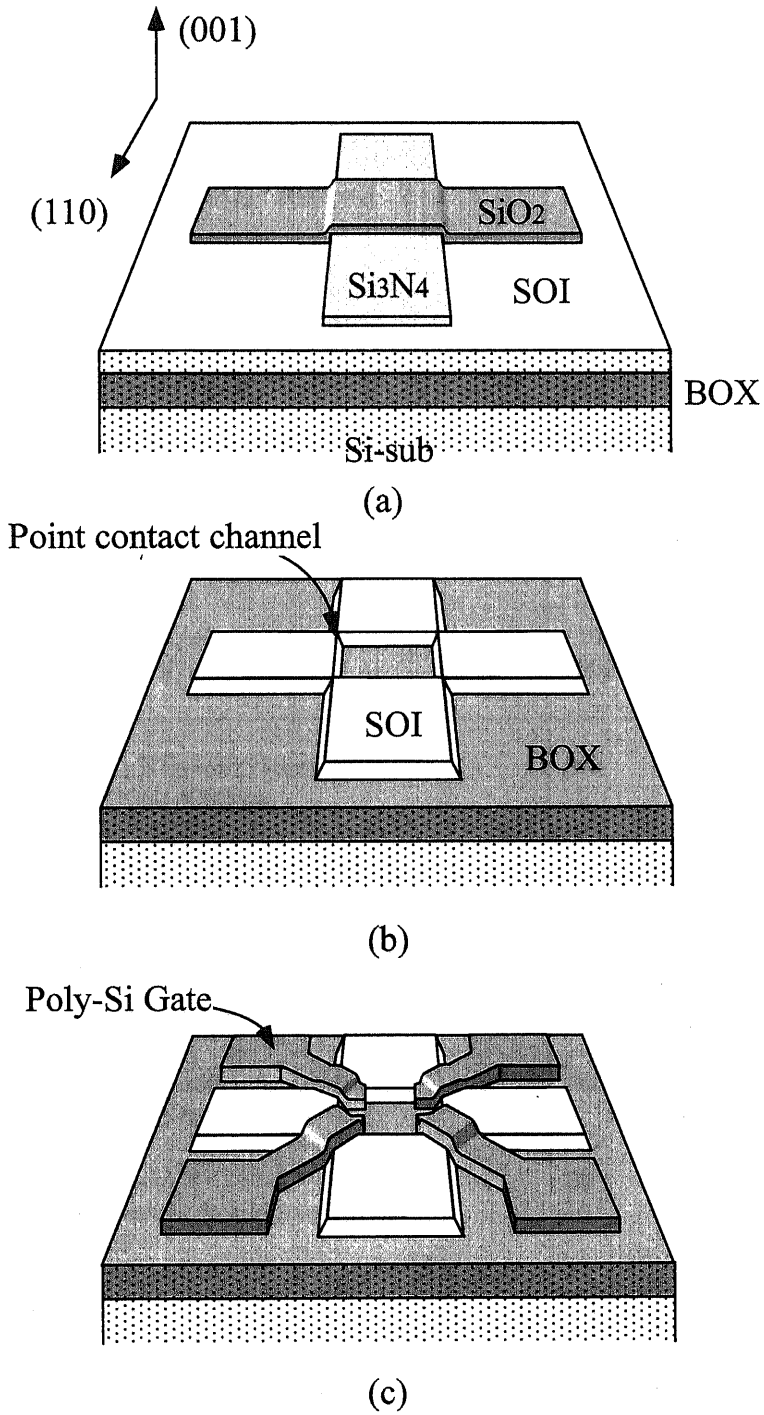

Figure 3.4: Fabrication process of the device for the characterization of the point contact channel. Four point contact channels are formed which can be controlled independently by four separate poly-Si gates.

Table 3.1: Conditions of the fabrication process of nano-scale point contact MOSFETs without using fine resolution lithography.

step	condition	temperature (°C)	time (min)	thickness (nm)	remark
Dicing	2cm×1.5cm (Low dose SIMOX)				
Wafer cleaning	$NH_4OH : H_2O_2 : H_2O = 1 : 2 : 8$ (SC1)	75	10		
SiO_2 remove	BHF				
RCA cleaning	DI water (DeIonized water)		3		
	$HF : H_2O = 1 : 100$		dip		
	DI water		3		
	$NH_4OH : H_2O_2 : H_2O = 1 : 2 : 8$ (SC1)	75	20		
	DI water		3		
	$HF : H_2O = 1 : 100$		1		
	DI water		3		
	$HCl : H_2O_2 : H_2O = 1 : 2 : 8$ (SC2)	75	20		
	DI water		3		
	$HF : H_2O = 1 : 100$		1		
	DI water		3		
Oxidation	$O_2 : 1.0l/\text{min}$	1100	140		
	$N_2 : 1.0l/\text{min}$	1000	5		
SiO_2 remove	BHF				
Si_3N_4 deposition	SiH_4:NH_3=40:150sccm 0.5Torr	800	7	20	
Photo lithography	AZ1350 4000rpm		40sec	400	
(Si_3N_4 mask)					
	Prebake	90	25		
	Exposure,development,rinse				
Si_3N_4 etching	CHF_3=40sccm 10mTorr 100W	20	1		
	O_2=70sccm 100mTorr 100W	20	1		*1
Resist remove	Acetone				
SPM cleaning	$H_2SO_4 : H_2O_2 = 3 : 1$	125	10		
SiO_2 deposition	SiH_4:O_2=80:100sccm 0.3Torr	600	13	22	
Photo lithography	AZ1350 4000rpm		40sec	400	
(SiO_2 mask)					
	Prebake	90	25		
	Exposure,development,rinse				
Pattern transfer	BHF		20 sec		
Resist remove	Acetone				
Anisotropic etching	TMAH (15%)	75	15sec		
Si_3N_4 etching	CHF_3=40sccm 10mTorr 100W	20	0.5		
	O_2=70sccm 100mTorr 100W	20	1		
SPM cleaning	$H_2SO_4 : H_2O_2 = 3 : 1$	130	10		
SiO_2 remove	BHF		12 sec		
RCA cleaning	Same as previous RCA cleaning		3		
Oxidation	$O_2 : 1.0l/\text{min}$	950	20	17	
SiO_2 removal	HF:H_2O=1:50		10 sec		*2
Si_3N_4 remove	H_3PO_4	180	5		

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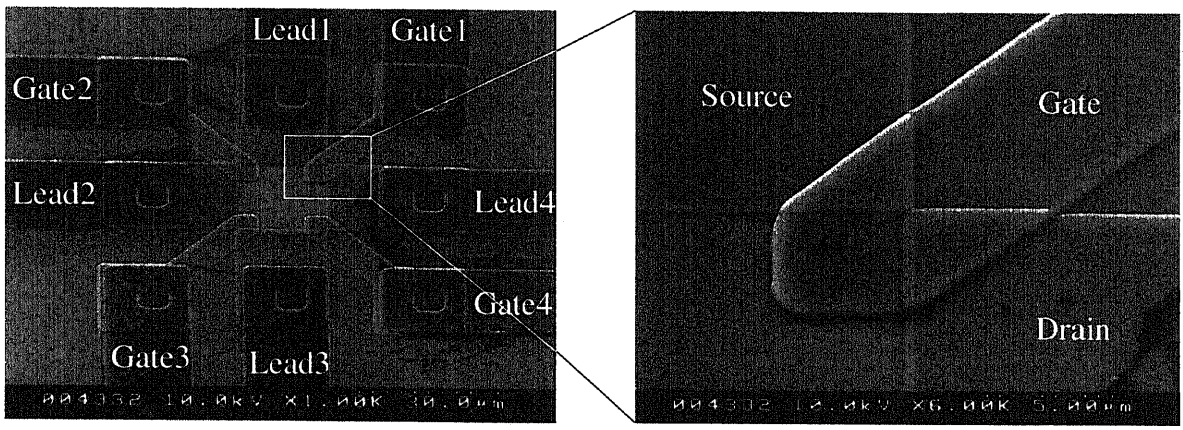
Anisotropic etching (Ion implantation)	TMAH (15%)	75	15sec		*3
SiO_2 remove	HF:H_2O=1:10		25 sec		
RCA cleaning	Same as previous RCA cleaning		3		
Gate oxidation	O_2 : 1.0l/min	1000	50	50	
	N_2 : 1.0l/min (Annealing)	1000	5		
Poly-Si deposition	SiH_4 200sccm 0.1Torr	600	30	20	
Photo lithography (gate)	AZ1350 3000rpm		40sec	400	
	Prebake	90	25		
	Exposure,development,rinse				
Gate RIE	SF_6 0.013Torr 100W 40sccm	0	15sec		
	SF_6 0.15Torr 25W 70sccm	0	90sec		
Resist remove	Acetone				
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	130	15		
Ion implantation source, drain, gate	P^+ 45keV $5\times10^{15}cm^{-2}$ $I_{beam} = 35\mu A$		$\sim$ 60		
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	130	15		
Passivation SiO_2 deposition	SiH_4:O_2 = 200 : 100sccm 0.3Torr	600	7.5	350	
Annealing	N_2 : 1.0l/min	950	30		
Photo lithography (contact hole)	AZ1350 3000rpm		40sec	400	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	130	20		
Contact hole etching	BHF		3		
Resist remove	Acetone				
Al evaporation				170	
Photo lithography (Al electrode)	AZ1350 3000rpm		40sec	400	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	130	20		
Al etching	$H_3PO_4 : CH_3COOH : HNO_3 : H_2O$ = 75:15:5:5	37	75 sec		
Resist remove	Acetone				

*1 To remove the polymer deposited on the wafer during the dry etching.

*2 Because the surface of Si_3N_4 film is slightily oxidized.

*3 To investigate the influence of impulity in the channel, three types of ions are implanted in several samples the following conditions.

O^+, 25 keV, 5×10^{13} cm^{-2}, 5×10^{14} cm^{-2}
P^+, 35 keV, 1×10^{12} cm^{-2} 1×10^{13} cm^{-2}
BF_2^+, 45 keV, 1×10^{13} cm^{-2}, 1×10^{14} cm^{-2}



(a) (b)

Figure 3.5: (a) Scanning electron micro-graph of the fabricated point contact MOSFETs. (b) Enlarged point contact channel. Although the width of the point contact channel seems wide in the micro-graph due to the gate poly-Si and passivation oxide, actual size of the channel is narrower than 30 nm.

3.3 Coulomb blockade characteristics in the devices with various dot size

To evaluate the uniformity of the fabricated point contact channels, the gate voltage (V_g) dependence of the drain current (I_{ds}) are characterized at room temperature. The devices on the same wafer whose average channel width is less than 30 nm are characterized. Figure 3.6 shows the semi-log plot of the $I_d - V_g$ curves of 10 channels. The devices without ion implantation into the channel are used. The drain voltage (V_{ds}) is kept at 100 mV. Most of the channels have almost identical characteristics and are denoted as type A in Fig. 3.6, which suggests that the variation of the channel width from device to device is very small. The variation of the trans-conductance, which is strongly related to the uniformity of the channel width, is about 10 %. Considering that the channel widths are less than 30 nm, it can be said that the channels are uniformly fabricated. Although a few devices (type B in Fig. 3.6) show very low trans-conductance, which indicates that the channel widths are reduced unintentionally, the uniformity can be improved when the process conditions are optimized.

Then, using the cryostat probe station, the devices were cooled down to the base

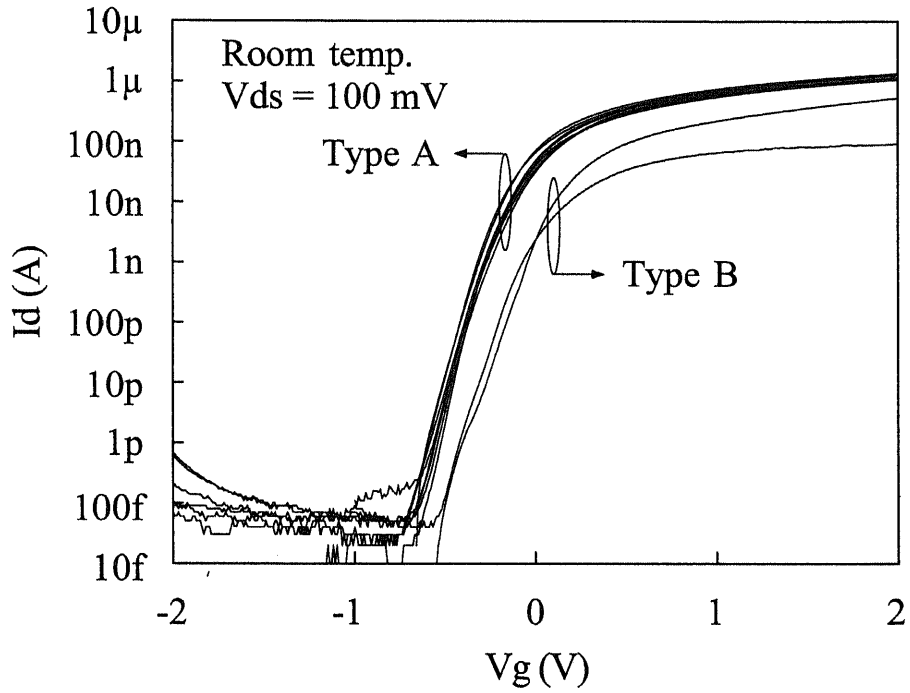


Figure 3.6: Dependence of the drain current (I_d) on the gate voltage (V_g) at room temperature. The drain voltage (V_{ds}) is fixed at 100 mV. The experimental results of 10 samples are indicated.

temperature of the equipments (21 K) and dc-characteristics were measured by HP4156A. Figure 3.7 shows the $I_d - V_g$ characteristics of three samples. V_{ds} was kept at 1.0 mV. Many samples show usual MOSFET characteristics like the curve A-1. However, even if the devices show usual MOSFET characteristics at room temperature, some of them show periodic oscillations like the curves A-2. These oscillations are attributed to the Coulomb blockade of single electron tunneling. Because only the devices with very narrow channel width showed Coulomb blockade oscillations,[6] the dot structures that weakly confine the electrons are formed in the constricted part of the point contact channel. This result suggests that the potential fluctuations in the channel which do not affect the transport properties at room temperature can influence the device characteristics as the temperature is decreased. As for the devices with low conductance at room temperature, Coulomb blockade oscillations with large peak to valley ratios like curve B-1 in Fig. 3.7 are observed. It should be noted that the oscillations with large peak to valley ratio is aperiodic which is the same as the experimental results in previous chapter. Single

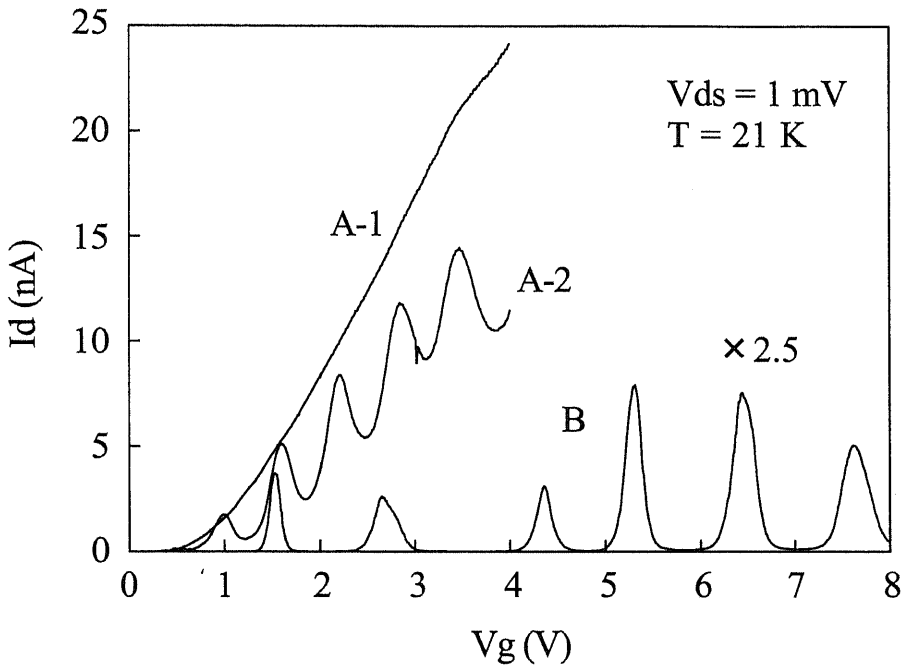


Figure 3.7: $I_d - V_g$ characteristics at low temperature (21 K). The drain voltage (V_{ds}) is fixed at 1.0 mV.

electron tunneling phenomena caused by the potential fluctuations in the channel are thought to affect the transport properties at higher temperatures as the channel width is decreased.

In this experiment, Coulomb blockade oscillations can be observed in all the samples when the channel width becomes extremely narrow and the influence of the impurity ions implanted into the channel could not be observed. One reason is that the donor or acceptor impurities are not ionized at low temperature because of the relatively small amount of dose and act as neutral impurities which have a slight influence on the channel potential. There are also some devices with characteristics that originate from multiple-dot structures or single tunnel barrier. Interesting features of transport properties in the multiple-dot systems are discussed in Appendix A, using the experimental results in quantum wire MOSFETs and numerical calculations. For the simplicity, only the device characteristics that originate from single dot systems are discussed in the following.

To evaluate the relation between the periodicity of the oscillations and the single electron charging energy, and subsequently the relation between the quantum confinement

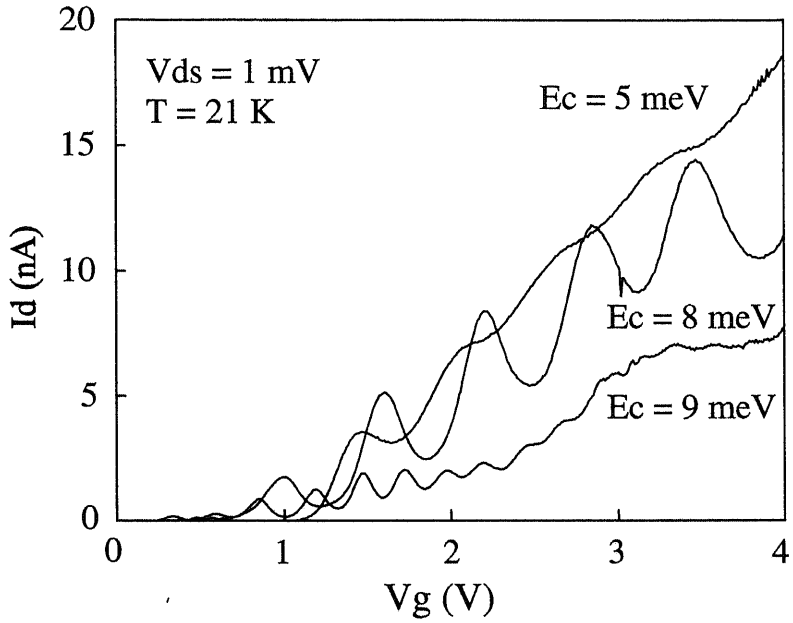


Figure 3.8: Periodic Coulomb blockade oscillations with small single electron charging energy. The single electron charging energy denoted in the figure are estimated from the fitting of measured curves with calculated curves.

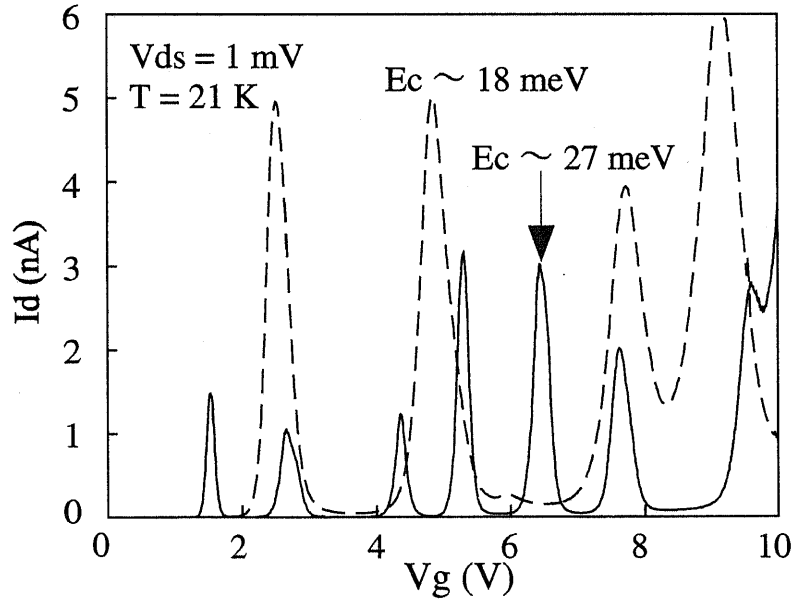


Figure 3.9: Aperiodic Coulomb blockade oscillations with large single electron charging energy. The charging energy is estimated from the minimum interval between the peaks of Coulomb blockade oscillations.

effects and the dot size, charging energy of the devices with Coulomb blockade oscillations are estimated.

Figure 3.8 shows some examples of the device characteristics with periodic Coulomb blockade oscillations. Single electron charging energies denoted in the figure are estimated by fitting the measured curves with numerically simulated characteristics. The charging energies are also estimated by the peak to valley ratios. Furthermore, it is determined by the ratio of peak width and oscillations period. From the evaluated charging energy, it is found that the periodic oscillations are caused by the dot whose charging energy is less than 10 meV. The dot size whose charging energy is less than 10 meV is much larger than 20 nm, and the separation of single particle energy levels in such relatively large dot is much smaller than the charging energy. As explained in the previous chapter, since the interval between the peaks are approximately determined by the sum of the single electron charging energy and single particle energy level separation by quantum confinement effects, the Coulomb blockade oscillations become quasi-periodic as long as the charging energy is much larger than the single particle energy level separation.

Examples of the device characteristics with aperiodic Coulomb blockade oscillations are also shown in Figure 3.9. In the devices with aperiodic oscillations, it is difficult to evaluate the single electron charging energy because the characteristics obtained in the experiments are much different from the numerically calculated results by semi-classical model. In this experiment, the minimum intervals between the peaks are used for the estimations of charging energy. From the figure, it is noticed that the aperiodic oscillations are apparent when the charging energy reaches around 20 meV. From a rough estimations, the dot size whose charging energy is 20 meV is smaller than 20 nm. The energy level separation in such small dot is larger than 5 meV. In this regime, the energy level separation by quantum confinement effects can not be neglected. Because the energy level separation depends on the number of electron in the dot whereas the charging energy is nearly constant, the periodicity is broken when the single particle energy level separation becomes large compared with the charging energy.

As mentioned in Chapter 2, the other features of quantum mechanical effects can be observed. Figure 3.10 shows contour plot of the differential conductance ($\partial I_{ds}/\partial V_{ds}$) as a function of V_g and V_{ds} at 21 K. Negative differential conductances (NDCs) and fine

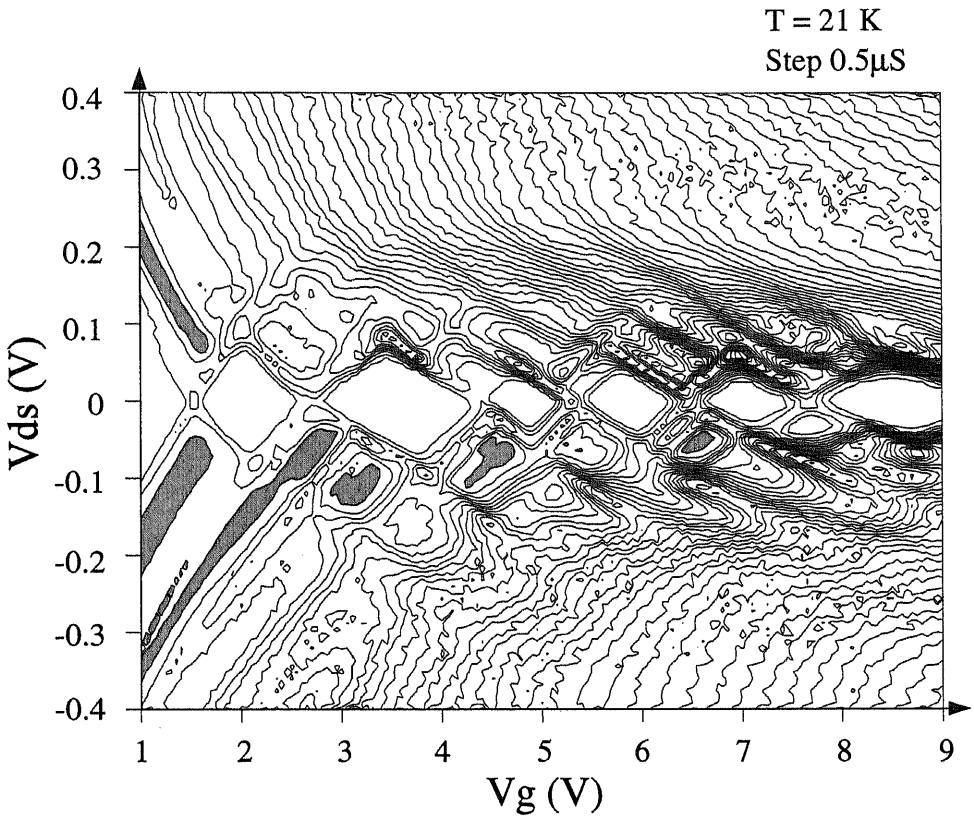


Figure 3.10: Contour plot of the differential conductance ($\partial I_{ds}/\partial V_{ds}$) as a function of V_g and V_{ds} at 21 K. The hatched areas indicate the NDCs and dotted areas show the fine structures.

structures which originate from the sparse energy levels in the lead and Si dots are also observed in this device. These kind of features are common in the other device with large charging energy and small dot.

Even though the gate voltage is increased and the characteristics are measured at a larger conductance regime, the phenomena of conductance quantization can not be observed. This may be caused by the relatively high temperature and high scattering rate by the potential fluctuation.

3.4 Calculation of energy levels in nano-size silicon dots

Effective mass Schrödinger equation solved by finite element method

From the previous experimental results, it is found that the aperiodicity of Coulomb blockade oscillations becomes apparent when the single electron charging energy gets around 20 meV. Furthermore, in the device with Coulomb blockade oscillations observed at high temperature, negative differential conductances and fine structures are observed in $I_d - V_{ds}$ characteristics. Although qualitative discussions were made from experimental results, it is difficult to estimate the influence of quantum confinement effects quantitatively. One of the reasons which makes it difficult is that the anisotropic effective mass of carrier in silicon.[7] To support the experimental results and to investigate the energy levels in silicon nano-size dots, numerical calculations were carried out.

There are some approaches to calculate the electronic structures in quantum dot such as effective mass approximation,[8] truncated crystal method,[9] and direct molecular calculations[10,11]. In the effective mass approximation, periodic lattice potential is replaced by constant potential and the kinetic energy operator is replaced by an effective mass operator derived from parabolic expansion of the bulk band structure. In the truncated crystal method, wave functions in the quantum dot are approximated by a linear combination of a few bulk Bloch wave functions. In the direct molecular calculations, the Hamiltonian consisting of the full kinetic energy and quasi-periodic potential is diagonalized. In usual, tight binding model in which a small implicit basis set is used or linear combination of atomic orbital (LCAO) method in which explicit basis functions are used. Pseudo-potential method[10-12] in which the total screened potential by a superposition of atomic pseudo-potentials are also used.

In each approach, there are advantages and disadvantages. Improvement in accuracy requires more calculation time. Therefore, the appropriate method should be selected depending on a problem. Usually the effective mass approximation is used in relatively large systems (larger than $3 \sim 4$ nm) because it does not require so many computer resources. On the other hand, the truncated crystal method or direct molecular calculations

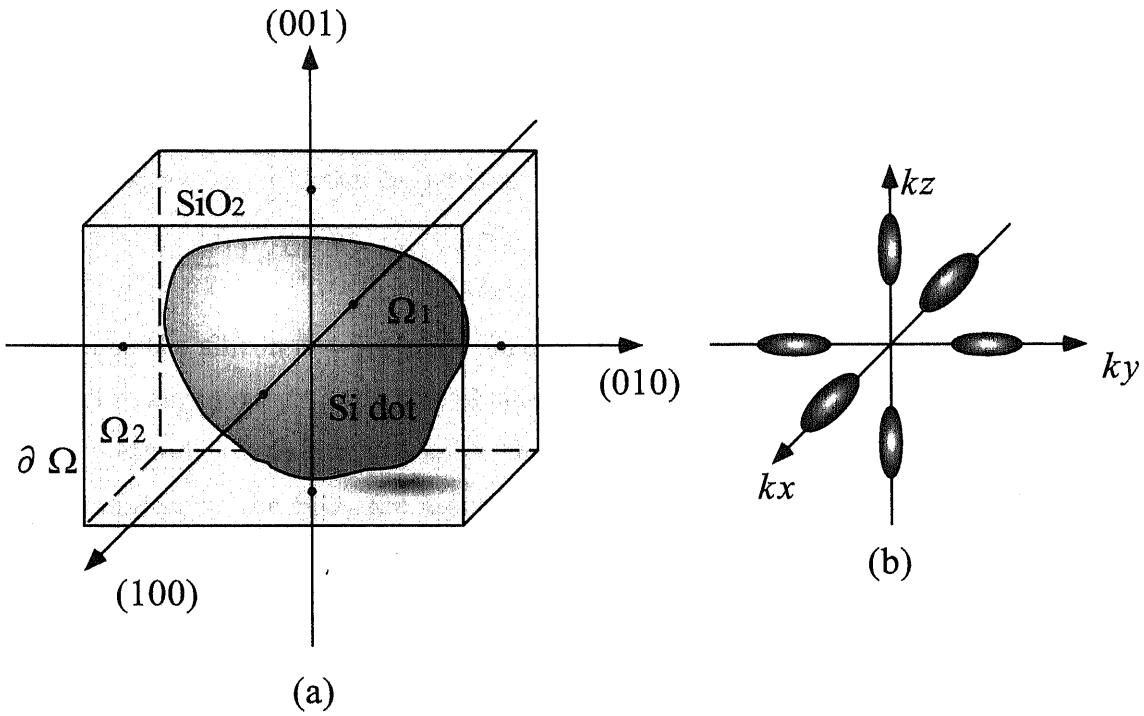


Figure 3.11: (a) Si dot surrounded by SiO_2 used in the calculation of energy levels. Three dimensional Schrödinger equations based on the effective mass approximations are solved. (b) Anisotropy of effective mass of the electrons in bulk silicon is taken into consideration.

are used in the investigations of small systems (smaller than 3 nm), because it becomes difficult to use the bulk band structure in such ultra small systems. In this study, the electronic structure in the silicon dot in which the quantum confinement effects become a problem must be evaluated. In other words, the silicon dot with size from 20 nm to several nm should be calculated. Therefore, in this study, the effective mass approximation are adopted for the calculation of electronic structure in the dot.

Three dimensional stationary state Schrödinger equations

$$\left(-\frac{\hbar^2}{2}\nabla \otimes M^{-1}\nabla + V(\boldsymbol{r})\right)\psi(\boldsymbol{r}) = \varepsilon\psi(\boldsymbol{r}) \tag{3.1}$$

where the M is the effective mass tensor, are solved. Anisotropy of the effective mass of carrier is taken into account. If the x, y, and z axes are taken along the (100), (010), and (001) direction respectively, the non-diagonal elements of the matrix become zero and the

effective mass tensor can be written as

$$M = \begin{pmatrix} m_{xx} & 0 & 0 \\ 0 & m_{yy} & 0 \\ 0 & 0 & m_{zz} \end{pmatrix}. \tag{3.2}$$

Therefore Equation (3.1) can be written as

$$\left[-\frac{\hbar^2}{2} \left(m_{xx}^{-1} \frac{\partial^2}{\partial x^2} + m_{yy}^{-1} \frac{\partial^2}{\partial y^2} + m_{yy}^{-1} \frac{\partial^2}{\partial z^2} \right) + V(\boldsymbol{r}) \right] \psi(\boldsymbol{r}) = \varepsilon \psi(\boldsymbol{r}). \tag{3.3}$$

Since the silicon dot naturally formed in the nano-size channel may be irregular in shape, arbitrary geometry and size of silicon dots must be treated. For this reason, finite element method is employed to solve the Equation (3.3). As shown in Figure 3.11, Si dot surrounded by the SiO_2 are assumed and the Equation (3.3) are solved on Dirichlet condition ($\psi(\boldsymbol{r}) = 0$) at boundary ($\partial\Omega$) of SiO_2. In the calculation, potential in the Si dot (Ω_1) is defined 0 eV and the potential in the SiO_2 (Ω_2) is assumed to be 3.1 eV or infinite depending on the problem. Only the single particle energy levels are calculated and many body effects are not taken into account. Detailed procedure of the calculation is explained in Appendix B.

First, accuracy of the calculations are evaluated using a simple cubic silicon dot. A cubic dot defined by {100} facet with 10 nm in size is assumed. If the infinite potential is assumed outside of the silicon dot, the weve functions and energy levels in the silicon dot can be theoretically expressed as

$$\psi(\boldsymbol{r}) = \sqrt{\frac{8}{l^3}} \sin\left(\frac{\pi}{l} n_x x\right) \sin\left(\frac{\pi}{l} n_y y\right) \sin\left(\frac{\pi}{l} n_z z\right) \tag{3.4}$$

$$\varepsilon_{n_x, n_y, n_z} = \frac{\hbar^2 \pi^2}{2l^2} \left(\frac{n_x^2}{m_{xx}} + \frac{n_y^2}{m_{yy}} + \frac{n_z^2}{m_{zz}} \right), \tag{3.5}$$

where the l is the dot size and (n_x, n_y, n_z) is the mode index of energy states.

From the Table 3.2, in which the calculated and theoretical values of energy levels in 10 nm size cubic dot are listed, it is found that the accuracy of the calculated single particle energy levels in the Si dot depends on their mode. The larger the number of mode index is, the larger the discrepancy from the theoretical values becomes. To suppress the error in calculation of the energy levels within 5 %, the number of division should be larger than three times of the number of mode index. The difference between the energy levels of the dot with and without SiO_2 are also evaluated (Table 3.3). When the dot

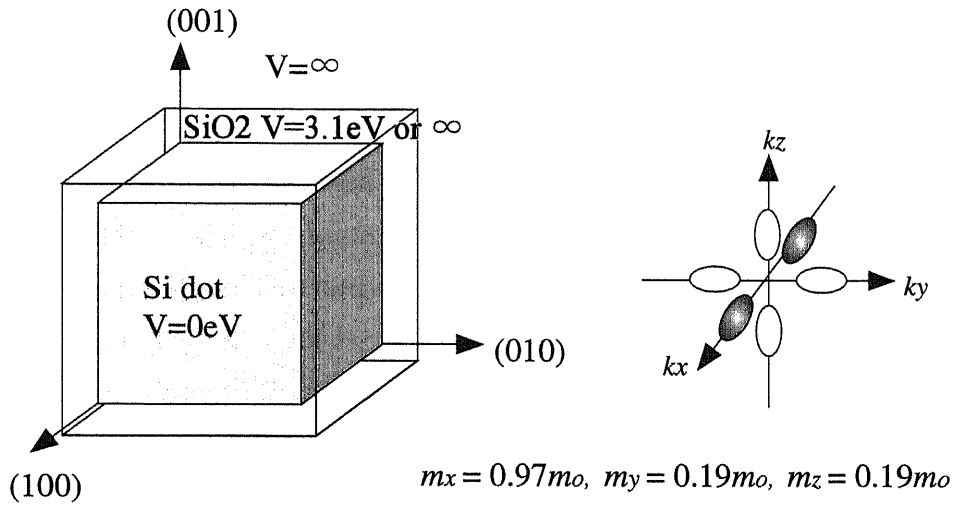


Figure 3.12: The cubic dot used for the evaluation of the accuracy of numerical calculations. Anisotropic effective mass of the electron in k_x valley is used. The energy levels in the Si dot surrounded by SiO_2 are also calculated.

Table 3.2: Comparison between the calculated results and theoretical values of the energy levels in a 10 nm-size cubic dot without SiO_2 layer.

	0	1	2	3	4	5	6	7
Mode (n_x, n_y, n_z)	(111)	(211)	(311)	(121)	(112)	(411)	(221)	(212)
Theoretical (meV)	43.5	55.2	74.6	103	103	102	115	115
Numerical (meV)	43.8	55.9	77.4	106	106	110	118	118
Deviation (%)	+0.7	+1.3	+3.8	+2.9	+2.9	+7.8	+2.6	+2.6

Table 3.3: Comparison between the calculated values of the energy levels in a 10 nm and 5 nm-size cubic dot with and without SiO_2 layer.

	0	1	2	3	4	5	6	7
	10 nm dot							
With SiO_2 (meV)	41.4	53.3	74.5	99.4	99.4	107	111	111
Without SiO_2 (meV)	43.8	55.9	77.4	106	106	110	118	118
Difference (%)	+5.8	+4.9	+3.9	+6.6	+6.6	+2.8	+6.3	+6.3
	5 nm dot							
With SiO_2 (meV)	158	205	289	376	376	416	424	424
Without SiO_2 (meV)	175	224	310	423	423	442	471	471
Difference (%)	+11	+9.3	+7.3	+13	+13	+6.3	+11	+11

size is relatively large, for instance, the dot size is 10 nm the difference between the levels in each dot is about 5 %. However, if the dot size becomes smaller, the energy levels in the dot without SiO_2 is 10 % larger than those in the dot with SiO_2. In the small dots, penetration of the wave function into SiO_2, which reduces the energy levels, cannot be neglected. From above obtained results, it can be said that one can obtain accurate results if the dots are divided into a number of finite element three times larger than the mode index of eigen state. Furthermore, if the dot size is about 10 nm, approximation by infinite potential outside the dot is appropriate whereas the error in calculations becomes large if the dot size becomes smaller.

Dependence of energy levels on the orientation and shape of silicon dot

Standing on the above results, calculations of the energy levels with more complicated situations are carried out. Figure 3.13 shows the energy level dependence on the orientation of Si dot. Cubic silicon dot with 10 nm side is assumed. Since the effect of penetration of wave function into SiO_2 are small in this size, the infinite potential is used outside the Si dot. The θ is defined as the angle of the dot from the (100) direction. The effective mass of electron in the valley locates at k_x axis is used for the calculations. The energy levels of the electron in the valley locates at k_y is symmetric with that of the electron in the k_x valley. The energy levels of the electron in the valley locates at k_z valley does not affected by the orientation of the dot. From the calculated results, separation of the single particle energy levels between the ground state and first excited state is larger than 10 meV. It should be noted that only the change in the dot orientation modify the energy level separation by 8 meV. It is also found that the energy levels of the higher states are more influenced by the change of the dot orientation. If the effective mass of the electron is isotropic, the energy levels of the electron are not affected by the dot orientation. However, in the case of Si, the anisotropy of the effective mass of electron causing the energy levels become complicated.

It is also considered that the single particle energy levels depend strongly on the shape of the dots even if the electron has isotropic effective mass. In the case of Si, due to the anisotropic effective mass of electron, the dependence on the dot shape becomes

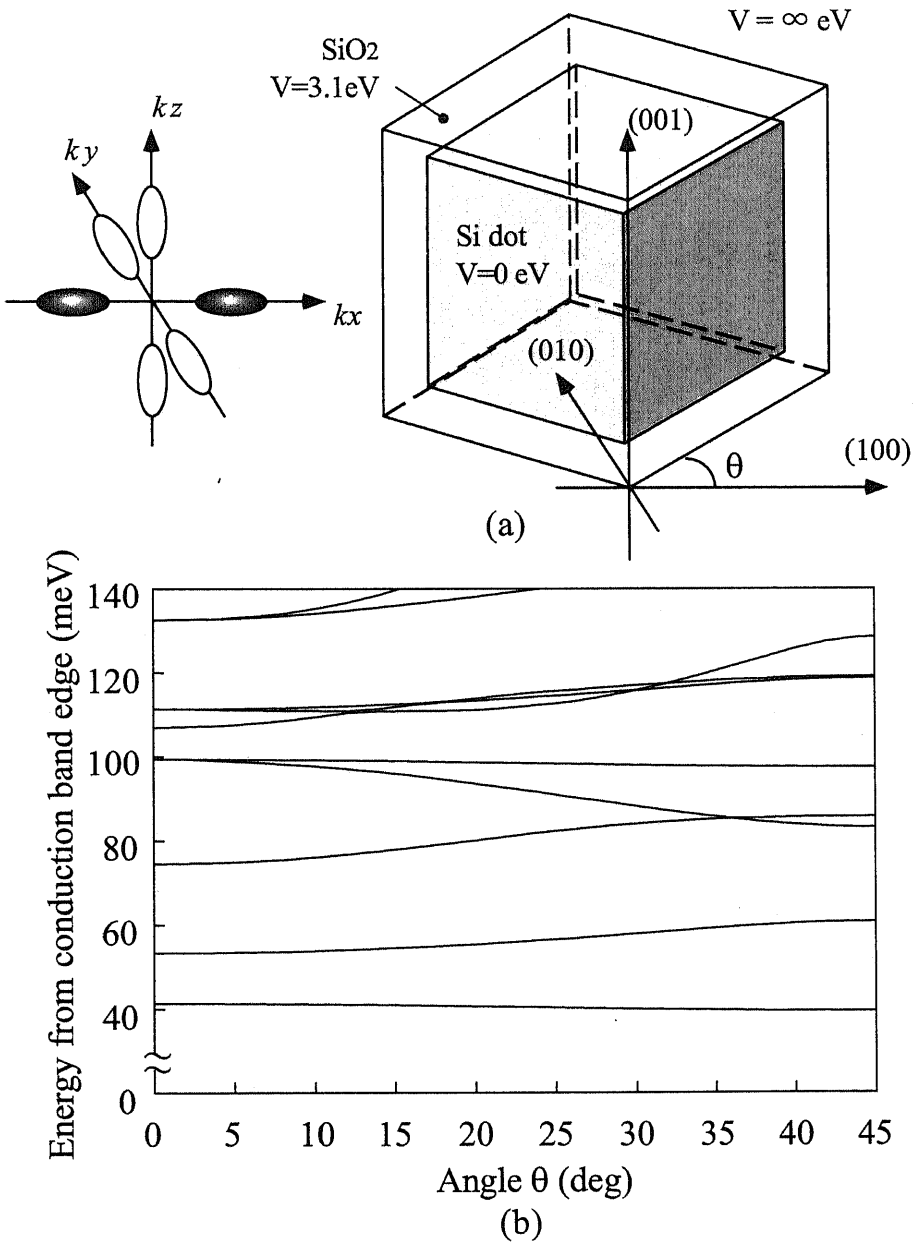


Figure 3.13: (a) Cubic Si dot used in the calculation. The Si dot are rotated by θ while the shape is unchanged. (b) Energy spectrum of electron that belong to the valley located along the k_x axis.

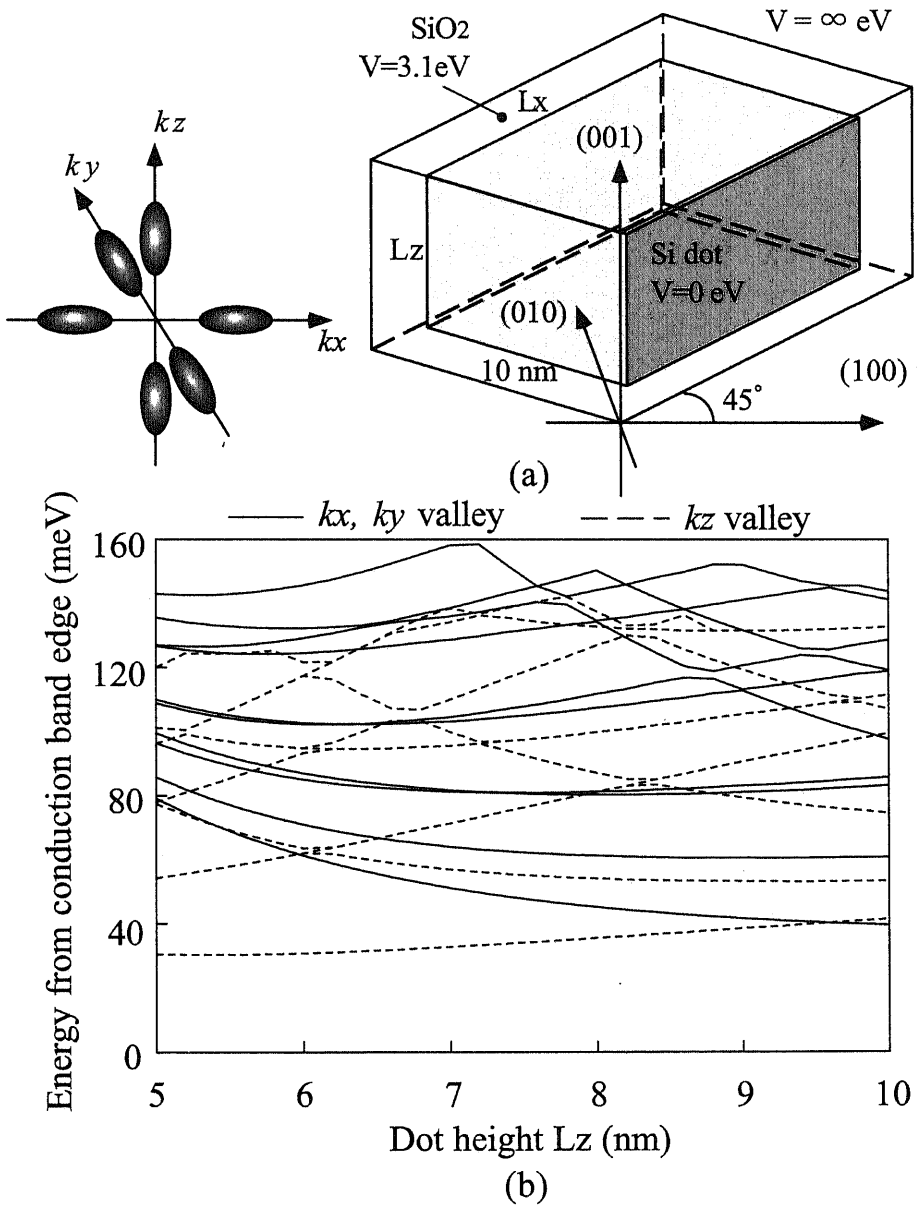


Figure 3.14: (a) Rectangular parallelepiped Si dot used for the calculation. The volume of the dot is kept constant. The electron in the six valleys are used in the calculation. (b) The dot shape dependence of the energy spectrum in the dot.

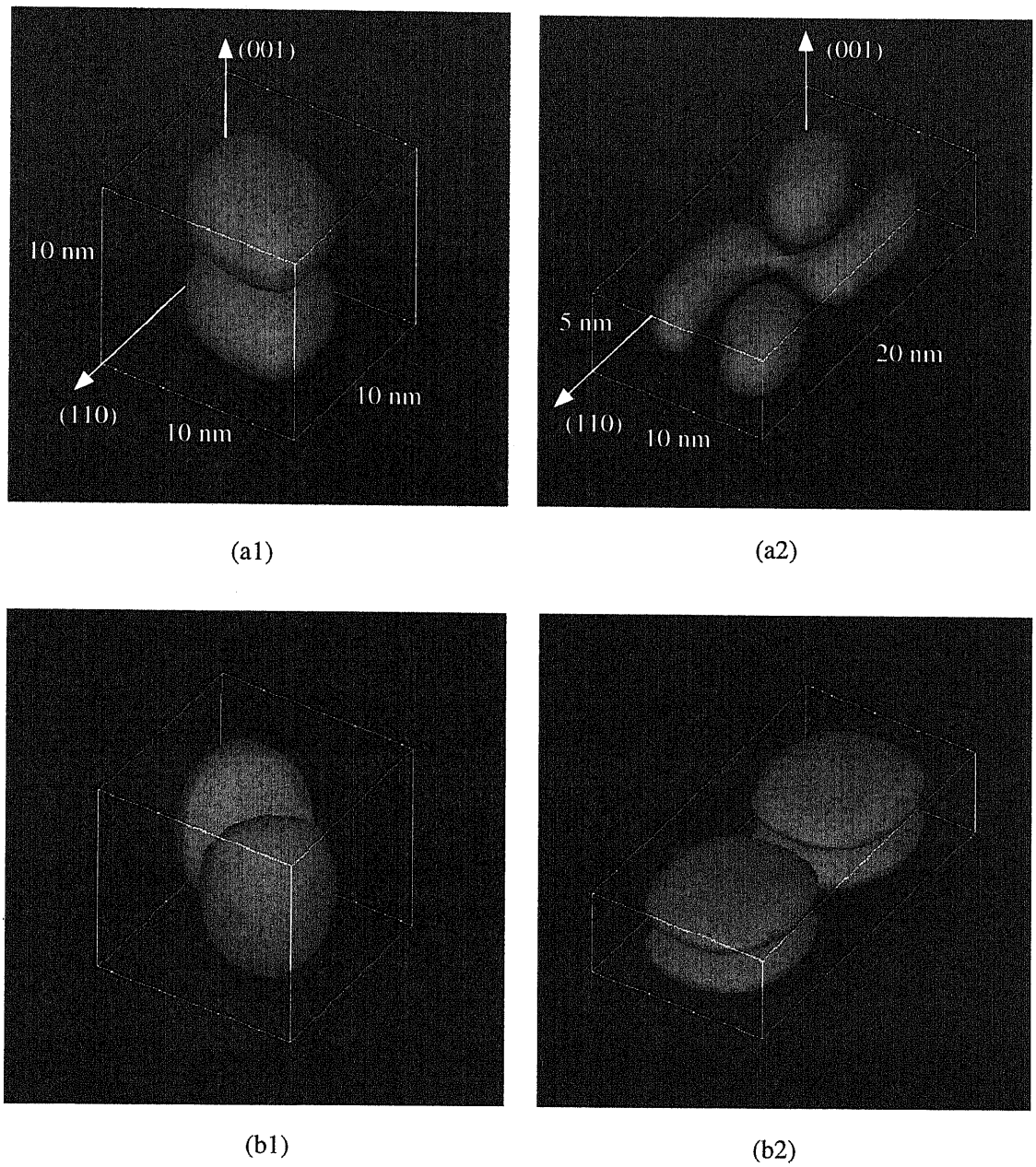


Figure 3.15: Shape of 5th excited states ($|\psi|^2$) of (a) electron in the k_x valley and (b) k_z valley. Even when the volume of the Si dot is constant, the shape of the wave functions change as the dot shape is changed. As a result, separation of the quantum confinement energy changes when the dot shape is changed.

more complicated. Figure 3.14 is the change of energy spectrum of electron when the dot shapes are changed while the volume of the dot is kept constant. The energy levels of electron in the valleys along k_x, k_y, and k_z axes are calculated. Although the volume of the Si dot is kept constant, the energy levels of electron change. Furthermore, the energy levels of the electron in k_x and k_y valleys are completely different from those of the electron in k_z valley. Figure 3.15 shows that wave function in the Si dot takes various forms according to the dot shapes, which results in the complicated behavior of energy spectrum. Therefore, it is very hard to predict the peak position of the Coulomb blockade oscillations due to the quantum confinement effects.

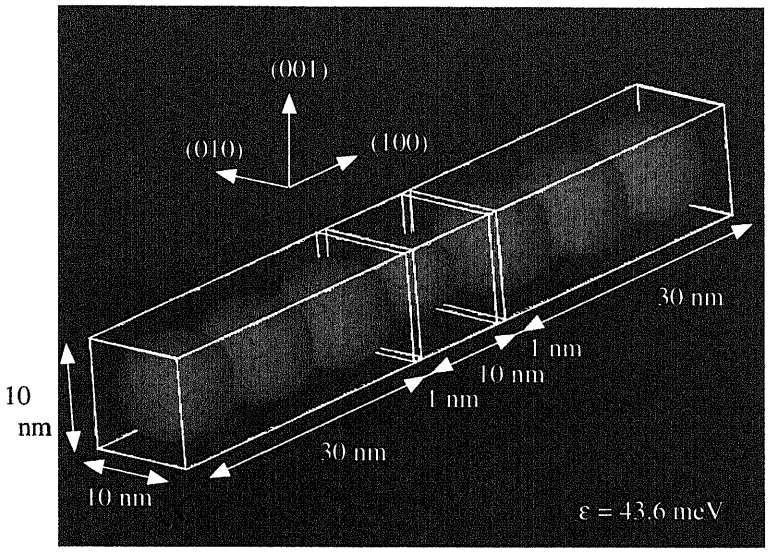
In both cases mentioned above, the single electron charging energy is about 30 meV. Therefore, the change of the energy levels as a function of dot orientation and shape, which is several meV, have large influence in the Coulomb blockade oscillations.

It is considered that the single particle energy level separations will have strong influence on the device characteristics due to the large degeneracy of the electronic state in Si (valley degeneracy (6) $\times$ spin degeneracy (2) = 12). However, from above calculated results, it is noticed that the degeneracy of the electron in the valley of different axis is removed in the Si dots because of the anisotropy of the effective mass.

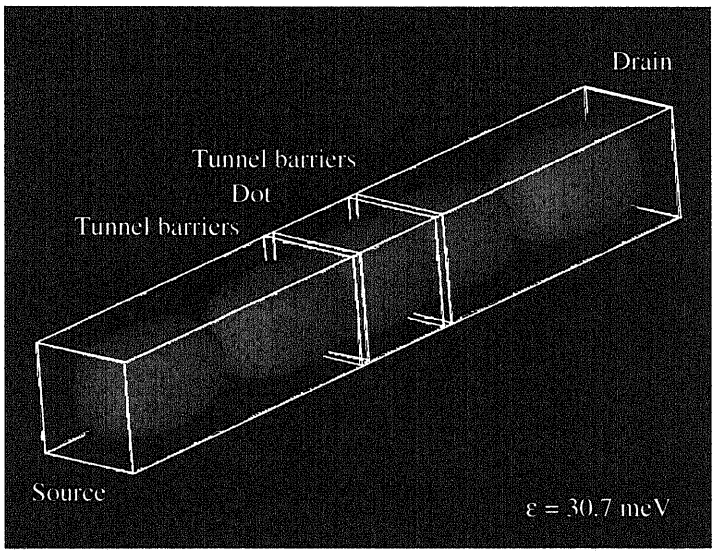
3.5 Coupling of electron states between dot, source, and drain

The anisotropy of effective mass also affects the coupling strength of electron states in the dot and that of source and drain. Electronic structure of the dot which is connected to the source and drain regions are calculated. Cubic dot in the channel along the (100) direction which is connected to source and drain via a thin tunnel barrier is assumed. The thickness and the height of the tunnel barrier is 1 nm and 100 meV, respectively. Infinite potential is assumed outside of the channel. The shape of the wave functions of the electron in k_x valley and k_y valley are shown in Figure 3.16.

If the effective mass of electron along the channel direction is large (in this case the electron in the valley along the k_x axis and show in Fig. 3.16(a)), the electron in the dot is well confined and isolated from the source/drain region. On the other hand, if the effective mass of electron along the channel direction is small, coupling between some of



(a)



(b)

Figure 3.16: Influence of anisotropy of effective mass on the coupling between the electronic states of dot and that of source and drain. (a) Shape of the wave function of electron in the valley of k_x axis. The effective mass along the channel is large and the electron in the dot is well isolated. (b) Shape of the wave function of electron in the valley of k_y axis. The effective mass along the channel is small. The coupling between the source and drain becomes very strong.

the electron states in the dot and those of source/drain region becomes extremely strong as shown in Fig. 3.16(b). The electron almost extends to the whole channel. Since the intrinsic width of the energy levels in the dot depends on the coupling strength with the electron states in source/drain region, the peak width becomes large if the coupling of the state with lead is strong. In the extreme case, a situation that the tunneling resistance is small and single electron charging effects does not work at some levels in the dot occurs. Although, the distributions of the peak width and peak height of Coulomb blockade oscillations are intensively studied on the system of GaAs.[14-17] However, different from the case of GaAs in which the electron have isotropic mass, in the Si dot system, the distribution of the peak width and height of Coulomb blockade oscillations may become much different due to the anisotropic effective mass of electron.

3.6 Quantum confinement effects on device operation temperature

In the previous sections, the influence of quantum confinement effects is evaluated from the experimental results and numerical calculations. As mentioned in the introduction, the quantum confinement effects can be useful for the improvement of the device operation temperature because the operation temperature is approximately determined by the sum of single electron charging energy and single particle energy level separation. To evaluate the contribution of the quantum confinement effects on the high temperature operation of the devices, energy levels of the spherical silicon dots are calculated as a function of radius.

Table 3.4 shows the observation and operation temperature of the silicon single electron devices with and without quantum confinement effects. The charging energy is calculated in the model that the silicon dot exists in the SiO_2 and coupling capacitance between the dot and the leads are neglected. From this table, it is noticed that the energy level separations between the ground state and first exited state become comparable with the single electron charging energy when the dot size is about 10 nm. In the silicon dot smaller the 10 nm, energy level separations rapidly increase. Observation temperature is defined as the energy three times larger than the thermal energy of the electron. At this temperature, Coulomb blockade oscillations are almost smeared out and only the

Table 3.4: Operation temperature of the silicon single electron devices with and without quantum confinement effects.

Dot size (nm)	50	20	10	5	2
Charging energy (E_C : meV)	7.2	18	36	72	180
Energy level separation (maximum $\Delta\varepsilon$: meV)	1.0	6.5	26	104	650
Observation temperature ($3k_BT$)					
without $\Delta\varepsilon$ (K)	28	70	140	280	700
with $\Delta\varepsilon$ (K)	32	93	240	680	3200
Operation temperature ($30k_BT$)					
without $\Delta\varepsilon$ (K)	2.8	7.0	14	28	70
with $\Delta\varepsilon$ (K)	3.2	9.3	24	68	320

fluctuations can be observed. Therefore, it is not enough for the application to the logic circuit. The operation temperature is defined at the point where the energy is 30 times larger than the thermal fluctuation. At this temperature, the error rate of the devices are reduced to the level for the logic applications. From the table, it seems impossible to attain the energy that is 30 times larger than the thermal fluctuations at room temperature only using charging energy. On the other hand, if one can utilize the quantum confinement effects, 2 nm size silicon dot is enough to use single electron devices at room temperature.

Since the behavior of the quantum confinement effects is very complicated and it is difficult to predict the device characteristics, a new method is required to adjust the peak position of the single electron devices after the device fabrications for the utilization of the quantum confinement effects for the high temperature. This issue is dealt with in Chapter 5.

3.7 Summary

In conclusion, nano-scale point contact MOSFETs have been successfully fabricated on SOI wafers without using any fine lithography. In the process, the point contact channel is formed using double layer mask, anisotropic etching, and selective oxidation. The width of the point contact channel is determined only by the thickness of the surface Si layer. The uniformity of the fabricated point contact channel has been confirmed by the experimental results. From the observe Coulomb blockade characteristics in the

device with various dot size, it has been found that the separation of single particle energy levels in the dot begins to have significant influence on the device characteristics when the single electron charging energies become around 20 meV. The numerical calculation based on the effective mass approximation including the anisotropy supports the experimental results. It is also found that the room temperature operation of single electron transistor is difficult to realize unless the quantum confinement effects are not utilized. One of the way to utilize the quantum confinement effects are proposed and demonstrated in Chapter 5.

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Chapter 4

Potential profiles in silicon nano-scale channels

4.1 Introduction

Recently, single electron tunneling phenomena at high temperature have been reported by many groups[1-5] using silicon nano-size narrow channel metal-oxide-semiconductor field-effect transistors (MOSFETs). Some of them are based on dot structures in silicon narrow channels although the barriers or dots are not intentionally formed as mentioned in the Chapters 2 and 3. In addition to the improvement of device operation temperature, many problems should be clarified for the application of silicon single electron devices. One of such issues is to elucidate the formation mechanisms of tunneling barriers and dots in the silicon nano-size channels. Although impurity ions, channel depletion in constricted part, or thickness fluctuations of the gate oxide are generally considered as the origin of the tunnel barriers, it has not been clarified yet.

So far, most of the experiments on the Coulomb blockade phenomena have been made using only the electron channel. Although some experiments on the hole channel have been reported,[6] the relation between the electron and hole systems have been rarely discussed. It is considered that information about the tunnel barriers can be obtained from the transport properties of both electrons and holes, which reflect the potential profile of the conduction band as well as the valence band. To strictly evaluate the relation between

electron and hole transport properties, it is essential to make experiments on the electron and hole systems which are formed in the same channel.[10] In such systems, difference of the transport properties caused by the different physical properties of electrons and holes can be also studied which attracts much attention from a viewpoint of physics.

In this chapter, transport properties of holes as well as electrons in the same channel are studied to clarify the channel potential profile. For this purpose, Si nano-size point contact MOSFETs with both n^+ and p^+ source/drain contacts connected to the same channels are fabricated on silicon-on-insulator (SOI) substrates using self-alignment technique. The origin of the tunnel barriers and the mechanism of dot formation are also discussed based on the experimental results.

4.2 Device with both n^+- and p^+- source/drain contacts

Figure 4.1 shows a fabrication process and schematic view of the device used in this experiment. The device is a point contact MOSFET with both n^+ and p^+ source/drain regions. The most important point of this device is that both electron channel (n-channel) and hole channel (p-channel) can be induced in the same channel. When positive voltage is applied to the gate, electrons are induced and the device acts as n-channel transistor using n^+ source and drain. On the other hand, when negative gate voltage is applied to the gate, holes are induced and the device acts as a p-channel transistor using p^+ source and drain. Therefore, the potential profile of the valence band as well as that of the conduction band can be investigated in an identical channel.

In this experiment, to investigate the influence of

- qualities of back interface (surface Si layer/buried oxide layer),
- thicknesses of surface silicon layer,
- surface roughness of the channel,
- thermal process during the device fabrication, and
- interface state density,

devices were fabricated by several different conditions.

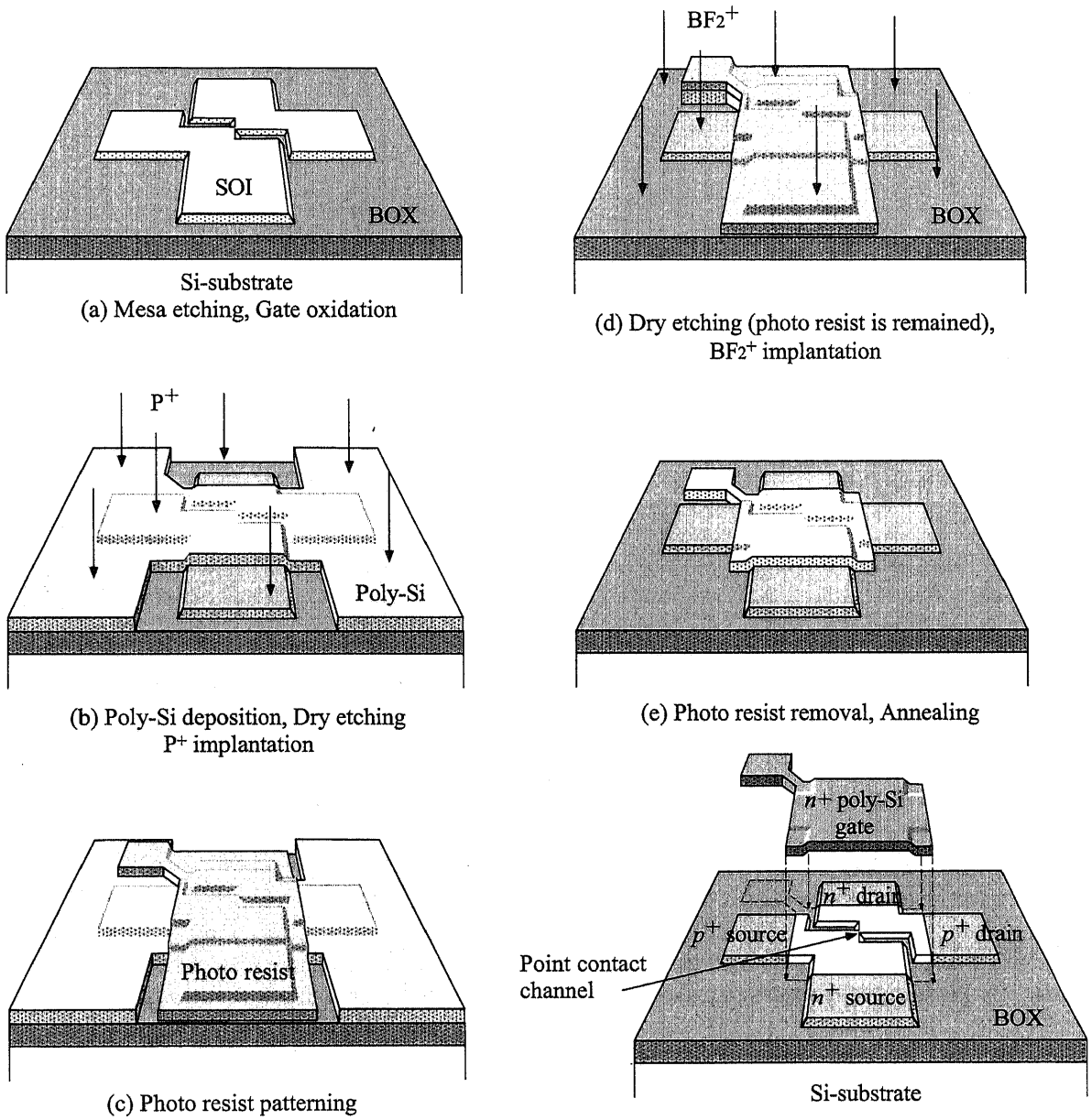

Figure 4.1: Fabrication process and schematic view of the device structure. Both n^+ and p^+ source/drain contacts are formed in the same device using a self-alignment ion implantation.

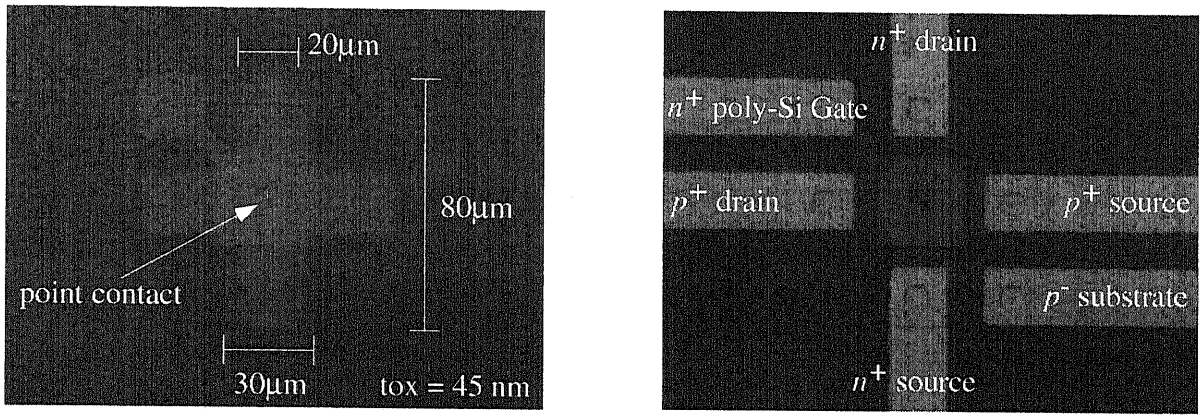

Figure 4.2: Micro-graphs of the fabricated device. (a) Photograph taken after the gate formation. (b) Fabricated device with both n^+ and p^+ source/drain contacts.

For the investigation of the influence of back interface, two types of SOI wafers are employed. One is a UNIBOND wafer prepared by Smart-Cut process[11] and the other is a separation-by-implanted-oxygen (SIMOX) wafer. Since the buried oxide layer of UNIBOND wafer is formed by thermal oxidation, the quality of the back interface of UNIBOND wafer is considered to be superior to that of SIMOX wafer. Both wafers are $\langle 100 \rangle$ oriented, p-type with resistivity of $20 \sim 30$ Ωcm. The thicknesses of the surface Si layer and the buried oxide layer are 205 nm and 400 nm for the UNIBOND wafer, and 168 nm and 106 nm for the SIMOX wafer, respectively.

First, surface Si layers of UNIBOND and SIMOX wafers are thinned by thermal oxidation and subsequent wet etching. Several wafers with different thickness of surface Si layer were formed for the evaluation of the influence of the surface Si layer thickness. Then 10 nm thermal oxide is formed as a mask for anisotropic wet etching. Using the electron beam (EB) lithography, point contact patterns with various channel widths are defined on the EB resist. After the development of the resist, the patterns are transferred to the SiO_2 mask by buffered hydrofluoric acid (BHF). Then anisotropic wet etching by Tetramethylammonium-hydroxide (TMAH) is used to form the point contact structure (Figure 4.1(a)).[2,3,12,13] Since the anisotropic wet etching automatically stops as explained in the fabrication process in Chapter 2, the width of the point contact can be precisely

controlled by the dose of electron at EB lithography. After the removal of SiO_2 mask, on some of the wafers, Si nano-crystals whose average size is 7 nm and average density is 10^{12} cm^{-2} are deposited by low-pressure chemical-vapor-deposition (LPCVD) to investigate the influence of surface roughness of SOI layer. Then, the gate oxide is formed by thermal oxidation at 1000 °C. The oxide thickness of (100) surface is 45 nm. Since the stress induced during the thermal oxidation can become one of the cause of the tunnel barriers, samples were oxidized in two ways. One is the usual process in which the temperature is gradually increased from room temperature to 1000 °C. The other is the process in which the temperature is rapidly increased in several seconds.

Using a self-alignment technique, which makes it possible to reduce the area of parasitic MOSFET, both n^+ and p^+ source/drain contacts in a single device are formed as follows. Poly-Si film is deposited by LPCVD. Then the poly-Si film only on the area for n^+ source/drain contacts is removed by photo-lithography and chemical dry etching. After the removal of photo-resist, phosphorus ions (P^+) were implanted into the wafer (Fig. 4.1(b)). Then, the areas for a gate and n^+ source/drain contact are covered with photo-resist (Fig. 4.1(c)) and the poly-Si film on the area for p^+ source/drain contact are removed by chemical dry etching. Photo-resist is remained at this time and boron ions (BF_2^+) are implanted (Fig. 4.1(d)). After the removal of resist and SiO_2 film deposition for passivation, annealing for the activation of the implanted ions are carried out. In this way, n^+ poly-Si gate, n^+ source/drain, and p^+ source/drain contacts are formed (Fig. 4.1(e)). Some of the samples are annealed in the hydrogen and nitrogen mixture gas at 430 °C to reduce the interface state density. Etching of contact holes and aluminum evaporation for electrode are performed to complete the devices. The final thicknesses of surface Si layers of the samples range from 5.1 nm to 28 nm. Since the thicknesses of surface Si layers are much thinner than the depletion length, that is, the devices operate in a fully-depleted mode, electron and hole transport can be strictly distinguished by the bias applied on the gate.

More detailed conditions of each steps of the process and combination of the process used for each samples are described in Table 4.1.

Figure 4.2 shows the geometry of the fabricated device. The electron and hole flow from source to drain through a point contact formed at the center of the device.

Table 4.1: Conditions of the fabrication process of point contact MOSFETs with both n^+ and p^+ source-drain contacts.

step	condition	temperature (°C)	time (min)	thickness (nm)	remark
Dicing	2cm×1.5cm (SIMOX & UNIBOND)				
Wafer cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$ (SPM)	130	10		
	$NH_4OH : H_2O_2 : H_2O = 1 : 2 : 8$ (SC1)	75	10		*1
RCA cleaning	DI water (DeIonized water)		3		
	$HF : H_2O = 1 : 100$		dip		
	DI water		3		
	$H_2O : H_2O_2 : NH_4OH = 4 : 1 : 1$ (SC1)	75	20		
	DI water		3		
	$H_2O : HF = 10 : 1$		1		
	DI water		3		
	$H_2O : H_2O_2 : HCl = 4 : 1 : 1$ (SC2)	75	20		
	DI water		3		
	$H_2O : HF = 10 : 1$		1		
	DI water		3		
Oxidation	$O_2 : 1.0l/\mathrm{min}$	1100			
Oxide remove	Buffered HF (BHF)				
Oxidation	$O_2 : 1.0l/\mathrm{min}$	900	10	10	
EB lithography	OEBR1000(100cp):ECA=1:2 4000rpm		40 sec	160	
(JEOL:JBX6000FS)	Prebake	170	30		
	Line 2.1 nC/cm, Area 420 $\mu C/cm^{-2}$ 50 keV 200 pA				
	MIBK:IPA =1 : 3 (develop)		1.5		
	IPA (rinse)		1		
	DI water (rinse)		3		
	Postbake	90	10		
Pattern transfer	BHF		10 sec		*2
Anisotropic etching	TMAH 15 wt%	75	~1		
(Ion implantation)					*3
SiO_2 mask remove	BHF		10 sec		
(Si-nano crystal deposition)					*4
RCA cleaning	Same as previous RCA cleaning				
Gate oxidation	$O_2 : 1.0l/\mathrm{min}$	1000	45	43	*5
	$N_2 : 1.0l/\mathrm{min}$	1000	5		
Poly-Si deposition	SiH_4 200sccm 1.0Torr	600	30	270	
Photo lithography	AZ1350 4000rpm		40sec	400	
(gate)					
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	130	20		
Gate RIE	SF_6 40sccm 0.013Torr 100W	0	1		
	SF_6 70sccm 0.15Torr 25W	0	2		
Resist remove	Acetone				
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	130	15		

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Ion implantation (n^+ source, drain, gate)	P^+ 45keV $5\times10^{15}cm^{-2}$ $I_{beam} = 30\mu A$		$\sim$ 50		
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	125	10		
Annealing	N_2 : 1.0l/min	950	15		
Photo lithography (gate)	AZ1500 4000rpm		40sec	800	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	125	20		
Gate RIE	SF_6 40sccm 0.013Torr 100W	0	20sec		
	SF_6 70sccm 0.15Torr 25W	0	4		
Ion implantation (p^+ source, drain)	BF_2^+ 55keV $3\times10^{15}cm^{-2}$ $I_{beam} = 15\mu A$		$\sim$60		
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	130	15		
O_3 ashing	O_2 0.5l/min	300	30		
SPM cleaning	$H_2O_2 : H_2SO_4 = 1 : 3$	130	15		
SiO_2 deposition	SiH_4:O_2 = 200:100 sccm 0.3 Torr	600	12.5	430	
Annealing (H_2 Annealing)	N_2 : 1.0l/min	950	10		*6
Photo lithography (contact hole)	AZ1350 4000rpm		40	400	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	125	20		
Contact hole etching	BHF		6		
Resist remove	Acetone				
Al evaporation				220	
Photo lithography (Al electrode)	AZ1350 3000rpm		40	400	
	Prebake	90	25		
	Exposure,development,rinse				
	Postbake	130	20		
Al etching	$H_3PO_4 : CH_3COOH : HNO_3 : H_2O$ = 75 : 15 : 5 : 5	40	2.5		
Resist remove	Acetone				

*1 To remove particles contaminated on wafers during the wafer dicing.

*2 Do not use diluted HF.

*3 To investigate the influence of impurity in the channel, oxygen ions are implanted into some of the devices. (25 keV, 5×10^{14} cm^{-2})

*4 To investigate the influence of surface roughness, Si nano-crystals are deposited on some wafers. (SiH_4 195sccm, 0.4 Torr, 574°C 120 sec)

*5 In some cases, the temperatures are rapidly increased from 20 °C to 1000 °C in a few seconds.

*6 Some of the samples are treated by hydrogen annealing. ($N_2 : H_2$ = 1000 : 100 sccm, 430 °C, 25 min.)

4.3 Characterization at room temperature

The fabricated devices are characterized at room temperature. In Figure 4.3, transistor characteristics of the devices with large channel ($L \times W \sim 25\mu\text{m} \times 25\mu\text{m}$) are shown. It is confirmed that both p-channel (at $V_g < -0.5$ V) and n-channel (at $V_g > -0.5$ V) are induced in the same channel. Turning point between the p-channel and n-channel locates not at $V_g = 0$ V but at $V_g \sim -0.5$ V because of the work function of the n^+ poly-Si gate. From the transistor characteristics at linear regime (Fig. 4.3(a)), the drain current of electron channel is much larger than that of hole channel due to the difference in carrier mobility. Drift mobilities of electron and hole are roughly estimated to be about 600 cm^2/Vsec and 200 cm^2/Vsec, respectively. Both the drift mobilities of electron and hole decrease as the thickness of surface Si layer decreases. Furthermore, in the device with extremely thin surface Si layer, the drain current immediately saturates because of large parasitic resistances in the source/drain regions. From the sub-threshold characteristics in Fig. 4.3(b), it is found that good cut-off characteristics are obtained in both n-channel and p-channel. Sub-threshold slope ($S = (\frac{\partial \log_{10} I_d}{\partial V_g})^{-1}$), which is affected by the interface state density, is excellent ($\sim$ 70 mV/dec) in the devices treated with hydrogen annealing. In the devices without hydrogen annealing, sub-threshold slope becomes worse as the thickness of surface Si layer decreases.

The decreased drift mobility and inferior sub-threshold slope in the devices with thinner surface Si layer originate in large interface state densities. Since the interface states can become one of the reasons of dot formation in narrow channel, the interface state densities in all the samples are characterized by charge pumping method. By connecting the n^+ and p^+ drain contact to the ground and applying a periodic pulse bias on the gate, charge pumping current from n^+ drain contact to p^+ drain contact, which is in proportion to the interface state density and area of channel, can be measured. Subsequently, the interface state density can be extracted from the measured charge pumping current. Figure 4.4 shows the measured interface state density as a function of surface Si layer. The interface state density increases as the thickness of surface Si layer decreases. In the sample with hydrogen annealing, the interface state density is significantly reduced by the effect of termination of dangling bond. These results are consistent with the transistor characteristics in Fig. 4.3. It is considered that the stress induced in the thin surface

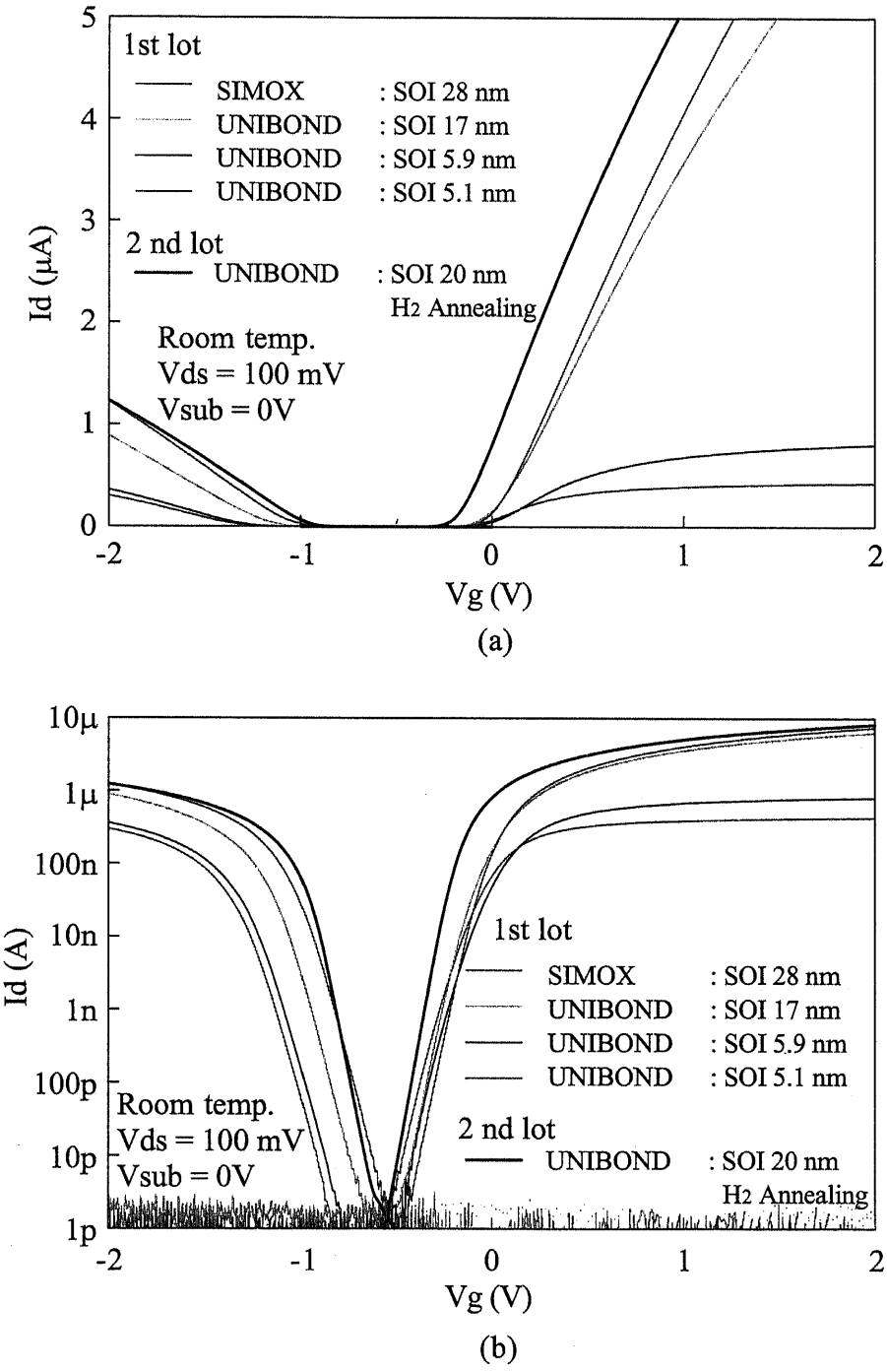


Figure 4.3: Gate voltage (V_g) dependence of the drain current (I_d) at room temperature. (a) Characteristics of linear operations. (b) Characteristics at sub-threshold regime.

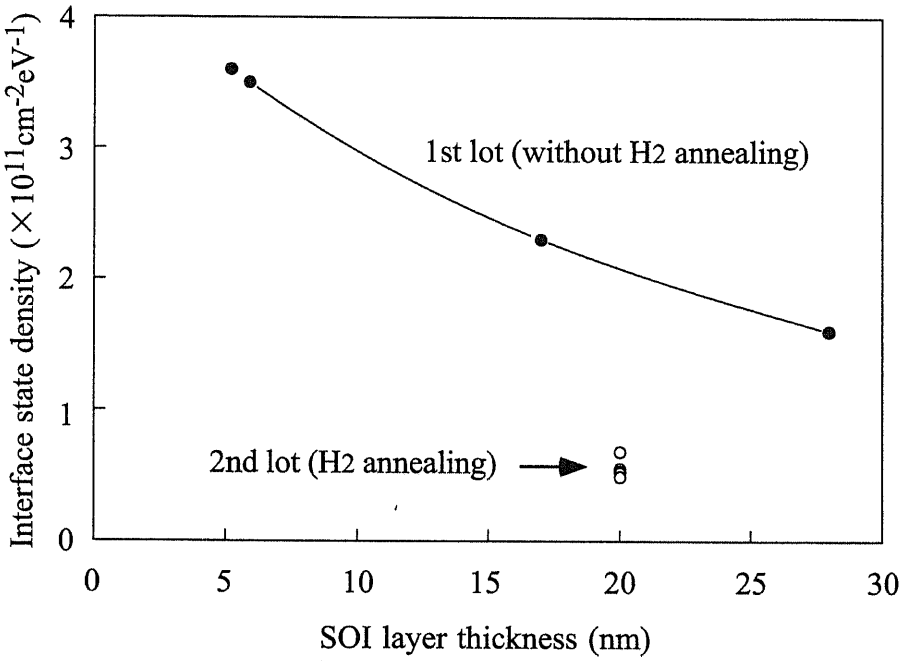


Figure 4.4: Interface state density of the fabricated devices obtained by the charge pumping method. Considering the thickness of surface Si layer, both the interface states at gate oxide/surface Si layer and buried oxide/surface Si layer contribute to the measured interface state density.

Si layer becomes a cause of increased interface state density. The above obtained interface state density is the average in the whole channel. It is likely that more interface states are generated around the narrow channel because much larger stress is induced in the constricted part of the channel. However, the average interface states can be used as a reference for the evaluation of the influence of interface states on the dot formation.

4.4 Coulomb blockade oscillations in n-channel and p-channel

At 20 K, the devices fabricated on both types of the wafers show Coulomb blockade oscillations as the channel widths decrease (typically less than 10 nm). Figure 4.5 shows some of the experimental results of the devices on SIMOX wafer. It is found that the devices with no oscillations at n-channel do not show oscillations at p-channel and the devices

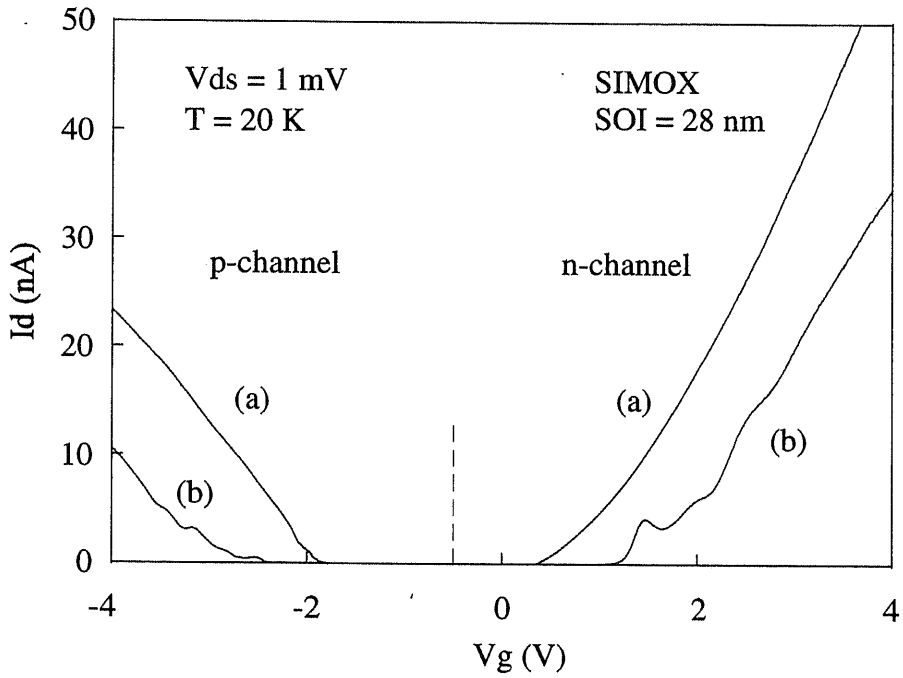


Figure 4.5: Gate voltage (V_g) dependence of the drain current (I_d) of devices on a SIMOX wafer. Devices show normal MOSFETs operation like curve (a) when the channel width is large. As the channel widths decrease, Coulomb blockade oscillations are observed in both electron and hole channel like curve (b).

that show Coulomb blockade oscillations at n-channel always show Coulomb blockade oscillations at p-channel. The result indicates that tunnel barriers for both electrons and holes are formed in the channel. Therefore, tunnel barriers are formed at valence band as well as conduction band. Similar tendency is obtained in the experimental results of the other samples. That is, the Coulomb blockade oscillations can be observed in the device on all wafers when the channel becomes extremely narrow. Although, in the limited number of devices, it is difficult to conclude that there is not strong correlation between the difference in the condition of device preparation and dot formation, strong affects of the average interface state density, difference in wafer preparation (SIMOX, UNIBOND), the way for thermal oxidation, and the surface roughness could not be observed in this experiment.

Figure 4.6 shows one of the experimental results of Coulomb blockade oscillations in a device on SIMOX wafer. In this figure, Coulomb blockade oscillations with almost the same peak-to-valley ratios are observed in n-channel and p-channel. It is suggested

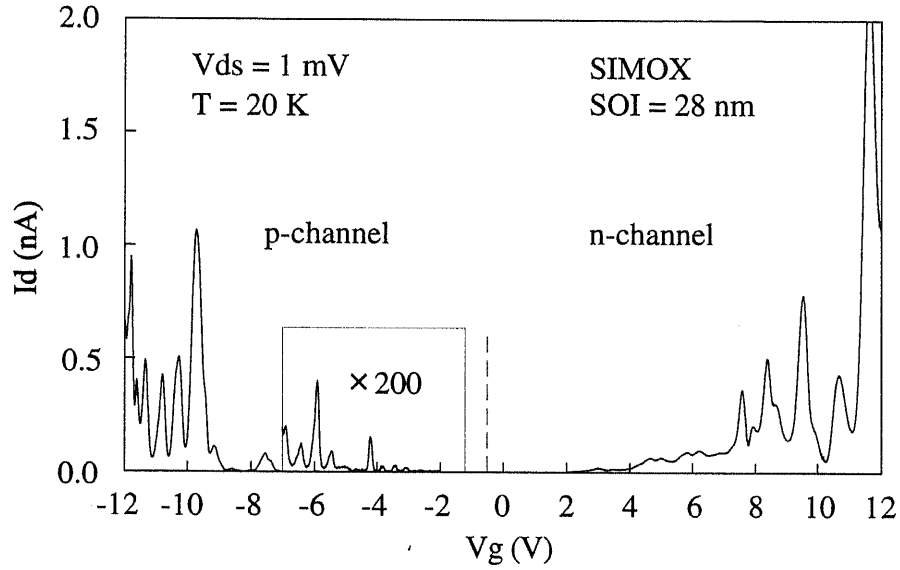


Figure 4.6: Coulomb blockade oscillations with relatively large charging energy observed in a device on a SIMOX wafer. Peak to valley ratios in n-channel and p-channel are almost the same which suggests that the size of the dots formed in the conduction band and valence band are almost same.

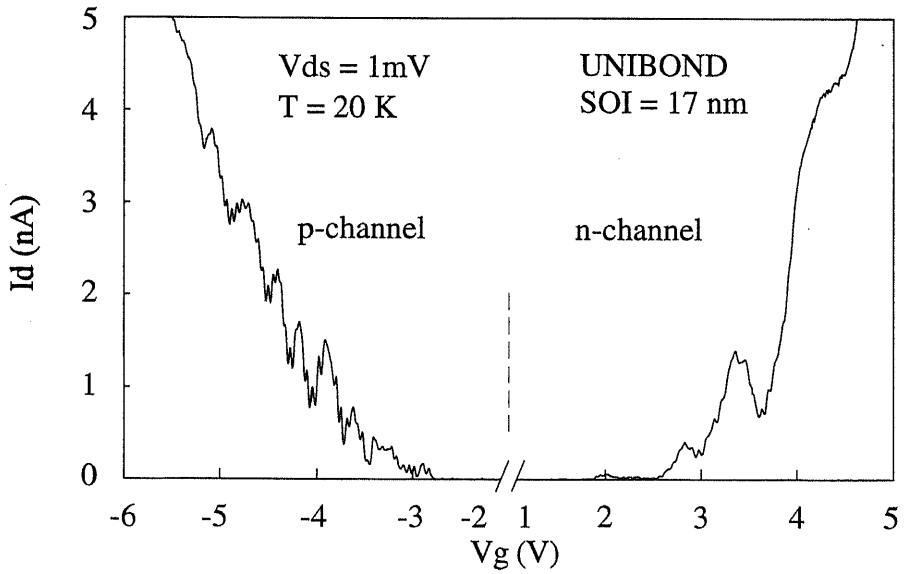


Figure 4.7: Coulomb blockade oscillations with large period modulated by fine oscillations in a device on a UNIBOND wafer. The characteristics suggests coupled double-dots formed in both the conduction band and the valence band.

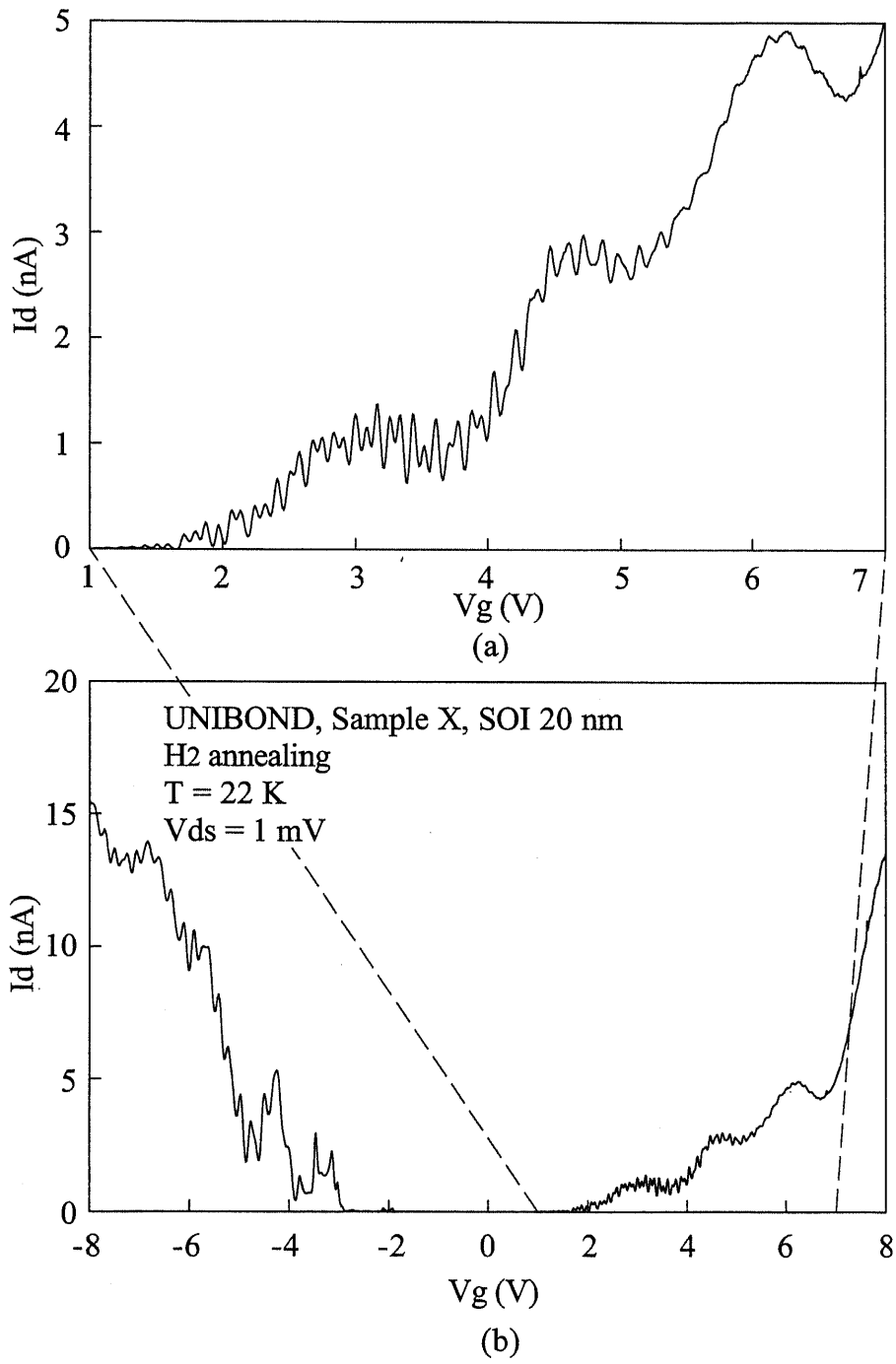


Figure 4.8: Coulomb blockade oscillations in a device on a UNIBOND wafer. This device was treated with hydrogen annealing and the interface state density is reduced. (a) Complicated Coulomb blockade oscillations in the n-channel. (b) Coulomb blockade oscillations in both n-channel and p-channel. The period of the n-channel and p-channel is completely different.

that the dot with the same charging energy (> 10 meV), and consequently, the same size is formed in both n-channel and p-channel. Figure 4.7 shows another example of the Coulomb blockade oscillations in a device on UNIBOND wafer. In the figure, oscillations with large period which are modulated by fine oscillations are observed in both n-channel and p-channel. This kind of characteristics are often observed in coupled double-dot system. Therefore, the result indicates that coupled double-dots are formed in both the n-channel and p-channel. From the peak to valley ratio, single electron charging energies in the large dot and the small dot are estimated at 7 meV and 5 meV, respectively. In the devices mentioned above, channel potential profiles of the conduction band and valence band are similar and the tunnel barrier for electron also acts as the tunnel barrier for hole.

On the other hand, another type of Coulomb blockade oscillations is also observed as shown in Figure 4.8. In this device, although Coulomb blockade oscillations are observed in both n-channel and p-channel, the characteristics are different in n-channel and p-channel. The characteristics in n-channel are very complicated. Fine oscillations modulated by large oscillations with period ($\Delta V_g \sim 1.7$ V) are seen in all range of gate voltage. Whole characteristics including the fine oscillations are completely reproducible and stable at fixed temperature. It should be noted that the period of fine oscillations in 1 V $< V_g <$ 4 V is half of the period of oscillations in 5 V $< V_g <$ 7 V. The each doubly split peak at 1 V $< V_g <$ 4 V gradually merges into single peak above $V_g = 4$ V. Same as the characteristics in Fig. 4.7, the fine oscillations are caused by coupled double-dots, which become a single-dot at high gate voltage, formed in the conduction band. However, the characteristics in this device is just the opposite of the experimental results on double-dot system reported in Ref. 14, 15, and 16, in which the period at low gate voltage is double of the period at high gate voltage. In the devices reported in Ref. 14, 15, and 16, the coupling strength between the double dots are increased, resulting in the formation of large dot at high gate voltage and decreased period of oscillations. In the device used in this study, not the coupling strength between the double dots but the coupling strength between the source/drain and one of the dots are increased according to the increased gate voltage. As a result, the period of oscillations are not decreased even when the gate voltage is increased. As for the Coulomb blockade oscillations in the p-channel, the period

is nearly constant in whole gate voltage range, which suggests the single dot formed in the valence band. Therefore, in this device, there is not strong correlation between the potential profiles of conduction band and valence band.

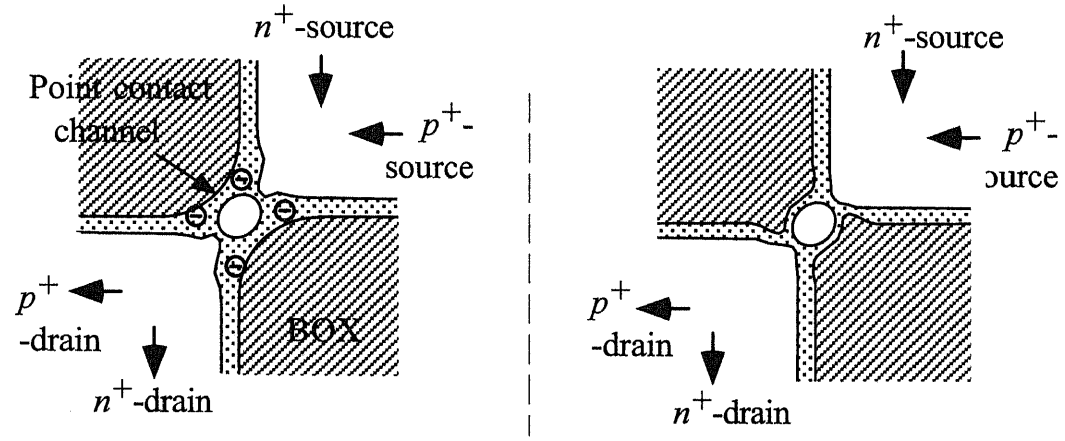
4.5 Potential profiles of conduction band and valence band

The potential profiles in the constricted point contact channel are discussed based on the experimental results in the followings.

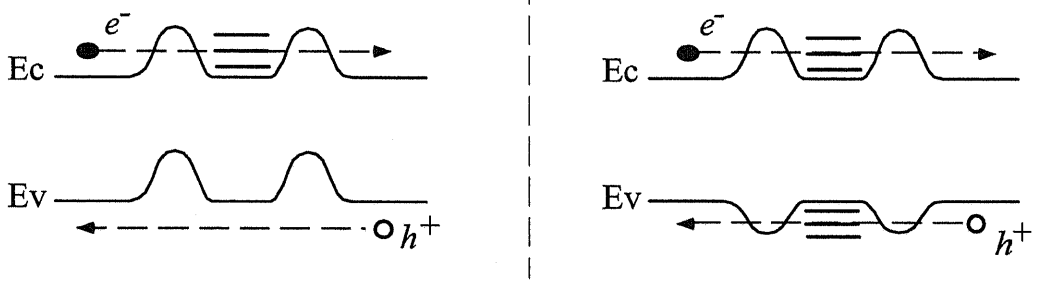
First, channel depletion caused by ionized impurities or carriers trapped at interface states is considered as shown in Figure 4.9(a). In this case, the tunnel barrier could be formed only for one type of carrier. For example, if there are negative charges trapped at the interface between gate oxide and channel, they would act as tunnel barrier for electron but would not act as tunnel barrier for hole. As a result, Coulomb blockade oscillations should be observed only at n-channel. There is also a possibility that fixed charges with both types of polarity exist in the channel. In this case, tunnel barriers are formed in both conduction band and valence band, and Coulomb blockade oscillations are observed in both n-channel and p-channel. However, the correlation between the characteristics in n-channel and in p-channel is very week due to the random location of the fixed charges.

Next, let us consider the channel with width fluctuations or the channel which is cut by the silicon oxide (SiO_x) as shown in Fig. 4.9(b). In the narrow channel with width fluctuations, lateral quantum confinement effects raise the ground state energy of the carriers, and effectively increase the band gap at squeezed points of the channel. In the channel cut by the (SiO_x), the band gap along the channel is widened at the hetero-interface. In both cases, the tunnel barriers are formed at valence band as well as at conduction band. As a result, Coulomb blockade oscillations can be observed both at n-channel and p-channel and the correlation between the Coulomb blockade oscillations in n-channel and in p-channels must be strong.

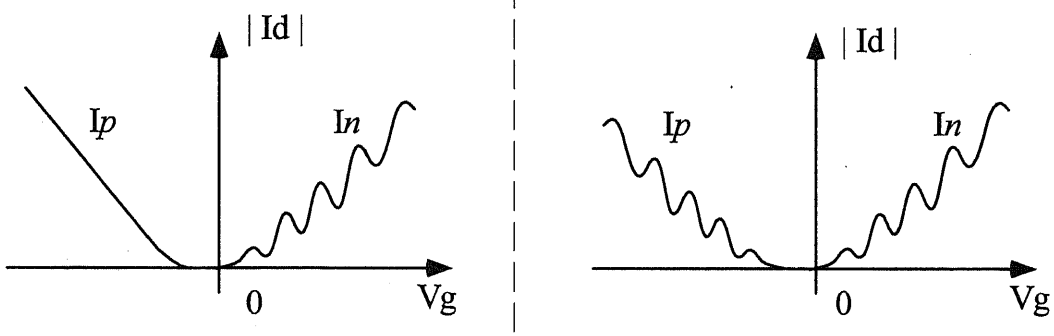
From the Coulomb blockade oscillations in the devices used in this experiment, the tunnel barriers are formed in both conduction band and valence band. Some devices, especially devices with large charging energy and small dot, show strong correlation between the characteristics in n-channel and p-channel. In such devices, the origin of tunnel bar-



Schematic view of the point contact channel. The area without hatches indicates where the carrier is induced.



Band diagram along the point contact channel.



Id - Vg characteristics.

(a) (b)

Figure 4.9: Band diagram along the Si nano-size channel. (a) The case where the tunnel barriers are caused by channel depletion by ionized impurities. (b) The case where the tunnel barriers are caused by the quantum confinement effects or silicon oxide (SiO_x).

riers is considered to be the band gap widening by lateral quantum confinement effects or silicon oxide (SiO_x). The other type of devices show Coulomb blockade oscillations with slight correlation between the n-channel and p-channel. In the devices, the potential profiles in conduction band and valence band are different due to the random location of impurity ions or interface states.

4.6 Summary

The transport properties of holes as well as electrons in the same channel have been investigated using Si nano-size MOSFETs with both n^+ and p^+ source/drain contacts. Both the n^+ and p^+ source/drain contacts were formed using a self-aligned implantation of ions. In the devices that show Coulomb blockade oscillations, the tunnel barrier for electrons also acts as tunnel barrier for holes. Two types of Coulomb blockade oscillations were observed. One is the oscillations that the correlation between the characteristics in n-channel and p-channel is strong. The origin of tunnel barriers in this kind of devices is considered to be the band gap widening by lateral quantum confinement effects or silicon oxide (SiO_x). In the other types of Coulomb blockade oscillations, slight correlation between the characteristics in n-channel and p-channel were observed. In the devices, the potential profiles in conduction band and valence band are different due to the random location of impurity ions or interface states.

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Chapter 5

Adjustment of peak positions of single electron transistors

5.1 Introduction

Room temperature operation of silicon single electron transistors (SETs) requires extremely small size of silicon dot (typically less than 10 nm).[1-4] In addition to background charges or traps near the dot of single electron devices, quantum confinement effects will have more influences on the characteristics of silicon single electron devices as the dot size becomes smaller, because the separation of single particle energy levels is in inversely proportional to the square of the dot size, whereas the single electron charging energy is in inversely proportional only to the dot size.

In Chapters 2 and 3, the influences of the quantum confinement effects, in particular, the dependencies on the dot size and dot shape in silicon single electron transistors have been discussed based on the obtained experimental results and numerical simulation. It is suggested that, in extremely small devices operating at room temperature, it is very hard to predict the peak positions of the Coulomb blockade oscillations due to the complex behavior of quantum confinement effects. On the other hand, if the quantum confinement effects can be utilized, the improvement in device operation temperatures can be achieved as mentioned in Chapter 3. For the application of single electron devices, the way to control the peak positions of Coulomb blockade oscillations after the device

fabrication is strongly desired.

In this chapter, a new method to adjust the peak positions after the device fabrication by injecting charges into silicon nano-crystals or traps is proposed. The method make it possible to utilize the quantum confinement effects. The devices are actually fabricated and the adjustment of the peak positions are experimentally demonstrated.

5.2 Device preparations

In this experiment, two types of devices which show Coulomb blockade oscillations at relatively high temperature are used. One is the nano-size point contact channel metal-oxide-semiconductor field-effect transistor (MOSFET) (Figure 5.1(a)) used in the experiment in Chapter 3. The other is a device which is newly proposed and fabricated for this experiment (Fig. 5.1(b)). In this device, silicon nano-crystals are deposited on thin tunnel oxide using low-pressure chemical-vapor-deposition (LPCVD). Although this device is similar to a memory structure,[5-11] it is used for the adjustment of peak positions instead. By controlling the injection of the charges into the Si nano-crystals, the peak positions can be easily adjusted. The fabrication process of the device with Si nano-crystals is briefly explained as follows.

First, the surface silicon layer of p-type $\langle 100 \rangle$ UNIBOND substrate doped with 10^{15} cm^{-3} acceptor is thinned to 25 nm. Point contact channels with various width are defined using electron beam lithography and anisotropic wet etching technique. Then, 4.4 nm-thick tunnel oxide is formed by thermal oxidation at 800 °C. Deposition of the Si nano-crystals, whose average diameter is 7 nm and density is about 10^{12} cm^{-2}, is performed at 574 °C and 0.4 Torr using 20 % SiH_4 gas source diluted by He.[12] Subsequently, without exposing the devices to air, 30 nm-thick gate oxide is deposited at 600 °C, and thermal annealing at 800°C and 1.0 Torr, in O_2 atmosphere is performed in the same reactor of LPCVD to improve the quality of Si nano-crystals as well as the gate oxide. For comparison, the devices without Si nano-crystals were also fabricated whose gate oxide is deposited by LPCVD. The following fabrication process is compatible with conventional MOSFET fabrication process, that is, poly-Si gate formation, phosphorus ion (P^+) implantation into the source and drain region, deposition of passivation oxide, and formation of aluminum electrode. More detailed fabrication process and the mechanism

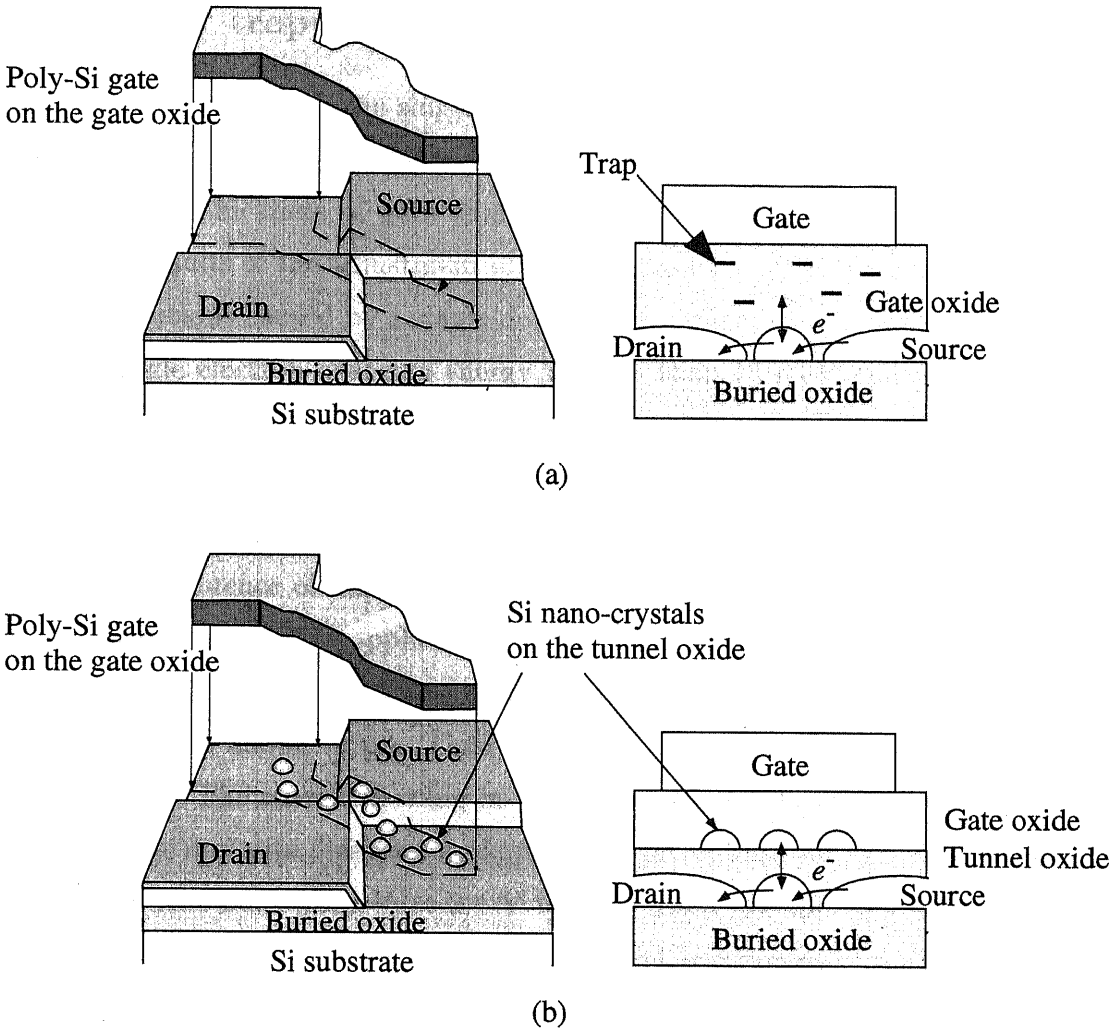


Figure 5.1: Schematics of device structures for the adjustment of peak positions. (a) Device without Si nano-crystals. The peak positions are shifted by captured charges at the trap after the gate current is flowed. (b) Device structure proposed in this study. Si nano-crystals are deposited on the tunnel oxide. The peak positions are shifted by electrons injected in the Si nano-crystals.

of the charge retention characteristics are described in Refs. 10, 11, and 13.

5.3 Adjustment of peak positions

Peak shift by trapped charge in gate oxide

First, the peak positions of the single electron transistor without Si nano-crystals which is used in the experiment in Chapter 3 were shifted by injecting the charges into the gate oxide. The thickness of gate oxide in this device is 50 nm. Figure 5.2(a) is the experimental results of the adjustment of peak positions at 21 K. In this device, Coulomb blockade oscillations caused by a single-dot structure naturally formed in the channel are observed. Single electron charging energy is more than 15 meV and it should be noted that the oscillations are not periodic due to the quantum confinement effects.

As long as the device is operated below $V_g = 14$ V, in which the current flowing in the gate oxide is extremely small (Fig. 5.2(b)), the device characteristics are stable. Therefore, the influence of mobile ions in the gate oxide can be ignored. Then, the gate voltage larger than 14 V is applied. The first peak that locates at $V_g = 1.2$ V before electron injection is shifted to $V_g = 1.9$ V by applying +15 V to the gate. In this case, the gate current is about 10 pA. Then it is shifted from $V_g = 1.9$ V to $V_g = 2.4$ V by applying +16 V. The current flowing in the gate oxide reaches to 40 pA. The peak can be shifted in the opposite direction by applying negative gate voltage. In the experiment, the peak is shifted back from $V_g = 2.4$ V to $V_g = 1.9$ V by applying -20 V on the gate. By this way, the positions of the peaks in single electron transistor can be controlled, and the possibility to utilize the quantum confinement effects are indicated. In this sample, since the suppressed region of the drain current between the first peak and second peak are large due to the quantum confinement effects, the device operation temperature can be increased.

Although the intervals between the peaks in Coulomb blockade oscillations are not changed even after the charge injection into the oxide traps, the peak heights are much affected by the injected charges. In this sample, the height of first peak is reduced by 70% after +16 V is applied on the gate and becomes almost the same height with the second peak of the oscillations before the charge injection. The trapped charges in the

gate oxide have influence not only on the potential of the dot but also on the shape and height of tunnel barriers. Even the slight change in the shape and height of tunneling barriers results in large variation of tunneling rate.[14] As a result, the peak height of the Coulomb blockade oscillations are strongly affected by the trapped charge near the tunneling barrier. Therefore, it is suggested that some of the trapped charges locate aside of tunnel barrier in the channel.

The peak positions can be shifted by the injected charge in the gate oxide, however, the writing and erasing voltages are too high for practical operations. Furthermore, the magnitude of the gate voltage required to adjust the peak positions toward negative direction must be larger than the case for adjustment toward positive direction. This is because the current flowing in the gate is dominated by electron current, and therefore, electron trapping can easily occur whereas hole trapping or electron emission rarely occur. Another problem is that the location of the traps can not be controlled. As a result, the shift of the peak positions becomes small because the Coulomb effects of the electrons trapped near the gate electrode are screened by the gate and do not effectively work for peak shift.

Electron injection into Si nano-crystals with low voltage

Operation voltage for the adjustment of peak positions can be much reduced using the Si nano-crystals on thin tunnel oxide.[5, 6, 15, 16]

In Figure 5.3(a), gate voltage (V_g) dependence of drain current (I_d) at 50 K of the device with Si nano-crystals is shown. In this device, as the temperature decreases, $I_d - V_g$ characteristics becomes to oscillate cased by the dot structure naturally formed in the channel. Single electron charging energy of the dot is estimated at 12 meV. To avoid ambiguity, "channel dots" for the dots naturally formed in the channel and "floating dots" for the Si nano-crystals deposited on the channel are used in the following discussion.

The $I_d - V_g$ curves are stable and not changed as long as the device is operated below 4.5 V. Once the gate voltage larger than 4.5 V is applied, the $I_d - V_g$ characteristics are shifted as shown in Fig. 5.3(a). In the devices with no floating dots, shifts of $I_d - V_g$ curves were not observed even if the voltage larger than 8 V was applied on the gate. Therefore, the shifts of peak positions are caused not by interface traps or mobile ions

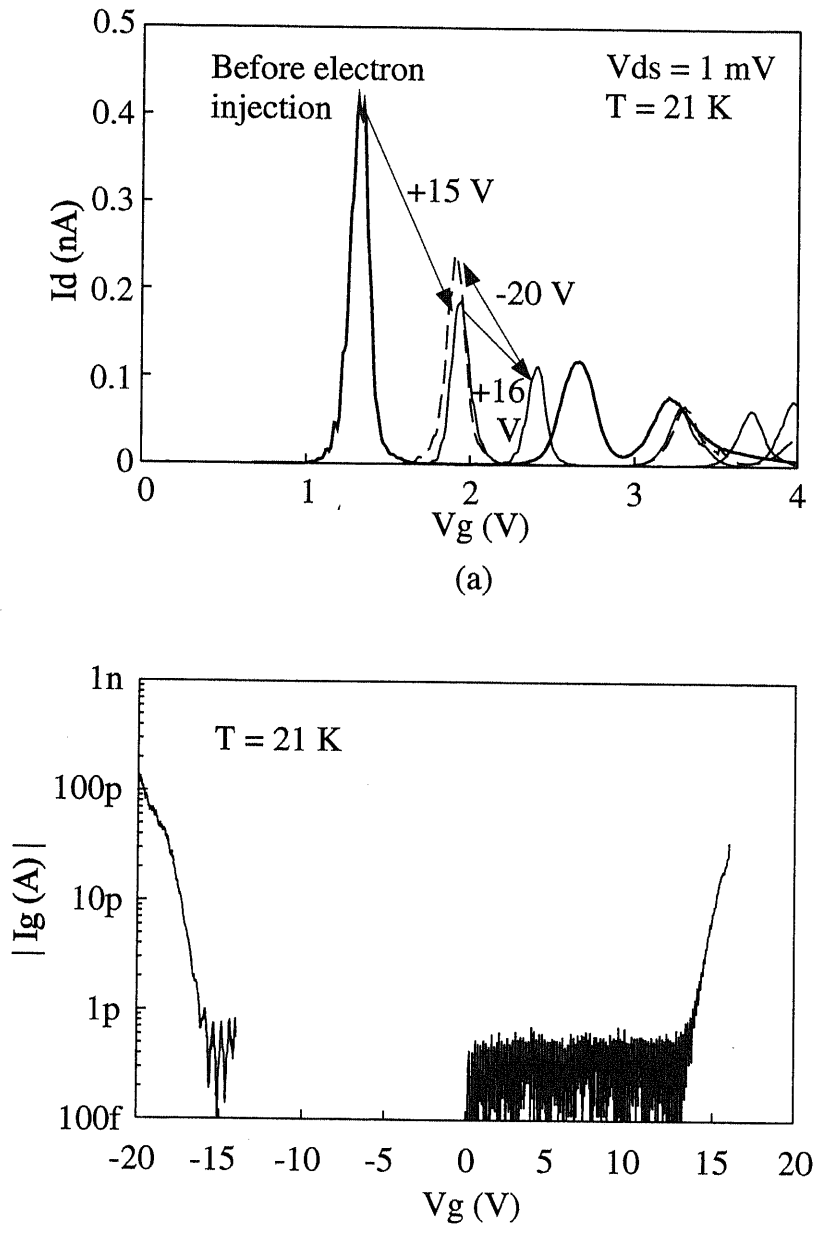
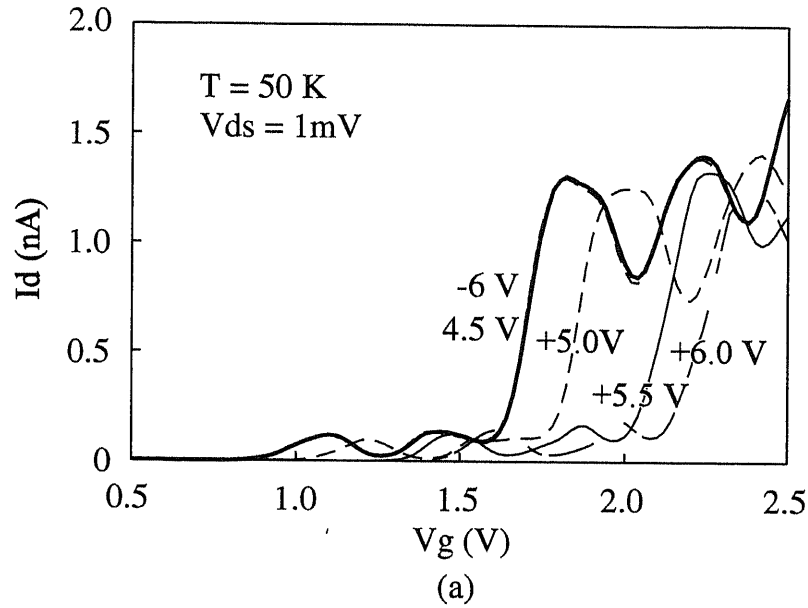


Figure 5.2: Adjustment of peak positions of a high temperature operating single electron transistor by charge injection into the traps in the gate oxide. (a) The peak was shifted from 1.2 V to 1.9 V by applying +15 V to the gate. It is shifted to 2.4 V by applying +16 V, while it is shifted back to 1.9 V by applying -20 V. (b) Gate leakage current characteristics. Above 14 V, measurable leakage current begins to flow caused by Fowler-Nordheim tunneling.



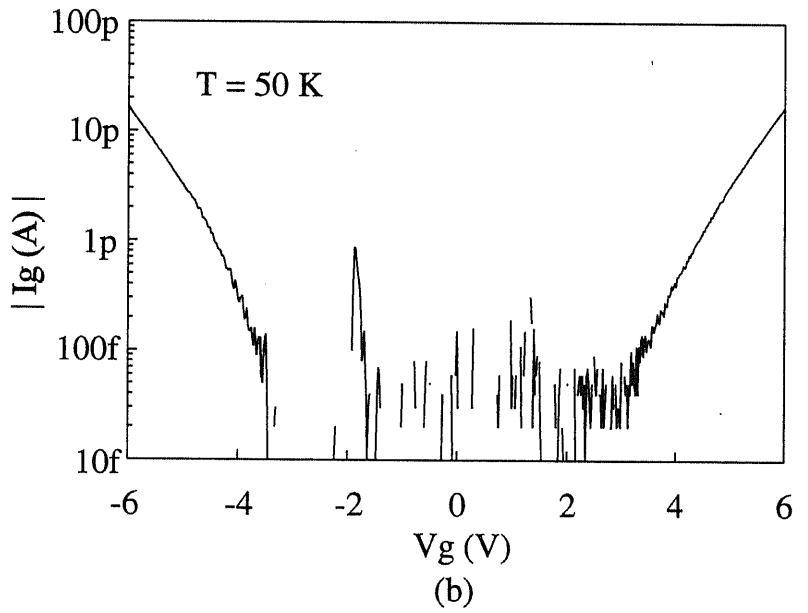


Figure 5.3: Adjustment of peak positions by charge injection into the Si nano-crystals on the channel. The adjustment of peak positions are realized with much lower gate voltage than the previous experiments. (b) Although the gate current begins to flow at $V_g = 3.5$ V, it is confirmed that the charge trapping out of the Si-nano-crystals are negligible from the experimental results of the device without Si nano-crystals.

but by the injected electrons into the floating dots, though the gate leakage current begins to flow from $V_g = 3.5$ V (Fig. 5.3(b)). In this system, potential of the channel dot is raised by the Coulomb effect of electrons injected into the floating dots, which results in the shift of threshold voltage of the device. The device characteristics return to the initial $I_d - V_g$ curves when negative gate voltages ($-6V \sim -8$ V) are applied on the gate and all the electrons in the floating dots are ejected. This result indicates the fact that the base configuration of channel dot structure and channel potential profile are stable, which could not be realized in the system with many interface states or mobile ions acting as uncontrollable background charges.

Different from the experimental results reported in Refs 15, 17, or 18, in our device, the $I_d - V_g$ curves are shifted continuously as a function of applied gate voltage. If a few electrons in the small number of floating dots dominate the change of the potential of the channel dots, the magnitude of peak shift (ΔV_{th}) becomes discrete as a function of applied gate voltage. On the other hand, when the potentials of the channel dot is determined by many electrons in a large number of Si nano-crystals, the $I_d - V_g$ curve is shifted continuously. Considering the large density ($\sim 10^{12}$ cm^{-2}) of the floating dots in our device, a large number of floating dots may locate near the channel dots, resulting in the continuous shift of $I_d - V_g$ curves. This continuous threshold voltage shift is suitable and important feature for the controlling the peak portions of Coulomb blockade oscillations.

5.4 Summary

To avoid the influence of energy level separation by quantum confinement effects and to utilize it for the improvement of the device operation temperature, device structures for the peak adjustment of single electron devices after the device fabrication have been proposed. The peak adjustment by the charge injection into the gate oxide traps is impracticable because of it's high voltage operation, whereas the charge injection into the Si nano-crystals on the channel make it possible to adjust the peak positions with low voltage.

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Chapter 6

Concluding remarks

Investigation of the silicon single electron devices was described in the previous Chapters, especially from the practical point of device application. The discussions were based on the experimental results of single electron tunneling phenomena observed in the silicon nano-size narrow channel MOSFETs. Much attentions were paid on the quantum mechanical effects on the Coulomb blockade characteristics which remain at high temperature, because the quantum mechanical effects play an important role in the devices operating at high temperature. Numerical calculations were also carried out to support the experimental results and evaluate the quantum confinement effects quantitatively. In conclusion, the results obtained in this study are summarized in the following.

In the experiment carried out using the nano-size point contact channel MOSFETs, which was described in Chapter 2, it has been found that

- Quantum mechanical effects become apparent as the aperiodic Coulomb blockade oscillations in the $I_d - V_g$ characteristics, and
- Negative differential conductances as well as fine structures can be observed in $I_d - V_{ds}$ characteristics in the high temperature operating single electron device.

In the experiments carried out to study the issues which have been brought up in the above mentioned experiment, the following results were obtained.

- For the quantitative evaluation of the transport properties in single electron devices, a novel fabrication techniques of silicon nano-scale narrow channels without using fine lithography have been developed.

- It was confirmed that the quantum confinement effects become prominent as the aperiodic Coulomb blockade oscillations when the single electron charging energy becomes around 20 meV.

- The numerical calculations including the anisotropy of the electron effective mass revealed the complex dependence of the energy levels not only on the silicon dot size but also on the shape and orientation.

- From the numerical calculations, it was also found difficult to realize the room temperature operating single electron devices without utilizing the separation of single particle energy levels in the small silicon dot.

- The potential profiles and the causes of the dot formation in the silicon nano-scale narrow channels were investigated based on the transport properties of electron and hole in the same channel.

- To utilize the separation of single particle energy levels in the dot, a method to adjust the peak positions of Coulomb blockade oscillations in single electron devices was proposed and experimentally demonstrated using the charge injection into the Si nano-crystals on the channel.

Appendix A

Transport properties in multiple-dot system

Introduction

In this appendix, some interesting features of transport properties in a multiple-dot system are discussed based on experimental results and numerical calculations. From the results obtained in the experiments [1)] of our laboratory, it is found that transport properties of a multiple-dot channel MOSFET show a thermally activated behavior in the Coulomb blockade regime. This phenomena was explained by a phonon assisted hopping transport model. To verify the hopping transport model, the numerical calculation has been made by solving the master equation of the multiple-dot system. It is also the purpose of this appendix to explain The calculation procedure based on the orthodox theory and used in some parts of this thesis.

Experimental results of a multiple-dot system

A multiple-dot system attracts much attention from the viewpoint of the practical applications as well as the physical interest. From the physical point of view, there are many analogies between the multiple-dot system and the molecule.[2,3)] The multiple-dot systems are also promising structures for the single electron memories which have a long retention time. In the multiple-dot system the inter-dot coupling such as capacitive coupling or

quantum mechanical coupling has a great influence on the transport properties and the energy spectrum in the dots.[4,5]

At first, the experimental results are reviewed.[1] The device used in the experiment is Si extremely narrow channel MOSFET fabricated on the silicon on insulator (SOI) substrate using a novel fabrication technique.[6,7] In the process, the channel width of MOSFET is determined by the thickness of the SOI layer using the anisotropic etching and selective oxidation of Si. The width of the channel is estimated to be less than 10 nm and the channel length is 100 nm. The device shows Coulomb blockade phenomena at room temperature and the oscillations split into some fine peaks when the temperature decreases.[6]

Figure 1 shows the experimental results of the gate voltage (V_g) dependence of the drain current (I_{ds}) at various temperatures. As mentioned before, the large oscillations at high temperatures ($>$ 20 K) split into fine peaks as the temperature decreases. It should be noticed that the current heights of the peaks have different temperature dependences from peak to peak. Furthermore the drain current is suppressed at small V_{ds} even if the V_g is fixed at oscillations peaks.

To investigate the transport properties in more detail, The current peak heights as a function of the inverse temperature are plotted in Figure 2. Peak 1 and Peak 2 are the peaks indicated by dashed lines in Fig. 1. In Fig. 1, the peak positions shift when the temperature is changed. The peak current at the maximum point of the peaks is taken. The reasons of the peak shifts have not been clarified, however, background charges such as interface traps, ionized accepter, or impurity ion in the gate oxide may be the reason. From 20 K to 5 K, when the split peaks are clearly resolved, the temperature dependences show the thermally activated behavior ($I_{ds} \propto \exp(-\frac{\Delta E_{act}}{k_B T})$). Above the 20 K, the temperature dependence becomes stronger. On the other hand, when the temperature is extremely low, the peak currents saturate.

From the fact that, i) the large oscillations at high temperatures split into some fine peaks when the temperature decreases, ii) the current heights of the fine peaks show a thermally activated behavior, and iii) $I_{ds} - V_{ds}$ characteristics show non-linearity at small V_{ds} even if the V_g is fixed at the oscillations peaks, the transport mechanisms in the Si narrow channel are speculated as follows. The channel would be separated into some

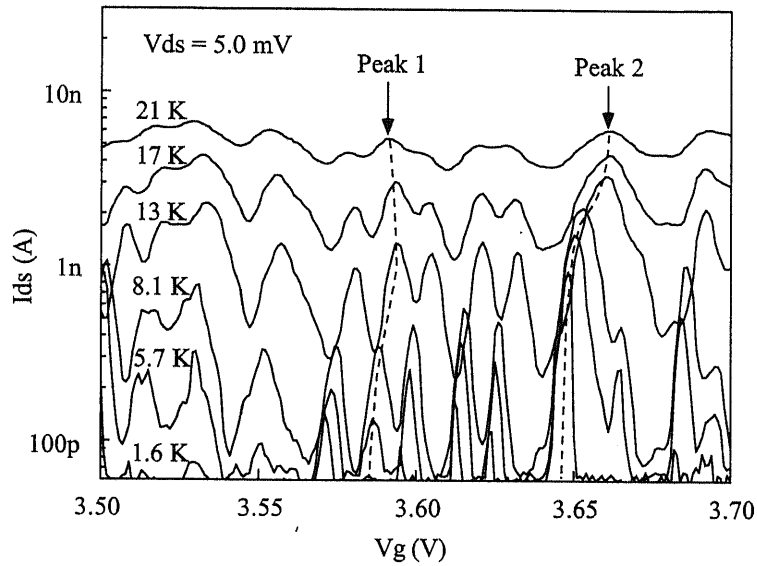

Figure A.1: Experimental transport properties in a Si extremely narrow channel ($W < 10$ nm) at various temperatures.

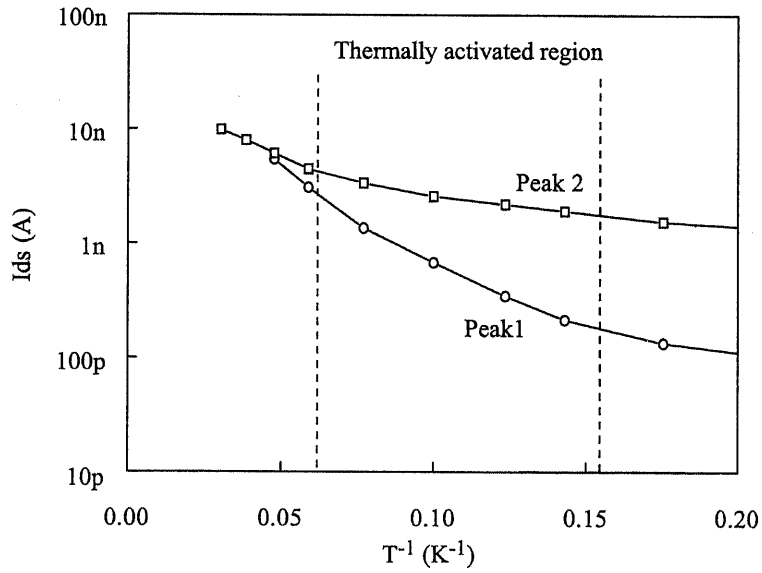

Figure A.2: Experimental peak current heights dependence on the inverse temperature. Peak 1 and Peak 2 are denoted in fig. 1

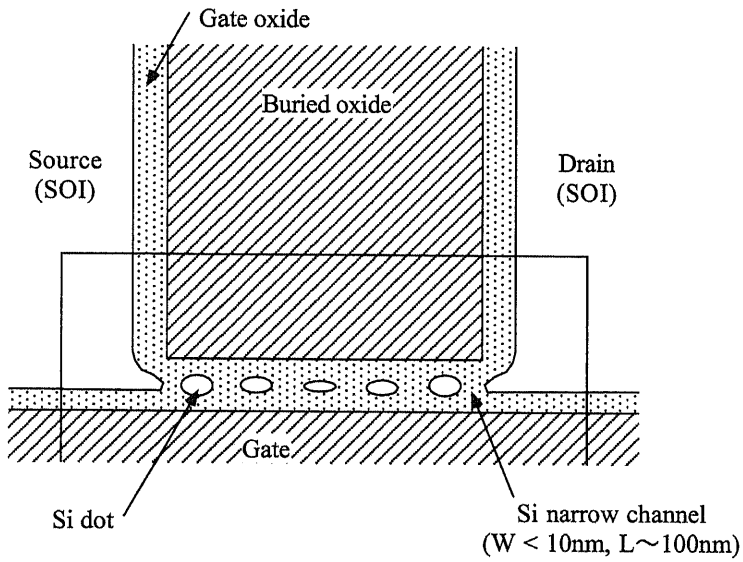

Figure A.3: Multiple-dot model in the Si extremely narrow channel (top view).

dots which are capacitively or quantum mechanically coupled each other as illustrated in Figure 3. The coupling between the dots breaks the degeneracy of the energy level of the dots, causing the peak split at low temperatures. The differences of size, capacitance and background charge of the dots make the energy level differences, which becomes the cause of the phonon assisted hopping transport. If the thermal energy is smaller than the single electron charging energy and coupling energy, the transport path is limited to only one. Thus, the temperature dependence becomes thermally activated behavior. It should be noted that the thermally activated hopping model is different from the one-dimensional variable hopping transport where the temperature dependence is proportional to $\exp(-(\frac{T_o}{T})^{\frac{1}{2}})$.[8)]

Calculation procedure

To verify the transport model in the multiple-dot system, numerical calculations of the $I_{ds} - V_g$ characteristics are carried out. The Si extremely narrow channel is represented by the serial capacitively coupled dots as shown in Figure 4. The configuration of the number of electrons at each dot is represented as $\boldsymbol{n} = (n_1, n_2, \ldots, n_N)$. When $\boldsymbol{n}$, the voltage of each lead, and capacitances are determined, electrostatic potential $E(\boldsymbol{n})$ of the

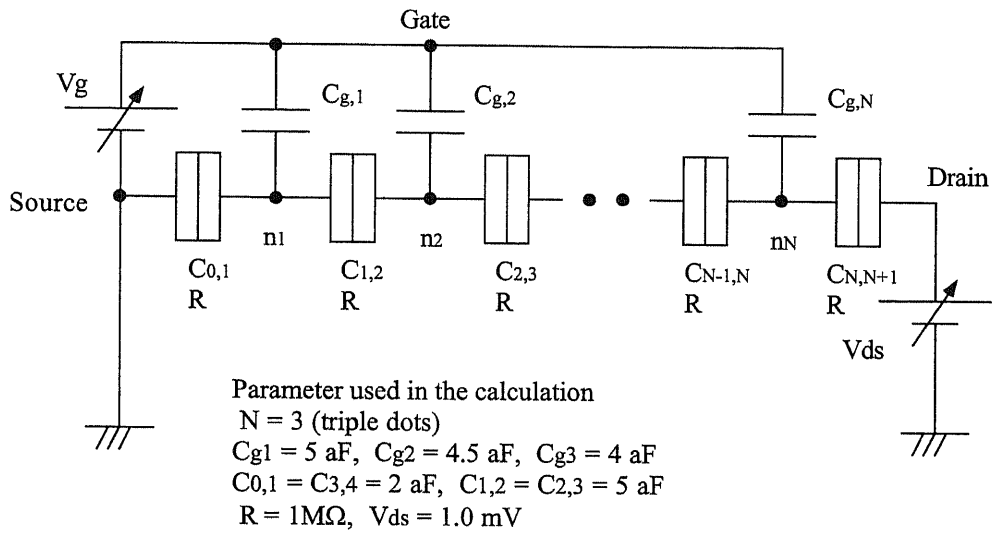

Figure A.4: Represented serial coupled dots model of the Si extremely narrow channel. The n_i indicates the electron number in the i th dot. $C_{g,i}$ is the capacitance between the gate and i th dot. Inter-dot capacitance is represented as the capacitance $C_{i,i+1}$. The calculations were carried out at $C_{1,g} = 5$ aF, $C_{2,g} = 4.5$ aF, $C_{3,g} = 4$ aF, $C_{0,1} = 2$ aF, $C_{1,2} = 5$ aF, $C_{2,3} = 5$ aF, $C_{3,4} = 2$ aF, $R = 1$ MΩ

system can be calculated. After the calculation of the $E(\boldsymbol{n})$, the transition rate from $\boldsymbol{m}$ state to $\boldsymbol{n}$ state is calculated using the next equation.[9)]

$$\Gamma_{\boldsymbol{m}\to\boldsymbol{n}} = \frac{1}{e^2 R}\frac{\Delta E}{1-\exp(-\frac{\Delta E}{k_B T})} \tag{A.1}$$

ΔE is the sum of the energy difference from $\boldsymbol{m}$ state to $\boldsymbol{n}$ state and the work done by the voltage source. R is the tunnel resistance at each tunnel junction and assumed to be constant in this calculation. After the calculations of the transition rates, the probability $P(\boldsymbol{n})$ that the system is in the state $\boldsymbol{n}$ is calculated by solving the master equation

$$\frac{\partial p(\boldsymbol{n})}{\partial t} = \sum_{\boldsymbol{m}}(\Gamma_{\boldsymbol{m}\to\boldsymbol{n}}p(\boldsymbol{m}) - \Gamma_{\boldsymbol{n}\to\boldsymbol{m}}p(\boldsymbol{n})). \tag{A.2}$$

The drain current through the i th tunnel junction is then calculated using the single electron tunnel rate through the i th junction ($\Gamma_i^{\pm}$) and

$$I_{ds} = e\sum_{\boldsymbol{n}}(\Gamma_i^{+} - \Gamma_i^{-})p(\boldsymbol{n}). \tag{A.3}$$

The tunneling only between the neighboring dots is considered and the other transitions are neglected. The co-tunneling effects and quantum confinement effects are also neglected.

Simulated transport properties in a multiple-dot system

A serial triple-dot system is taken as example in calculations. 1331 states from the lowest electrostatic energy are used for the calculation. From the peak valley ratio of the large oscillations in the experiments, the average single electron charging energy E_C of the dots can be evaluated. In the gate voltage range of Fig. 1, E_C is the order of 10 meV and the corresponding capacitance of each dot are about 10 aF. The average inter-dot capacitance is also estimated to be about 5 aF from the intervals of the split peaks. Based on the experimental results, the value of each capacitance and tunnel resistance are defined as shown in the caption of Fig. 4. In the real case, it is likely that the multiple-dot system is not symmetric because there must be the size difference of the dots or thickness fluctuations of the gate oxide. In the simulation, the asymmetry of the triple-dot system are taken into account by changing the gate capacitance of each dot.

Figure 5 shows the calculated electrostatic energy of a multiple-dot system. The state (n_1, n_2, n_3) stands for n_1, n_2, n_3 electrons in the left, middle, and right dots, respectively. The electron travels from source to drain via at least four states, for example, like $(000) \rightarrow (100) \rightarrow (010) \rightarrow (001) \rightarrow (000)$. If the four states degenerate, the electron can easily travel from source to drain. On the other hand, if the energy levels of four states are out of alignment, as shown in Fig. 5, the electron must be assisted by the phonon to transfer from one state to the other.

Figure 6 shows the simulated temperature dependence of the $I_{ds} - V_g$ characteristics. Because the exact structure in the channel cannot be determined, the absolute values of the peak positions or peak heights are different between experimental results and calculated results. Here, the qualitative characteristics of the experimental results are discussed. Qualitatively, the simulated results are similar to the experimental results. The large oscillations at high temperatures split into some fine peaks because of the capacitive coupling between dots. The intervals of the large oscillation peaks at high temperatures correspond to the single electron charging energy of the dots. The intervals of the split

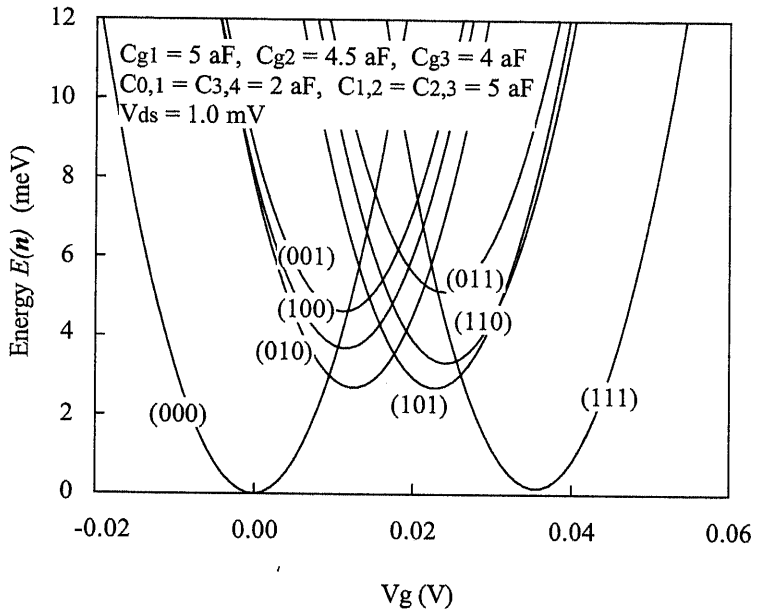

Figure A.5: Electrostatic potential of the system at each state.

peaks are determined by the inter-dot capacitances. The temperature dependences of the current peaks differ form peak to peak which is also in good agreement with the experimental results. Attentions are paid on the current peaks that are located at $V_g = 0.011$ V (Peak 1) and at $V_g = 0.054$ V (Peak 2).

Figure 7 shows the current heights of Peak 1 and Peak 2 as a function of the inverse temperature. Below 20 K (above 0.05 K^{-1} of the horizontal axis in the figure), the peak heights are thermally activated ($I_{ds} \propto \exp(-\frac{\Delta E}{k_B T})$). Therefore, it would not be due to the one-dimensional variable hopping transport ($I_{ds} \propto \exp(-(\frac{T_o}{T})^{\frac{1}{2}})$).[8] This result agrees with the experimental results. Above 20 K (below 0.05 K^{-1} of the horizontal axis in the figure), on the other hand, both the temperature dependences in the simulation and the experiment become like the one-dimensional variable range hopping transport.

In the multiple-dot system where the single electron charging energy (E_C) is larger than the thermal energy, the transport is dominated by the phonon assisted tunneling. Furthermore, if the inter-dot coupling energy (E_{couple}) is larger than the thermal energy, the transport becomes thermally activated behavior. That is, at low temperatures ($k_B T, V_{ds} < E_C, E_{couple}$), the electron transport is limited by only one energy cycle and the activation energy is determined by the energy difference between the states.[10,11] At high

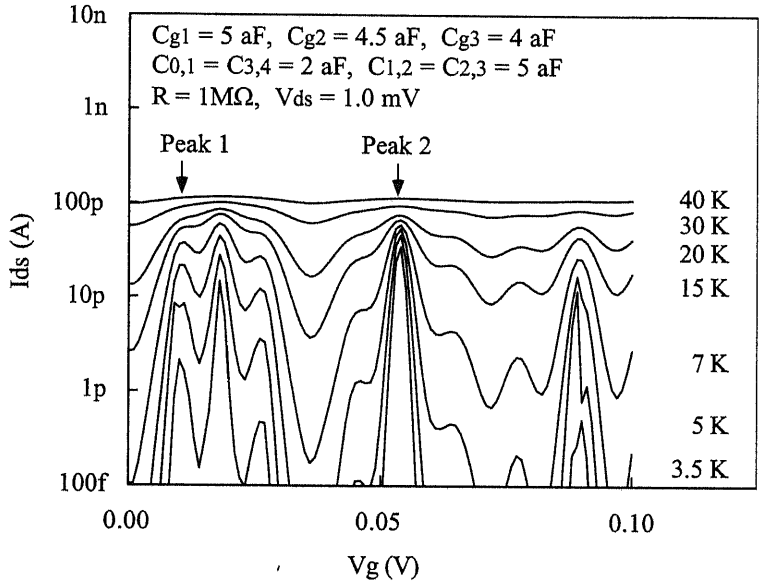

Figure A.6: Calculated characteristics of the $I_{ds} - V_g$ as a function of the temperature. V_{ds} is fixed at 1.0 mV

temperatures ($k_BT, V_{ds} > E_C, E_{couple}$), other cycles become to contribute to the current and the transport becomes like the variable range hopping. In this case, the hopping cites are not the spatially distributed localized states but the Si small dots.

To see the transport mechanisms in detail, the diagram of the transition cycle of the triple dots at $V_g = 0.011$ V is shown in Figure 8. The values denoted beside each state are the existence probability and the values denoted beside the arrows indicate the current which is carried by the transition. Transition cycles among seven states are shown. Fig. 8 (a) shows the result at 4.2 K (thermally activated transport regime). From the figure, it can be understood that I_{ds} is dominated by the cycle (000) $\rightarrow$ (100) $\rightarrow$ (010) $\rightarrow$ (001) $\rightarrow$ (000). The activation energy is determined by the energy difference between these states. The other cycles have almost no contribution to the I_{ds}. Fig. 8 (b) shows the result at 30 K (variable range hopping regime). Different from the result at 4.2 K, not only the cycle (000) $\rightarrow$ (100) $\rightarrow$ (010) $\rightarrow$ (001) $\rightarrow$ (000) but also other cycles have contribution to the I_{ds}. In Fig. 8 (b), the sums of the current at each node are not become zero, because there are many other cycles.

At very low temperatures, the experimental temperature dependences of the cur-

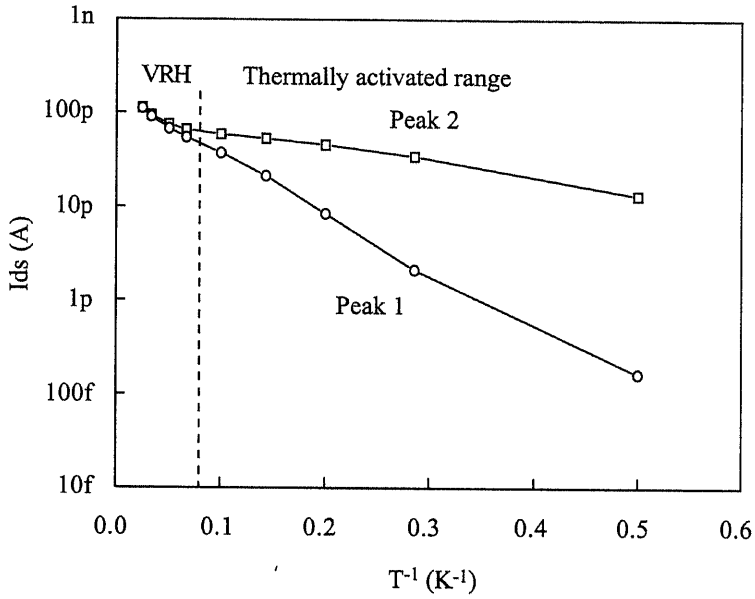

Figure A.7: Calculated peak current heights dependence on the inverse temperature.

rent peaks become weak and the discrepancy between the experimental and calculated results becomes large. This saturation of current at low temperatures would be attributed to a result of the relatively high drain voltage and resonant tunneling which is not considered in the simulation.

Summary

The transport in the Si narrow channel MOSFET were investigated using a phonon assisted hopping transport model in a multiple-dot. The experimental results are confirmed by the numerical calculation by solving the master equation. It is found by the calculation that in the multiple-dot system where the single electron charging energy and the inter-dot coupling energy is larger than the thermal energy, the transport is dominated by the thermally activated hopping.

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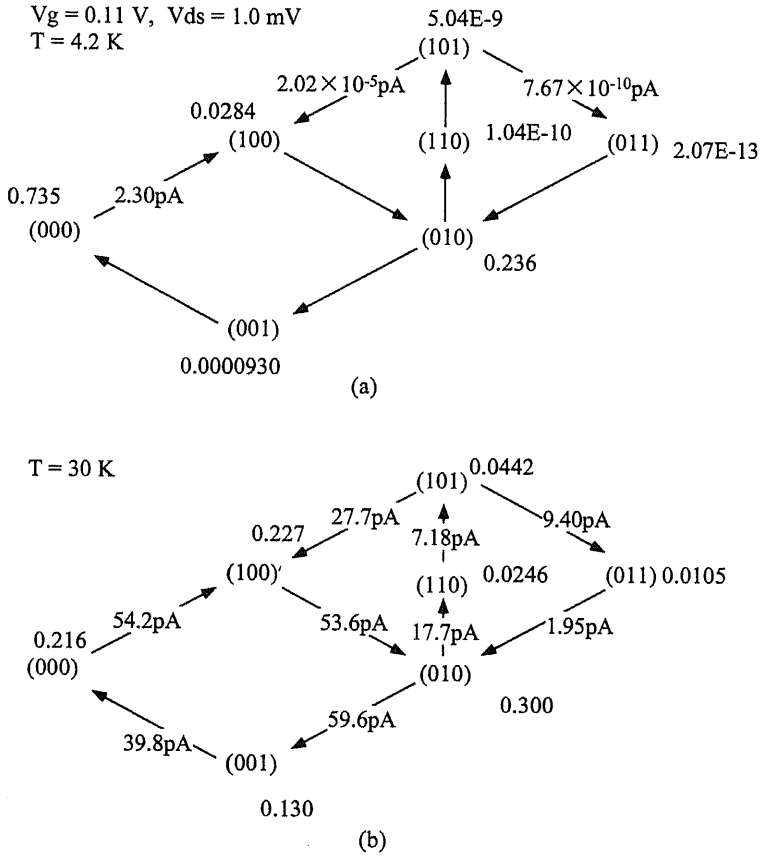

Figure A.8: Probability distribution of each states at (a) 4.2 K and (b) 30 K.

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Appendix B

Calculation of energy levels in Si dots by the finite element method

For the calculation of electronic structure in silicon quantum dots, many approaches are proposed and used. In this section, calculation procedure of energy levels in silicon dots by finite element method [1–5] are explained. Because of the requirement for the calculation of a relatively wide range of dot size ($2 \sim 20$ nm), effective mass approximation is employed.

In the effective mass approximation taking into account the anisotropy, three dimensional stationary state Schrödinger equations are described as

$$\left\{-\sum_{k=1}^{3}\sum_{l=1}^{3}\frac{\hbar^2}{2}\frac{\partial}{\partial x_k}\left(m_{kl}^{-1}\frac{\partial}{\partial x_l}\right)+V(\boldsymbol{r})\right\}\psi(\boldsymbol{r})=\varepsilon\psi(\boldsymbol{r}), \tag{B.1}$$

where the m_{kl} is the elements of effective mass tensor. In silicon, if the x, y, and z axes are taken along the (100), (010), and (001) directions, the Equation (B.1) is simplified as

$$\left\{-\frac{\hbar^2}{2}\left(m_{11}^{-1}\frac{\partial^2}{\partial x^2}+m_{22}^{-1}\frac{\partial^2}{\partial y^2}+m_{33}^{-1}\frac{\partial^2}{\partial z^2}\right)+V(\boldsymbol{r})\right\}\psi(\boldsymbol{r})=\varepsilon\psi(\boldsymbol{r}). \tag{B.2}$$

The solution of Equation (B.2) is transfered to the problem to find a function ψ that satisfies the next equation

$$\int_\Omega\left\{\frac{\hbar^2}{2}\left(m_{11}^{-1}\frac{\partial u}{\partial x}\frac{\partial \psi}{\partial x}+m_{22}^{-1}\frac{\partial u}{\partial y}\frac{\partial \psi}{\partial y}+m_{33}^{-1}\frac{\partial u}{\partial z}\frac{\partial \psi}{\partial z}\right)+uV\psi\right\}d\Omega=\varepsilon\int_\Omega u\psi d\Omega \tag{B.3}$$

for every smooth test function u which vanishes on $\partial\Omega$.

Assume that the domain Ω is divided into a mesh consisting of small simple non overlapping finite elements Ω_e such that $\Omega = \bigcup_{e=1}^{m} \Omega_e$ (m is the number of finite elements). Let $\{\boldsymbol{r}_i\}_{i=1}^{n}$ be the nodes in the grid, and $\{N_i\}_{i=1}^{n}$ the corresponding basis functions (n is the number of nodes). The approximation $\psi(\boldsymbol{r})$ to the solution of Eq. (B.2) is expressed as

$$\psi(\boldsymbol{r}) = \sum_{i=1}^{n} N_i(\boldsymbol{r})\phi_i, \tag{B.4}$$

where $\{\phi\}_{i=1}^{n}$ are unknown coefficients at each node. If the basis functions $\{N_i\}_{i=1}^{n}$ are chosen as test functions, then the Equation (B.3) can be expressed as

$$\sum_{j=1}^{n} \phi_j \int_\Omega \left\{ \frac{\hbar^2}{2} \left(m_{11}^{-1} \frac{\partial N_i}{\partial x}\frac{\partial N_j}{\partial x} + m_{22}^{-1} \frac{\partial N_i}{\partial y}\frac{\partial N_j}{\partial y} + m_{33}^{-1} \frac{\partial N_i}{\partial z}\frac{\partial N_j}{\partial z} \right) + N_i V N_j \right\} d\Omega$$

$$= \varepsilon' \sum_{j=1}^{n} \phi_j \int_\Omega N_i N_j d\Omega, \tag{B.5}$$

which is transformed to the following generalized eigen value problem

$$\mathbf{K}\boldsymbol{\phi} = \varepsilon \mathbf{M}\boldsymbol{\phi}. \tag{B.6}$$

Each matrix is constructed from

$$\mathbf{K} = [K_{ij}] \qquad \text{(Hamiltonian)} \tag{B.7}$$

$$\mathbf{M} = [M_{ij}] \qquad \text{(Mass matrix)} \tag{B.8}$$

$$\boldsymbol{\phi} = (\phi_1, \cdots, \phi_n)^T \qquad \text{(Wave function)} \tag{B.9}$$

whose matrix element is the sum from the contribution of each finite element and written as

$$K_{ij} = \int_\Omega \left\{ \frac{\hbar^2}{2} \left(m_{11}^{-1} \frac{\partial N_i}{\partial x}\frac{\partial N_j}{\partial x} + m_{22}^{-1} \frac{\partial N_i}{\partial y}\frac{\partial N_j}{\partial y} + m_{33}^{-1} \frac{\partial N_i}{\partial z}\frac{\partial N_j}{\partial z} \right) + N_i V N_j \right\} d\Omega \tag{B.10}$$

$$M_{ij} = \int_{\Omega^e} N_i N_j d\Omega \tag{B.11}$$

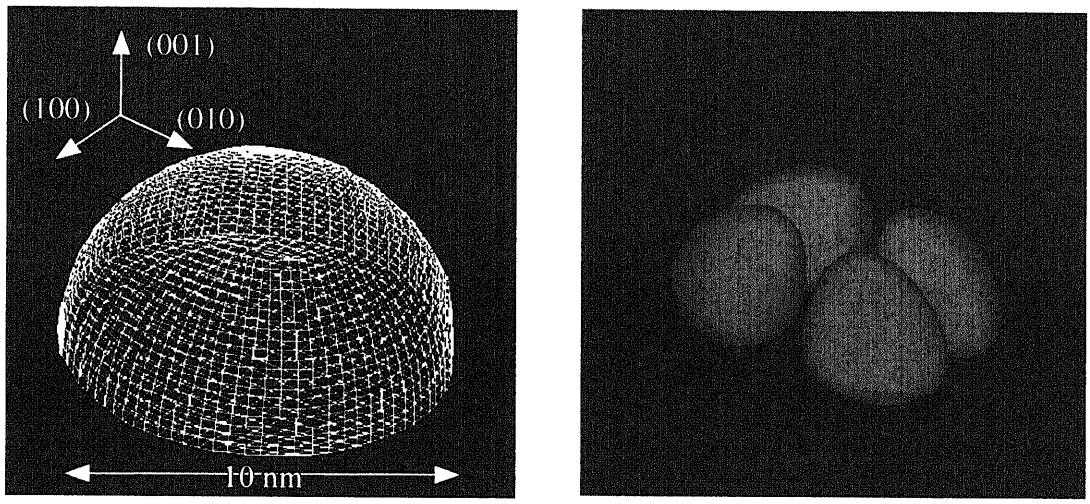
The equations are solved with the Dirichlet boundary condition

$$\psi(\boldsymbol{r}) = 0 \quad \text{on} \quad \partial\Omega. \tag{B.12}$$

Recent progress in the computer systems make it possible to solve a large linear algebra problem in a realistic calculation time with low cost. In this calculation, library

Table B.1: Calculation time of single particle energy states.

System		Calc. time
Pentium II (450 MHz)	Mesh generation	4 min 34 sec
FreeBSD 2.2.6	Eigen value calculation	2 min 53 sec
UltraSPARC II (336 MHz)	Mesh generation	6 min 45 sec
Solaris 2.6	Eigen value calculation	4 min 15 sec



(a) (b)

Figure B.1: (a) Hemispherical silicon dot whose diameter is 10 nm. The dot is divided into $20 \times 20 \times 20 = 8000$ hexahedral finite elements. (b) Calculated wave function of 5 th exited state. The effective mass of the electron in k_x valley is used.

package "Diffpack ver.1.4 [6]" and "Arpack++ [7]", which are free for academic use, are used to solve the problem. Since the current version of Diffpack does not support the eigen value problem, the library is a little modified for this calculation. Each library was complied using the GNU C++ compiler "g++ ver. 2.7". The calculation procedure is as follows.

First, the shape of the silicon dot is defined and divided into finite element using a program "makegrid" in Diffpack. In this calculation, hexahedral finite element is used. Then, based on the grid data generated by the "makegrid", the matrices are calculated using some class in Diffpack from Equation (B.11) whose elements are handed to the

function of Arpack++ in CSC format. The function of Arpack++ solves the generalized eigen value problem (Equation (B.6)) using implicitly restarted Arnoldi method. After the calculation of the eigen values (energy levels) and eigen functions (wave functions), the results are stored in UCD format which can be visualized using the AVS.

Calculation time of the single particle energy levels in 10 nm diameter Si hemisphere dot executed on two system is shown in Table. B.1. The calculated wave function is also indicated in Figure B.1.

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[7] Fortran source code of ARPACK96 and C++ header files of ARPACK++, which is designed to compute a few eigenvalues and corresponding eigenvectors of a general n by n matrix A, can be obtained from "ftp://ftp.caam.rice.edu/pub/people /sorensen/ARPACK/"

Publication list

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