Uniaxial Strain Effects on Silicon Nanowire MOSFETs and Single-Electron/Hole Transistors at Room-Temperature

シリコンナノワイヤ MOSFET および室温動作単電子/単正孔トランジスタにおける一軸歪みの効果

by

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Abstract

The size of a metal-oxide-semiconductor field-effect-transistor (MOSFET) in very-large-scale integrated circuits (VLSI) have been scaled down for higher integration and higher performance. However, potential coupling between source and drain becomes prominent as a gate length is shrunk below to sub-50 nm and this provokes large short-channel-effects (SCEs). As a result, gate controllability to surface potential is weakened, and accordingly, subthreshold leak current becomes remarkable. In order to obtain high SCE immunity using conventional bulk planar-type MOSFETs, high channel doping concentration is required, but high doping level causes mobility degradation and worsens characteristic fluctuation of MOSFETs. Thus, continuous scaling of the conventional bulk planer-type MOSFETs is now facing difficult situation and is challenged by physical and technological limitation.

Silicon nanowire is one of the most promising structure for future ultra-scaled device due to extremely small size and has two attractive devices: gate-all-around (GAA) nanowire MOSFET (NW FET) and SET/SHT. NW FET and SET/SHT are promising devices for ultra scaled nano regime device due to superior SCE immunity and high functionality, respectively. By recent progress in silicon nano-structure fabrication technique, high performance NW FETs having uniform channel size is fabricated, and large Coulomb blockade oscillation in SET/SHT is observed even at room-temperature. On the other hands, strain technology is extensively investigated for mobility enhancement in MOSFET. However, most of the studies have paid attention only to three-dimensional (3D) or two-dimensional (2D) channel MOSFETs, not to ultra-nano scaled one-dimensional (1D) or zero-dimensional (0D) devices, such as NW FET and SET/SHT. Although driving current is gradually not affected by mobility term as device scaled to sub-20 nm because ballistic transport becomes dominant, effective mass which determines incidence velocity is still influential on drain current and the effective mass is controllable by using strain technology. Also, strain in SET/SHT is expected to discover new physics of SET/SHT and improve understanding of operation principals. Therefore, demonstration of strain technology and confirmation of the effects on the NW FET and SET/SHT are strongly desired.

The objective of this work is to investigate the strain technology in the future nano-scaled NW FET and SET/SHT. We confirm the effectiveness of the strain even at ultra narrow NW FET and nanowire size dependency is studied systematically. Also, the strain effect on the novel device SET/SHT which is operated by tunneling mechanism is discussed to discover physics of SET/SHT.

After NW FETs and SETs/SHTs are fabricated by using ultra-narrow channel method, two directions of strain are applied by mechanically. In NW FETs, we observe simple strain effects, namely V_{th} shift and mobility

modulation at low V_{over} and high V_{over}, respectively. NW pFETs provide greater $\Delta I_d/I_d$ than NW nFETs, and nanowire width dependency of the effects is observed for the first time only in NW pFETs because the effective mass m^* modulation is decreased as nanowire width becomes narrower. In SETs/SHTs case, in addition to V_{th} shift and mobility enhancement, Coulomb blockade oscillation characteristics are changed by the strain. While current modulation is very complicated in SETs, strain effects on SHTs are easily analyzed by means of m^* modulation. More current improvement and characteristics modification can be expected, if relatively larger strain (~ GPa) is applied.

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Chapter1 Introduction

1.1 Background

For the past three decades, aggressive scaling of silicon metal-oxide-semiconductor field-effect-transistors (MOSFETs) has achieved great performance enhancement of the device and higher integration in very-large-scale integrated circuits (VLSI). In terms of the gate length of MOSFETs, its size has reached down to sub-50 nm for commercial mass production. According to International Technology Roadmap for Semiconductors (ITRS), it is predicted that the size scaling of MOSFETs will continue and the gate length of MOSFETs for micro process unit (MPU) will be as short as 5 nm in 2020 [1]. However, it is also anticipated that as the size becomes below several tens of nanometers, the gate controllability over electrons and holes in the channel is relatively weakened [2-3] because electrostatic distribution of the channel is easily modulated by drain electrode as the physical distance between the source and drain gets closer and scaling of power supply voltage (V_{dd}) is of much slower than MOSFET's size scaling. As a result, crucial problems, such as short-channel effects (SCEs), rapid increase in power dissipation, etc. have arisen and just simple scaling using a conventional planar structure MOSFET is difficult to guarantee overall performance improvement of the MOSFET. So, another strategies that does not depends on scaling only are required to continue performance enhancement.

Modifying the architecture of MOSFET is one of the ways. Ultra-thin-body (UTB) channel MOSFET using a silicon-on-insulator (SOI) and multi-gate MOSFET, such as double gate MOSFET, FinFET and GAA nanowire MOSFET (NW FET) provide excellent electrostatic characteristics, which are effective for suppressing SCEs [4-6].

The second approach is to introduce novel devices whose operation principle is different from the conventional MOSFETs. For example, impact-ionization MOS (IMOS) [7] or Tunnel FET (T-FET) [8] can lower fundamental minimum subthreshold swing (SS) value of a conventional MOSFET , i.e. 60mV/decade by employing new physical mechanisms, namely impact-ionization and tunneling. Suspended-gate FET (SG FET) [9] and negative ferroelectric capacitor [10] have been also proposed for overcoming SS limit thanks to their intrinsic voltage amplification. Above mentioned devices are very useful for reducing the power dissipation and relaxing from the heating problem. Single-electron transistor/single-hole transistor (SET/SHT) [11-12] is also considered to be one of the most promising devices operating by novel principle. Ultimately small size, high functionality and high compatibility with existing CMOS VLSI are well known for its advantage. Although

SET/SHT had suffered from the low operating temperature which is undesirable for the practical VLSI applications for a long time, recent progress in silicon nano-structure fabrication made SET/SHT to operate at room temperature [13-15]. In such SET/SHT, novel characteristics were observed as a consequence of strong quantum effect and opened up many new applications.

The third means is to improve the intrinsic properties of materials consisting of the MOSFET. Through the last several decades, MOSFET have adopted a silicon-based materials as a major proportion because as follows: Si is one of the cheapest semiconductor, SiO_2 gate dielectric has good interfacial state with Si channel, and finally poly Si gate stack makes enable to use self-align technique which results in easy definition of source and drain region. However, as the device scaled to nanometer regime, Si gradually becomes intolerable under extremely severe conditions. So, alternative materials are intensively investigated recently e.g., high-k dielectric for higher gate coupling with channel, metal gate for low gate depletion, Germanium channel for higher carrier mobility and so on. Instead of direct substitution Si for other materials, there has been a move to change the inherent properties of Si. The strain technology is extensively investigated for mobility enhancement of the MOSFET [16-20], and uniaxial strain is already widely used in mass production. However, most of the studies on strain have paid attention only to three-dimensional (3D) [16-19] or two-dimensional (2D) [20] channel MOSFETs, not to ultra-nano scaled one-dimensional (1D) or zero-dimensional (0D) devices, such as NW FET and SET. Moreover, mobility booster is more essential to the NW FET because carrier mobility is degraded as nanowire diameter decreases in NW FET [21-22]. Thus, demonstration and confirmation of the strain effect on the nano regime devices are strongly desired.

1.2 Objectives

The objective of this work is to investigate the strain technology in the future nano-scaled NW FET and SET/SHT. We confirm the effectiveness of the strain even at ultra narrow NW FET and nanowire size dependency is studied systematically. Also, the strain effect on the novel device SET/SHT which is operated by tunneling mechanism is discussed to discover physics of SET/SHT.

1.3 Chapter Organizations

In Chapter 2, the basics of the NW FETs and SETs/SHTs are introduced, and especially fundamental physics of SETs/SHTs are elucidated in detail. Also, fabrication techniques for NW FETs and room-temperature operating SETs/SHTs used throughout this study are introduced. In Chapter 3, experimental results of strain measurements are described. Some results are analyzed by means of hole band calculation. Finally in Chapter 4, the conclusion of this thesis is given.

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Chapter 2 Silicon Nanowire Structure and Strain Technology

2.1 Introduction

Nanotechnology has been attracted a high level of interest these ten years for its possibility to find new functions in ultra-small (nano) structures. Naturally, it has been the huge potential source of the new-principle VLSI devices and many kinds of materials such as silicon, compound semiconductors, carbon, organic materials, biomedical materials, etc... have been investigated for the use in nanotechnology. Among these various materials, silicon-based materials are the best candidates for its purpose because they can enjoy the highly qualified conventional technologies for miniaturization, which have been originally developed for the MOSFETs.

Silicon nanowire is one of the most promising device structure for future scaled down device, and there are two attractive devices using nanowire structure. Gate-all-around (GAA) nanowire MOSFET (NW FET) is showing excellent gate control to enable fast on/off switching and has good short channel effects (SCEs) immunity [1-3]. The other device adopting nanowire structure is a single-electron/hole transistor (SET/SHT) [4-8], which is expected highly functional devices due to its unique operation principle [9-11]. By recent progress in silicon nano-fabrication technique, it becomes possible to observe large Coulomb blockade oscillation (CBO) even at room temperature [7-8,12] and physical characteristics related to fundamentals of SET operation are partly reported by RT measurement [12-15]. However, basic analysis and enhancement of the device performance are still required for RT operating SET/SHT to be used in actual VLSI circuits.

On the other hand, strain-silicon has been extensively investigated for mobility enhancement and the large number of strained-silicon technologies already in production [16-19] because performance gain is significantly larger than other techniques and additional cost for fabrication is considerably low [20].

In this chapter, silicon GAA NW FET and SET/SHT are introduced as representative devices using nanowire structure, and basics of the devices as well as fabrication method are elucidated. Also, fundamentals of strained-silicon are discussed in detail, since they will be the basic backgrounds throughout this thesis.

2.2 Gate-all- around (GAA) Nanowire MOSFETs (NW FETs)

GAA NW FET has good SCE immunity by the surrounding gate as mentioned in Chapter 1. and has extremely small size. The better immunity to SCE in the same channel length makes it possible to aggressively reduce

impurity doping level in the channel (N_{sub}), which leads to greater carrier mobility at a given surface carrier concentration (N_s) in general [21]. In addition, recent studies show that carrier transport becomes ballistic in NW FET because the frequency of carrier scattering is diminished as the channel length becomes comparable with the mean free path of the carriers in the inversion layer [22-23], and a drive current enhancement is expected [24-25]. Also, quantum-mechanical size effects become important in nanoscale MOSFET where the inversion layer is just a few nanometers thick and wide [12,26], and the effects present new opportunities and new challenges to nano regime devices.

2.3 Single Electron/Hole Transistors (SETs/SHTs)

Single-electron transistors (SETs) and single-hole transistors (SHTs) are promising candidates for novel devices to overcome scaling limitation as described in the previous section. The operation of SETs/SHTs is based on the quantum mechanical single-charge tunneling and classical electrostatic Coulomb blockade. SETs/SHTs have many advantages compared to conventional MOSFETs. Since the typical dot size, the critical size of the device, is less than 10 nm and the performance of SETs/SHTs is enhanced by reducing dot size, they have high potential to form ultra-high-dense integrated system. Also, single-electron tunneling allow to pass only one carrier at one time, result in ultra-low power consumption because the power dissipation is proportional to the number of electrons participating in their operation. The biggest benefit is high functionality by taking advantage of current oscillation phenomenon originating from its unique operation principle.

2.3.1 Coulomb Blockade Effect

Coulomb blockade effect is the most fundamental phenomenon used in single-electron devices (not only in SETs/SHTs but also in single-electron memories, single-electron transport devices, etc…) to control the motion of a single electron. In this section, electron (SET) system is mainly considered for simplicity, since the charge polarity is just the opposite in the hole (SHT) case. Here, let us consider a small conductive dot connected to ground (large reservoirs as source) via tunnel junction as the simplest single-electron device, single-electron box, shown in Figure 2.1(a). Electrons can tunnel to the dot by applying voltage to the gate electrode which is capacitively coupled to the dot. If one electron tunnels to the dot, the increase of the electrostatic (Coulomb charging) energy ΔU in the system is expressed as

$$\Delta U = \frac{e^2}{2C_{dot}}, \quad (2.1)$$

where e is the elementary charge, and C_{dot} is the total capacitance of the dot. When the dot size becomes sufficiently small (C_{dot} is small) and ΔU starts to exceed the thermal energy, even a single electron cannot tunnel

to the dot without the help of external gate bias to overcome the Coulomb repulsion of the dot. This effect is called Coulomb blockade and it is the basic of the operation of SETs. When Coulomb blockade works in the system, electron is added to the dot one by one as the gate bias increases as e/C_g in a step-like manner at zero temperature as shown in Figure 2.1(b). Note that at finite temperature, this increase of the electron number is not step function since excited electrons by thermal energy make it blurry.

2.3.2 Operation Principle of SETs

Figure 2.2 shows the equivalent circuit of an SET. In general, SET is a three-terminal device having gate, source and drain electrode as a MOSFET, thus the three reservoirs are capacitively coupled to a small conductive dot. While the conventional MOSFET delivers electrons by diffusion or drift, in the SET source and drain reservoirs consist of tunnel junctions so that electrons can tunnel between the dot and source/drain. The gate manipulates the potential of the dot and flow of the electron from source to drain (drain current).

A. I_d - V_g Characteristics

The drain current characteristics of the SET are roughly given by the following manner. When there is n electrons in the dot, the total energy $E(n)$ of the system is expressed as

$$E(n) = U(n) + \sum_{k=0}^{n} \varepsilon_k = \frac{(ne - C_g V_g - C_d V_{ds})^2}{2C_{dot}} + \sum_{k=1}^{n} \varepsilon_k , \quad (2.2)$$

where $U(n)$ is the electrostatic energy of n electrons, ε_k is the k-th quantum energy level in the dot, C_d is the drain capacitance to the dot, and V_{ds} is the drain voltage. Since we assume a semiconducting dot here, ε_k is comparable to $U(n)$ when the Fermi wavelength becomes small as the dot size and quantum confinement occurs. In the following discussions, we assume that V_{ds} is sufficiently small (i.e. very small bias). Also, absolute zero temperature is assumed.

The electrochemical potential of the nth electron in the dot, μ_n is expressed as a difference of the total free energy of the system when electron number changes from n-1 to n,

$$\mu_n = E(n) - E(n-1) = \frac{(2n-1)e^2 - 2eC_g V_g}{2C_{dot}} + \varepsilon_n . \quad (2.3)$$

When the electrochemical potential of the dot is between that of source and drain as shown in next expression,

$$\mu_{n+1} > \mu_s \geq \mu_n \geq \mu_d > \mu_{n-1} , \quad (2.4)$$

where μ_s and μ_d are the electrochemical potential in the source and the drain, respectively, an electron can move from source to drain via dot one by one. This is called single-electron tunneling shown in Figure 2.3(a) and the

number of electrons in the dot can be n or n - 1. Meanwhile, when μ_n is below μ_d,

$$\mu_{n+1} > \mu_s \sim \mu_d > \mu_n , \quad (2.5)$$

an electron tunneling is forbidden by Coulomb blockade as shown in Figure 2.3(b). Now, the number of electrons in the dot is fixed to n. By increasing gate voltage V_{gs}, the condition of single-electron tunneling and that of Coulomb blockade are alternately satisfied and the drain current I_d oscillates as shown in Figure 2.4. This oscillation is called Coulomb blockade oscillation (CBO). Whenever V_{gs} comes to the valley of the oscillation, the number of electron in the dot increases by one. The interval between the each peak ΔV_g is determined by the single-electron addition energy E_a, which is the energy for adding another electron to the dot, and gate coupling ratio $\alpha = C_g/C_{dot}$.

$$\Delta V_g = \frac{E_a}{e\alpha} = \frac{C_{dot}}{eC_g} E_a , \quad (2.6)$$

Here, E_a is expressed as follows,

$$E_a = \mu_n - \mu_{n-1} = \frac{e^2}{C_{dot}} + (\varepsilon_n - \varepsilon_{n-1}) = E_c + \Delta\varepsilon , \quad (2.7)$$

where E_c (= e^2/C_{dot}) is the single-electron Coulomb charging energy and $\Delta\varepsilon$ (= ε_n - ε_{n-1}) is the quantum level spacing. Substituting Equation 2.7 to 2.6, ΔV_g can be rewritten as

$$\Delta V_g = \frac{C_{dot}}{eC_g}(E_c + \Delta\varepsilon) = \frac{e}{C_g} + \frac{\Delta\varepsilon}{e\alpha} . \quad (2.8)$$

It is worth noting that the interval of the Coulomb blockade oscillation is constant to e/C_g in quantum dot with very small quantum level spacing ($\Delta\varepsilon \approx 0$), such as metal dot or large semiconductor dot case.

B. I_d - V_d Characteristics

Next, we consider the case when V_{ds} is not negligibly small. When V_{gs} is at the peak of Coulomb blockade oscillations, I_d monotonously increases as $|V_{ds}|$ is increased from zero, as shown by the solid line in Figure 2.5. On the other hand, when V_{gs} is set to the Coulomb blockade condition (valley of the oscillation), I_d is suppressed (Coulomb blockade continues) until a certain $|V_{ds}|$, where μ_d goes below μ_n or μ_{n+1} becomes smaller than μ_s due to capacitance coupling between drain and dot, is applied, shown by the dashed line in Figure 2.5. Above this $|V_{ds}|$, Coulomb blockade is lifted and I_d monotonously increases.

While Coulomb blockade oscillations are observed in the I_d-V_g characteristics at low V_{ds}, Coulomb staircase, stepwise increase in I_d, is observed in the I_d-V_{ds} characteristics of some kinds of SETs as shown in Figure 2.6.

Each steps of I_d increase corresponds to the increase in the number of electrons that can simultaneously tunnel through the dot when V_{ds} is increase. This curious phenomenon is only observed when the two tunnel barriers of SETs have large difference in the tunneling rates [27]. However, few studies have been done on the applications of Coulomb staircase.

C. Multiple-Dot Type SET

All the basics of the SETs discussed above is assuming single-dot type SET which consists of only a single dot between source and drain. Multiple-dot type SET is an SET with more than two dots connected in series. The size of the each dot may be different. In multiple-dot system, its current characteristics are basically more complicated than that of the single-dot type. Since each dot has different electrochemical potential due to their different size, the condition for the single-electron tunneling becomes so complex (electrochemical potential of all the dots must satisfy Equation 2.4) that the drain current will be the combination of Coulomb blockade oscillation of the small dots and large dots. Figure 2.7(a) and 2.7(b) are the comparison of the Coulomb blockade oscillations in single-dot type and multiple-dot type SET, respectively [28-29]. Compared to the single-dot type in Figure 2.7(a), sharp and non-periodic oscillation is frequently observed at low temperature in Figure 2.7(b) due to the contribution of the Coulomb blockade oscillation in the large dot that suppresses the oscillation of the small dot. As the temperature increases, some peaks merge into a large one, indicating that the oscillation originating from small dot now dominates the whole transport characteristics at high temperature. These nature of the Coulomb blockade in multiple-dot system is called stochastic Coulomb blockade [30,31]. Also, temperature dependence of the I_d is much stronger in multiple-dot system. This is also the result of the stochastic Coulomb blockade in multiple-dot SETs [31].

D. Quantum Effect in SETs/SHTs

As can be easily imagined from Equation 2.7, if the quantum level spacing $\Delta\varepsilon$ significantly contributes to the single-electron/hole addition energy E_a, interval of the Coulomb blockade oscillation peak ΔV_g may not be periodic as e/C_g in the case of conventional SETs/SHTs, since $\Delta\varepsilon$ hardly be the same for every quantized energy level. This non-periodic oscillation appears even if the SET/SHT is single-dot type.

In fact, this effect has been intensively studied and utilized in SETs made of compound semiconductors like GaAs to extract quantized energy spectrum in the quantum dot [32]. It has been found that quantum dots show atom-like energy spectrum (shell structure) and act as artificial atoms [33]. These results have been opened up broad fields to investigate physics of quantum dot physics. However, Non-periodicity generally behaves as a

drawback for integrating system in the semiconductor SET.

2.3.3 Requirements for SET Operation

In order to realize the SET operation described in the previous section, two requirements have to be satisfied. The first requirement is that the single-electron addition energy E_a must be sufficiently larger than the thermal energy k_BT. At finite temperatures, the peak width of Coulomb blockade oscillations broadens because thermally excited electrons at the reservoirs can tunnel through the dot even when the condition for single-electron tunneling (Equation 2.4) is not satisfied. When the temperature increases, the current of Coulomb blockade oscillations, especially of valley current, increases and the oscillations starts to smear out. Hence, E_a must be much larger than k_BT for the observation of large Coulomb blockade oscillations for practical use. Typically, it is known that $E_a > 20 \sim 100\ k_BT$ is required [5]. For room-temperature SET operation, the dot size (diameter) should be less than 3 nm, assuming silicon sphere dot [34]. Figure 2.8 shows huge Coulomb blockade oscillation obtained at room temperature in fabricated silicon SHT [35]. The peak-to-valley current ratio (PVCR) of the oscillation is 1280, which is the highest value till now. Compared to the conventional SETs/SHTs operating at low temperature, the range of the operation voltage (voltage from zero gate bias to the first peak, or peak interval) is considerably large, at the order of 100 mV to 1 V, due to the huge single-electron additional energy.

The second requirement results from the uncertainty principle. Electrons must be strongly localized inside the dot and well separated from the source and drain reservoirs so that the electron number will not fluctuate and be uncertainty. That means, the products between the time $\Delta t \approx R_tC_{dot}$ to transfer charge into and out of the dot, where R_t is the resistance of the tunnel barrier, and the energy $\Delta E \approx E_c = e^2/C_{dot}$ (quantum level spacing $\Delta\varepsilon$ is ignored for simplicity) must ensure the following uncertainty relationship,

$$\Delta t \cdot \Delta E = R_t C_{dot} \cdot E_c = R_t \cdot e^2 > h . \quad (2.9)$$

Therefore, for the observation of clear Coulomb blockade oscillation, tunnel resistance R_t should satisfy the following condition,

$$R_t >> h/e^2 = 25.8\text{k}\Omega . \quad (2.10)$$

Here, $R_q = h/e^2 = 25.8$ kΩ is called the quantum resistance. This requirement indicates important disadvantages of SETs, that is, SETs are inherently high resistive and not suitable for high speed operation.

2.4 Fabrication Techniques of Silicon NW FET and Room-Temperature Operating SETs/SHTs

2.4.1 Fabrication Method of Ultra-Narrow Channel MOSFETs

In our fabrication, NW FETs and SETs/SHTs can be fabricated by totally same process because ultra-narrow channel MOSFET process, basically using the nanowire to form the tunneling barrier and dot of SETs/SHTs, is adopted. The method is the most successful fabrication technique for the room-temperature SETs/SHTs operation. All the fabrication process in this thesis is based on this ultra-narrow channel process.

Ultra-narrow channel MOSFETs [7-9,11-15,31,35] are fabricated by patterning nanowire on silicon-on-insulator (SOI) substrate. A (001)-oriented, p-type bonded SOI wafer, with resistivity of 10 ~ 20 Ωcm, is employed. The thickness of the buried oxide (BOX) layer is 200 nm. First, the SOI layer, initially 100nm thick, is thinned down to 20 ~ 30 nm by performing thermal oxidation and HF treatment repeatedly. Then 5 nm SiO_2 hard mask is thermally grown. 30 ~ 60 nm wide wire patterns at intervals of 2.5 nm and mesa patterns are formed by electron beam (EB) lithography using hydrogen silsesquioxane (HSQ) resist as shown in Figure 2.9(a). HSQ is a negative EB resist that is often used for patterning small patterns [36-37]. The nanowire length is 200 nm. The resist pattern is transferred to SOI layer by anisotropic dry etching using Cl_2 gas based reactive ion etching (RIE). Then isotropic etching by SC1 ($NH_4OH/H_2O_2/H_2O$=1/1/6) solution is performed to further narrow the channel. Here, note that the SOI thickness is kept the same during this etching because the top of the nanowire is protected by the mask oxide and HSQ resist as shown in Figure 2.9(b). Therefore, only the lateral side of the nanowire are etched and width of the nanowires are shrunk down to 15 ~ 35 nm. The top mask oxide and HSQ is removed by HF treatment. At this process, since HF solution etches BOX layer as well as the HSQ, the nanowire becomes suspended shape. After the surface cleaning, thermal oxide is grown for gate oxide. Normally, gate thermal oxidation is performed slightly at relatively low temperature (around 900 ℃). Typical gate thermal oxide thickness is about 10 nm. Due to the silicon consumption by the surface cleaning and gate oxidation, the channel is further squeezed and now nanowire width is 1 ~ 20 nm and thickness is less than 5nm as shown in Figure 2.9(c). In fact, some NW FETs with nanowire width narrower than 5nm act as SETs/SHTs operating at room temperature, this will be explained in the next section. Then, additional gate oxide is deposited by low-pressure chemical vapor deposition (LP-CVD). Figure 2.9(d) shows the scanning-electron-microscopy (SEM) pictures of one narrowest nanowire channel just before the gate thermal oxidation. Then, poly-silicon gate electrode is formed by CVD deposition, gate photo-lithography and gate RIE etching. The rest of the processes are ion implantation into gate, source and drain regions (P^+ for NW nFET and SETs, BF^{2+} for NW pFET and SHTs), deposition of passivation oxide, and formation of contact holes and Al electrodes as the normal MOSFETs fabrication. Therefore, room-temperature operating SETs/SHTs can be fabricated by the same fabrication process as NW FET. Figure 2.10 is relationship of threshold voltage (V_{th},

defined as V_g at I_{d0}= 10^{-12}A) vs. nanowire width in fabricated NW FET. Clear V_{th} increasing due to quantum confinement effect is observed for both NW nFET and NW pFET.

2.4.2 Mechanism of Room-Temperature SET/SHT Operation

The formation mechanism of potential wells and barriers in the fabricated ultra-narrow nanowire channel SETs/SHTs is focused. One of the most possible reasons is that potential fluctuations in the channel induced during the fabrication process should act as potential dots and barriers. In the channel formation process, there are two important steps, which probably affect the potential profile of the channel; one is micro-roughness induced during the EB lithography and etching processes, and the other is slight oxidation process.

First, it is considered that the micro-roughness on the nanowire channel surface is responsible for modulating the channel potential profile. There are two etching processes that induce the micro-roughness. The first one is the EB lithography process. In HSQ resist, the root mean square of this roughness is 1 ~ 2 nm [37] and this is transferred to the SOI layer by isotropic RIE etching.. The other source for the roughness is the SC1 wet etching. This alkaline solution is also well-known for inducing micro-roughness of 1 nm on the silicon surface [38]. Although it seems that the roughness from these processes is small, this roughness is large enough to modulate the potential profile of the ultra-narrow wire channel whose width is less than 5 nm due to the strong quantum confinement effect.

The other important process, the slight gate oxidation process, comes after SC1 etching. Choosing appropriate condition, the etching-induced roughness is enhanced and the potential fluctuations in the channel increase. Furthermore, inhomogeneous strain is induced along the roughened channel by the oxidation. The non-uniform band-gap modulation due to the oxidation-induced strain [39,40] might occur along the channel and further increases the potential fluctuations in the channel.

Important experiments have been done to prove that the tunnel barriers and dots are self-formed by the potential fluctuation in the ultra-narrow channel under quantum confinement [12,41-42]. Ishikuro et al. fabricated n- and p-type point-contact channel MOSFETs (the details are described below) as shown in Figure 2.10 and found that the devices with no oscillations in n-type operation do not show oscillations in p-type operation while those with oscillations in n-type always show oscillations in p-type [41]. Since the n^+ and p^+ source/drain regions are connected to the common channel as can be seen from Figure 2.11, this experiment clarifies that the tunnel barriers and quantum wells are self-formed in the conduction band as well as in the valence band. If the potential fluctuations are induced by charges fixed in gate oxide or trapped in interfacial sites, oscillations should be observed at either type of charge polarity. Same experiment has been done in

ultra-narrow channel MOSFETs by Saitoh et al. and the same results were obtained in room-temperature operating SETs/SHTs [42]. Therefore, it can be concluded that the channel potential is actually modulated by the quantum confinement in roughened channel surface.

2.5 Strain Technology

Strained Si has been studied for 50 years [43], but for a long time it had not been adopted in CMOS logic technologies for several reasons. It suffers from defects and performance loss at high vertical electric fields [44], and requires different stress types (tensile and compressive for n- and p- channel, respectively) to simultaneously improve both n- and p- channel devices. However, as MOSFET is scaled down continuously, the distance between the channel and localized stress source gets closer than ever before, and the amount of the strain, that decay rapidly away from a stress source, becomes significantly large value at anywhere on the channel when its size become below deep submicron technologies [43]. Also, additional cost for applying strain is relatively low and the fabrication is simple. As a result, the industry is becoming recognized strain technology as offering the best potential to enhance performance because larger performance gain than high-k gates, fully depleted SOI, or multi-gate devices [20], and today almost every semiconductor manufacturer has exploited strained CMOS [16-19]. In this section, fundamental physics of strained Si and several methods for implementing strain on MOSFETs are illustrated.

2.5.1 Fundamental Physics of Mobility in Strained Si

Before covering strain-altered mobility, we briefly check that which is crucial factor to determine strained MOSFET mobility. The mobility in the MOSFET is simply expressed as

$$\mu = \frac{e\tau}{m^*}. \quad (2.11)$$

where, m^* is conductivity effective mass and τ is scattering rate. So, the effective mass and scattering rate are responsible for mobility modification. The effective mass has three different directions, i.e. two in-plane effective mass (parallel, m_x, and perpendicular, m_y, to transport direction) and out-of-plain effective mass (m_z). Note that we assume that carrier is transported along x axis. m^* in the Equation 2.11 is of course meaning m_x, small effective mass along conductive direction is most important in three m^* for high mobility. However, since density-of-states (DOS) mass is proportional to $(m_x m_y)^{1/2}$, small m_x causes low DOS mass and the subband with light m_x can contain only small number of carriers. Heavy m_y is of advantage to break this limitation due to its large DOS mass. Therefore, light m_x and heavy m_y are ideal to enhance the mobility. Moreover, effective mass vertical to the channel, m_z is also influential term under high vertical electric field. Higher m_z makes thinner

inversion layer [45], and subband energy increasing under strong confinement (high gate bias) is suppressed. Consequently, if the lowest subband has higher m_z than other excited subband, carriers in lowest subband is kept even at high vertical field. Next, we consider scattering rate in MOSFET. It is well known that the mobility in the MOSFET is affected by many scattering sources, such as ion scattering, phonon scattering, and roughness scattering, of which intervalley scattering (a kind of phonon scattering) is most important in mobility modulation in strained MOSFET. The intervalley scattering between two valleys strongly depends on the energy difference. When the strain is applied to material, the energy difference of two subbands is widened (or narrowed), then intervalley scattering probability is reduced (increased). As a result, the mobility is enhanced when the splitting becomes comparable or larger than the optical phonon energy (60 meV).

A. Conduction Band

The conduction band minimum in silicon lies on the Δ symmetry line near the X-point resulting in six equivalent valleys as shown in Figure 2.12(a). If longitudinal direction tensile stress is applied to [110]/(100) oriented MOSFET, six valleys split into lower 2 (Δ_2) and upper 4 (Δ_4) fold valleys as shown in Figure 2.12(b). Therefore, the strain improves the mobility by increasing the electron concentration in the Δ_2 valleys because the repopulation decreases the average conductivity mass and reduces intervalley scattering. In addition, unlike [100] direction strain which is simply understood in terms of energy splitting effect, [110] direction strain has to consider effective mass change [46].

B. Valance Band

Hole transport is more complicated since strain significantly warps the valence band altering both the in- and out-of-plane mass and DOS mass. Under [110] uniaxial stress, great effective mass change along the stress direction takes place by hole band warping [47], while stress-induced energy splitting between heavy and light hole band is negligibly small for strain less than 1 GPa [46]. Further, the mass changes with stress is not constant in k space, an advantageous strain for holes needs to warp the valence band to create a low m_x, and high m_y and m_z as above stated [20].

2.5.2 Sources of Strain

Two approaches exist for implementing strain on MOSFETs: (1) a process-induced strain, where the strain is introduced from standard CMOS unit processes, such as the shallow trench formation (STI) [48], oxidation [49], silicide formation [50], and contact etch stop layer (CESL) [51]. (2) a epitaxial strain, where the strain is engineered into the device mostly by means of SiGe buffer layer [52-53]. Of them, from first- to fourth-

generation strained Si MOSFETs [16,18-19,54-55], the industry is adopting process-induced uniaxial stress. Because larger hole mobility enhancement can be achieved at low strain, stress-induced threshold voltage shift in n-type MOSFET is significantly smaller than biaxial strain [47] and mobility enhancement is maintained to high vertical electric field [20].

In this thesis, we applied mechanical stress to NW FETs and SETs/SHTs by using 4-point bending apparatus as shown in 2.12 and the amount is estimated with analytical model expressed as

$$strain = \frac{yt}{2a\left(\frac{L}{2} - \frac{2a}{3}\right)}. \quad (2.12)$$

Although the mechanical strain has limitation in strain amount, it can easily change strain magnitude, apply same amount of strain repeatedly and investigate strain direction dependence using only one device. So, mechanical strain after MOSFET fabrication is widely used to study strain effect and compare the effect in devices [56-58].

2.5 Summary

In this chapter, characteristics and fabrication methods of NW FET and room-temperature operating SETs/SHTs have been introduced. Starting from merits of NW FET, classical physics and some basic current characteristics in SET, such as Coulomb blockade oscillation, were illustrated. Then, fabrication method of NW FETs and SETs/SHTs is overviewed. Since ultra-narrow channel MOSFETs are used throughout this thesis, NW FET and SET can be fabricated totally same process. Also, strain technology in MOSFET has been explained. In n-type MOSFET, carrier repopulation by band splitting modulates average effective mass and intervalley scattering rate. On the contrast, conductivity mass change by hole band warping makes large mobility modulation in p-type MOSFET. Mechanical strain is applied to MOSFET in this thesis because it can easily switch strain directions and precisely compare the strain effect in different devices.

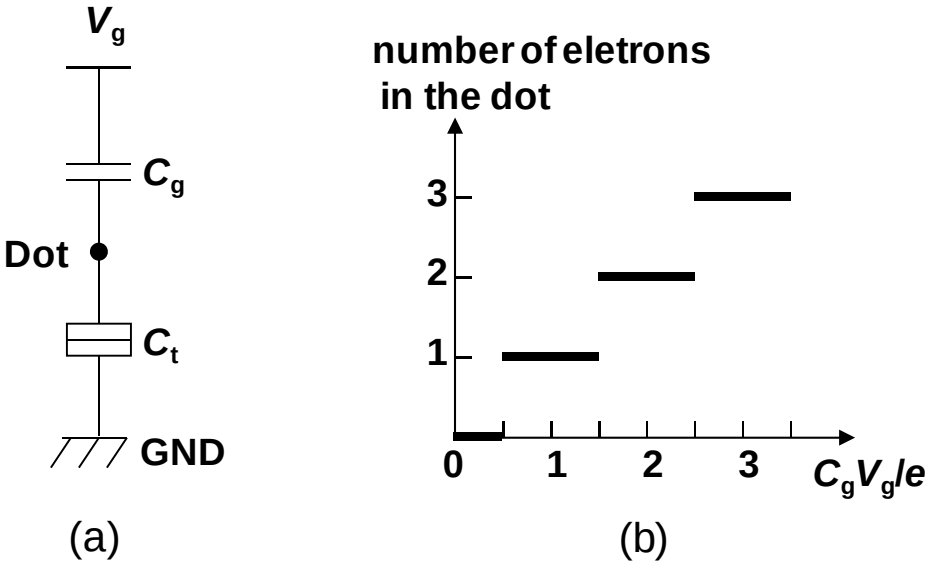


Figure 2.1 (a) Equivalent circuit diagram of a single-electron box. A small conductive dot is capacitively connected to ground (source) and gate electrode (V_g). Electron can tunnel into the dot via tunnel junction. (b) The number of the electron in the dot is added one by one as the gate bias increases as e/C_g.

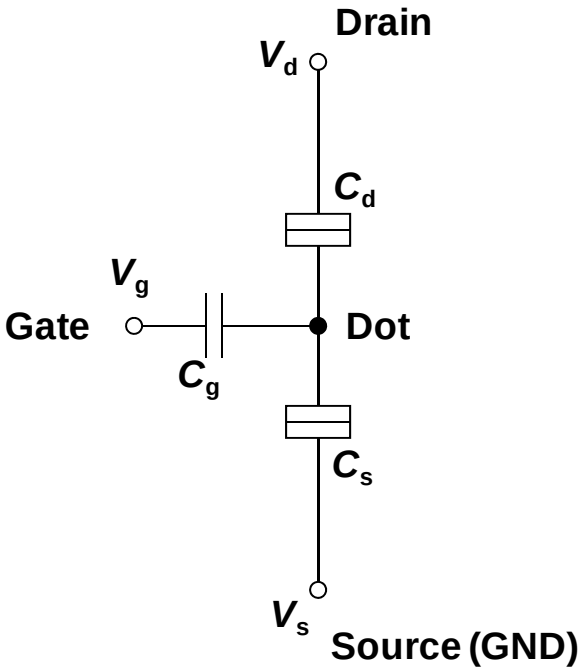


Figure 2.2 Equivalent circuit diagram of a single-electron transistor (SET). Gate, source and drain electrodes are capacitively coupled to a small conductive dot. Electrons can flow from source to drain via tunnel barriers and dot by controlling the dot potential by gate.

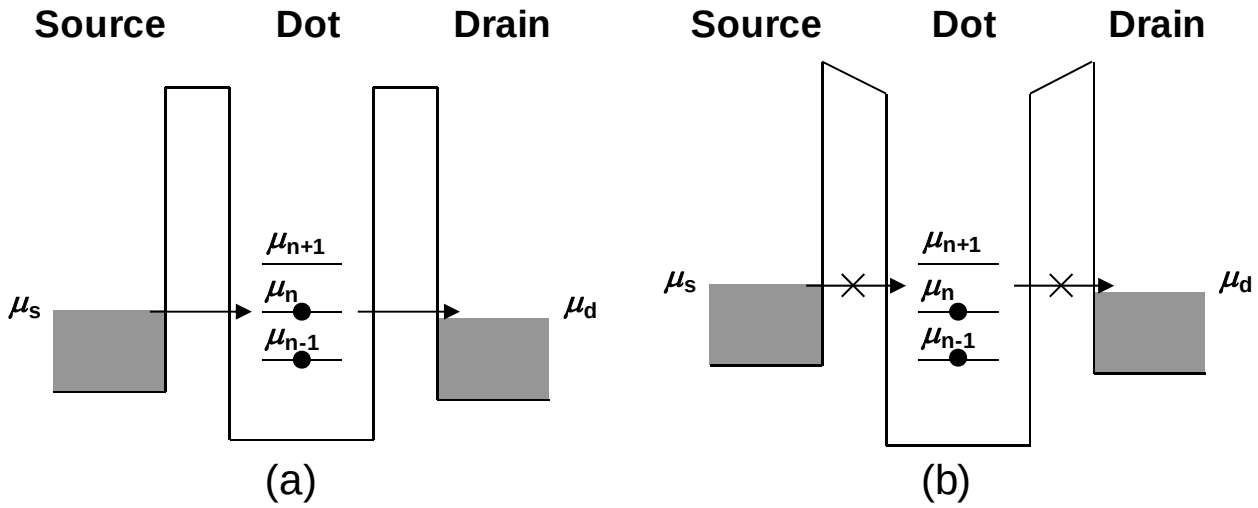


Figure 2.3 Potential profile of an SET. (a) SET is in single-electron tunneling condition (peak current). Electron can tunnel into the dot from source and tunnel out to drain one by one. (b) SET is in Coulomb blockade condition (valley current). Electron tunneling is prohibited and no current flows.

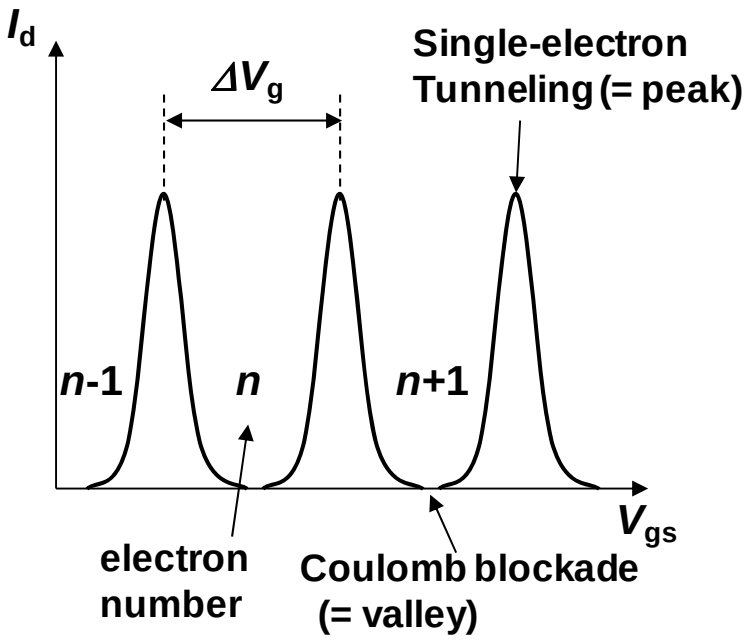


Figure 2.4 Schematic diagram of I_d-V_g characteristic in SET when V_{ds} is low. Coulomb blockade phenomenon makes current oscillation called Coulomb blockade oscillation (CBO). The number of electrons in the dot increases by one when ever V_{gs} comes at the valley of the oscillation.

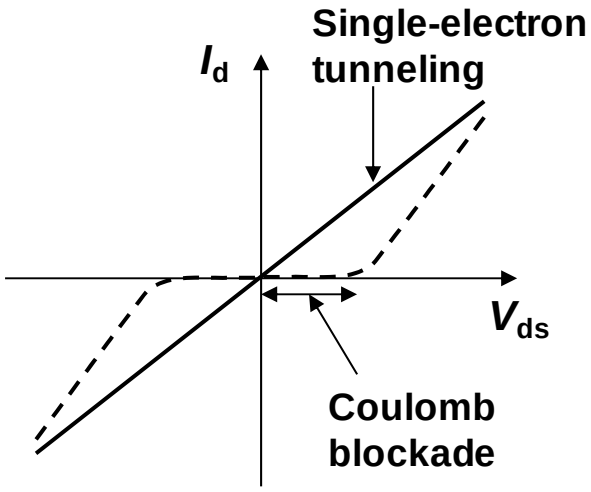


Figure 2.5 Coulomb blockade characteristics observed in I_d-V_{ds} characteristics. Solid line indicates that V_{gs} is at single-electron tunneling condition where dashed line shows V_{gs} at Coulomb blockade condition. I_d is suppressed unless the Coulomb blockade condition is lifted by applying sufficient drain bias.

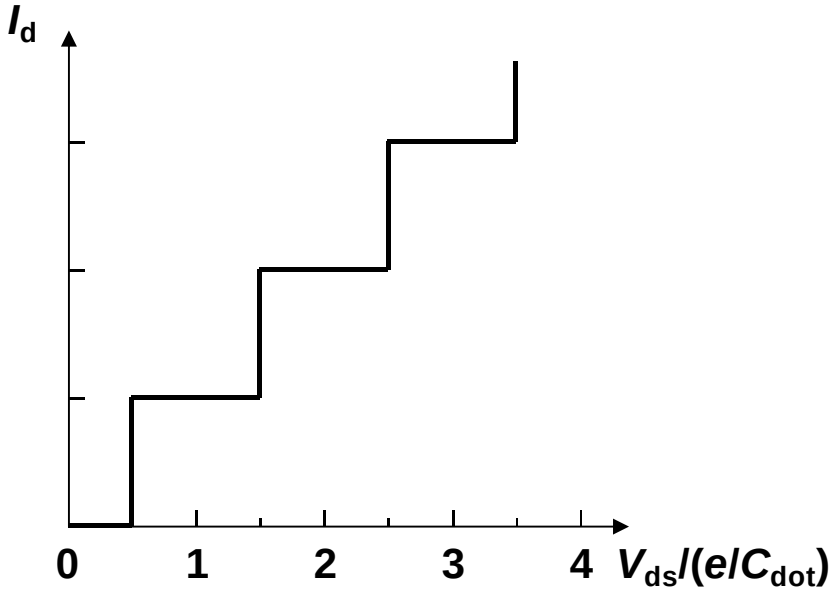
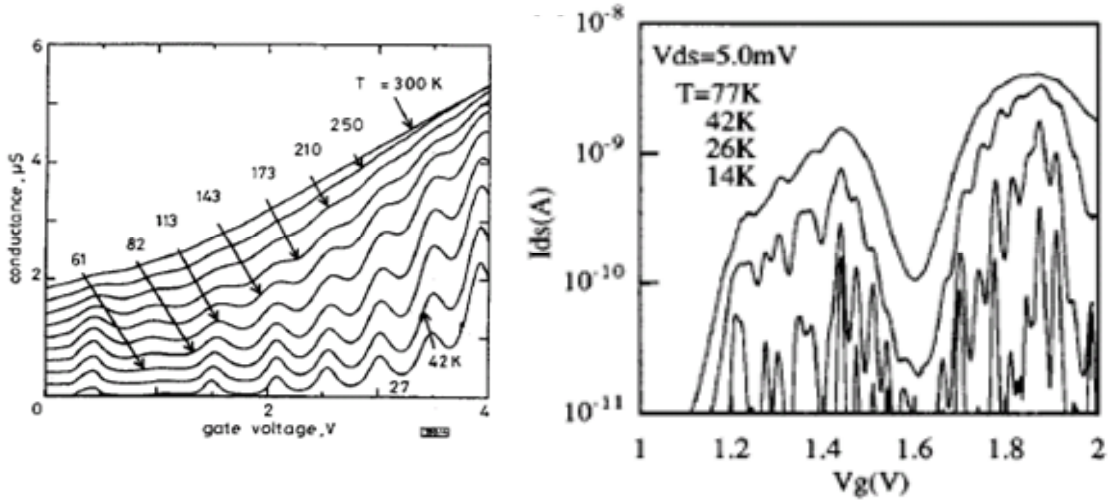


Figure 2.6 Ideal Coulomb staircase at 0 K in an SET with strong asymmetric tunnel barriers. Each current step occurs whenever the electrochemical potential of the dot newly goes under the μ_s so that the number of the electrons that can simultaneously tunnel through the dot increases. The current staircase fades as the temperature increases.



(a) (b)

Figure 2.7 (a) Coulomb blockade oscillation in single-dot type SET [28]. The cycle of the oscillations is periodic. (b) Coulomb blockade oscillation in multi-dot type SET [29]. The oscillations are non-periodic and complicated. Note that the drain current is shown in logarithmic scale. The temperature dependence of the drain current is much stronger than the single-dot type.

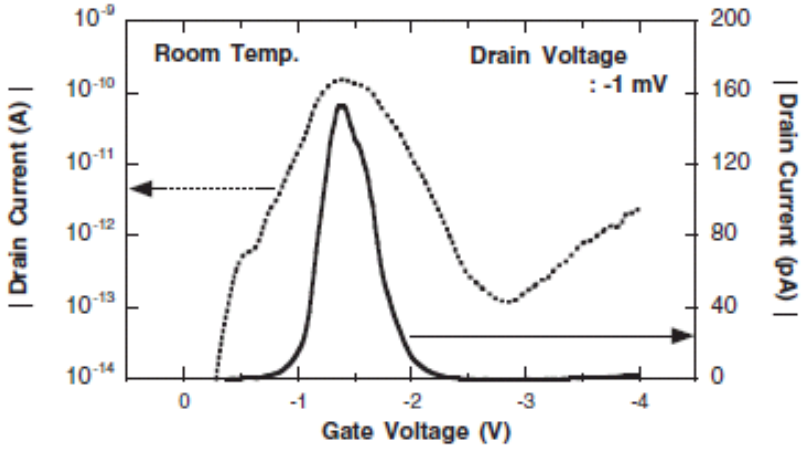


Figure 2.8 Huge Coulomb blockade oscillation observed at room temperature (left axis: logarithmic plot, right axis: linear plot) [34]. The PVCR of 1280 is the record high value observed at room temperature.

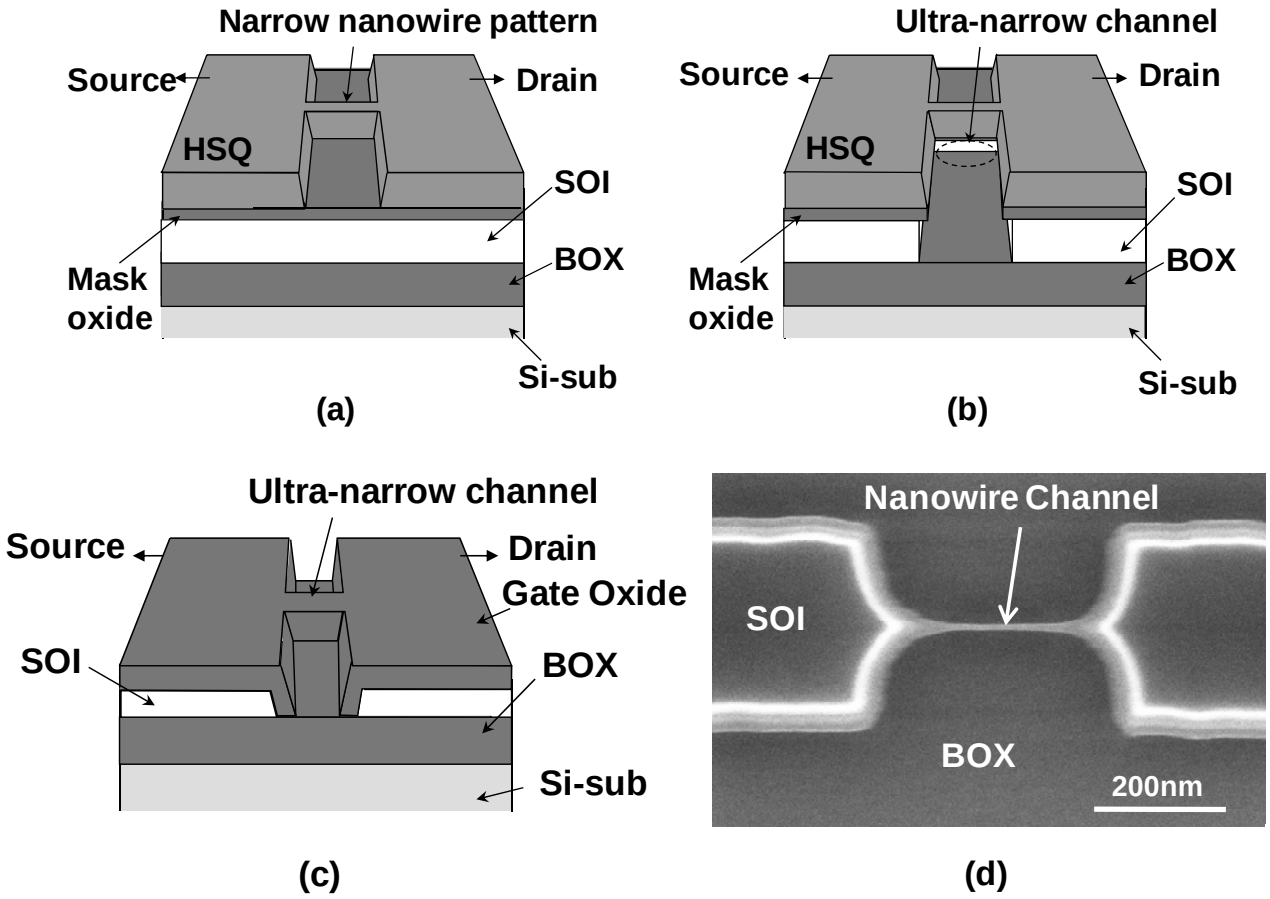


Figure 2.9 Schematic views of the fabricated ultra-narrow channel MOSFETs for NW FET and room-temperature operating SETs/SHTs. (a) After the development of the EB lithography. Narrow nanowire is patterned on HSQ resist. (b) After dry etching and SC1 etching. The sides of the silicon wire are further narrowed by the isotropic SC1 etching. (c) After HSQ and SiO_2 mask removal and gate oxidation. Channel Thickness is less than 5 nm and width is varied from 1 nm to 20 nm. (d) SEM images of the fabricated ultra-narrow nanowire channel before the gate thermal oxidation. The channel width is less than 10 nm at this stage and will further decrease after the thermal oxidation.

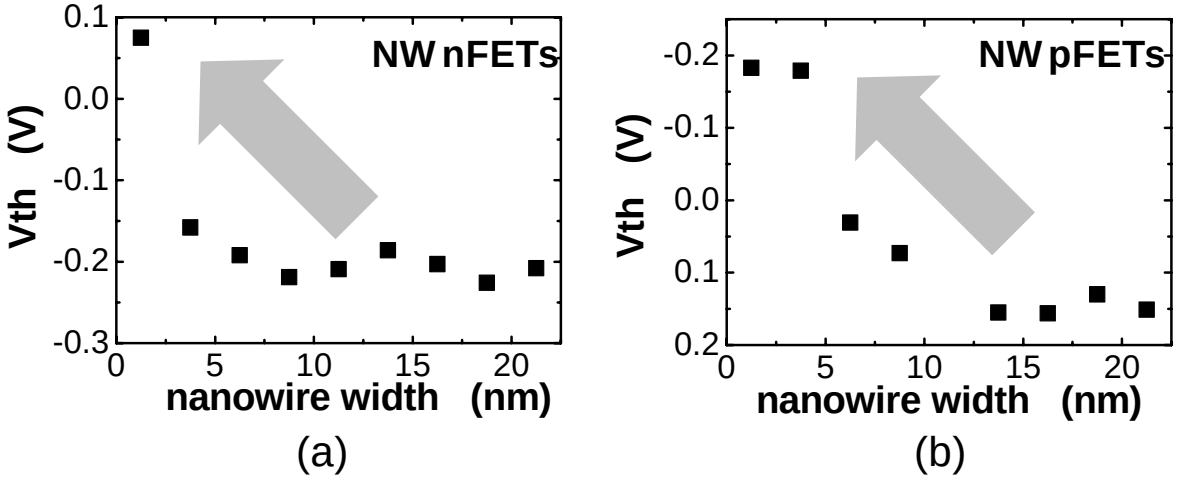


Figure 2.10 Relationship of threshold voltage (V_{th}, defined as V_g at I_{d0}= 10^{-12} A) vs. nanowire width in fabricated (a) NW nFETs and (b) NW pFETs. The nanowire width is varied from 1nm to 20 nm. In both NW nFETs and NW pFETs, V_{th} increasing by quantum confinement effect is clearly observed.

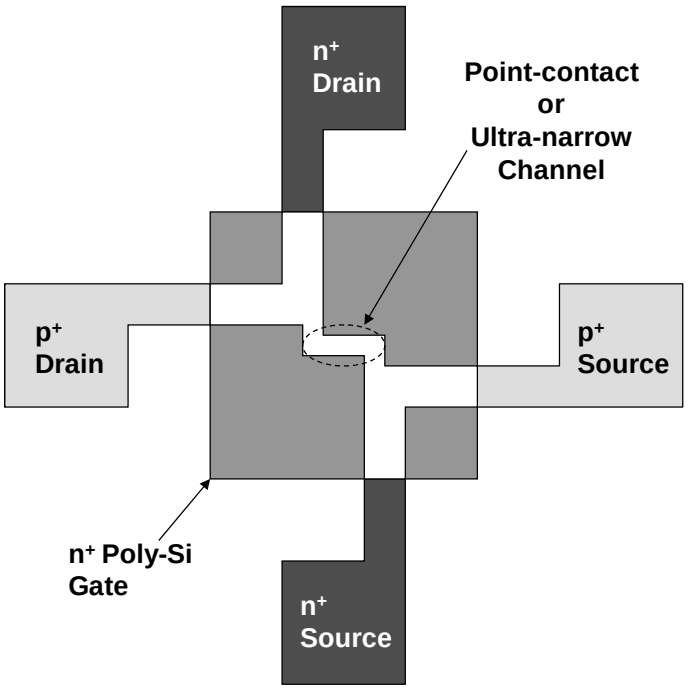


Figure 2.11 Schematic view of the n- and p-type common channel MOSFETs. The point-contact or ultra-narrow channel is p^- and it is connected to both n^+ and p^+ source/drain regions. The gate is doped to n^+. This device structure is suitable for comparing the charge polarities of transport characteristics in ultra-small structure which is very sensitive to its configuration.

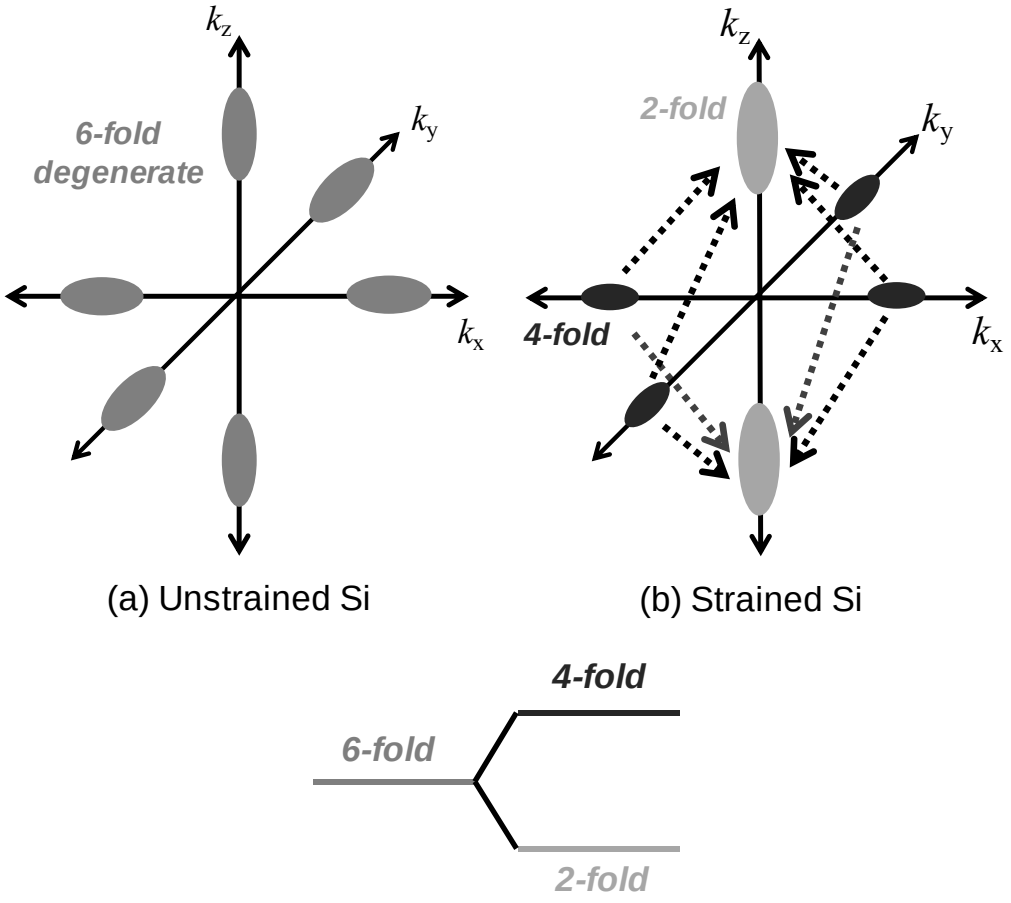


Figure 2.12 Conduction band structure in silicon. (a) Six equivalent valleys near the X-point in k space are degenerated. (b) When [110] direction tensile strain is applied, six valleys are lifted and split into lower 2-fold and upper 4-fold valleys. As a result, electrons concentrate in 2-fold valleys lowering average conductivity mass and suppressing the intervalley scattering. Therefore strained silicon enhances the MOSFET mobility.

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Chapter 3 Uniaxial Strain Effects on NW FETs and SETs/SHTs

3.1 Introduction

Strained Silicon has been extensively investigated for mobility enhancement of MOSFETs [1-5]. Uniaxial strain is already widely used in mass production. However, most of the studies on strain have paid attention only to three-dimensional (3D) [1-4] or two-dimensional (2D) [5] channel MOSFETs, not to ultra-nano scaled one-dimensional (1D) or zero-dimensional (0D) devices, such as NW FETs and SETs/SHTs.

gate-all-around (GAA) nanowire MOSFET (NW FET) and SET/SHT are promising devices for ultra scaled nano regime device due to superior SCE immunity [6-8] and high functionality [9-11], respectively. In NW FET, the MOSFET carrier transport becomes ballistic and the carrier transport can best be described by carrier injection at the source [12]. The saturation drain current in nanoscale channel limit becomes

$$I_d = WC_{ox}\sqrt{\frac{2k_B T_L}{\pi m^*}\left(V_g - V_t\right)}, \quad (3.1)$$

where T_L is the lattice temperature and m^* is effective mass [13]. From Equation 3.1, it can be seen that strain-induced recutions in the effective mass will still enhance the drive current in ballistic MOSFETs. Recently in SET/SHT, physical characteristics related to fundamentals of SHTs operation are partly reported by room temperature measurement [14-17]. However, there are still a lot of questions about the physics in SET/SHT and it should be cleared so that SET/SHT pratically integrate into the existing complementary metal-oxide-semiconductor (CMOS) very-large-scale integration (VLSI) circuits. Checking the response to applied strain is one method to reveal the physics in SET/SHT because the strain significantly modulate band structure which is directly connected to forming of SET/SHT as mentioned in chapter 2. Therefore, demonstration of strain technology and confirmation of the effects on the NW FET and SET/SHT are strongly desired.

In this chapter, the uniaxial strain effects on NW FETs and SETs/SHTs are described [18-19]. Two types of strain, transverse (= $\sigma_{tran.}$) and longitudinal (= $\sigma_{long.}$) to channel direction is applied to by using mechanical bending machine. Also, to account for strain effects in NW pFETs and SHTs, hole band structure under the strain is calculated.

3.2 Current Modulation by Strain

Many studies treating the strain technology employ mobility (μ) as a strain effect indicator because μ is intrinsic property not depend on devices feature ideally. In MOSFET scaled to nano regime, however, the mobility extraction is difficult since CV measurement commonly used for mobility measurement needs adequate channel area over several μm. Therefore in this thesis, strain effect in NW FETs and SETs/SHTs is indicated by current modulation factor $\Delta I_d/I_d$ because mobility is proportional to drive-current. Figure 3.1 shows an example of I_d-V_g characteristic with (W/) and without (W/O) strain in NW nFET, I_d is increased ~ 0.7 %.

[110] directed NW FET on (100) surface is used and NW FETs have various nanowire width from 1 nm to 20 nm. Mechanical strain is applied in two different direction, transverse (= $\sigma_{tran.}$) and longitudinal (= $\sigma_{long.}$) to nanowire channel as shown in Figure 3.2. All of the measurements were carried out at room temperature with Kelvin probes. Drain voltage (V_D) is fixed to + and – 10 mV for n- and p-type devices, respectively.

3.3 NW FETs under Strain

3.3.1 NW nFET under $\sigma_{tran.}$ (90 MPa)

Figure 3.3 shows tensile $\sigma_{tran.}$ effects on the current of NW nFETs. The x axis is over-drive voltage V_{over} (=V_g-V_{th}) and the y axis is current modulation factor $\Delta I_d/I_d$. At low V_{over}, negative $\Delta I_d/I_d$ is observed which is caused by the increase in V_{th} due to the strain. However, as V_{over} gets larger and inversion charge density becomes higher, current reduction fades and finally $\Delta I_d/I_d$ turns to positive value. This is because the mobility increases by strain and the mobility enhancement overcomes the effect of V_{th} increase. At V_{over} higher than ~0.4 V, current improvement resulting from mobility enhancement converges to ~0.7 %, even at the narrowest NW FET. Mobility enhancement by tensile $\sigma_{tran.}$ is qualitatively consistent to the bulk Piezoresistance coefficient as shown in Table 3.1 and it is inferred that compressive $\sigma_{tran.}$ will result in current degradation because tensile and compressive strain typically show opposite effects. The Piezoresistance coefficient (π) teaches resistivity changing in bulk Silicon: π>0 refers to the resistivity increasing and decreasing under tensile and compressive strain, respectively. Although carrier transport in bulk Silicon is different from in MOSFET (inversion layer), Piezoresistance coefficient generally shows same tendency with strained bulk MOSFET [5,20]. On the other hand, the increase in V_{th} is different tendency from the bulk MOSFET case, which we do not know the reason yet. These results suggest that strain technology is still effective even at ultra-nano scaled devices as a mobility booster and tensile $\sigma_{tran.}$ is favorable because it leads to I_{on} improvement by enhancing the mobility and I_{off} reduction by reducing V_{th}.

3.3.2 NW nFET under $\sigma_{long.}$ (110 MPa)

Figure 3.4 shows tensile $\sigma_{long.}$ effects on the current of NW nFETs. In contrast to tensile $\sigma_{tran.}$, $\Delta I_d/I_d$ begins with positive value at low V_{over}, attributed to V_{th} decrease under tensile $\sigma_{long.}$. This is same tendency with bulk nMOSFET case [21]. Then, up to high V_{over}, current increase is maintained and $\Delta I_d/I_d$ converges to ~0.5% thanks to mobility enhancement by tensile $\sigma_{long.}$. This mobility improvement is also consistent with bulk case as shown in Table 3.1. NW nFET having wide range of nanowire width from 1 nm to 20 nm is used, but noticeable width dependency of strain effect is not observed for both tensile $\sigma_{tran.}$ and $\sigma_{long.}$

3.3.3 NW pFET under $\sigma_{tran.}$ (50 MPa)

Next, we take a look at NW pFET cases. Figure 3.5(a) and (b) show current modulation under tensile and compressive $\sigma_{tran.}$, respectively. On contrary to NW nFETs, we don't discuss about V_{th} modulation because V_{th} shift is so small (below ± 1 mV) that could not be measured precisely. Large current increase (2 ~ 4 %), attributed to strain-induced mobility enhancement, is observed under tensile $\sigma_{tran.}$, and compressive $\sigma_{tran.}$ simply has effect opposite to the tensile one as above stated. So, the tensile strain is beneficial direction of $\sigma_{tran.}$ for mobility booster and this is same tendency with bulk Piezoresistance coefficient (Table 3.1). In addition, $\Delta I_d/I_d$ percents at low V_{over} are kept to almost constant value even at high V_{over}, especially for narrow width NW pFETs, which indicates that in NW pFETs effective mass modulation has much stlonger impact on strain effect than energy level splitting [1, 5, 22]. Furthermore, it is observed for the first time that strain effect in NW pFETs is dependent on nanowire width that has not been observed in NW nFETs. The strain effect represented by $\Delta I_d/I_d$ is weakened linearly as nanowire width decreases as shown in Figure 3.6. G_m is increased by tensile $\sigma_{tran.}$ and G_m modulation at $G_{m\text{-}max}$ is also showing width dependence that strain effect is decreased as nanowire width becomes narrower as shown in Figure 3.7(a) and (b).

To clarify the reason of the strain effect dependency on nanowire width, first we check the physical origin of strain effect in p-type MOSFET. In bulk case, effective mass (m^*) is considerably changed by hole band warping and subband energy splitting by strain modulates scattering probablity and repopulates carrier density of each subbands even though energy splitting effect is small. However, in NW pFET case, they have already large energy splitting by strong quantum confinement effect as shown in Figure 3.8 and most of holes occupy the lowest subband, so energy splitting effect becomes negligible and m^* modulation of only the lowest subband is most influential in strain effect. Therefore we calculate m^* change under stress in nanowire structure by using six-band k·p Hamiltonian [23-24]. Small strain, 100 MPa is applied, SOI thickness is fixed to 4 nm and

nanowire width is assumed from 3 nm to 12 nm to reproduce the similar condition as measurement. In the calculation, m^* of ground valence band is decreased by tensile $\sigma_{tran.}$ as shown in Figure 3.9 which leads to mobility enhancement, and by $\sigma_{long.}$ m^* is increased and mobility will be degraded. Moreover, m^* modulation becomes smaller as nanowire width decreases for both $\sigma_{tran.}$ and $\sigma_{long.}$ resulting in weaker strain effect at narrower NW pFETs. These tendencies agree with experimental data.

3.3.4 NW pFET under $\sigma_{long.}$ (50 MPa)

Tensile $\sigma_{long.}$ effects on NW pFETs are shown in Figure 3.10. The current is decreased by the tensile $\sigma_{long.}$ due to m^* increasing as mentioned in the band calculation. We can infer compressive strain is proper direction in longitudinal strain and this is just same tendency with the bulk case (Table 3.1). Nanowire width dependence is also observed in $\sigma_{long.}$, which current modulation becomes smaller as nanowire width decreases as shown in Figure 3.10(b). This is explained by small m^* modulation at narrow nanowire as well and agree with calculation results. Figure 3.11 is G_m characteristics and width dependency, respectively. As shown in Figure 3.9(b), small m^* modulation by strain at narrow NW pFET is the reason why the strain effect is weakened as NW width narrower. G_m is increased by tensile $\sigma_{long.}$ and $G_{m\text{-}max}$ modulation is also showing same width dependence as shown in Figure 3.11(a) and (b).

3.3.5 Overview of Strain Effects on NW FETs

Table 3.2 is summary of strain effects on NW FETs. V_{th} shift is only observed for NW nFETs and V_{th} increasing by tensile $\sigma_{tran.}$ is different with bulk nMOSFET. Proper strain type for enhancing mobility is totally same with bulk case. In NW nFET, both tensile $\sigma_{tran.}$ and $\sigma_{long.}$ enhance drain current at high V_{over}, however in terms of I_{on}/I_{off} ratio, $\sigma_{tran.}$ offers more favorable effects, because of current decreasing at low V_{over}. In addition, the current increase in NW nFETs by strain is only less than 1%, while NW pFETs performance is greatly improved about 2 ~ 4 %. This difference may be derived from small m^* modulation in NW nFET like bulk nMOSFET [1]. Finally, for the first time strain effect dependency on nanowire width is observed only in NW pFETs case, attributed to small m^* modulation in narrow NW pFETs.

3.4 SETs/SHTs under Strain

3.4.1 SET under $\sigma_{tran.}$ (90 MPa) and $\sigma_{long.}$ (110 MPa)

In this section 3.4, strain effects on SETs/SHTs are described. Figure 3.12 shows characteristics of (a) a good SET and (b) a poor SET under tensile $\sigma_{tran.}$. The solid lines are I_d-V_g curves without and with strain, and open

dotted line means current modulation factor $\Delta I_d/I_d$ by the strain. We classify a SET having higher tunneling barriers as a good SET, and hence, current oscillation continues to high gate voltage in a good SET, but oscillation is vanished at some gate voltage in a poor SET. Three noticeable effects are observed: (i) $\Delta I_d/I_d$ begins with minus at low V_g, (ii) at the V_g region where current oscillations (Coulomb oscillation) appears, $\Delta I_d/I_d$ takes various values and its behavior is very complicated, and (iii) in the case of a poor SET, when V_g is higher than the last Coulomb blockade oscillation, $\Delta I_d/I_d$ converges to constant positive value just as the NW nFETs case.

(i) is caused by V_{th} increase under tensile $\sigma_{tran.}$, which is similar to NW nFETs under the $\sigma_{tran.}$.

(ii) is original to SETs. To account for this complicate current modulation in the Coulomb blockade oscillation (CBO) region by the strain, we check the oscillation region of the good SET in detail. Figure 3.13 shows detailed I_d-V_g curves of the SET in Figure 3.12(a). Solid line is without strain and dotted line is with strain. We observe that both peak and valley voltage of the SET oscillations shift to smaller V_g side under strain. Note that direction of the peak shift doesn't correspond to that of V_{th} increase observed at low V_g as stated at (i). The reason of this shift is considered that the potential structures of barriers and dots are modulated by the strain.

Another reason of the complicated behavior would be the transport in a SET with multiple dots. It has been found that a SET which operates and shows a single-dot-like behavior at room temperature has strong temperature dependence and that this behavior is caused by stochastic Coulomb blockade in a multiple-dot system [25]. It is considered that a SET shown in Figure 3.12 and Figure 3.13 also has a multiple dots although the room temperature characteristics are single-dot like because the smallest dot in multiple dots dominates the room temperature behavior. In a SET with multiple dots, tunnel condition where the energy levels of the dots align may be rearranged and configuration of the oscillation is altered by strain as shown in Figure 3.14. In some energy levels of the dots, tunneling probabilities degrade as energy difference of corresponding two levels increases by strain; in others, the probabilities increase as levels in two dots get closer. So, tunneling condition in multiple dots is complexly-modulated by strain as the number of dots increases. These two factors, i.e, modulation of potential structure and rearrangement of tunneling condition, are considered as possible reasons for complicated strain effect at oscillation region in SETs.

(iii) can be explained by carrier transport mechanism in a SET. At low V_g, electrons are transferred from source to drain through the dot by tunneling. However, at high V_g, a large number of carriers jump over the tunneling barriers because V_g lowers the barriers potential height electrically and transport mechanism turns to drift approaching to ordinary NW nFETs characteristics. Therefore, after oscillation vanishes, drift current governs entire transport and mobility enhancement by the strain results in constant positive $\Delta I_d/I_d$ like the NW

FETs case.

Figure 3.15 shows characteristics of two SETs under tensile $\sigma_{long.}$. At low V_g, $\Delta I_d/I_d$ starts from positive value due to V_{th} decrease just same with NW nFETs under tensile $\sigma_{long.}$. Similar to SETs with $\sigma_{tran.}$, complicated strain effect at oscillation region as well as constant positive $\Delta I_d/I_d$ after last oscillation is observed.

3.4.2 SHT under $\sigma_{tran.}$ (50 MPa) and $\sigma_{long.}$ (50 MPa)

Figure 3.16 (a) shows characteristics of a SHT under tensile $\sigma_{tran.}$ at room temperature and Figure 3.16 (b) shows CBO region of (a) in detail. V_{th} shift by the strain is negligibly small as the NW pFETs. Two strain effects are observed: (i) at the Coulomb blockade oscillation region, not only the current increase, but I_d-V_g curve shifts to higher V_g side are observed, and (ii) after CBO is vanished, $\Delta I_d/I_d$ converges to constant positive value which is observed in SETs.

(i) is accounted for by considering the tunneling probability from source to drain through tunneling barrier and the energy level spacing in potential dot consisting SHT. The tunneling probability (Γ_{tunnel}) and the energy level spacing (ΔE) are expressed as follows:

$$\Gamma_{tunnel} \quad \alpha \quad exp(-m^{*1/2}), \qquad (3.2)$$

$$\Delta E \quad \alpha \quad 1/m^*, \quad (3.3)$$

In our k·p calculation, m^* is reduced by tensile $\sigma_{tran.}$ as shown in Figure 3.9 (a) leading to the increase in Γ_{tunnel}, which results in current enhancement in a SHT. Furthermore, the m^* reduction causes ΔE widening in the dot as well. Consequently, the first oscillation peak moves to higher V_g side under $\sigma_{tran.}$ Although only one SHT is measured and more investigation is needed, these experimental data indicate that strain effects in SHT is simply understood by m^* modulation and this is very different from SETs case, where very complicated strain behaviors are observed.

(ii) can be explained by the carrier transfer mechanism of SHT as mentioned in section 3.4.1.

Figure 3.17 shows characteristics of a SHT under tensile $\sigma_{long.}$. In opposite to $\sigma_{tran.}$ case, SHTs current is decreased and I_d-V_g curve shifts to lower V_g side. Considering m^* increase by $\sigma_{long.}$ as shown in Figure 3.9 (b), Γ_{tunnel} and ΔE are reduced under stress, and current is decreased and current oscillation moves to lower V_g side. Also, $\Delta I_d/I_d$ converges to minus value after CBO is disappeared, attributed to mobility degradation as the NW pFETs under $\sigma_{long.}$.

3.5 Summary

In this chapter, strain effects on NW FETs and room-temperature operating SETs/SHTs have been introduced.

Figure 3.18 organizes main points of strain effects on NW FETs and SETs/SHTs. In NW FETs, we observe simple strain effects, namely V_{th} shift and mobility modulation at low V_{over} and high V_{over}, respectively. NW pFETs provide greater $\Delta I_d/I_d$ than NW nFETs, and nanowire width dependency of the effects is observed for the first time only in NW pFETs. In SETs/SHTs case, in addition to V_{th} shift and mobility enhancement, CBO characteristics are changed by the strain. While current modulation is very complicated in SETs, strain effects on SHTs are easily analyzed by means of m^* modulation. More current improvement and characteristics modification can be expected, if relatively larger strain (~ GPa) is applied.

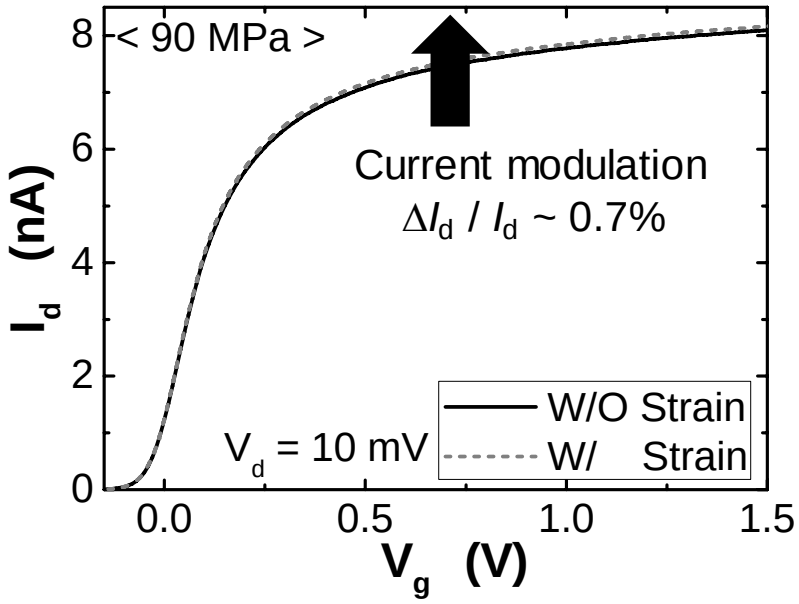

Figure 3.1 An example of current modulation by strain in NW nFET. ΔI_d means current difference between w/ and w/o strain. We use current modulation factor $\Delta I_d/I_d$ as a strain effect indicator in this thesis.

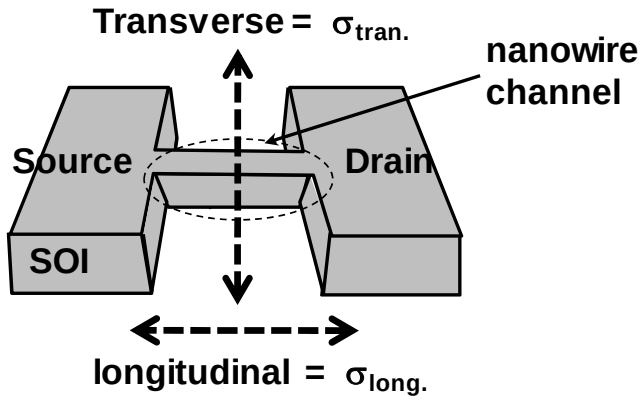

Figure 3.2 Schematic of SOI pattern in for NW FET. Mechanical strain is applied in two different direction, transverse (= $\sigma_{tran.}$) and longitudinal (= $\sigma_{long.}$) to nanowire channel.

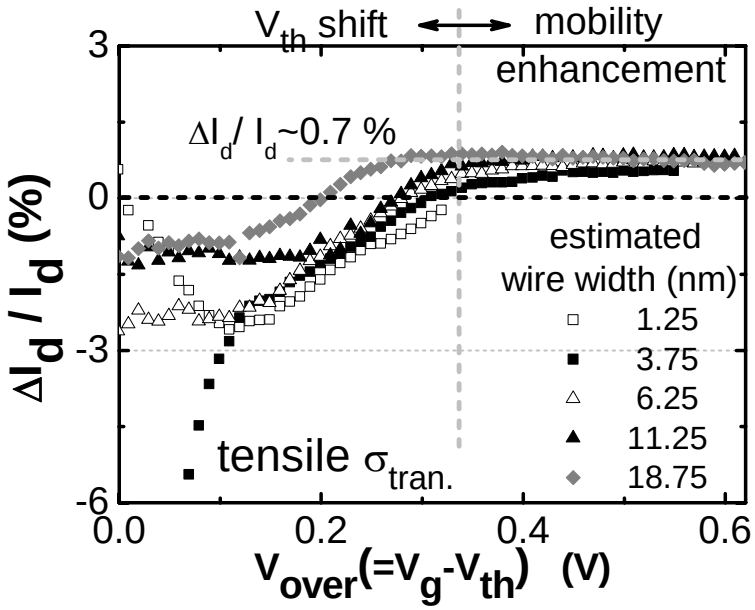

Figure 3.3 Tensile $\sigma_{tran.}$ effects on the current of NW nFETs. The x axis is over-drive voltage V_{over} ($=V_g-V_{th}$) and the y axis is current modulation factor $\Delta I_d/I_d$. At low V_{over}, negative $\Delta I_d/I_d$ due to the increase in V_{th} is observed. However, as V_{over} gets larger the mobility increases by strain overcomes the effect of V_{th} increase and finally current is enhanced. Mobility enhancement by the tensile $\sigma_{tran.}$ is qualitatively consistent to the bulk Piezoresistance coefficient as shown in Table 3.1, while the increase in V_{th} is different tendency from the bulk MOSFET case, which we do not know the reason yet. These results suggest that tensile $\sigma_{tran.}$ is favorable because it leads to I_{on} improvement by enhancing the mobility and I_{off} reduction by reducing V_{th}.

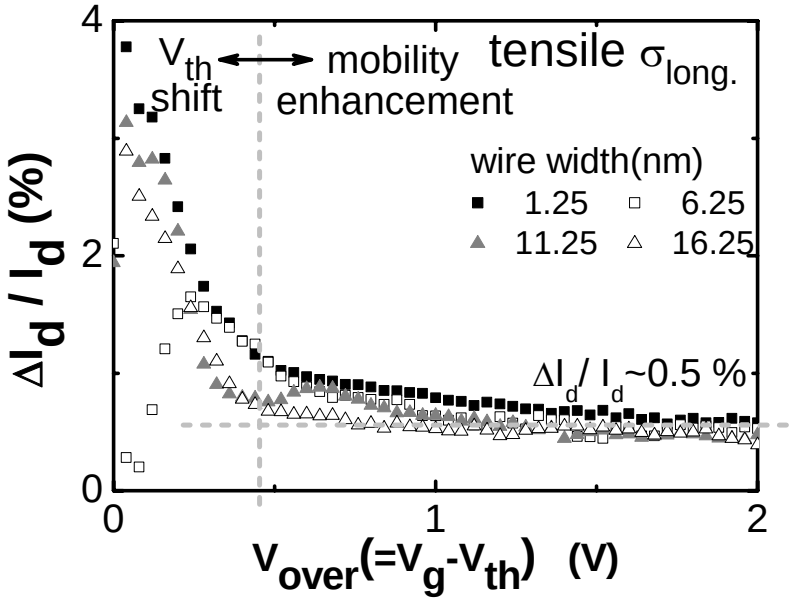

Figure 3.4 $\Delta I_d/I_d$ - V_{over} characteristics of NW nFETs under tensile $\sigma_{logn.}$. Negative V_{th} shift at low V_{over} and current increase at high V_{over} are measured.

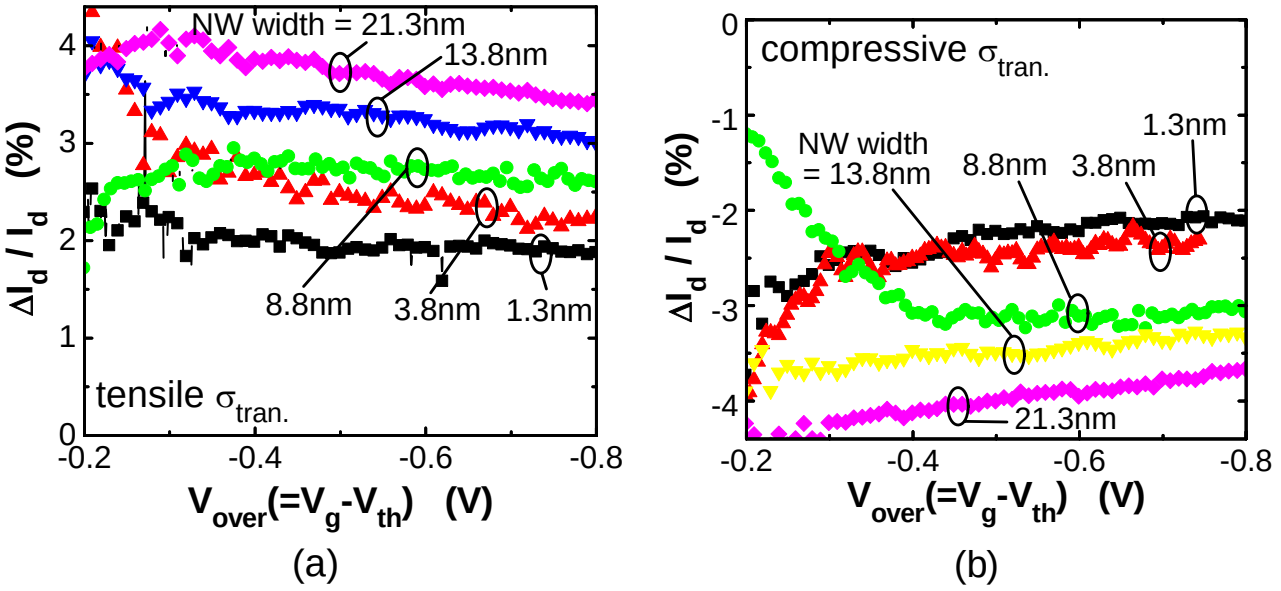

Figure 3.5 Current modulation under (a) tensile and (b) compressive $\sigma_{tran.}$. On contrary to NW nFETs, V_{th} shift is so small (below ± 1 mV) that could not be measured precisely. Large current increase (2 ~ 4 %) is observed under tensile $\sigma_{tran.}$, and compressive $\sigma_{tran.}$ has effect simply opposite to the tensile. In addition, $\Delta I_d/I_d$ percents at low V_{over} are kept to almost constant value even at high V_{over}, which indicates that in NW pFETs effective mass modulation has much stlonger impact on strain effect [1, 5, 22]. Furthermore, it is observed for the first time that strain effect in NW pFETs is dependent on nanowire width that has not been observed in NW nFETs. The strain effect represented by $\Delta I_d/I_d$ is weakened linearly as nanowire width decreases.

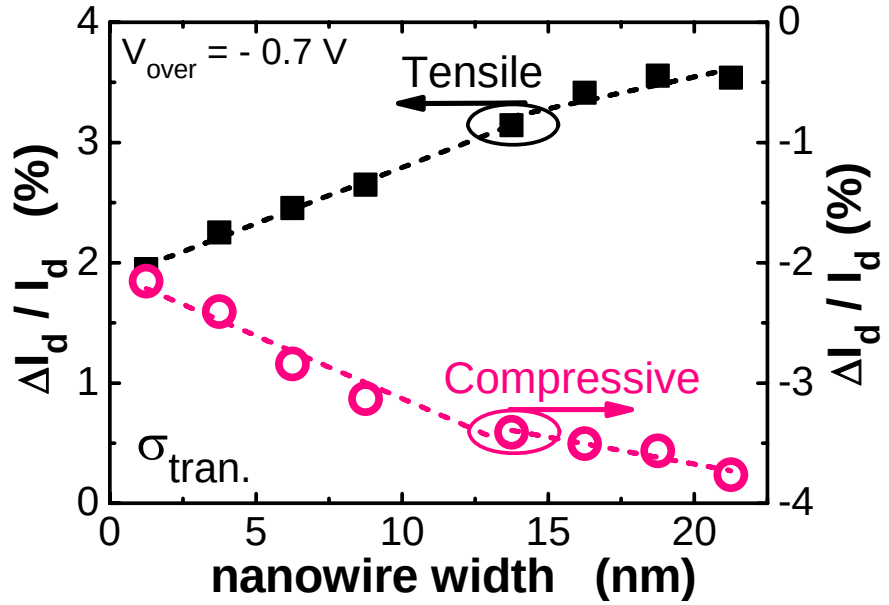

Figure 3.6 Nanowire width dependence of strain effect in NW pFETs. As nanowires become narrower, the effect is diminished linearly. V_{over} is fixed to – 0.7 V.

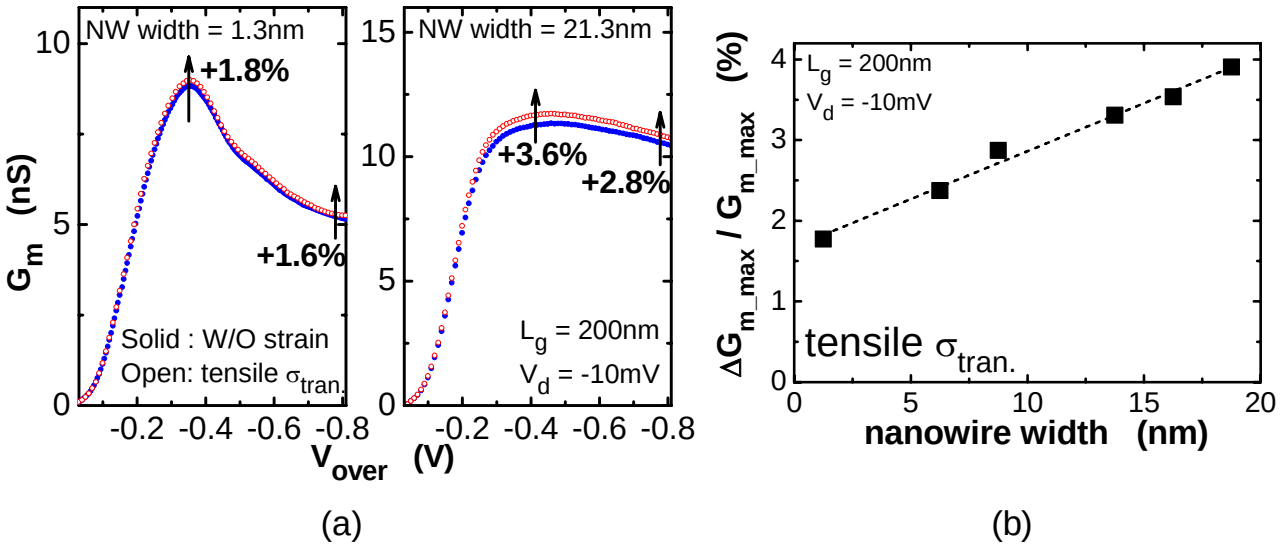

Figure 3.7 (a) G_m Characteristics of 1.3 nm-wide and 21.3-wide NW pFETS. G_m is increased by tensile $\sigma_{tran.}$ and (b) G_m modulation at $G_{m\text{-}max}$ is also showing width dependence that strain effect is decreased as nanowire width becomes narrower.

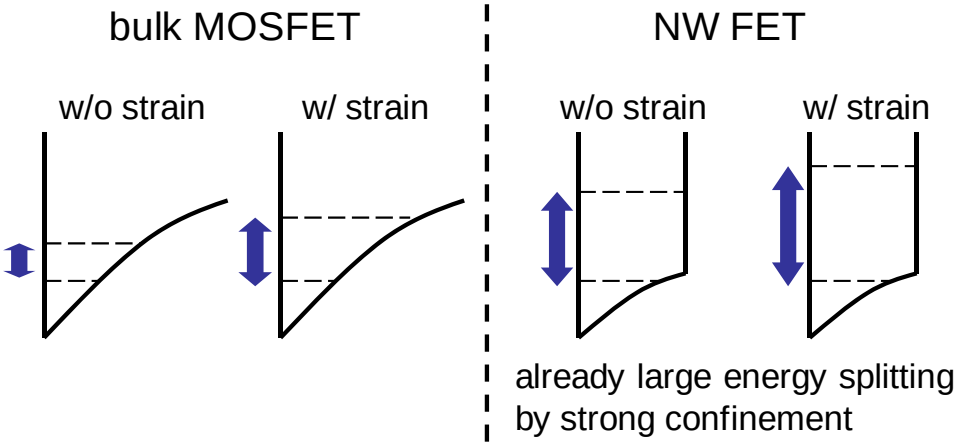

Figure 3.8 Physical origin of strain effect in p-type MOSFETs. In bulk case, effective mass (m^*) is considerably changed by hole band warping and subband energy splitting by strain modulates scattering probability and repopulates carrier density of each subbands even though energy splitting effect is small. However, in NW pFET case, they have already large energy splitting by strong quantum confinement effect and most of holes occupy the lowest subband, so energy splitting effect becomes negligible and m^* modulation of only the lowest subband is most influential in strain effect. Therefore we calculate m^* change under stress in nanowire structure.

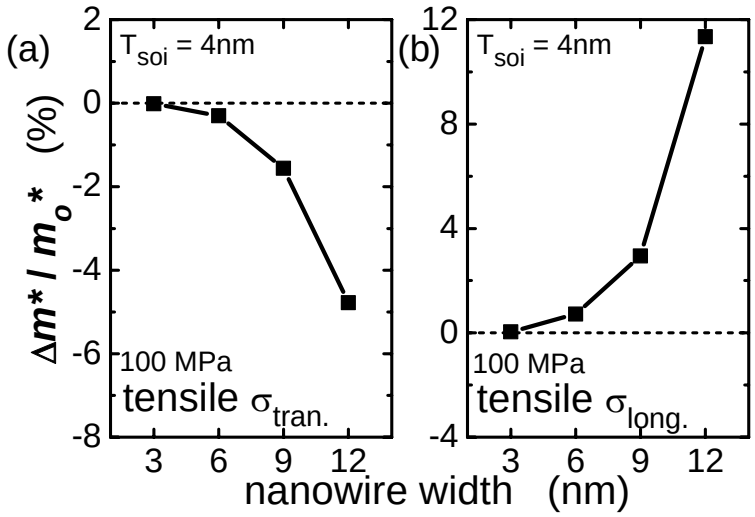

Figure 3.9 We use six-band k·p Hamiltonian [23-24], where small strain 100 MPa is applied, SOI thickness is fixed to 4 nm and nanowire width is assumed from 3 nm to 12 nm to reproduce the similar condition as measurement. In the calculation, m^* of ground valence band is decreased by tensile $\sigma_{tran.}$ which leads to mobility enhancement, and by $\sigma_{long.}$ m^* is increased and mobility will be degraded. Moreover, m^* modulation becomes smaller as nanowire width decreases for both $\sigma_{tran.}$ and $\sigma_{long.}$ resulting in weaker strain effect at narrower NW pFETs. These tendencies agree with the experimental data.

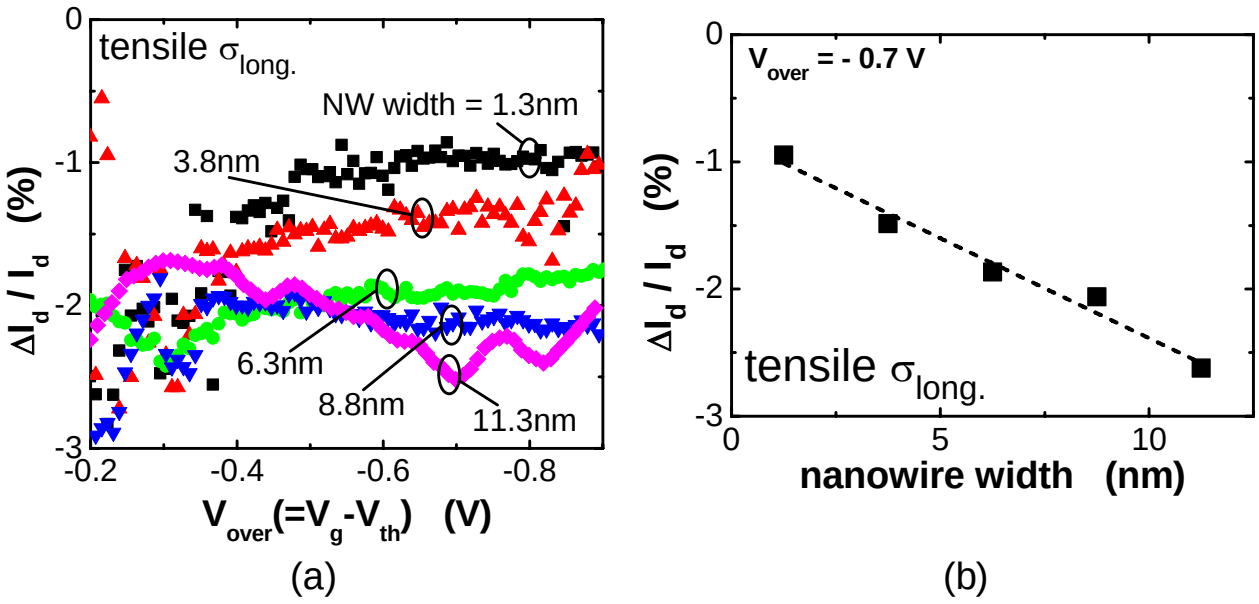

Figure 3.10 Tensile $\sigma_{long.}$ effects on NW pFETs. The current is decreased by the tensile $\sigma_{long.}$ due to m^* increasing as mentioned in the band calculation and we can infer compressive strain is proper direction in longitudinal strain. Nanowire width dependency is also observed in $\sigma_{long.}$, which current modulation becomes smaller as nanowire width decreases, attributed to small m^* modulation at narrow nanowire.

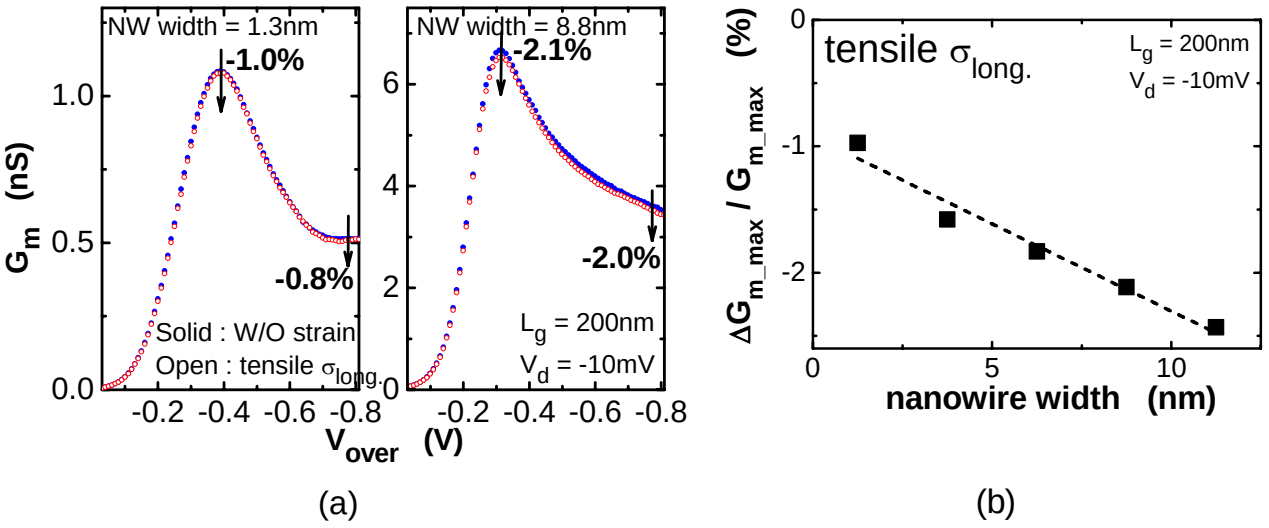

Figure 3.11 (a) G_m Characteristics of 1.3 nm-wide and 21.3-wide NW pFETS. G_m is decreased by tensile $\sigma_{long.}$ and G_m modulation at $G_{m\text{-}max}$ is also showing width dependence that strain effect is decreased as nanowire width becomes narrower.

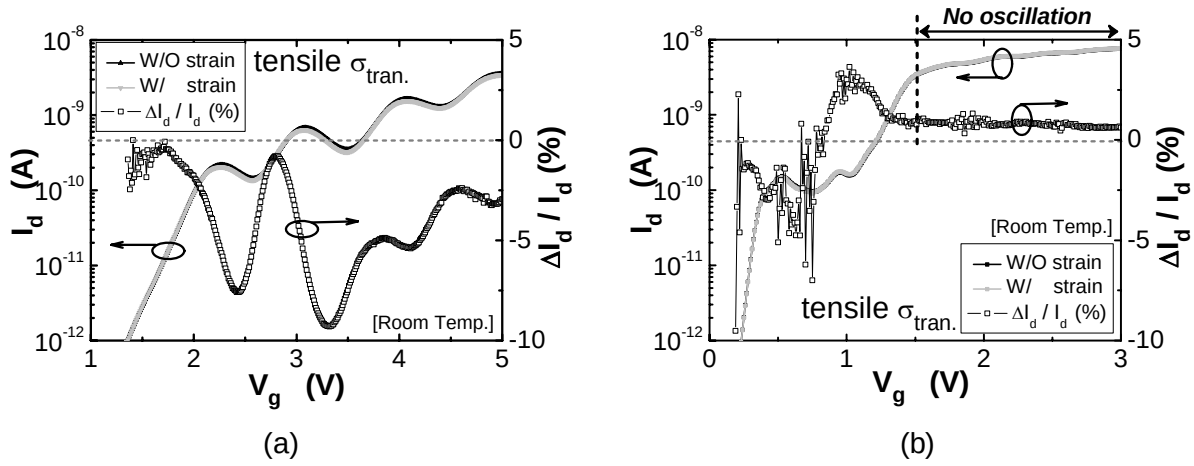

Figure 3.12 Characteristics of (a) a good SET and (b) a poor SET under tensile $\sigma_{tran.}$. The solid lines are I_d-V_g curves w/o and w/ strain, and open dotted line means current modulation factor $\Delta I_d/I_d$. We classify a SET having higher tunneling barriers as a good SET, and hence, current oscillation continues to high gate voltage in a good SET, but oscillation is vanished at some gate voltage in a poor SET. Three noticeable effects are observed: (i) $\Delta I_d/I_d$ begins with minus at low V_g, (ii) at the V_g region where current oscillations (Coulomb oscillation) appears, $\Delta I_d/I_d$ takes various values and its behavior is very complicated, and (iii) in the case of a poor SET, when V_g is higher than the last Coulomb blockade oscillation, $\Delta I_d/I_d$ converges to constant positive value just as the NW nFETs case.

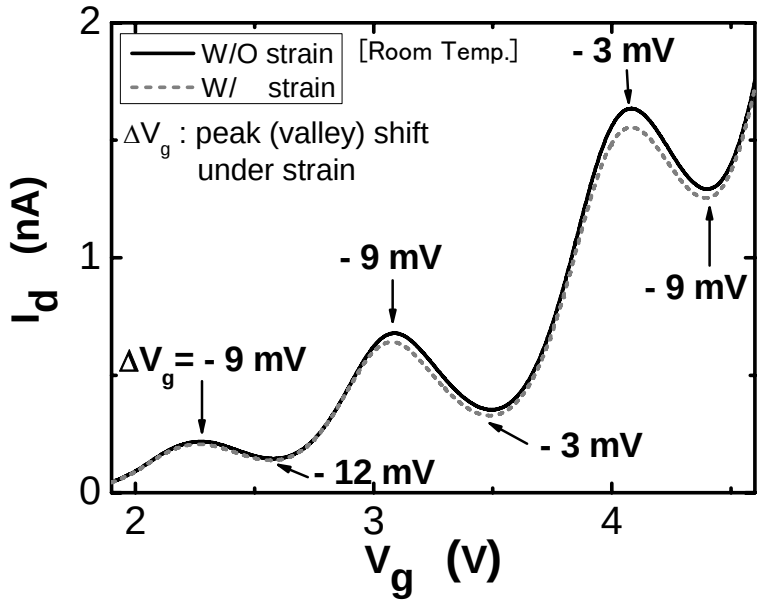

Figure 3.13 To account for this complicate current modulation in the Coulomb blockade oscillation (CBO) region, we check the oscillation region of the good SET in Figure 3.12(a) in detail. Solid line is without strain and dotted line is with strain. We observe that both peak and valley voltage of the SET oscillations shift to smaller V_g side under strain. Note that direction of the peak shift doesn't correspond to that of V_{th} increase observed at low V_g. The reason of this shift is considered that the potential structures of barriers and dots are modulated by the strain.

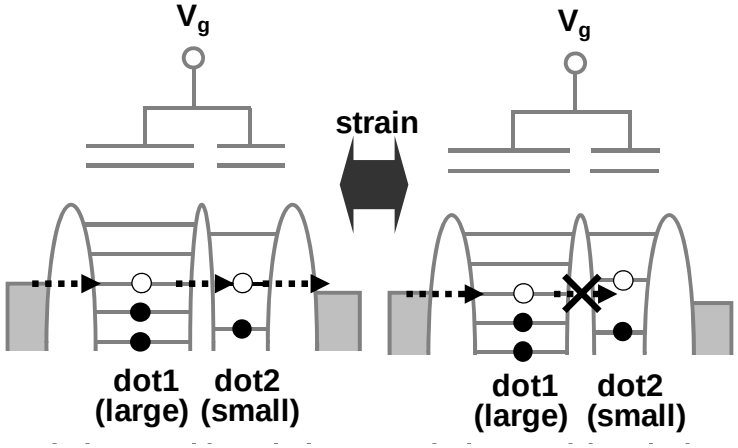

Figure 3.14 Another reason of the complicated behavior would be the transport in a SET with multiple dots. In a SET with multiple dots, tunnel condition where the energy levels of the dots align may be rearranged and configuration of the oscillation is altered by strain. In some energy levels of the dots, tunneling probabilities degrade as energy difference of corresponding two levels increases by strain; in others, the probabilities increase as levels in two dots get closer. So, tunneling condition in multiple dots is complexly-modulated by strain as the number of dots increases and strain effects become complicated.

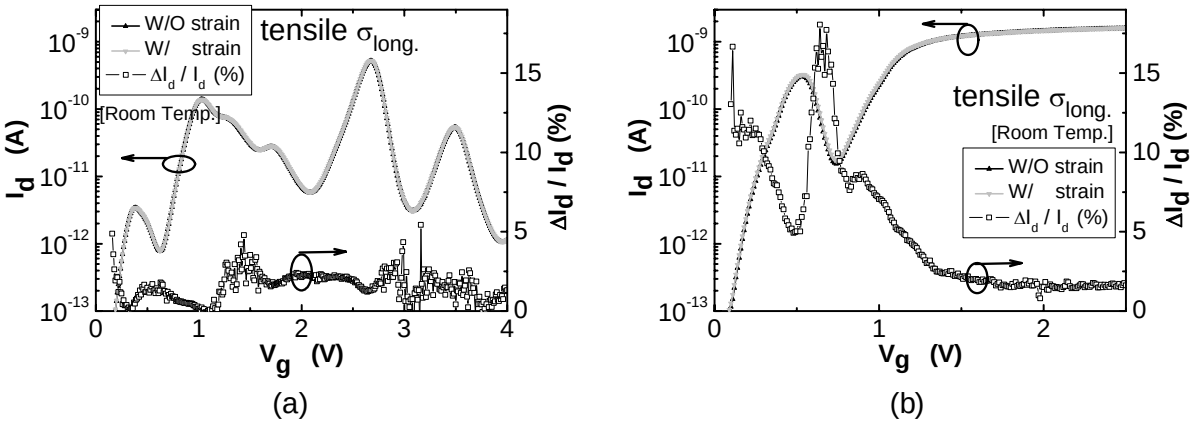

Figure 3.15 Characteristics of two SETs under tensile $\sigma_{long.}$. At low V_g, $\Delta I_d/I_d$ starts from positive value due to V_{th} decrease just same with NW nFETs under tensile $\sigma_{long.}$. Similar to SETs with $\sigma_{tran.}$, complicated strain effect at oscillation region as well as constant positive $\Delta I_d/I_d$ after last oscillation is observed.

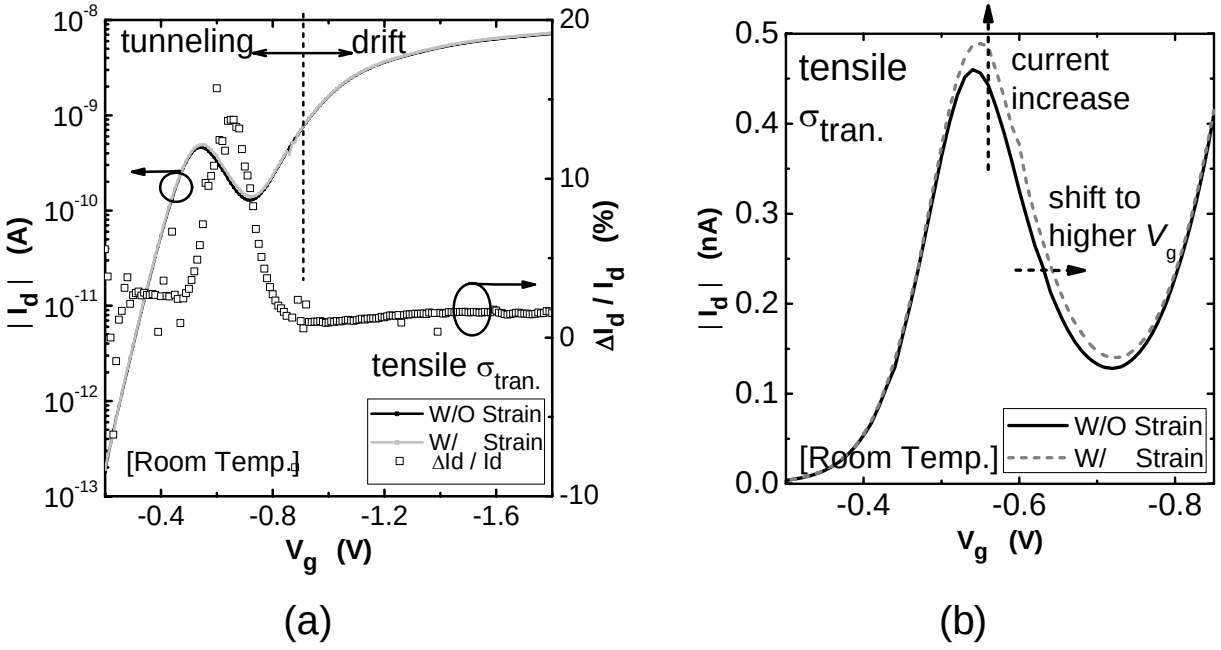

Figure 3.16 (a) Characteristics of a SHT under tensile $\sigma_{tran.}$ at room temperature and (b) CBO region of (a) in detail. V_{th} shift by the strain is negligibly small as the NW pFETs. At the Coulomb blockade oscillation region, not only the current increase, but I_d-V_g curve shifts to higher V_g side are observed because m^* reduction as mentioned in band calculation makes tunneling probability (Γ_{tunnel}) increase and energy level spacing (ΔE) widen. Also, after CBO is vanished, $\Delta I_d/I_d$ converges to constant positive value same as the SETs which is explained by increasing drift current.

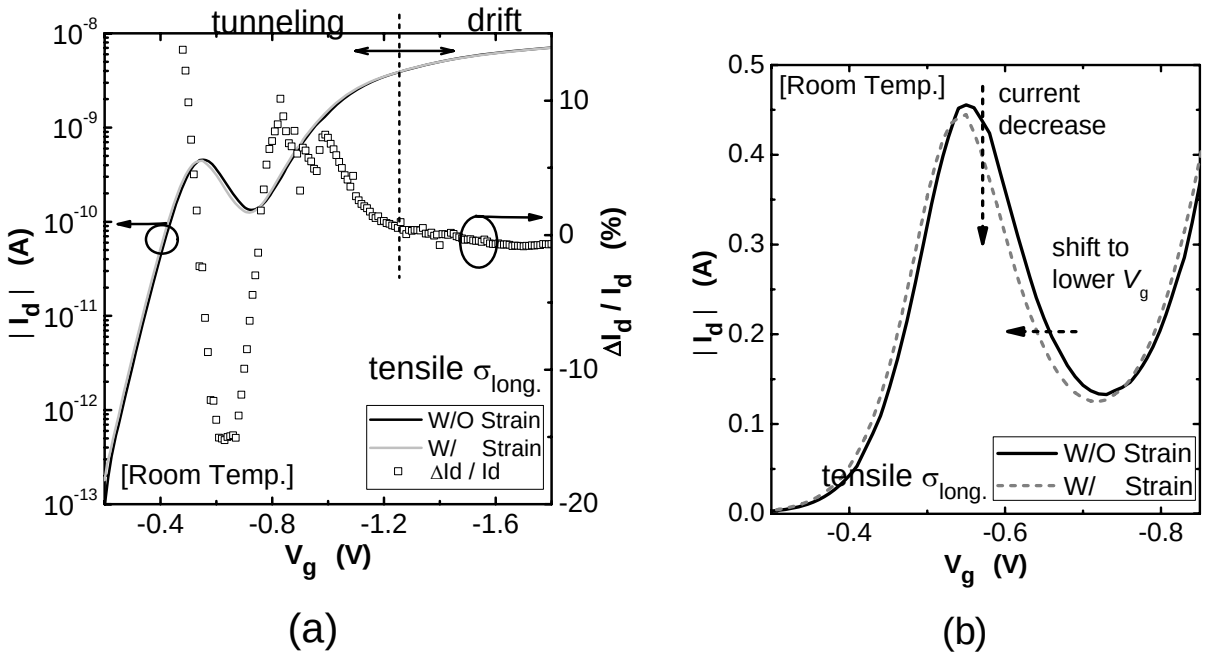

Figure 3.17 Characteristics of a SHT under tensile $\sigma_{long.}$. In opposite to $\sigma_{tran.}$ case, SHTs current is decreased and I_d-V_g curve shifts to lower V_g side. Considering m^* increase by $\sigma_{long.}$ as shown in Figure 3.9 (b), Γ_{tunnel} and ΔE are reduced under stress, and current is decreased and CBO moves to lower V_g side. $\Delta I_d/I_d$ converges to minus value after CBO is disappeared, attributed to mobility degradation as the NW pFETs under $\sigma_{long.}$.

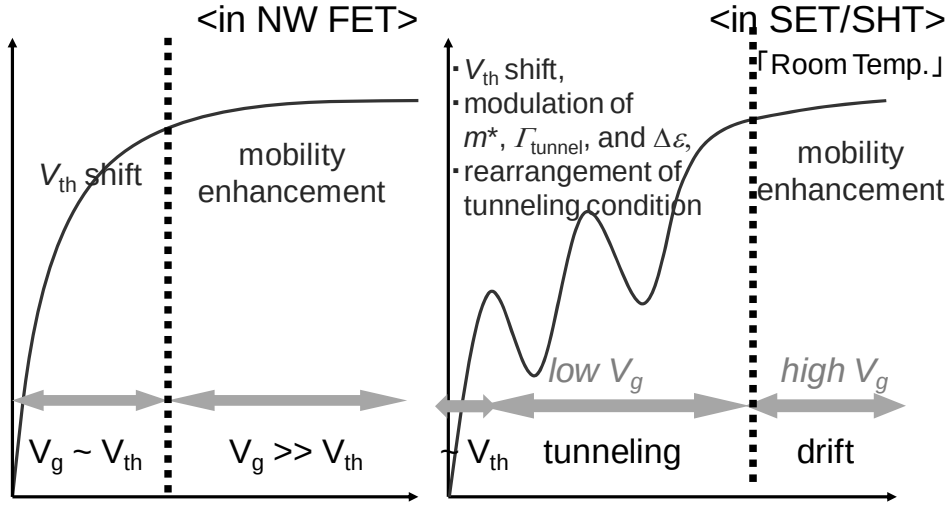

Figure 3.18 Summary of strain effects on NW FET and SET/SHT. In NW FETs, we observe simple effects, namely V_{th} shift and mobility modulation at low V_{over} and high V_{over}, respectively. NW pFETs provide greater $\Delta I_d/I_d$ than NW nFETs, and nanowire width dependency of the effects is observed for the first time only in NW pFETs. In SETs/SHTs, in addition to that effects, CBO characteristics are changed by the strain. While current modulation is very complicated in SETs, strain effects on SHTs are easily analyzed by means of m^* modulation.

	$\Pi_{tran.}$	$\Pi_{long.}$
n-type	− 17.6	− 31.6
p-type	− 66.3	+ 71.8

Table 3.1 Bulk Piezoresistance coefficients [20]. The Piezoresistance coefficient (π) teaches resistivity changing in bulk Silicon: π>0 refers to the resistivity increasing and decreasing under tensile and compressive strain, respectively. Although carrier transport in bulk Silicon is different from in MOSFET (inversion layer), Piezoresistance coefficient generally shows same tendency with strained bulk MOSFET [5,20].

	NW nFET		NW pFET	
	$\sigma_{tran.}$ (90 MPa)	$\sigma_{long.}$ (110 MPa)	$\sigma_{tran.}$ (50 MPa)	$\sigma_{long.}$ (50 MPa)
V_{th}	↑	↓	–	–
favorable type	tensile	tensile	tensile	compressive
current enhancement	small	small	large	large
width dependency	x		o	

Table 3.2 Summary of strain effects on NW FETs. V_{th} shift is only observed for NW nFETs and V_{th} increasing by tensile $\sigma_{tran.}$ is different with bulk nMOSFET. Proper strain type for enhancing mobility is totally same with bulk case. In NW nFET, both tensile $\sigma_{tran.}$ and $\sigma_{long.}$ enhance drain current at high V_{over}, however in terms of I_{on}/I_{off} ratio, $\sigma_{tran.}$ offers more favorable effects, because of current decreasing at low V_{over}. In addition, the current increase in NW nFETs is only less than 1%, while NW pFETs performance is greatly improved about 2 ~ 4 %. This difference may be derived from small m^* modulation in NW nFET like bulk nMOSFET [1]. Finally, for the first time strain effect dependency on nanowire width is observed only in NW pFETs case, attributed to small m^* modulation in narrow NW pFETs.

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Chapter 4 Conclusions

In this dissertation, NW FETs and SETs/SHTs both adopting nanowire structure are fabricated and uniaxial strain effects on the devices are analyzed. The effectiveness of the strain technology at ultra narrow devices are evaluated by measurements and analyzed by means of band calculation.

In the first half of the Chapter 2, characteristics and fabrication methods of NW FET and room-temperature operating SETs/SHTs have been illustrated. After brief introduction of NW FET, Coulomb blockade oscillation and other important current characteristics in SET/SHT were derived from the classical physics. Then, fabrication method of NW FETs and SETs/SHTs which are sharing wholly same process is overviewed. In the second half, strain technology in MOSFET has been elucidated. Influential factors that determine strain effect are considered and several types of strain sources are introduced. In n-type MOSFET, carrier repopulation by band splitting modulates average effective mass and intervalley scattering rate. On the contrast, conductivity mass change by hole band warping makes large mobility modulation in p-type MOSFET. Mechanical strain is applied to MOSFET in this thesis because it can easily switch strain directions and precisely compare the strain effect in different devices.

In the chapter 3, experimental results of strain measurements on NW FETs and room-temperature operating SETs/SHTs have been described. In NW FETs, we observe simple strain effects, namely V_{th} shift and mobility modulation at low V_{over} and high V_{over}, respectively. NW pFETs provide greater $\Delta I_d/I_d$ than NW nFETs, and nanowire width dependency of the effects is observed for the first time only in NW pFETs because larger m^* modulation than NW nFETs and the m^* modulation is decreased as nanowire width becomes narrowe. In SETs/SHTs case, in addition to V_{th} shift and mobility enhancement, CBO characteristics are changed by the strain. While current modulation is very complicated in SETs, strain effects on SHTs are easily analyzed by means of m^* modulation. More current improvement and characteristics modification can be expected, if relatively larger strain (~ GPa) is applied.

In conclusion, strain technology is still effective even at ultra narrow NW FETs as a mobility booster and is useful to modulate SET/SHT characteristics after fabrication. In order to maximize strain effect at future scaled devices, favorable nanowire direction which shows positive dependency on nanowire width is needed.

Appendix Process Flow of Ultra-Narrow Channel NW FETs and SETs/SHTs

Table 1. Flow and detailed conditions of the fabrication process of ultra-narrow channel MOSFETs for NW FETs and SETs/SHTs. The thickness of SOI and other layers were determined by ellipsometry.

Step		Condition	Thickness
Sample preparation	Dicing	8 inch UNIBOND SOI wafer (p-type, (100), 10 ~ 20 Ωcm) → 2 cm × 1.5 cm	SOI: 100 nm BOX: 200 nm
	Cleaning 1	Buffered HF (BHF) 15 sec SC1 NH_4OH:H_2O_2:H_2O = 1:1:6, 75 ~ 85 degC, 10 min BHF 15 sec SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min	
	Cleaning 2	Numbering BHF 15 sec SC1 NH_4OH:H_2O_2:H_2O = 1:1:6, 75 ~ 85 degC, 10 min	
SOI thinning	RCA cleaning	HF:H_2O = 1:100, 90 sec SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min HF:H_2O = 1:100, 90 sec SC1 NH_4OH:H_2O_2:H_2O = 1:1:6, 75 ~ 85 degC, 10 min HF:H_2O = 1:100, 60 sec SC2 HCl:H_2O_2:H_2O = 1:1:6, 75 ~ 85 degC, 10 min HF:H_2O = 1:100, 90 sec	
	SOI thinning	Pyro oxidation 1000 degC, O_2 3.0 l/min, H_2 3.0 l/min, 10 ~ 25 min	SiO_2: 100 ~ 300 nm / SOI: 20 ~ 30 nm
	Oxide removal	BHF 2 min	
Mask oxidation	Cleaning	HF:H_2O = 1:100, 90 sec SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min HF:H_2O = 1:100, 90 sec	
	Mask oxidation	Dry oxidation 900 degC, O_2 1.0 l/min, 3 ~ 5 min	SiO_2: 5 nm

EB lithography	Spin coating	HSQ (FOx-12) 4000 rpm, 40 sec	FOx-12: ~ 100 nm
	Pre-baking	120 degC, 2 min	
	Exposure	Beam current 120 pA, Acceleration voltage 50 keV Area dose 690 ~ 750 μC/cm^2 (for wire channel) Area dose 330 μC/cm^2 (for mesa)	
	Development	NMD-3 (TMAH 2.38 %) 60 sec	
Channel and mesa RIE	Helicon RIE	Step 2 (mask oxide etching): 35 ~ 50 sec, Step 3 (anisotropic silicon etching): 8 ~ 15 sec, Step 4 (isotropic silicon etching): 0 sec	
Channel Narrowing	Isotropic SC1 etching	SC1 $NH_4OH:H_2O_2:H_2O$ = 1:1:6, 75 ~ 85 degC, 10 ~ 60 min	
	HSQ (BOX) removal	BHF 20 sec SPM $H_2O_2:H_2SO_4$ = 1:3, 110 ~ 130 degC, 10 min	
Gate oxidation	Cleaning	HF:H_2O = 1:100, 90 sec SPM $H_2O_2:H_2SO_4$ = 1:3, 110 ~ 130 degC, 10 min HF:H_2O = 1:100, 90 sec SC1 $NH_4OH:H_2O_2:H_2O$ = 0.25:1:5, 75 ~ 85 degC, 10 min HF:H_2O = 1:100, 60 sec	
	Gate oxidation	Dry oxidation 900 degC, O_2 1.0 l/min, 3 ~ 10 min	SiO_2: 5 ~ 10 nm / Channel SOI: ~ 5 nm
	(Additional gate oxide deposition)	CVD 840 degC, SiH_4Cl_2 20 sccm, N_2O 50 sccm, 80 Pa, 30 ~ 60 min	SiO_2: 15 ~ 30 nm
Gate deposition	Poly-Si deposition	CVD 580 degC, SiH_4 250 sccm, 33 Pa, 45 min	Poly-Si: 250 ~ 350 nm
Gate lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec	
	Pre-baking	100 degC, 10 min	
	Exposure	Karl Suss aligner 2.8 sec	
	Development	NMD-3 (TMAH 2.38 %) 60 sec	
	Post-baking	100 degC, 15 min	
Gate etching	Helicon RIE	Step 2: 5 sec, Step 3: 100 ~ 105 sec, Step 4: 30 sec	
	Resist removal	Acetone SPM $H_2O_2:H_2SO_4$ = 1:3, 110 ~ 130 degC, 10 min	
Ion implantation		P^+ 35 keV, 3×10^{15} cm^{-2} (for n-type) BF^{2+} 35 keV, 3×10^{15} cm^{-2} (for p-type)	

Passivation deposition	Cleaning	SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min	
	Oxide deposition	CVD 400 degC, SiH_4 15 sccm, O_2 60 sccm, 33 Pa, 140 min	SiO_2: 300 ~ 400 nm
Annealing	Cleaning	SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min	
	N_2 Annealing	950 degC, N_2 1.0 l/min, 20 min	
	H_2 Annealing	430 degC, N_2 6.5 l/min, H_2 100 sccm, 25 ~ 45 min	
Contact hole lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec	
	Pre-baking	100 degC, 10 min	
	Exposure	Karl Suss aligner 10 sec	
	Development	NMD-3 (TMAH 2.38 %) 90 sec	
	Post-baking	110 degC, 15 min	
Contact hole etching	Contact hole etching	BHF 3 ~ 5 min	
	Resist removal	Acetone SPM H_2O_2:H_2SO_4 = 1:3, 110 ~ 130 degC, 10 min	
Al evaporation	Cleaning	HF:H_2O = 1:100, 90 sec	
	Al evaporation		Al: 200 ~ 300 nm
Al electrode lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec	
	Pre-baking	100 degC, 10 min	
	Exposure	Karl Suss aligner 2.5 sec	
	Development	NMD-3 (TMAH 2.38 %) 60 sec	
	Post-baking	110 degC, 15 min	
Al etching	Al etching	Al etchant 45 ~ 55 degC, 1 min	
	Resist removal	Acetone	

List of Publications and Presentations

Journals

[1] YeonJoo Jeong, Kousuke Miyaji, Takuya Saraya, and Toshiro Hiramoto, “Silicon nanowire n-type metal-oxide-semiconductor field-effect-transistors and single-electron transistors at room temperature under uniaxial tensile strain,” to be submitted to *J. Appl. Phys*..

Presentations (International)

[1] YeonJoo Jeong, Kousuke Miyaji, and Toshiro Hiramoto, “Experimental Study on Silicon Nanowire nMOSFET and Single-Electron Transistor at Room Temperature under Uniaxial Tensile Strain”, *IEEE Silicon Nanoelectronics Workshop*, Honolulu, USA, M0930, Jun. 2008.

[2] YeonJoo Jeong, Jiezhi Chen, Takuya Saraya, and Toshiro Hiramoto, “Uniaxial Strain Effects on Silicon Nanowire pMOSFET and Single-Hole Transistor at Room Temperature,” *IEDM Tech. Dig.*, San Francisco, USA, pp. 761-764, 2008.

Presentations (Domestic)

[1] 鄭然周, 宮地幸祐, 更屋拓也, 平本俊郎, “ナノワイヤ MOSFET 及び室温動作単電子トランジスタにおける一軸引っ張り歪みの効果” 第 69 回応用物理学会連合講演会, 名古屋, 2008 年 9 月.

[2] 鄭然周, Chen Jiezhi, 更屋拓也, 平本俊郎, “ナノワイヤpMOSFET及び室温動作単正孔トランジスタにおける一軸歪みの効果” SDM 研究会, 北海道, 2009 年 2 月

[3] 鄭然周, Chen Jiezhi, 更屋拓也, 平本俊郎, “シリコンナノワイヤpMOSFET及び室温動作単正孔トランジスタにおける一軸歪みの効果” 第 56 回応用物理学会連合講演会, つくば, 2009 年 4s 月発表予定.

Other Presentations

[1] 鈴木龍太, 鄭然周, 更屋拓也, 平本俊郎, “CMOS ディジタル回路との連携による単電子トランジスタの自動的特性制御の検討” 第 56 回応用物理学会連合講演会, つくば, 2009 年 4 月発表予定.

Awards

[1] IEEE EDS Japan Chapter Student award, January, 2009.