PROPOSAL OF UNILATERAL SINGLE-FLUX-QUANTUM LOGIC GATE

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Abstract

A new type of single flux quantum logic gate is proposed, which can perform unilateral propagation of signal without using three-phase clock. This gate is designed to be built with bridge-type Josephson junctions. A basic logic gate consists of two one-junction interferometers coupled by superconducting interconnecting lines, and the logical states are represented by zero or one quantized fluxoid in one of one-junction interferometers. The bias current of the unequal magnitude to each of the two one-junction interferometers results in unilateral signal flow. By adjusting design parameters such as the ratio of the critical current of Josephson junctions and the inductances, circuits with the noise immunity of greater than 50% with respect to the bias current have been designed. Three cascaded gates were modeled and simulated on a computer, and the unilateral signal flow was confirmed. The simulation also shows that a switching delay about 2 picoseconds is feasible.

Introduction

In Josephson junction circuits, which have been built so far, the voltage change of Josephson junctions is used to represent logical states, and Josephson junctions are either in the superconducting state or latched in the voltage state during the logic cycle.[1,2]

On the other hand single flux quantum logic circuits[3,4,5] in which zero or one quantized fluxoid in one-junction interferometer represents logical states "0" or "1" are attractive from viewpoints of very high switching speed and extremely low power consumption, because they can be built with bridge-type Josephson junctions having small capacitances in contrast to the conventional tunneling junctions and the Josephson junctions are in the voltage state only for switching transient. Single flux quantum logic circuits, which have been proposed so far, have needed a three-phase clock to ensure the unilateral propagation of signal. However, three-phase clock scheme increases the signal propagation delay and the size of the gate.

In this paper, we propose a new type of single flux quantum logic gate which makes unilateral propagation of signal possible without using three-phase clock. This circuit configuration is designed to be built with bridge-type Josephson junctions, which do not have pysteresis in their current-voltage characteristics, and is expected to be useful as high-speed logic gate because of the small capacitances of bridge-type Josephson junctions.[6]

Basic Gate Configuration

A basic logic gate consists of two one-junction interferometers coupled by superconducting interconnecting lines, as shown in Fig. 1 (a) and (b), where λ_i is the characteristic phase of the inductor L_i given by

$$\lambda_i = 2\pi L_i I_o / \Phi_o \quad . \tag{1}$$

Unilateral propagation of signal can be realized by the basic configuration shown in Fig.1 (a), but the Josephson junction J_3 and inductor L_4 in the gate as illustrated in Fig.1 (b) are added to obtain large noise immunity with respect to the bias current large, as will be mentioned later.

Manuscript received September 10, 1984

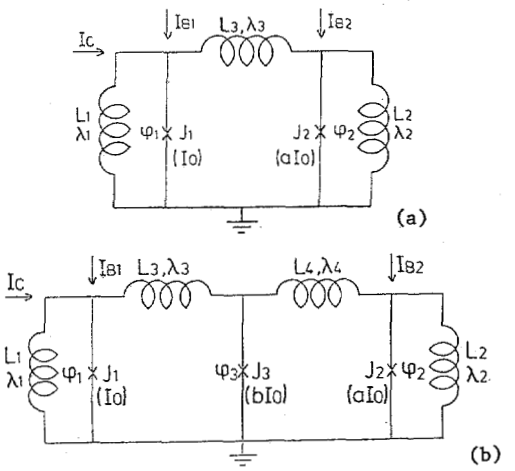

Fig.1 Proposed logic gate; J_1, J_2 and J_3 are Josephson junctions, I_o is the critical current of J_1, I_{B1} and I_{B2} are the bias currents. (a) basic configuration (b) configuration with large noise immunity.

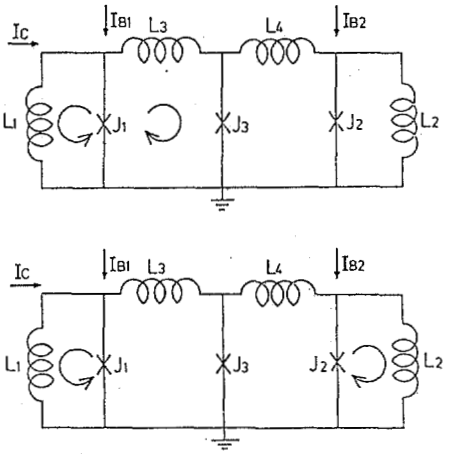

Fig.2 Transmission of signal in the gate of Fig.1 (b) for the forward direction. (a) after J_1 is switched, and (b) after J_3 and J_2 are switched successively.

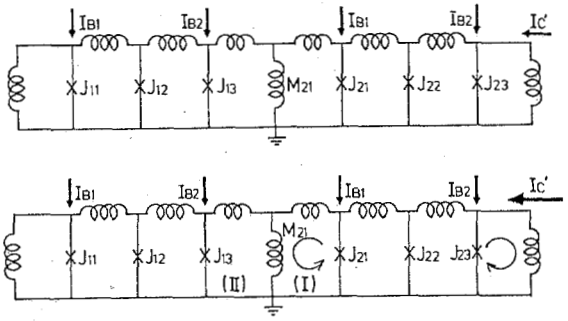

Fig.3 Attenuation of signal in the gate of Fig.1 (b) for the reverse direction . (a) J_{23} is not switched by the same input current as in Fig.3.(b) A pair of quantized fluxoids is generated in the gate when larger current is injected to J_{23}, but it does not propagate the preceeding gates through the coupling, because J_{13} is not switched to the voltage state.

The bias currents of the unequal magnitude to each of the two one-junction interferometers results in unilateral signal flow. Small additional input current given to the left one-junction interferometer can generate a pair of quantized fluxoids, but large additional input current is necessary to generate a pair of quantized fluxoids in the right one-junction interferometer. The forward transfer of the quantized fluxoid from the left interferometer to the right interferometer is achieved by injecting large clockwise circulating current into the adjacent junctions J_3 and successively J_2, as shown in Fig.2. On the other hand the reverse transfer from the right interferometer to the left interferometer cannot be achieved, because the injected current through the coupling M_{21} from the loop (I) to (II) is so small that the Josephson junction J_{13} cannot be brought to the voltage state, as shown in Fig.3.

Figure 4 (a) and (b) show the calculated threshold characteristics of the gate shown in Fig.1 (a) and (b) for the parameters listed in the figure captions, respectively. The threshold characteristics were obtained by considering the stability condition of the gate. The numbers in the parentheses represent the number of quantized fluxoid in each loop, where a positive sign represents the quantized fluxoid associated with clockwise circulating current and a negative sign represents the quantized fluxoid associated with counterclockwise circulating current. The sum of these numbers must be zero because of the flux quantization condition by the outer superconducting inductance loop,

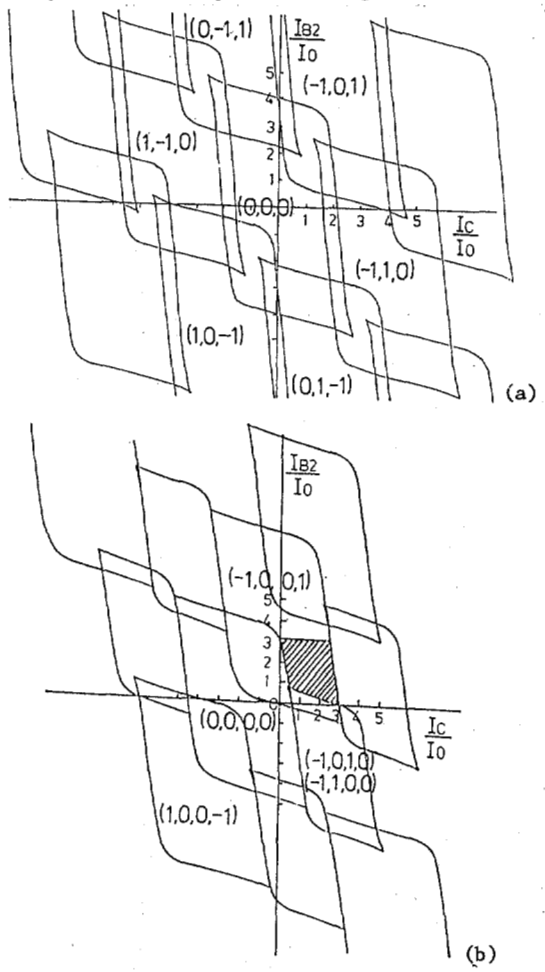

Fig.4 Calculated threshold characteristics for the gate in Fig.1 (a) and (b) for the following parameters values, respectively. The parameters are; (a) a=2, $\lambda_1=\lambda_3=\pi$, $\lambda_2=\pi/2$, and $I_{B1}=0$. (b) a=2, b=1, $\lambda_1=9\pi/10$, $\lambda_2=9\pi/20$, $\lambda_3=\lambda_4=3\pi/10$, and $I_{B1}=2.0I_0$.

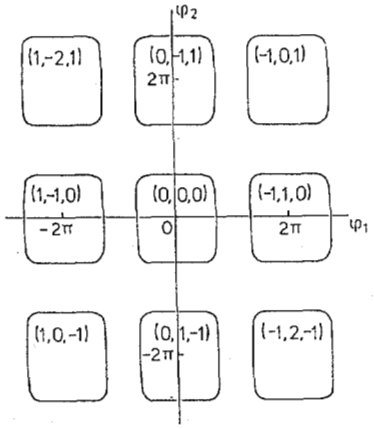

Fig.5 Calculated threshold characteristics in the phase-plane for the gate in Fig.1 (a). The parameters are the same as in Fig. 4 (a).

and of the initial condition with zero flux quantum.

In the case of the gate shown in Fig.1, different from dc SQUID, there exist some quantum modes in the whole current-plane as shown in Fig.4, therefore, Josephson junctions can not be in the voltage state steadily and one quantum mode corresponds to only one mode in the whole phase-plane, as shown in Fig.5.

Principles of Operation

The principles of operation for the gate shown in Fig.1 (b) are as follows. Without the input current I_c there is no fluxoid in any loop, or (0,0,0,0) mode; this represents logical state "0". The input current drives the junction J_1 from the superconducting state to the voltage state and the voltage induces a counterclockwise circulating current in the leftmost loop and a clockwise circulating current in the adjacent loop, as shown in Fig.2 (a). In consequence the current flowing through J_1 becomes too small to keep the junction in the voltage state and the junction J_1 returns to the superconducting state. It must be notified that the duration of the voltage state is so short that the power consumption is negligibly small and this situation is significantly different from the latching operation of circuits built with tunnel type junctions. This clockwise circulating current switches J_3 and J_2 successively to the voltage state, resulting in a transfer of the quantized fluxoid to the rightmost loop, or (-1,0,0,1) mode as shown in Fig.2 (b); this represents logical state "1".

The coupling between the basic gates can be accomplished by mutual inductance, or its T transform as shown in Fig.3. Using the T transform a part of the clockwise circulating current is injected into the next gate directly, so that current injection logic can be built. Moreover, the coupling between non-adjacent gates can be accomplished by connecting the gates with superconducting transmission lines as same as the voltage mode Josephson junction gates. In this case, however, the voltage pulse accompanied with the switching of the rightmost Josephson junction causes the injecting current into the next gate to cause mode transition.

Without the bias current, the gate is in the (0,0,0,0) mode, therefore, resetting the gate to logical state "0" can be accomplished by reducing the bias current to zero, similar to resetting commonly used in Josephson logic gates built with tunnel junctions. In

this case, however, Josephson junctions are not in the voltage state, therefore, "punchthrough" which is inherent in tunnel type Josephson junction logic gates[8] does not take place.

Design Consideration

Circuit parameters, such as the ratio of the critical current of Josephson junctions and inductances were chosen to obtain the largest noise immunity with respect to the bias current and the inclination $\Delta I_{B2}/\Delta I_C$ in the threshold characteristics. This inclination is related to the isolation between the input and the output, if it is large enough, the change of the phase difference across the output junction gives little effect on the input junction. Unilateral propagation of signal can be accomplished without J_3 as aforementioned, however, in the case of the gate shown in Fig.1 (a) these two parameters are in trade-off, therefore, the maximum noise immunity with respect to the bias current I_{B2} obtained with keeping the $\Delta I_{B2}/\Delta I_C$ as 7 is about 20%. The roll of J_3 is to obtain the large noise immunity with respect to the bias current large, keeping the $\Delta I_{B2}/\Delta I_C$ sufficiently large. If the products of the critical current of J_3 with L_3 and L_4 are chosen to be small enough with keeping the $\Delta I_{B2}/\Delta I_C$ as large as 7, a circulating current can be made not to flow in the middle two loops steadily. This means that the area in the threshold characteristics corresponding to the modes (-1,1,0,0) and (-1,0,1,0), which are not related to any of the logical state, can be made small and the noise immunity with respect to the bias current becomes larger. Figure 4 (b) shows the calculated threshold characteristics of a gate, whose noise immunity is larger than 50% with respect to the bias current I_{B2} for large $\Delta I_{B2}/\Delta I_C$, such as 7.

Thermal Stability of Gate

In the presence of the thermal noise, it is known that thermally activated switching of Josephson junctions may take place.[9] In the case of the gate shown in Fig.1, there is only one potential well in the whole phase-plane corresponding to one quantum mode, and any of the junctions cannot be steadily on the voltage state, so that the phases of the junctions are not rotating. This is different from the situation of dc SQUID.

The hatched region in Fig.4 (b) shows the operating region of the gate shown in Fig.1 (b), where only one stable point exists in the phase-plane. With the bias current and input current, therefore, the gate can be brought to (-1,0,0,1) mode. Without the input current, however, the operating point is in the overlapping region of (0,0,0,0) and (-1,0,0,1) modes, and in the presence of thermal noise the undesirable mode transition from (0,0,0,0) to (-1,0,0,1) mode may take place.

Contour maps of potential energy for the gate[10,11] were calculated in order to study the stability of the gate. Figure 6 shows the contour map of the potential energy in the overlapping region of the two modes for the parameters given in the figure caption. In this figure, there are two stable points at A and B corresponding to the mode (0,0,0,0) and (-1,0,0,1), respectively. The potential difference between these stable points and the saddle point at C is sufficiently large enough to ensure that the mean time between failure for the system containing 10^6 gates is longer than one year in the presence of the thermal noise at 4.2 K. Even though the thermal noise at 4.2 K is considered in the design of the operating bias point for the gate, the noise immunity for the gate in Fig.4 (b) is as large as 50% with respect to the bias current I_{B2}.

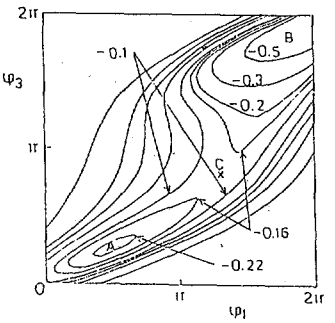

Fig.6 Contour map of potential energy for the gate in Fig.1 (b), with the bias current. A and B are the stable points and C is the saddle point. The parameters are the same as in Fig.2 (b), and $I_{B2}=2.3I_0$ and $I_C=0.7I_0$. The number in the figure shows the value of potential energy in eV for $I_0=50\ \mu A$.

Computer Simulation

Three cascaded gates shown in Fig.1 (b) were modeled and simulated on computer, where bridge-type Josephson junctions were represented with a resistively shunted junction model in the limit of heavy damping. The relevant equations are for fluxoid quantization in each loop and current continuity at each node, given by the next equations.

$$\rho_{11}+\lambda_1\left(\sin\rho_{11}+\frac{\Phi_o}{2\pi}\frac{G_{11}}{I_o}\frac{d\rho_{11}}{dt}\right)+\frac{\lambda_1}{\lambda_3}(\rho_{11}-\rho_{12})-\lambda_1(i_c+i_{B1})=0 \quad (2)$$

$$\rho_{i2}-\rho_{i1}+\lambda_3\left(b\sin\rho_{i2}+\frac{\Phi_o}{2\pi}\frac{G_{i2}}{I_o}\frac{d\rho_{i2}}{dt}\right)+\frac{\lambda_3}{\lambda_4}(\rho_{i2}-\rho_{i3})=0 \qquad (i=1,2,3) \quad (3)$$

$$\rho_{i3}+\lambda_2\left(a\sin\rho_{i3}+\frac{\Phi_o}{2\pi}\frac{G_{i3}}{I_o}\frac{d\rho_{i3}}{dt}\right)+\frac{\lambda_2}{\lambda_4}(\rho_{i3}-\rho_{i2})-\lambda_2 i_{B2}+\lambda_M\left(\sin\rho_{(i+1)1}+\frac{\Phi_o}{2\pi}\frac{G_{(i+1)1}}{I_o}\frac{d\rho_{(i+1)1}}{dt}\right)+\frac{\lambda_M}{\lambda_1}\rho_{(i+1)1}+\frac{\lambda_M}{\lambda_3}(\rho_{(i+1)1}-\rho_{(i+1)2})-\lambda_M i_{B1}=0 \qquad (i=1,2) \quad (4)$$

$$\rho_{i1}+\lambda_1\left(\sin\rho_{i1}+\frac{\Phi_o}{2\pi}\frac{G_{i1}}{I_o}\frac{d\rho_{i1}}{dt}\right)+\frac{\lambda_1}{\lambda_3}(\rho_{i1}-\rho_{i2})-\lambda_1 i_{B1}+\lambda_M\left(a\sin\rho_{(i-1)3}+\frac{\Phi_o}{2\pi}\frac{G_{(i-1)3}}{I_o}\frac{d\rho_{(i-1)3}}{dt}\right)+\frac{\lambda_M}{\lambda_2}\rho_{(i-1)3}+\frac{\lambda_M}{\lambda_4}(\rho_{(i-1)3}-\rho_{(i-1)2})-\lambda_M i_{B2}=0 \qquad (i=2,3) \quad (5)$$

$$\rho_{33}+\lambda_2\left(a\sin\rho_{33}+\frac{\Phi_o}{2\pi}\frac{G_{33}}{I_o}\frac{d\rho_{33}}{dt}\right)+\frac{\lambda_2}{\lambda_4}(\rho_{33}-\rho_{32})-\lambda_2(i_c'+i_{B2})=0 \quad (6)$$

Here, ρ_{ij} represents the phase difference across the j_{th} junction of the i_{th} gate, and G_{ij} is the parallel conductance of the j_{th} junction of the i_{th} gate, and i_c, i_{B1}, and i_{B2} are I_c/I_o, I_{B1}/I_o, and I_{B2}/I_o respectively. The existence of a fluxoid quantum in any one-junction interferometer is represented by the change about 2π of the phase difference across the Josephson junction contained in that interferometer.

Figure 7 shows the results of computer simulation indicating the forward transfer of a quantized fluxoid,

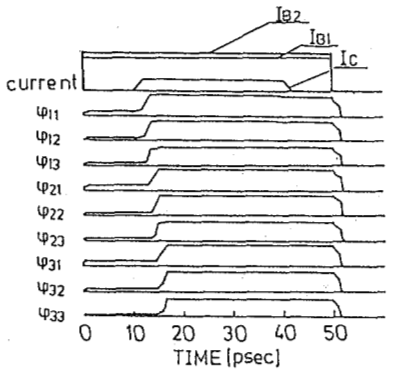

Fig.7 Simulated switching behavior of three cascaded gates, when I_C is applied to the input junction of the first gate. The parameters are the same as in Fig.5.

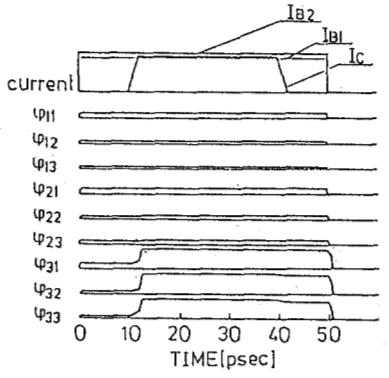

Fig.8 Simulated switching behavior of three cascaded gates, when I_C' is applied to the output junction of the third gate. The parameters are the same as in Fig.6, except for $I_C'=2.1I_0$.

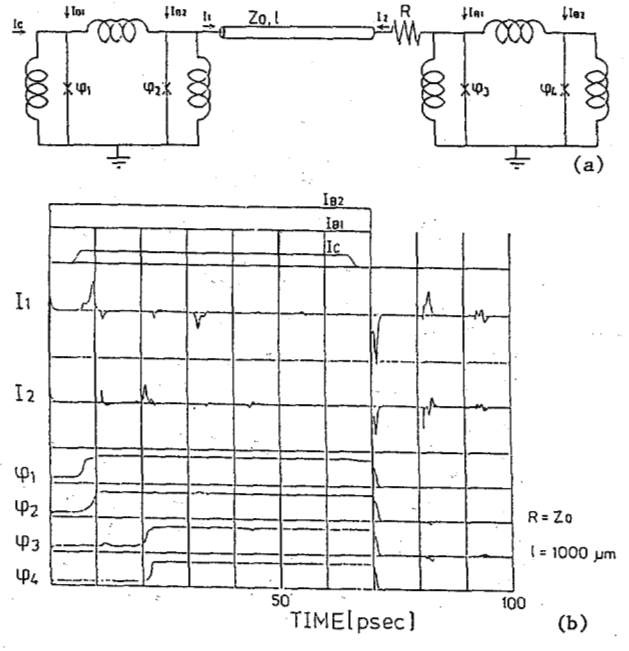

Fig.9 The coupling between the distant gates by connecting with the superconducting transmission line. (a) Schematic drawing of this coupling. (b) Results of computer simulation of the circuit in (a).

when I_C is applied to the input junction of the first gate. It can be seen that switching delay about 2 picoseconds per gate is feasible, when I_C overdrives about 20 percents. Figure 8 shows the results of computer simulation indicating that a pair of quantized fluxoids is generated in the third gate, but it does not propagate to the preceeding gates.

Thus, the unilaterality of signal flow was confirmed from the results of computer simulation.

Two gates coupled with superconducting transmission line shown in Fig. 9 (a) were also modeled and simulated in the same way. Figure 9 (b) shows the results of computer simulation indicating that the voltage pulse accompanied with the switching of the output junction of the first gate causes the injecting current in the next gate to generate a pair of quantized fluxoids and transfer a quantized fluxoid to the right one-junction interferometer.

Conclusion

A new type of single flux quantum logic gate which can perform unilateral propagation of signal has been designed to be built with bridge-type Josephson junctions. High switching speed of 2 picoseconds is predicted by the computer simulation. A gate, whose noise immunity is as large as 50% with respect to the bias current when the thermal noise at 4.2 K is considered and $\Delta I_{B2}/\Delta I_C$ is as large as 7, was found by adjusting design parameters such as the ratio of the critical current of Josephson junctions and inductances Three cascaded gates were modeled and simulated on a computer, and the unilaterality of signal flow was confirmed.

Acknowledgement

This work was supported by the Ministry of Education, Research and Culture under Grant-in-Aid "Special Promotion Research No.57060001".

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