Architectural Considerations for Photonic Switching Networks

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(Invited Paper)

Abstract—This paper will review some of the photonic technologies that could become important components of future telecommunications systems. It will begin by dividing photonic devices and systems into two classes according to the function they perform. The first class, relational, will be associated with devices, which under external control, maps the input channels to the output channels. The second class, logic, requires that the devices perform some type or combination of Boolean logic functions. After the classes are defined, some of the strengths and weaknesses of the photonic domain will be presented. Relational devices and their applications will then be discussed. Finally, there will be a review of optical logic devices and their potential applications.

I. INTRODUCTION

WITHIN recent years there has been a significant amount of interest in applying the new and developing photonics technology in telecommunications switching systems [1]. As the transmission plant has converted its facilities to fiber, there is an economic interest in completing the optical path through the switching system to the terminal facilities without requiring optical-to-electrical (o/e) conversions. There are several devices that have emerged within the past few years which have the capability of meeting this goal. These devices can be arranged into two major classes according to the function they perform [2]. The first of these classes, called *relational* devices, perform the function of establishing a *relation* or a mapping between the inputs and the outputs. This *relation* is a function of the control signals to the device and is independent of the signal or data inputs. As an example, if the control signal is not enabled, the relation between the inputs and the outputs of a 2 × 2 device might be input port 1 → output port 1 and input port 2 → output port 2. When the control is enabled, the relationship might be input port 1 → output port 2 and input port 2 → output port 1. This change in the *relation* between the inputs and outputs corresponds to a change in the state of the device. Another property of this device is that the information entering and flowing through the devices cannot change or influence the current *relation* between the inputs and outputs. An example of this type of device is the directional coupler as it is used in switching applications. Thus, the strength of relational devices is that they

cannot sense the presence of individual bits that are passing through them which allows them to pass high bit rates. The weakness of relational devices is that they cannot sense the presence of individual bits that are passing through them which reduces their flexibility.

The second class of devices will be referred to as *logic* devices. In these devices, the data or information carrying signal that is incident on the device controls the state of the device in such a way that some Boolean function or combination of Boolean functions is performed on the inputs. For this class of device, at least some of the devices within a total system must be able to change states or *switch* as fast or faster than the signal bit rate. This high-speed requirement for logic devices will limit the bit-rates of signals that can eventually flow through their systems to less than those that can pass through relational systems. Thus, the strength of logic devices is the added flexibility that results from their ability to sense the bits that are passing through them while their weakness is that they sense the bits that pass through them which limits the maximum bit-rate that they can handle.

This paper will begin by discussing both the strengths and limitations of the photonic technology. Some of the items to be discussed include power, speed, bandwidth, and parallelism. The next section will discuss optical relational systems with a focus on the directional coupler. The reason for this focus is that directional couplers will most likely be the initial photonic switching component to enter the marketplace. Finally, there will be a discussion of optical logic systems. These systems are still primarily in the research labs and not ready for development.

II. STRENGTHS AND LIMITATIONS OF THE PHOTONIC TECHNOLOGY

Prior to discussing either photonic devices or their applications it is important to understand both their potential and limitations. This section has the purpose of discussing the strengths and weaknesses of the photonics switching technology. It will begin by discussing the power, speed, and bandwidth limitations of photonic devices. Next it will focus on parallelism and how it can be used in photonic systems. Finally, there will be a brief discussion on the size of future devices.

A. Power, Speed, and Bandwidth

There are two speed limitations that must be considered in the design of photonic switching systems. The first of

these limitations is the time required to *switch* or change the state of a device. *Switching*, in this case, refers to the changing of the present state of a device to an alternate state, as opposed to the "switching" that is analogous to an interconnection network reconfiguration. In the normal operating regions of most devices, a fixed amount of energy, the switching energy, is required to make them change states. This switching energy can be used to establish a relationship between both the switching speed and the power required to change the state of the device. Since the power required to switch the device is equal to the switching energy divided by the switching time, then a shorter switching time will require more power. As an example, for a photonic device with an area of 100 μm^2 and a switching energy of 1 fJ/μm^2 to change states in 1 ps requires 100 mW of power instead of the 100 μW that would be required if the device were to switch at 1 ns. Thus, for high-power signals the device will change states rapidly, while low-power signals yield a slow switching response.

Some approximate limits on the possible *switching* times of a given device, whether optical or electrical, are illustrated in Fig. 1 [3]. In this figure the time required to *switch* the state of a device is on the abscissa while the power/bit required to *switch* the state of a device is on the ordinate. The region of spontaneous switching is the result of a background thermal energy that is present in a device. If the switching energy for the device is too low, the background thermal energy will cause the device to change states spontaneously. To prevent these random transitions in the state of a device, the switching energy required by the device must be much larger than the background thermal energy. To be able to differentiate statistically between two states, this figure assumes that each bit should be composed of at least 1000 photons [4]. Thus, the total energy of 1000 photons sets the approximate boundary for this region of spontaneous switching. For a wavelength of 850 nm, this implies a minimum switching energy on the order of 0.2 fJ.

For the thermal transfer region, Smith assumed that for continuous operation the thermal energy present in the device cannot be removed any faster than 100 W/cm^2 (1 μW/μm^2). There has been some work done to indicate that this value could be as large as 1000 W/cm^2 [5]. This region also assumes that there will be no more than an increase of 20°C in the temperature of the device. Devices can be operated in this region using a pulsed rather than continuous mode of operation. Thus, high-energy pulses can be used if sufficient time is allowed between pulses to allow the absorbed energy to be removed from the devices.

The cloud represents the performance capabilities of current electronic devices. This figure illustrates that optical devices will not be able to *switch* states orders of magnitude faster than electronic devices when the system is in the continuous rather than the pulsed mode of operation. There are, however, other considerations in the use of optical computing or photonic switching devices than
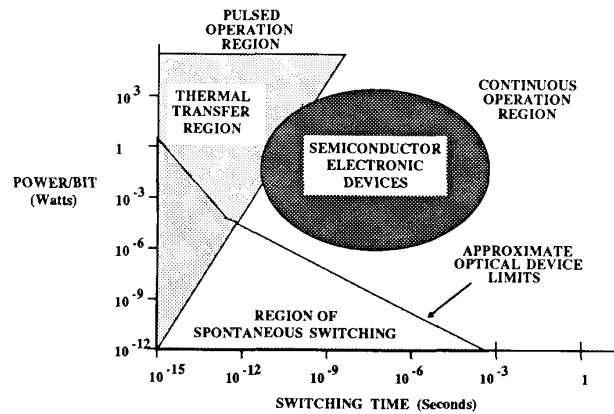

Fig. 1. Fundamental switching limits at 850 nm.

how fast a single device can change states. Assume that several physically small devices need to be interconnected so that the state information of one device can be used to control the state of another device. To communicate this information, there needs to be some type of interconnection with a large bandwidth that will allow short pulses to travel between the separated devices. Fortunately, the optical domain can support the bandwidth necessary to allow bit rates in excess of 100 Gbits/s, which will allow high-speed communication between these individual *switching* devices. In the electrical domain, the communications bandwidth between two or more devices is limited by the resistance, capacitance, and inductance of the path between the different devices. Therefore, even though photonic devices cannot *switch* orders of magnitude faster than their electronic counterparts, the communications capability or transmission bandwidth present in the optical domain should allow higher speed *systems* than are possible in the electrical domain.

The second speed limitation, which applies only to relational devices, will be referred to as the transmission bandwidth. After a relational device has been put into a particular state, it acts like a transmission line to any data entering its inputs. This input data cannot change the state of the device, thus the signal bit-rates passing through a relational device are not limited by the constraints outlined in Fig. 1. For most relational devices, this transmission bandwidth should be able to support bit-rates in excess of 100 Gbits/s.

In summary, networks composed of relational devices will have their signal bit rates limited by the transmission bandwidth and their reconfiguration rates limited by the switching time of the devices, while switching networks based on optical logic will have both their signal bit-rates and reconfiguration rates limited by the switching time of their devices.

B. Parallelism

Another method of increasing the capacity of a system, in addition to operating at higher speeds, is to operate on information in parallel instead of in series. In pursuing

this parallelism, attention has recently been placed on free-space optics. These types of systems normally are composed of multiple two-dimensional (2-D) arrays of optical devices that are interconnected through either bulk optics or holography. Fig. 2 shows the optical interconnection between two 2-D arrays of optical elements. The interconnection in this case is a simple lens system. The optical elements, which will be referred to as pixels, could be optical NOR gates, optical light valves, etc. The number of pixels that can be interconnected in this manner is limited by the resolution of the optical interconnection system. Even relatively inexpensive optical imaging systems exhibit resolutions on the order of 10 μm over a 1 mm field. This provides access to 100×100 or 10^4 pixels. If each pixel can be equated to a pin-out, then for a 2-D array there can be greater than 10^4 pin-outs. The maximum number of pixels or pin-outs that can be supported by a lens or any optical system is referred to as its space–bandwidth product [6] (SBWP) or the degree of freedom of the system. Satellite imaging systems have been made that have an SBWP of 10^8 pixels.

Fig. 3, on the other hand, illustrates an optical interconnect based on holograms. Holography offers the promise of extremely high SBWP ($>10^{10}$). This will be discussed in more detail in Section IV-B-2.

There is no reason to limit the pixels of these 2-D arrays to all-optical logic gates; they could also be a mixture of electronic and optical devices (smart pixels) as shown in Fig. 4. This mixture of electronic and optical devices is designed to take advantage of the strengths in both the electrical and optical domain. The optical devices include detectors to convert the signals from the previous 2-D array to electronic form and modulators (surface emitting lasers or LED's) to enable the results of the electronically processed information to be transferred to the next stage of 2-D arrays. The electronics does the intelligent processing on the data. Since the electronics is localized with short interconnection lengths, the speed of this electronic island should be fast. The applications of smart pixels will be discussed later in Section IV-A-2.

To take advantage of the parallelism inherent in free-space optics, a device should have the capability of driving other devices (fan-out) in addition to being controlled by more than one device (fan-in). Since fan-out corresponds to a division of the energy emitted from a device output to the inputs of other devices, the output energy must be significantly larger than the energy required by the input to the subsequent device. Another factor that affects the fan-in is the contrast ratio, the contrast ratio being the ratio of the transmitted intensity of both states of a device. For low contrast ratios, unwanted noise is present in the system, thus reducing the ability of a device to sample the input correctly.

C. Device Size

The minimum size of an optical switching device cannot be reached below a volume of $(\lambda/n)^3$ [3] where n is
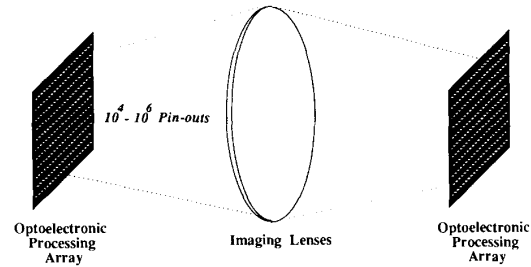
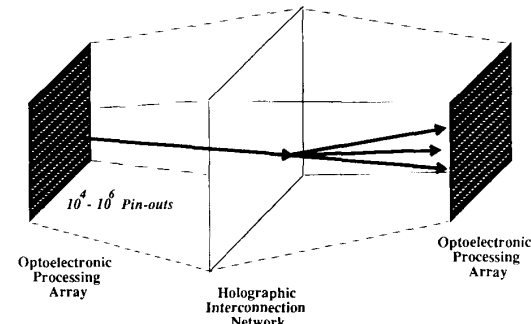

Fig. 2. Optical parallel interconnections.
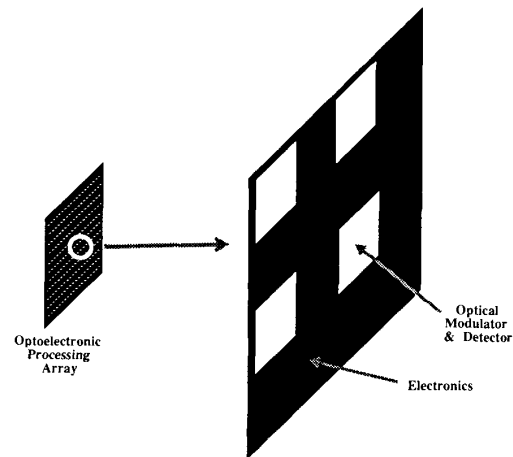

Fig. 3. Holographic interconnects.

Fig. 4. Smart pixels.

the index of refraction of the device. For the case of a 2-D array of devices, assuming that these devices are fabricated such that there is a separation of λ/n between the devices, then approximately 25 million devices per square centimeter could be possible at $\lambda/n = 1$ μm. As the device switching speed increases, the thermal transfer capacity of the devices will most likely prevent such a large number of devices from ever being realized. As an example, if there are 25 million devices per square centimeter that require 1 pJ to switch, and it is desired to switch these devices in 100 ps, then the total array would require 250 kW/cm^2 of optical power if all of the devices were to switch at the same time.

III. OPTICAL RELATIONAL SYSTEM

In this section, several photonic switching systems that are based on relational devices will be reviewed. The first type of system to be discussed is based on spatial light modulators (SLM) which are 2-D arrays of devices, each of which has the capability of modulating the light that is incident upon it. The second example of a relational system is based on wavelength-division switching. Finally, the systems based on Ti : LiNbO$_3$ directional couplers will be discussed.

A. Spatial Light Modulators

An SLM is a two-dimensional array of optical modulators [7]. Each of these modulators is independent of the others and has the capability of modulating the incident light. For the applications described in this paper, the modulators will be assumed to be digital, in that they possess two states: transparent to be the incoming light (on) and opaque to the incoming light (off). These arrays are electrically controlled such that an electrically enabled pixel will be transparent while a disabled pixel will block the incident light. An SLM that is currently available in the marketplace is based on the magnetooptic effect [8]. Some other SLM's include the liquid crystal light valves (LCLV) [9], PLZT modulators [10], deformable mirrors [11], and GaAs multiple-quantum well (MQW) modulators [12].

One example of how an SLM can be used as a photonic switch is shown in Fig. 5 [13], [14]. In this figure, the fiber inputs are horizontally aligned as a row of inputs. The inputs are aligned to associate each fiber with a unique column of the SLM. A lens system is used to spread these inputs vertically so that the light emitted from each input is spread over all the elements' of the SLM's associated column. The appropriate pixels of the SLM are enabled before the data pass through the system. The one or more enabled pixels in each column allow the incident light to be transmitted through the device while the remaining pixels block the incident light. The output column of fibers acccepts the light that is passed through the SLM. An important restriction for this type of structure is that only one pixel on each row can be enabled at any time. The relational nature of this structure is evident in that each row of the SLM acts like an $N \times 1$ switch where N is the number of pixels per row. The total structure is topologically equivalent to a nonblocking crossbar interconnection network. The weakness of these systems is the losses that occur in the spreading and collection of the light going to and from the SLM can be greater than $1/N^2$.

As with all relational structures, high signal bit-rates pass through the switch with the speed limitation being the system reconfiguration time.

B. Wavelength-Division Switching Systems

Another type of relational architecture that has received a considerable amount of attention is wavelength-division switching [15]. This is schematically shown in Fig. 6. In this figure, the entering information is used to modulate a light source that has a unique wavelength for each input. All the optical energy is combined and then split so it can be distributed to all the output channels. The tunable filter on each ouput is adjusted such that it only allows the wavelength associated with the desired input channel to pass to the detector. Thus, by varying the tunable filter, an output has access to any or all of the input channels. Obviously, another method of detecting the appropriate wavelength would be through the use of coherent detection techniques [16]. This wavelength-division concept can be generalized to include other orthogonal basis functions as the carrier instead of wavelength [17], [18].

C. Directional Couplers

A directional coupler is a device that has two optical inputs, two optical outputs, and one control input. The control input is electrical and has the capability of putting the device in the *bar* state, input port 1 → output port 1 and input port 2 → output port 2, or the *cross* state, input port 1 → output port 2 and input port 2 → output port 1 [19]. The most advanced implementations of these devices have occurred using the Ti : LiNbO$_3$ technology [20]. The strength of directional couplers is their ability to control extremely high bit rate information. They are limited by several factors: 1) the electronics required to control them limits their maximum reconfiguration rate, 2) the long length of each directional coupler prevents large scale integration, and 3) the losses and crosstalk associated with each device limit the maximum size of a possible network unless some type of signal regeneration is included at critical points within the system [21]. A modest number of these devices have been integrated onto a single substrate to create larger photonic interconnection networks such as an 8 × 8 crossbar interconnection network [22]. As another example, a 4 × 4 crossbar interconnection network composed of 16 integrated directional couplers, all having crosstalk less than −35 dB with an average fiber-to-fiber insertion loss of less than 5.2 dB, has been fabricated [23]. The following sections will discuss some of the practical considerations that need to be addressed in the design of a photonic switching system based on directional couplers. Several potential applications will then be discussed.

1) Practical Considerations: There are several practical issues that need to be considered when designing a system based on Ti : LiNbO$_3$ directional couplers. These issues include the required parallel development of polarization maintaining (PM) fiber, optical amplifiers, and the packaging required to make the devices reliable and easy to use.

a) Polarization Maintaining Fiber: To minimize the required drive voltages, directional couplers have been optimized to operate with a single linear polarization. This requirement reduces the required switching voltage from approximately 50 V to the 10–15 V range. These lower voltages are desired to allow high-speed switching of the directional couplers. One problem with using single po-
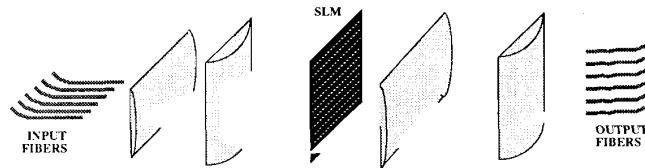
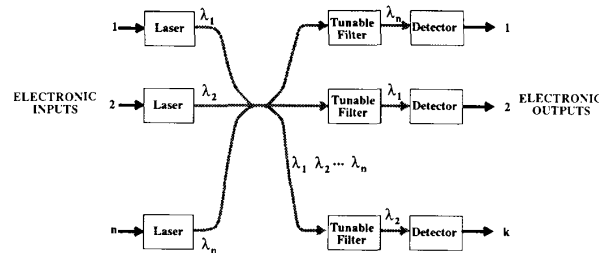Fig. 5. Optical crossbar interconnection network.

Fig. 6. Wavelength-division switching system.

larization devices is that as light propagates through standard single-mode fiber, the state of polarization can be changed from a linearly polarized wave to a wave having an elliptical polarization. Another complicating factor is that this change in the state of polarization does not remain constant over time. To solve this problem, a PM fiber is required for the interconnection from all the laser sources to the $Ti:LiNbO_3$ substrates and for any substrate-to-substrate interconnection. In addition to PM fiber, there must also be PM fiber connectors. These connectors become important when networks involving the interconnection of multiple $LiNbO_3$ substrates are required.

b) Optical Amplifiers: The eventual size of a switching fabric composed of directional couplers is limited by either the losses through the system or the individual crosstalk terms which degrade the system signal-to-noise ratio (SNR) below an acceptable value [24]. To avoid this problem, thresholding optical amplifiers can be inserted at critical points in the network to both boost the strength of the signal and remove accumulated noise. Unfortunately, most of the optical amplifiers under investigation are linear amplifiers [25], these amplifiers have the disadvantage of amplifying the low-level noise signals as well as the desired signals. It is desired to have an amplifier that will not amplify low-level signals associated with the logic level "0" but will amplify signals above the threshold of the logic level of a "1." The characteristics of a thresholding optical amplifier [26] are shown in Fig. 7. In the ideal case, there would be no amplification for signals below a given intensity level. Once an intensity threshold has been surpassed, a large gain is desired until a saturated or maximum value of output intensity is obtained [27]. Such a device could both amplify a signal and improve the SNR of the signals passing between substrates of a dimensionally large relational photonic switching system.
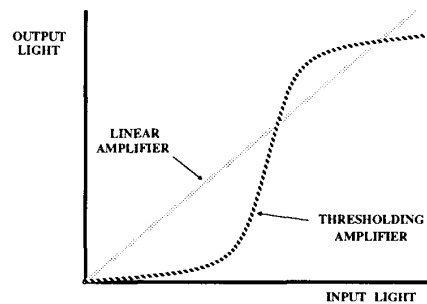
OPTICAL AMPLIFIERS

Fig. 7. Optical amplifier characteristic curves.

A component required in conjunction with optical amplifiers is an optical isolator. In addition to isolating lasers from reflections that can occur at connectors, splices, and other interfaces, optical isolators are required to prevent optical amplifiers from lasing. This lasing action can occur since the two requirements for a laser are met: optical gain and positive feedback. The optical amplifier provides the gain and the connectors, splices, or other reflecting interfaces on both sides of the optical amplifier provide the positive feedback required. For high-gain optical amplifiers, this lasing action can occur with small interface reflectivities. By placing an isolator between the unwanted reflections and the optical amplifier, the positive feedback is reduced, thus preventing the undesired lasing.

c) Packaging: To develop both a marketable and reliable system, devices have to be packaged in a useful and reliable manner. This is one of the most overlooked aspects in the development of this technology. At the current time, most of the devices are packaged in their own separate package. For large systems, this could involve an enormous amount of physical space just to house all the individual components. High-speed packaging is an-

other unresolved issue. This subject will require a large amount of attention before this technology can successfully enter the marketplace.

2) *Applications of Directional Couplers:* Perhaps the key event required to drive the Ti : LiNbO$_3$ directional coupler technology into the marketplace within the next three to five years is a *good* application. Therefore, several potential applications will be outlined in this section. The first application to be discussed utilizes the directional couplers in a space switching environment. Second, the signal formats required to allow these relational devices to operate in a time-division application will be outlined. Finally, there will be brief examples of both time-multiplexed and packet switching.

a) Space Switching: This type of switching will most likely be the first application of the Ti : LiNbO$_3$ directional couplers. It requires long hold times with moderate reconfiguration rates. Once a path has been set up, high-speed data, multiplexed speech, or video can be transferred through the fabric.

The implementation of a large space switch requires the interconnection of many smaller photonic switches that are used as building blocks. These building blocks will most likely have dimensions less than 16 × 16 because of the large size of directional couplers and the large bending radii required in the integrated waveguides. Two examples of topologies for these building blocks are the crossbar interconnection network [21] and the broadcast network proposed by Spanke [28]. For point-to-point networks, the interconnection of these building blocks to construct a larger switching system can be done with Clos, Benes, banyan, omega, or shuffle networks. If video information is to be a main component of the system traffic, then a broadcast environment becomes important. A good topology for a broadcast network is a Richards network [29]. An example of a space-switching experiment is shown in Fig. 8 [30]. In this system, each terminal has the capability of transmitting and receiving one of two wavelengths. Initially a path is set up between two terminals through the folded optical switching network. This network is composed of switching arrays made using Ti : LiNbO$_3$ directional couplers. After the path is set up, an input signal is sent to terminal *B* on a light source of wavelength λ_1. Terminal *B* will then create the return path to terminal *A* using the same physical path but modulating the information onto the light source of wavelength λ_2.

A good application of a directional coupler is a protection switch. In this environment, the only time the switch will need to be reconfigured is when a failure occurs in an existing path. Thus, high bit rates can be passed through the switch with moderate reconfiguration rate requirements. This application matches the capabilities of the directional coupler.

b) Signal Formats: As high bit rate transmission systems are being developed, there is pressure to build switching systems that will switch these complex signals. Transmission systems are designed such that the high bit-rate signal only passes through a few elements as it is
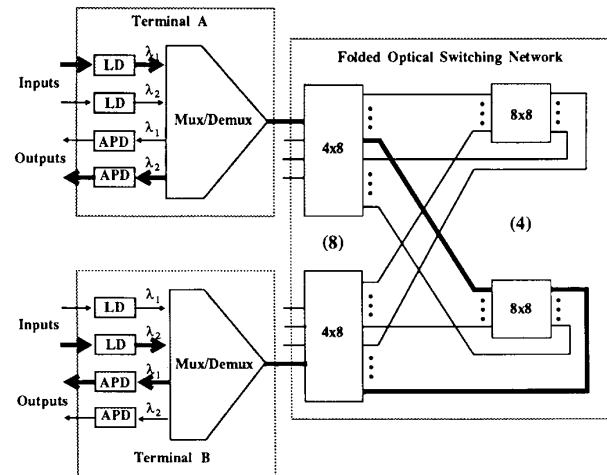

Fig. 8. 32 line optical space switch [30].

generated or processed. These few elements allow all the controlling electronics to be placed close together. In a switching system, the signal must pass through a large number of switching elements which are normally spread over a large physical space; this makes switching difficult at high bit-rates. As bit-rates continue to increase, there will need to be a compromise between the complexity of transmission and the switching systems [31]. One solution to this problem is to change the signal format from a bit-multiplexed to a block-multiplexed format. By changing this format, transmission systems will become more complex because buffers will be required at all the inputs to the multiplexers. Such a new format will simplify switching systems by allowing them to operate directly on the information rather than having to demultiplex the information and then switch the lower bit-rate signals. An example of such a proposed format is SYNTRAN [32]. The concept of this block-multiplexed format is good for future photonic applications but the DS3 bit rate (45 Mbits/s) it proposes is too slow for the photonic domain. These slower bit rates can be handled easily in the electronic domain. This concept does have merit if it is extended to higher bit rates by using individual 125 μs frames of the 45 Mbit/s DS3 information as the basic block of data for the system. As an example, in the FT series G transmission systems, a single 125 μs frame of the 1.7 Gbit/s data stream contains 36 frames of DS3 information. The bits in these frames, plus overhead bits, are interleaved and mixed so that individual DS3 frames cannot be extracted from the stream unless that stream is at least partially demultiplexed down to DS3 channels. By requiring that the DS3 frames be block multiplexed onto the high-speed channel with a small gap between them, individual extraction and insertion of DS3 frames should be possible. The characteristics of a directional coupler (slow reconfiguration rates, but high signal bit rates) make it an ideal device to be used with a block-multiplexed format.
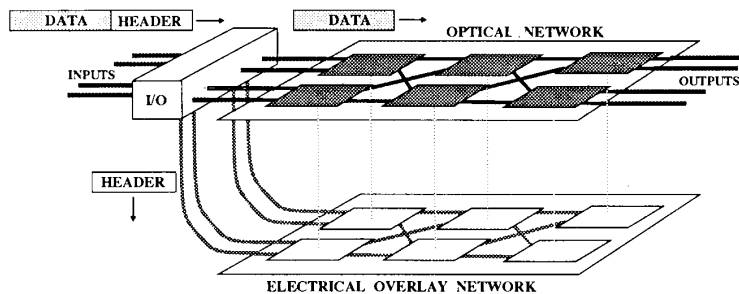
c) Time-Multiplexed Switching: As the bit rates

Fig. 9. Directional coupler-based packet switching system [63].

passing through these photonic switches increase, there approaches a point where no single information source can occupy all the bandwidth without some type of time-division multiplexing. As an example, uncompressed digital NTSC television signals require approximately 100 Mbits/s while digital high-definition television will be about 600 Mbits/s. Thus, if the transmission system operates at 1.7 Gbits/s then at least 16 NTSC channels or two high-definition channels can be time-multiplexed together. To build such a system will require a time-slot interchanger, and an elastic store. The elastic store will also be required to remove both frequency and phase jitter from the system inputs. Proposed elastic stores and time-slot interchangers have been demonstrated using fiber delay lines as the memory [33] or bistable laser diodes as bit memories [26].

d) Packet Switching Systems: The problem in implementing a packet switching system based on directional couplers is that a header has to be read to determine the final destination of the packet. This can be done by stripping off a portion of the optical energy and monitoring the header (trailer) electronically [63] as illustrated in Fig. 9. If necessary, the header (trailer) could be at a lower bit rate than the packet data thus allowing the slower electronics to respond to the controlling information. If the header bit rate is at the same bit rate as the data, then the eventual bit-rate upper limit would be governed by the speed of the electronics. It would be possible to have headers encoded at slower bit rates than the data at the cost of reducing the total throughput of the switching system. The cost for such a system is the large amount of electronics that is surrounding the small number of photonic devices. Thus, to be economically justifiable, large packet lengths are required.

IV. OPTICAL LOGIC SYSTEMS

There are certain applications that are not well suited for relational devices. One such application requires the ability to both sense and respond to individual bits of information. A packet switch is a good example of this requirement. A packet entering a network requires a system of devices that can read and understand the header and then reconfigure the network to allow the packet to pass to its desired destination. The ability to interact and sense

the individual bits in a stream of information is one of the strengths of optical logic devices [34].

To make a useful system, these devices need to be interconnected, as in current electronic switching systems, to create a large interconnection network. The purpose of the following sections is to discuss several of the optical logic devices that have been fabricated in addition to describing two methods of optically interconnecting these devices. The section on optical logic systems will begin by discussing several optical logic devices. Next, two possible methods of optically interconnecting 2-D arrays of logic devices will be discussed. Finally, there will be a brief discussion of a packet switching system that could be based on these devices.

A. Digital Optical Logic Devices

Digital optical logic devices can be further classified according to the effective number of ports, where a port is either a physical input or output. The discussion on optical logic devices will begin by reviewing several two-port devices and the constraints they impose upon a switching system architecture. Multiport devices and their associated system issues will then be discussed.

1) Two-Port Devices: Two-port devices can be divided into two different types. The first, which will be referred to as combinatorial, are devices whose output is a function of present inputs. These devices include any device that simulates a Boolean logic function. The characteristic curves of these devices are shown in Fig. 10. Part (a) illustrates the characteristic curve of an inverter. Normally, there is a bias beam, separate from the signal beam, which provides the optical energy to be modulated by the device. When the energy from the signal beam is added to the energy of the bias beam, this combined energy is enough to exceed the nonlinear threshold of the device. As the device changes states, the output level goes from a high value or a ''one'' to the lower value which is equated to a ''zero.'' By reducing the energy in the bias beam and adding more signal beam energy through the use of multiple signal beams, an optical NOR gate can be formed. Part (b) is the characteristic curve of a thresholding optical amplifier. By reducing the bias beam and adding more inputs, this device could be an optical AND gate.

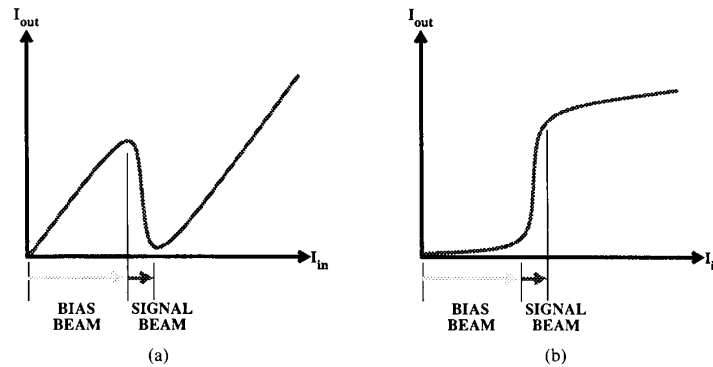The second type of device is sequential in nature. These

Fig. 10. Characteristics curves of two-port combinational devices.

devices could be smart pixels with one optical input, one optical output, and some high-speed electronics configured as a sequential finite state machine. Perhaps the simplest example of these structures is a bistable device [35]. Since these devices have memory, their outputs are a function of the present inputs and their present state (previous inputs). Another example of this type of two-port device is an optical regenerator. When an optical signal enters the device, the information is both amplified and retimed prior to outputting the reconstructed signal.

   a) Proposed Devices: There are two optical logic devices that have received a considerable amount of attention in the past few years. The first of these devices, the self-electrooptic effect device (SEED)[36], is an electrooptical device that requires both optical and electrical energy. The second device, referred to as a nonlinear Fabry–Perot etalon (NLFP) is an all-optical device [34] in that all the energy required to switch the device is supplied optically. Both of these devices can be fabricated into 2-D arrays of devices that are both optically enabled and controlled. The purpose of the 2-D arrays is to provide the opportunity to exploit the parallelism present in the optical domain.

   A functional diagram of the SEED is shown in Fig. 11. A p-i-n diode with a multiple quantum well (MQW) material in the intrinsic region is connected in series with a resistor to form the SEED structure. The characteristic curve for the device is shown in part (a) of Fig. 10. A bias beam is required to provide the energy that will be modulated by the signal beam. This modulation of the energy source by the signal beam provides the differential gain that is required in a digital logic system. With low signal beam intensities, the SEED is virtually transparent. This allows nearly all the energy present in the bias beam to pass through the device to become the output beam. When the signal beam is added with the bias beam, the combined energy is enough to force the SEED structure to become an absorber, thus reducing the total amount of energy in the output beam. This characteristic curve is equivalent to the characteristic curve of an optical NOR gate. SEED structures have been integrated into two-dimensional arrays [36]. It is conceivable that within 10
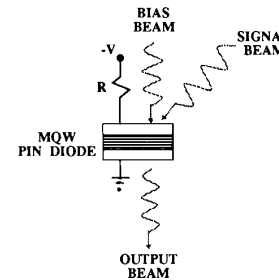

Fig. 11. The self-electrooptic effect device.

years, arrays of 10 000–100 000 individual SEED's per square centimeter will be possible. Currently, 4 fJ/μm^2 of optical energy and 16 fJ/μm^2 of electrical energy are required to change the state of the SEED.

   A second possible device for the optical logic domain is a nonlinear Fabry–Perot etalon (NLFP). This device exploits reflection instead of absorption to control or modulate a bias beam. This is shown in Fig. 12. Part (a) of this figure illustrates that without a signal beam, the bias beam passes through the NLFP. With an incident signal beam, part (b) of the figure, the NLFP changes states which forces the bias beam to be reflected instead of transmitted. This device, like the previously described SEED, is operating as a NOR gate. The NLFP can also be designed such that it can operate as an AND, OR, NAND, or XOR gate [34]. These devices, like SEED's, can also be integrated into large arrays [37]. The optical switching energy for NLFP's has been measured to be less than 40 fJ/μm^2 [38] with achieved switching times less than 100 ps [39].

   At the current time, there are two types of NLFP etalon structures being studied. The first is based on a thermal nonlinearity which makes it slow, on the order of microseconds [34]. The hope for these devices is that large arrays can be fabricated to exploit the strength of parallelism. The other type of device, referred to as an optical logic etalon (OLE) is a pulsed device that requires two separate wavelengths, one for the bias and one for the signal [40]. The pulsed operation is illustrated in Fig. 13. The two inputs, the data and clock, are separated in both
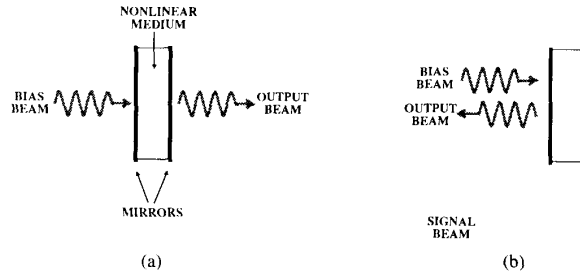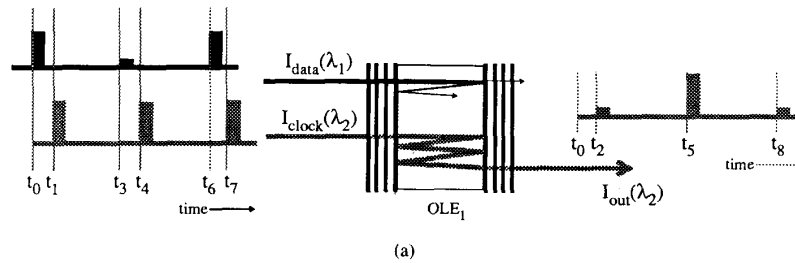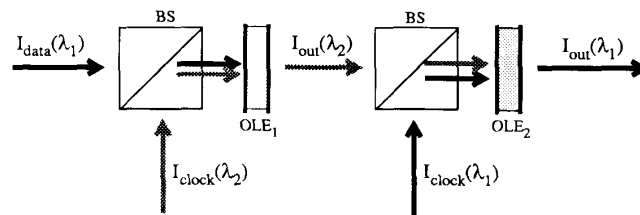
Fig. 12. The nonlinear Fabry-Perot etalon optical gate.

(a)

(b)

Fig. 13. OLE operation. (a) Input and output signals for OLE operation.
(b) Complementary pair of OLE's.

time and wavelength. The input data $I_{data}(\lambda_1)$ is incident on the OLE a short period of time prior to the clock input $I_{clock}(\lambda_2)$. In part (a) of the figure, $I_{data}(\lambda_1)$ is incident upon the device at t_0 while $I_{clock}(\lambda_2)$ arrives at t_1. Ideally, $I_{data}(\lambda_1)$ is chosen such that λ_1 corresponds to an absorption peak of the nonlinear material in the OLE, bulk GaAs. Thus, nearly all of the energy associated with the incoming data is absorbed by the material. This absorbed energy alters the effective index of refraction in the GaAs intercavity material [41]. This change in the index of refraction shifts the resonant peak of the Fabry-Perot etalon by changing the optical path length of the cavity. Through the proper choice of initial detuning, several potential optical logic gates can be implemented. In this figure, the initial detuning was set so that the OLE would behave like an optical NOR gate. If the material relaxation time of the intercavity material is long compared to the pulse duration, the state of the device will not change significantly prior to the arrival of the clock pulse $I_{clock}(\lambda_2)$. When the clock arrives, the OLE will be in either a transmissive or reflective state depending on the value of $I_{data}(\lambda_1)$. In this figure, if there was a logical "one" on the data input,

then the OLE would be reflective forcing the output to be a logical "zero." On the other hand, if the input data was a logical "zero," the device would be transmissive allowing the majority of the clock energy through the OLE creating a logical "one" output. Since λ_2 is not near the absorptive peak of the intercavity material, clock signals much larger than the data signals can provide an effective gain through the device. This separation of the data and clock inputs in either time or wavelength has converted a two-port device into an effective three-port device.

Part (b) of this figures shows what is required to integrate these devices into larger systems. Because the input wavelength of an OLE is different from the output wavelength, the devices are not cascadable. Therefore, to implement any type of system will require a complementary device that will change the output wavelength of the two devices back to the original input wavelength. This part of the figure shows how, through the use of polarization beamsplitters, the two devices can be interconnected. Unfortunately, at the current time a complementary pair has not been demonstrated.

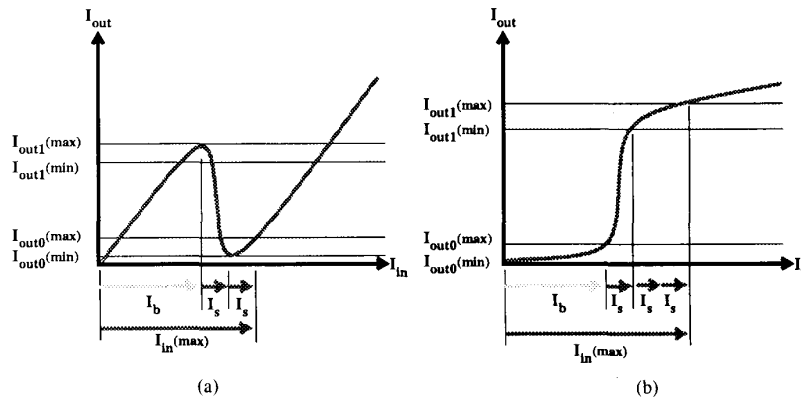 *b) System Considerations:* When any of the two-port

Fig. 14. Input/output levels of critically biased two-port devices.

devices operate with a bias beam as shown in Fig. 14, there are strict requirements on the bias beam's stability [42]-[44]. If the bias beam varies in intensity, it could spontaneously exceed the nonlinear threshold forcing the device to change states. Also, if the intensity of the bias beam decreases significantly, it could prevent the device from changing states when a signal beam is incident upon it. In addition to the bias beam, the point of nonlinearity in the characteristic curve must also remain constant. This required stability puts tight restrictions on thermal control for most devices. As an example, for any structure using a Fabry–Perot cavity, temperature variations will cause changes in the location of the resonant peaks of the cavity. This in turn alters the initial detuning of the device which can alter the characteristic curve of the device. Such variation could cause erroneous device behavior. Also, any device that is based on a material resonance could also suffer detrimental effects with temperature variations.

Another problem associated with the critically biased devices that have been previously described is the size of the fan-in and fan-out of the device. The fan-in is the maximum number of inputs (signal, not clock beams) that can be used as inputs to a given device and can be represented, as shown in Fig. 14, by fan-in = $(I_{in}(\max) - I_b)/I_s$. The fan-out, which is the maximum number of input signals that an output signal can be decomposed into, is represented by fan-out = $(I_{out1}(\min) - I_{out0}(\max))/I_s$. These two equations imply that for a large fan-out and fan-in, which is desirable, a large sharp nonlinearity is required. The problem with a sharp nonlinearity is the strict requirement on the stability of the bias beam. Because of these stability requirements, it is unlikely that for critically biased devices, fan-out greater than five will be practical.

Another area of concern with respect to fan-in occurs when the light in a system has a large coherence length and a single polarization. In this situation, both constructive and destructive interference could occur when two or more beams are incident on the same physical input. As the devices become smaller, which will be required to re-

duce the switching energy, it will be possible for this interference to prevent a device from operating properly. To avoid this problem, the fan-in could be limited to two inputs with each input being associated with a different polarization. Another alternative is to separate all inputs in time as in the case of the OLE.

2) Multiport Devices: The devices discussed so far can be classified as two-port devices in that they have one input and one output. By adding more inputs and outputs, many of the problems associated with two-port devices can be removed. As an example, by adding more physical input ports, the problem of low device fan-in can be resolved even though the fan-in per port is small (the desired fan-in per port is two, one for each polarization). Also, the effects of critical biasing can be removed by separating the signal input from the bias input thus creating a three-port device.

a) Proposed Devices: There are several devices that have been proposed that could be classified as "multiport devices." The first device to be discussed will be a three-port device in which the signal input is separated from the bias input. The second device is a four-port device referred to as the *symmetric SEED.* This device consists of two electrically interconnected MQW p-i-n diodes. Finally, a five-port device that performs an exchange–by-pass operation will be discussed.

An example of a three-port device is shown in Fig. 15 [45]. In this figure, an MQW modulator is electrically connected to a phototransistor [46]. The objective of this device is twofold: 1) increased sensitivity for the input signal (optical gain) and 2) isolation between the input and output signal. With an input signal present on the phototransistor, a photocurrent is created which is roughly proportional to the input signal power. The optical bias beam also gives rise to a photocurrent through the modulator which is proportional to the power absorbed. These two currents must be equal or a charge will build up on the modulator affecting the absorption such that the two currents will equalize. If the operating wavelength is set just below the band edge, then with no input signal, the majority of the voltage will be dropped across the pho-
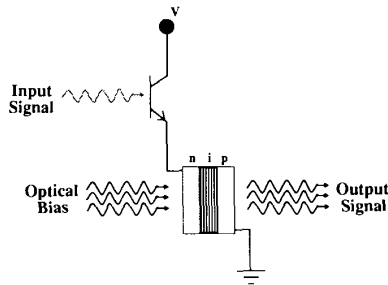
Fig. 15. Photonic three-port device.

totransistor which puts the modulator in the transmissive state. When an input signal is present, the phototransistor will turn on putting the majority of the voltage across the modulator. With this applied voltage, the band edge of the MQW material will shift, putting the modulator in the absorptive state. Thus, a lower power input signal has the capability of modulating the higher power optical source providing gain. The modulation effect provides both gain between the input and output signal and a logical inversion of the input data. A noninverting three-port device has also been demonstrated [47].

The symmetric SEED (S-SEED) is a four-port device with two inputs and two outputs as shown in part (a) of Fig. 16 [48]. This device is the result of electrically interconnecting two MQW p-i-n diodes in series. When the diodes are connected in this fashion, they become complementary, in that, when one of the diodes is "on" the other will be "off." Thus, one of the diodes will be in the absorbing state while the other is in the transmissive state. This is illustrated in the characteristic curves shown in parts (b) and (c). Perhaps the greatest strength of these devices is that changing states is a function of the *ratio* of the two input powers and not the function of the absolute intensity of the input beams. This can be seen in the characteristic curves of part (b) and (c). The optically bistable loop is centered around the point where the two inputs, P_{in1} and P_{in2}, are equal. From these figures, it can be seen that the device will remain in its current state until that ratio exceeds 1.3 or is less than 0.7. The importance of this is that the allowable noise on the signal inputs can be much greater than for the case of a critically biased device such as a SEED.

The S-SEED can be configured such that it can operate as an *S-R* latch. This is illustrated in Fig. 17. In part (a) of this figure, the inputs are separated into an S (set) input, and R (reset) input, and a clock input, where the clock has approximately the same intensity for both inputs. The S and R inputs are also separated in time from the clock inputs as shown in part (b) of this figure. Note that this clocking scheme is similar to that used by the OLE. The S or R inputs are used to set the state of the device. When the S input is illuminated, the S-SEED will enter a state where the upper MQW p-i-n diode will be transmissive while the lower diode will be absorptive. When the R input occurs, the opposite condition will occur. Since the

energy required to change the state of the devices is a function of the ratio of the S and R inputs, then when only one of those two inputs occurs, low switching intensities should be able to change the device's state. After the device has been put in its proper state, the clock beams are incident on both inputs. Since the two clock beams are roughly equivalent, the ratio between the incident beams should be close to one which will prevent the device from changing states. This higher energy clock pulse will be used to transmit the state of the device to the next stage of the system. Since the S or R inputs are low-intensity pulses and the clock is a high-intensity pulse, a large differential gain may be achieved.

Another example of a multiport device is an exchange–bypass node that has been proposed by Midwinter [49]. This device tries to capitalize on the advanced device fabrication and large scale integration capabilities of the electronic domain and the effective large number of pin-outs possible in the optical domain. Each bypass–exchange node is composed of three optical inputs, one electrical input (it could be optical), and two optical outputs as shown in Fig. 18. The optical inputs and outputs are to be implemented using MQW p-i-n diodes. By sensing the current, these diodes are detectors, while applying a time-varying voltage allows them to modulate light incident upon them. All of the processing on the data is done in the electrical domain. Since all of the interconnections are local, high-speed operation should be possible. The device is a logic device implementation of the directional coupler. If I_c is a logical "one" and the clock is a logical "one," then the inputs I_a and I_b will effectively *bypass* the node being directed to outputs O_a and O_b. On the other hand, if I_c is a logical "zero," then the node will *exchange* the inputs sending I_a to O_b and I_b to O_a with an asserted clock signal. Note that one of the main advantages of this device over a directional coupler is that there is gain and the thresholding nonlinearity of optical logic gates which will reduce the signal-to-noise requirements of the nodes. Eventually, large numbers of these nodes or "smart pixels" can be integrated into two-dimensional arrays to take advantage of the large pin-out capability available in the optical domain. Another example of a multiport device is the 4 × 4 OEIC switch implemented by Iwama *et al.* [50]. This device, or collection of devices, is composed of an array of optical detectors that receive the optical information. This array is then electrically connected to an electrical GaAs 4 × 4 switch. The output of this switch then drives four laser diodes that have been integrated onto a single substrate. This device has operated at 560 Mbits/s.

When integrating large numbers of these multiport devices into arrays, thermal problems could eventually limit their maximum size. This limitation occurs because both the electrical and optical devices dissipate power, and as the bit rates increase so does the required power.

3) Device Capabilities: In Fig. 19, the two strengths of photonics, bandwidth (data capacity) and parallelism (connectivity), are each assigned to an axis of a graph.
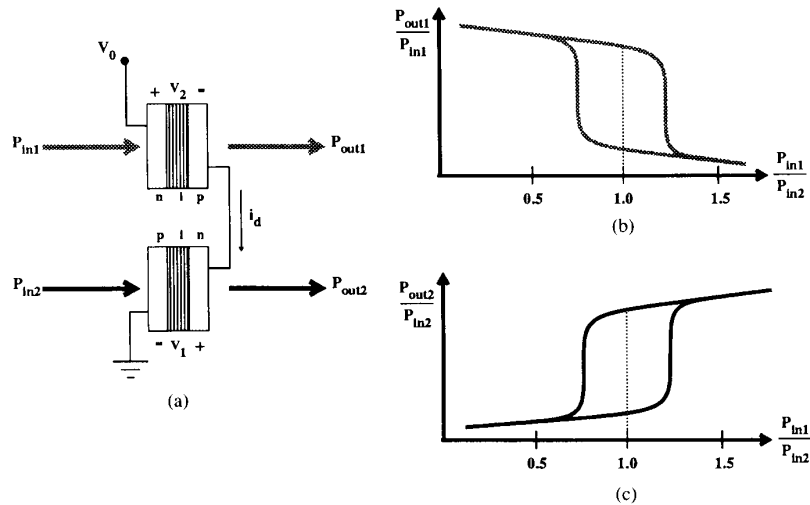
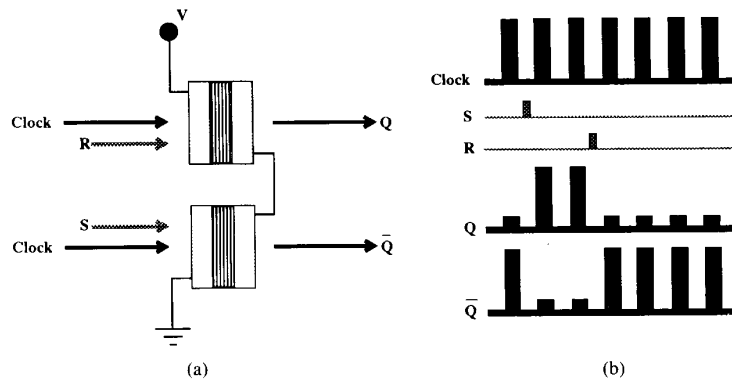Fig. 16. Symmetric SEED operating characteristics.

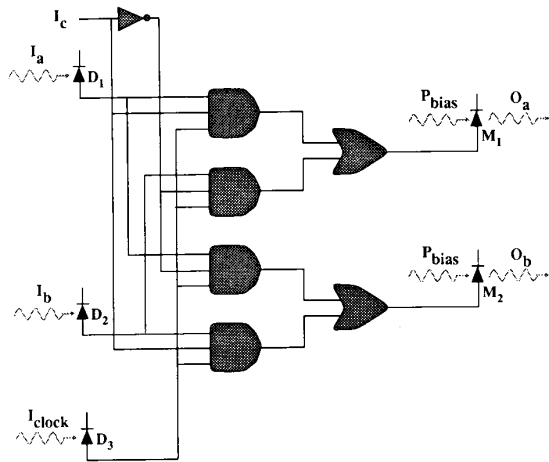Fig. 17. Symmetric SEED as an S-R latch.

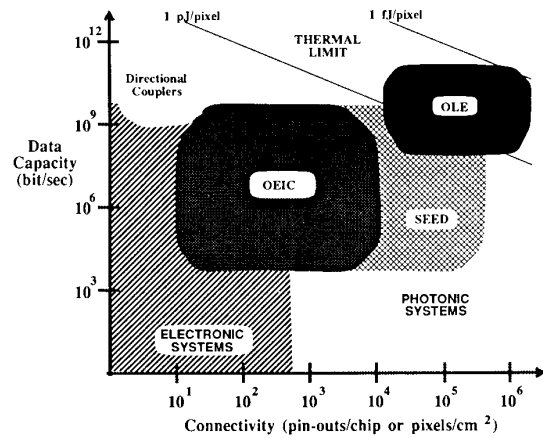Fig. 18. Exchange-bypass smart pixel.

Fig. 19. Photonic device capabilities.

The ordinate, which is the bandwidth component, is labeled as data capacity and has the units of bits per second. The abscissa represents parallelism and is listed as connectivity with the units of either pin-outs per chip or pixels per square centimeter. The capabilities of current electronic systems are located in the lower left hand corner of the graph. The upper limit of electronic systems data capacity is approximately 10 Gbits/s with the maximum number of pin-outs of approximately 500. For the direc-

tional coupler, which is a relational device, the upper data capacity limit is in excess of 100 Gbits/s while the number of pin-outs is less than 100. Pin-outs in this case refers to the number of optical fiber inputs and outputs that can be connected to a single LiNbO₃ substrate. The lower boundary on the area designated for directional couplers was chosen at a data capacity of approximately 1 Gbit/s where high-speed electronics has been successfully demonstrated. Optoelectronic integrated circuits (OEIC) are devices that combine both the optical and electronic domains; thus, the data capacity limit will be the same as for the electronic domain while the connectivity can approach an effective pin-outs/chip of 10^4. A good example of an OEIC is a smart pixel. The lower boundary was chosen at a data capacity of 64 kbits/s (a single digital voice channel requires 64 kbits/s). The left boundary was chosen to be approximately 10. This boundary includes the possibility of simple linear arrays of optoelectronic regenerators. The self-electrooptic effect device (SEED) is a specific example of a simple OEIC which has the potential for a large number of pin-outs/chip. Finally, the optical logic etalon (OLE) is an all-optical device that has the potential of fabricating pixels (optical NOR gates) with diameters on the order of 1 μm. This small device size could potentially allow more than 10^6 pixels per cm² to be fabricated. The left boundary was set in excess of 10^4 pixels since OLE devices need to be small to maintain low switching energies. The lower bound on data capacity was chosen in the Gbits/s region to accommodate the pulsed mode of operation although this boundary could extend to the 64 kbit/s level.

The thermal limit region of this figure illustrates the maximum energy required to change the state of each pixel to maintain thermal stability. This is based on the assumption that 100 W/cm² can be removed from an array of devices for continuous operation. As an example, if an array of NLFP's with a pixel density of 10^6/cm² is to have the capability of handling 10^{12} bits per second, it would require the switching energy of the pixels to be less than 1 fJ. For the case of OEIC's, this implies that the combination of electrical and optical energy required to change the state of the pixel be less than the thermal limit.

B. Device-to-Device Interconnection

Once two-dimensional arrays of optical logic gates are available, it will become necessary to interconnect the individual devices on the arrays. This interconnection, which can be thought of as the photonic wires of the network, can be accomplished through the use of either space-variant or space-invariant interconnects. A space-variant network has the property that each input into the network can be redirected (connected) to any or all of the outputs and is dependent on its spatial location. This type of interconnect provides a different interconnection pattern for each spatially separated input. Alternatively, a space-invariant network can interconnect an input to any or all of the outputs, but is independent of its spatial location. These interconnects provide a single pattern for

all inputs regardless of their spatial location. This spatial independence implies that the output pattern created by the inputs will be the same only shifted in space. These concepts are illustrated in Fig. 20. In part (a) the space-variant interconnect shows how the optical energy from two spatially separated inputs impinging upon the interconnection network redistribute the energy differently creating different input/output connection patterns. In part (b), the energy from the two inputs is redistributed in the same manner only shifted in spatial dimensions.

The following sections will begin by discussing free-space interconnection networks based on bulk optics and then outline some of the constraints of holographic interconnection networks.

1) Bulk Optics: The first type of free-space interconnection network can be implemented with bulk optics (lenses, prisms, mirrors, etc.). The simplest example of this type of an interconnection network is an optical imaging system composed of conventional lenses (see Fig. 2). Such a system is space-invariant and can be used to transfer the information present on the outputs of one array to the inputs of a second (or the same) array, effectively creating a large pin-out capability. As an example, the minimum resolvable spot size of a lensing system is given by $a = 1.22 \lambda (f/\#)$ where a is the diameter of the minimum resolvable spot size, λ is the wavelength of the light, and $f/\#$ is the f number of the lens (f/D where $f =$ focal length, $D =$ clear aperature of lens). This implies that for a lens system with $f/\# = 8$ and $\lambda = 850$ nm, the minimum resolvable spot size is 8.3 μm. Assuming that the image to be supported by the lens system is square, the SBWP is given by $(F/a)^2$ where F is the size of the unabberated field in one direction. From our previous example, if $F = 1$ cm then the SBWP = 1.45×10^6 pixels or pin-outs. In order to maximize the SBWP of a lens system, the $f/\#$ must be kept small.

Another type of interconnect that is used in several types of multistage networks is the perfect shuffle, [51]–[53]. An example of a perfect shuffle interconnect that can be implemented with bulk optics is shown in Fig. 21 [54]. Part (a) of this figure illustrates the permutation performed by a perfect shuffle network. Part (b) shows how an optical perfect shuffle can be implemented with a beamsplitter, a lens, and two mirrors. Each of the inputs passed through the beamsplitter where their power is divided and directed to mirrors M_1 and M_2. The optical beams incident on M_2 will be shifted upward, pass again through the beamsplitter, and on to the lens where a spatial magnification of the row of inputs takes place. Thus, the lower four rays of information (5–8) will be shifted and magnified imaged onto the pixels associated with the output plane. On the other hand, the light rays reflecting from M_1 will be shifted downward and then magnified. The top four rays (1–4) controlled by M_1 will then be shuffled between the rays imaged by M_2. In this way, the process of perfect shuffling is accomplished by splitting, shifting, and then magnifying the rows of inputs. It should also be pointed out that there are other methods of creat-
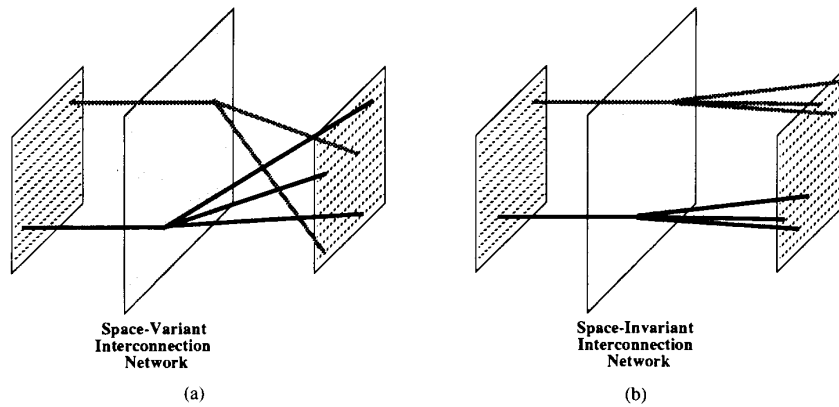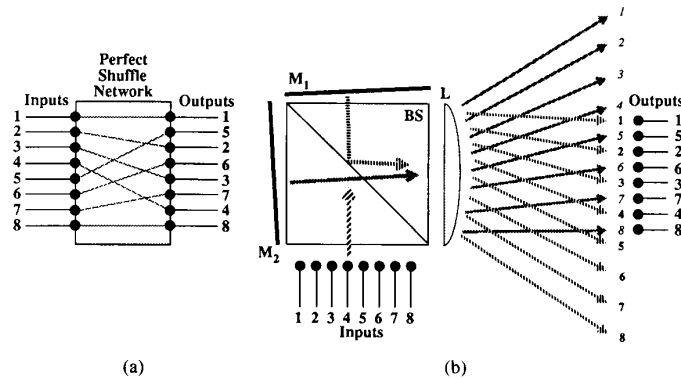
Fig. 20. Space-variant versus space-invariant networks.

Fig. 21. Optical perfect shuffle [55].

ing a perfect shuffle interconnect using bulk optics [55], [56].

2) Holography: A hologram is a mechanism that can be used to modify and redirect a light wave that is incident upon it [57]. Because of this capability, a hologram or collection of holograms can be thought of as the photonic wires interconnecting optical logic gates [58]. An example of a holographic interconnection network is illustrated in Fig. 22. In this figure, the optical output of a logic device (point *a*) will be directed by mirror M_1 to the hologram (point *b*) which will redirect the light via M_2 to one or more other logic devices (points *c*, *d*, and *e*). This redistributed light will be used as the signal beams for the devices they are incident upon. The hologram located at point *b* could be either space-variant or space-invariant.

There is a price to pay for the flexibility of space-variant connections in terms of the SBWP. Assuming that each of the N^2 subholograms has the capability of addressing any or all of the N^2 pixels of the next stage, this implies a required SBWP $\propto N^4$ [59]. If a computer-generated hologram (CGH) is to be used as the optical interconnect, its SBWP will be determined by dividing the maximum size of the hologram by the minimum feature size and then squaring the result. As an example, for a Fourier hologram, if the minimum linewidth of an elec-
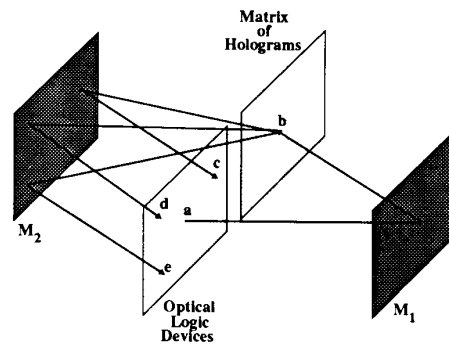

Fig. 22. Holographic interconnection network.

tron-beam system is 0.5 μm and with a maximum hologram size of 10 cm on each side, the maximum SBWP = 4×10^{10}. This implies that the theoretical maximum value of N for a space-variant network must be less than 450. This is the maximum value and for practical systems, N will have to be much smaller than this [59].

For the case of a space-invariant hologram, each point on the hologram should be able to redirect incoming light to all N^2 pixels of the next array and since all the pixels perform the same operation then the SBWP $\propto N^2$. Thus,

for space-invariant CGH with the available SBWP of 4×10^{10}, a maximum value of $N \ll 200\ 000$ is possible.

A third approach is a hybrid interconnection scheme in which the space-variance requirement is relaxed in an attempt to increase N. If there are N^2 subholograms, each of which can redirect incoming light to $M^2 \ll N^2$ pixels of the next array, then the SBWP $\propto (MN)^2$. Note that M^2 is the effective fan-out of the energy incident on the subhologram. If $M = 3$ (fan-out = 9) the CGH will have $N \ll (4 \times 10^{10}/M^2)^{1/2} = 65\ 000$. For networks that require a large N either a space-invariant or a hybrid interconnect will be required.

At the current time, most of the work on holographic interconnects has been theoretical and has yet to be engineered to the point of being practical.

C. Potential Applications of Optical Logic Devices

There are many applications that require the capability of sensing and reacting to each and every bit that passes through the system. As an example, packet switching systems require the ability to sense the information present in the headers and then provide the appropriate network routing. One type of control strategy used for packet systems is to sort the input packets by their destination addresses [51], [60].

This is illustrated by the Batcher bitonic sorting network shown in Fig. 23. In this figure, the entering packets, represented by their destination address, encounter the first rank of nodes. When a node has an up arrow, it means that the largest of the two destination addresses will be directed to the upper output. The lower address will then be directed to the lower output. On the other hand, when the arrow is pointing down, the larger (smaller) address will be directed to the lower (upper) output. After each node determines whether it will provide the exchange or bypass function, the incident packet information will be directed to the appropriate output port. The Batcher network begins with adjacent pairs of input lines, entering the first rank, being ordered in either ascending or descending order depending on the configuration of the node. The upper half (lower half) of rank 1 will be interconnected to the upper half (lower half) of rank 2 through a four-element perfect shuffle network. Rank 2 will then sort the upper half (lower half) of its inputs creating an ascending (descending) sequence which is directed through an eight-element perfect shuffle to rank 3. Finally, rank 3 will sort its interleaved ascending and descending four-element sequences into an ascending eight-element sequence which corresponds to sorting the inputs according to their destination address. As an example, the path corresponding to the output destination address 4 has been highlighted in the figure. Thus, for this type of switching network each node will be required to have a modest amount of intelligence. These nodes must be able to read a packet header, and then reconfigure the node so that the entering packet is directed to the proper output channel. The topology of the Batcher bitonic sort-

ing network can be rearranged such that all the interconnects use the same size of perfect shuffle [51]. An example of this is shown in Fig. 24. This adds more space-invariance to the system, thus reducing the overall required SBWP.

An example of a packet switching system based on sorting networks that could eventually be implemented using optical logic and interconnects is the STARLITE wideband digital switch [61]. The basic architecture of this switch is shown in Fig. 25. The STARLITE switch is a self-routing, nonblocking, constant latency packet switch that has the capability of handling gigabit data rates [62]. The concentrator directs the active inputs, which are much less than the total system inputs, to the sort-to-copy subnetwork. The sort-to-copy and copy subnetworks provide the broadcast capability for this switching system. The output of the copy subnetwork is then sorted according to destination. The expander then redirects the data to its final destination. Each of these basic functions (concentrator, sort-to-copy, copy, etc.) can be decomposed into some type of shuffle network that interconnects 2×2 switching nodes.

It is important to understand that optical logic devices and their associated systems are not at the point of development at this time. The devices that have been discussed are research prototypes that are not ready to be manufactured.

D. Applications of Smart Pixel Devices

Smart pixels are devices that attempt to take advantage of the strengths of both the optical and electrical domain. The strength of the electrical domain is that electrons interact easily which allows an electronic signal to control another electronic signal. Conversely, the strength of the optical domain is that photons do not interact with each other which creates an ideal communications environment. Once a collection of photons are encoded with information, they travel directly to their destination without interacting with other photons. The cost of this communications capability is that photons have a difficult time controlling other photons. Combining these two strengths, in that the electronics will be responsible for the processing of information while the photonics will handle the communications between processing elements, two-dimensional processing based on smart pixels should offer some performance advantage.

An example of such a system has been proposed by Midwinter [49]. This system is illustrated in Fig. 26. For this system, the input data enters as a row of information where each element is a single serial channel. This row of information enters the top row of smart pixels which are multiport devices that functionally behave like exchange–bypass modules. They have the capability of comparing packet addresses and directing the incident packets to the appropriate outputs. After processing, the information from the top row is directed via mirror M_1 to the perfect shuffle optics. Following the perfect shuffle operation, the data are directed by mirrors M_2, M_3, and
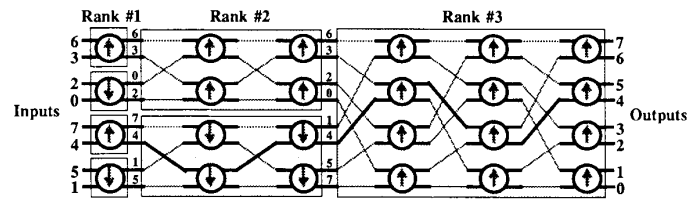
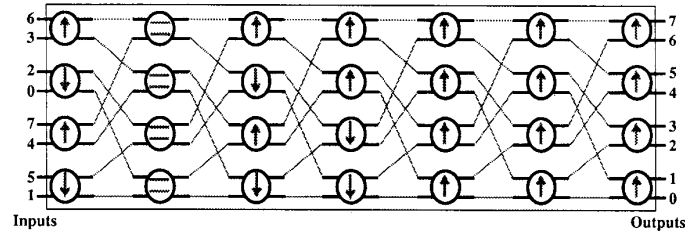Fig. 23. A Batcher bitonic sorting network [52].

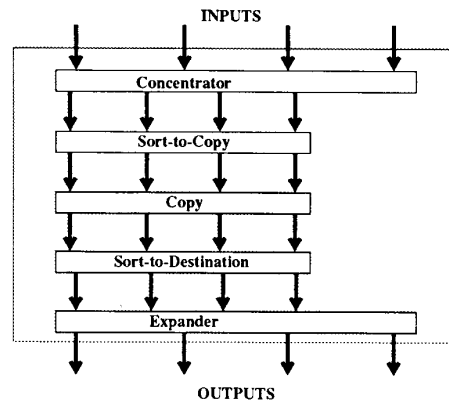
Fig. 24. Sorting network using perfect shuffles.

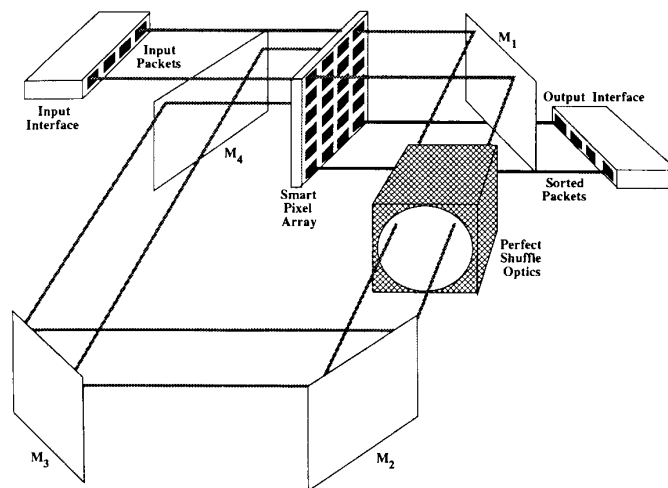Fig. 25. STARLITE wide-band digital switch.

Fig. 26. Photonic sorting network.

M_4 to the second row of the smart pixel array. This looping procedure continues until the information has passed through all rows of the smart pixel array. At this point, the sorted information will be directed to the output interface.

V. CONCLUSIONS

This paper has reviewed some of the possible photonic technologies that could become important components of future telecommunications systems. It began by dividing photonic devices and systems into two classes according to the function they perform. The first class, relational, was associated with devices which under external control mapped the input channels to the output channels. The second class, logic, required that the devices perform some type of Boolean logic function. After the classes were defined, the strengths and weaknesses of the photonic domain were shown to be bandwidth and parallelism. Relational devices and their applications were then discussed. It was pointed out that the directional coupler holds the most promise for near-term development. Optical logic devices and systems were then presented. The systems that were outlined were based on SEED, NLFP, or smart pixel devices with either holograms or bulk optics serving as the optical interconnects.

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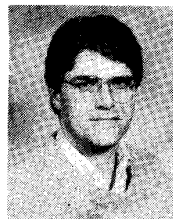
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