# An Optical Backplane Demonstrator System Based on FET-SEED Smart Pixel Arrays and Diffractive Lenslet Arrays

D. V. Plant, B. Robertson, H. S. Hinton, W. M. Robertson, G. C. Boisset, N. H. Kim, Y. S. Liu, M. R. Otazo, D. R. Rolston, and A. Z. Shang

*Abstract*— **We have demonstrated a representative portion of an optical backplane using FET-SEED smart pixels and free-space optics to interconnect Printed Circuit Boards (PCB's) in a two board, unidirectional link configuration. 4 × 4 arrays of FET-SEED transceivers were designed, fabricated, and packaged at the PCB level. The optical interconnection was constructed using diffractive microoptics, and custom optomechanics. The system was operated in two modes, one showing high data throughput, 100 MBit/sec, and the other demonstrating large connection densities, 2222 channel/cm$^2$.**

## I. Introduction

FUTURE digital systems such as ATM switching systems and massively parallel processing computer systems will have large printed circuit board (PCB) to printed circuit board connectivity requirements to support the large aggregate throughput demands being placed on such systems [1]. Current electronic technology may not be capable of supporting both the connection densities and the bandwidth required due to connector limitations at the PCB to backplane interface [2]. Two-dimensional, free-space optical interconnects represent a potential solution to the needs of these connection-intensive digital systems. When implemented at the PCB-to-PCB level in the form of an optical backplane, this technology is potentially capable of providing greater connectivity at higher data rates than can be supported by current or projected electronic backplanes [3].

An optical backplane can be constructed using two-dimensional arrays of passive, free-space, parallel optical communication channels which optically interconnect PCB's via smart pixels arrays. The smart pixel optoelectronics are two-dimensional device arrays capable of electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion of digital data. In addition to the E/O and O/E conversion, these devices can perform processing operations at the backplane level such as address recognition, or packet routing. By interconnecting PCB's with 10 000 channels/board (10 smart pixel arrays per PCB at 1000 communication channels per smart pixel array), each channel running at 100 Mbits/second will support greater than a TeraBit/sec of aggregate data traffic.

The identification of critical research issues in optical backplanes is being pursued in the form of system demonstrator experiments [4]. This letter describes a system demonstrator based on FET-SEED smart pixels, PCB level optoelectronic packaging, diffractive microoptics, and baseplate optomechanics which demonstrates a simple unidirectional PCB-to-PCB optical interconnection. The letter describes initial operational testing and characterization of the system, and is organized as follows. The FET-SEED smart pixel arrays are presented, followed by a description of the optics and optomechanics used to establish the interconnect. The system performance is described in the two modes of operation, followed by concluding remarks.

## II. FET-SEED Smart Pixel Arrays

4 × 4 arrays of individually addressable FET-SEED transmitters and receivers were fabricated using the batch fabrication process made available through the ARPA COOP and AT&T [5]. The FET-SEED technology monolithically integrates GaAs based field-effect transistors with normal-incidence multiple-quantum-well (MQW) modulators and detectors to form a smart pixel [6]. In both arrays the optical windows were 25 × 25 $\mu$m, separated by 50 $\mu$m, and pitched at 200 $\mu$m. Fig. 1(a) and (b) show schematics of the individual transmitter and receiver circuits respectively. Both circuits are designed to work in a differential mode. In Fig. 1(a), the transmitter circuit operates by electrically modulating the voltage drop across the series MQW diode pair, subsequently modulating the reflectivity of the diodes [7]. The electrical input impedance was designed for 50 Ω to ensure efficient coupling of high frequency, electrical digital data onto the chip, thus ensuring high frequency differential optical operation. The receiver circuit shown in Fig. 1(b) operates by demodulating dual rail optical signals which are detected using a series connected detector-diode pair to form a diode-clamped receiver [8]. The input node to the first FET is charged and discharged as a function of the state of the incident

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D. V. Plant, B. Robertson, G. C. Boisset, N. H. Kim, Y. S. Liu, M. R. Otazo, D. R. Rolston, and A. Z. Shang are with the Department of Electrical Engineering, McGill University, Montreal, PQ H3A 2A7 Canada.

H. S. Hinton is with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309 USA.

W. M. Robertson is with the National Research Council of Canada, Institute for Information Technology, Ottawa, Canada.

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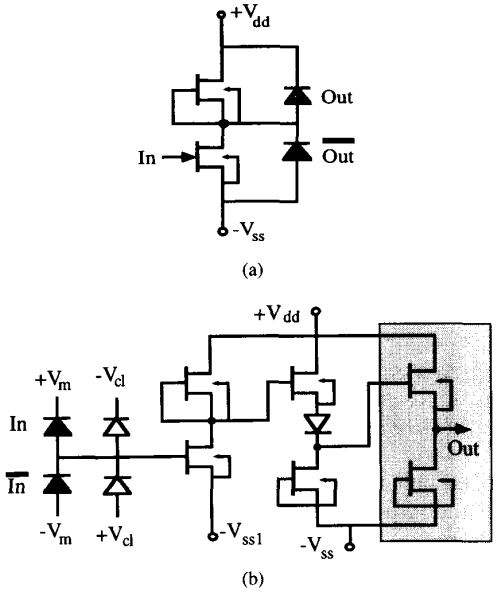


Fig. 1. (a) Transmitter circuit and (b) receiver circuit.

optical power. The demodulated optical signal drives a 3-stage amplifier circuit. The first two stages form an inverting amplifier section and the third stage (shaded) is the power FET (375 $\mu$m wide gates) designed to drive 100 $\Omega$ transmission lines off chip.

The device arrays were packaged in quad flat packs (QFP's) capable of supporting forty, 3-GHz bandwidth signals. The QFP's were subsequently packaged onto the PCB's via solderless, impedance tunable connections. This tunable connection allowed for impedance matching of the device output impedance to the PCB transmission line impedance. Measurements of the rising edges of the PCB level packaged smart pixel transmitter and receiver circuits yielded 0.811 nsec and 2.57 nsec, respectively [9], [10]. A description of the modeling, packaging, and characterization of the FET-SEED transceiver circuits will be the subject of a subsequent paper.

## III. Optics and Optomechanics

Board-to-board optical interconnection was achieved using a two-sided PCB approach. The optics and optomechanics used in the demonstration established optical communication channels using diffractive optics, bulk optics, microlens arrays, and a fiber delivery system for the optical power supply. Microoptic lens arrays, were used to implement the board-to-board relay so as to produce a system that is scalable and to obtain a board spacing that is comparable to current electronic systems [13]. Fig. 2 shows a schematic of the optical system. The optical power was delivered from a 850-nm single frequency, unidirectional Argon ion pumped Ti : Sapphire laser coupled into single mode, polarization maintaining fiber and collimated with a 10 mm focal length lens at the fiber output tip. The system spot array generator consisted of a binary phase grating and a 40.34 mm achromat lens to produce the required 32 spot pattern at the power plane. The efficiency of the binary

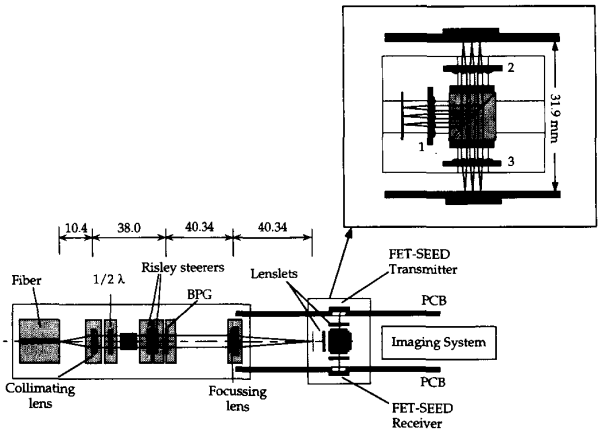


Fig. 2. Optical system layout.

phase grating was measured to be 67%. Fine adjustment of the beam positioning was accomplished using Risley beam steerers packaged with ball bearings for ease of rotation. Using three 6.5 mm focal length, 8 level diffractive microlens, and a 5 mm polarizing beam splitter, two 4F relays, as shown in Fig. 2 insert, were established [11]. The first relay was setup between the power plane and the transmitter array with microlenses one and two, and the second relay with microlenses two and three. The microlenses had a measured throughput efficiency of 90%. The total optical losses of the system were estimated to be 20.7% from the fiber output to the transmitter array, and 70.5% from the transmitter array to the receiver array. The system was typically operated with 0.5 mW/window (1.0 mW watt per channel) on the transmitter array, and an average of 0.35 mW/window on the receiver array.

The optomechanical system was constructed using a slotted magnesium baseplate and pre-aligned optical components mounted into one inch holders. The components were held in place by a stacked magnet/steel bar combination which allowed for tailoring the strength of the retaining force. The PCB's were mounted onto five axis positioning stages secured to the baseplate. The optical system was designed and operated with 10 micron mechanical tolerancing. The system demonstrated excellent long term stability, and remained aligned over several days.

## IV. System Performance

The system was operated in two configurations [12]. Based on the 600 $\mu$m center-to-center spacing of the lenslets arrays, in the first configuration the 4 corners of the transmitter/receiver smart pixel arrays were interconnected optically. Fig. 3 shows the results of transmitting data from board to board over one of these micro-optical channels. In this configuration, each lenslet supported one dual rail optical channel. The system was operated in this configuration at data rates up to 100 MBit/sec on an individual channel. Based on the received optical power, and the bias voltages of the diode clamped receiver circuit, the switching energy was calculated to be 50 femtojoule/bit. To our knowledge, this is the first time

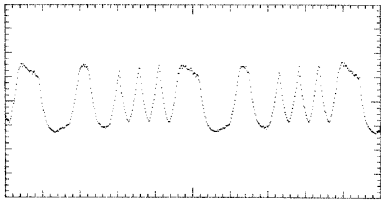


Fig. 3. 16 bit patterns and a PRBS at 50 MBit/sec.

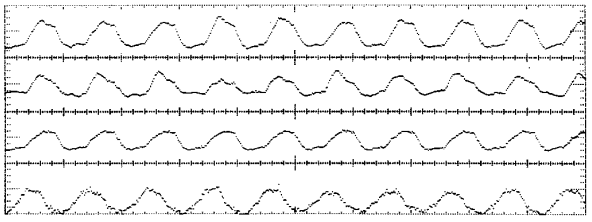


Fig. 4. Cluster pixel output at 25 MBits/sec.

a single lenslet based optical interconnect has been used to support differential optical signals. We detected no significant optical crosstalk in the system.

In the second configuration, a single lenslet (600 $\mu$m in diameter) was used to support four dual rail optical channels, a total of eight optical channels, in a Cluster Pixel configuration. This was possible due to the robustness of the lenslet design. In this optical configuration, we used 2 $\times$ 2 transceiver subarrays. In particular, we interconnected a 2 $\times$ 2 modulator array (center-to-center spacing 200 $\mu$m) in the center of the 16 element array with the center 2 $\times$ 2 sub-array on the receiver chip. Fig. 4 shows a typical recording of the output of the system with all four channels being driven simultaneously at 25 MBits/sec. This result is significant in that it demonstrates an effective channel density of 2222 channels/cm$^2$, and points toward the scalability of free space interconnects at the backplane level of the interconnection hierarchy.

## V. Conclusion

In conclusion, we have constructed an optical backplane demonstrator system capable of PCB-to-PCB optical interconnection. Digital data, fed onto a PCB, was optically encoded, transmitted, demodulated, and read out electrically. FET-SEED smart pixel transceiver arrays were used for the E/O and O/E conversion. Free-space optical communication channels were established using binary diffractive gratings, multilevel diffractive microlenses, polarizing optics, all integrated onto a slotted baseplate. Operational testing of the system was performed at data rates of 100 MBit/s sec. Finally, a single lenslet based interconnect was used to support four differential, eight total, optical channels, each operating at 25 MBit/sec. This result points to the scalability of backplane level, free space optical interconnects for future, large switching and computing systems. Future demonstrators will expand on these results by implementing sophisticated architectures such as the Hyperplane which utilizes the increased connectivity provided by an optical backplane [13].

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