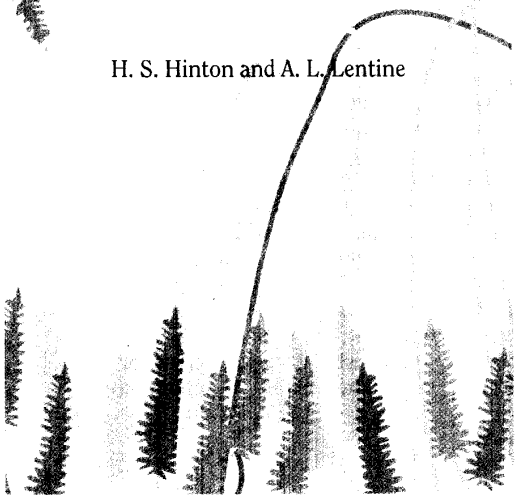
Multiple Quantum-Well Technology Takes SEED

Self-electro-optic effect devices are a leading candidate for securing dense, high-bandwidth interconnections

H. S. Hinton and A. L. Lentine



As clock rates for digital electronic systems continue to rise, the need grows for multiple high bandwidth interconnections at all levels of the system hierarchy. This includes the need to link frame to frame, shelf to shelf, printed circuit board to printed circuit board, multichip module to multichip module, and even chip to chip. Photonic interconnection of electronic circuit boards using fiber optics has already begun to satisfy this need. As the demand for greater bandwidth increases, photonic interconnections consisting of many parallel channels will be needed. One approach is to use many fibers in parallel. For even greater connectivity, beams of light imaged onto and off of each chip are seen as the link from one electronic IC to another. Looking further out, each optoelectronic integrated circuit (OEIC) will have thousands of optical detectors to receive information from other OEICs, and thousands of optical modulators or optical emitters sending information to other OEICs. The OEICs themselves may be very simple, such as an array of NOR gates; or very complex, such as an array of self-routing switching nodes or other processing elements. The self-electro-optic effect device (SEED) technology, which can incorporate detectors and optical modulators along with traditional electronic components, is a leading candidate for these optically interconnected OEICs [1,2].

The SEED technology is based on multiple quantum well (MQW) modulators. These wells consist of thin, alternating layers of narrow and wide bandgap materials such as GaAs and AlGaAs. Because of confinement of carriers in the quantum wells, the absorption spectrum shows distinct peaks, which are termed exciton peaks. When an electric field is applied perpendicular to the plane of the quantum wells, the position of the peaks shift (Fig. 1). This electro-absorption mechanism is called the quantum confined Stark effect (QCSE) [3,4], and it is strong enough that a 1 μm thick multiple quantum well stack can have changes in absorption coefficient of a factor of two or so for a 5 volt change across the stack. By placing the multiple quantum well material in the intrinsic region of a reverse biased p-i-n diode, the resulting device can modulate light in response to a change in voltage. The same device can also detect light.

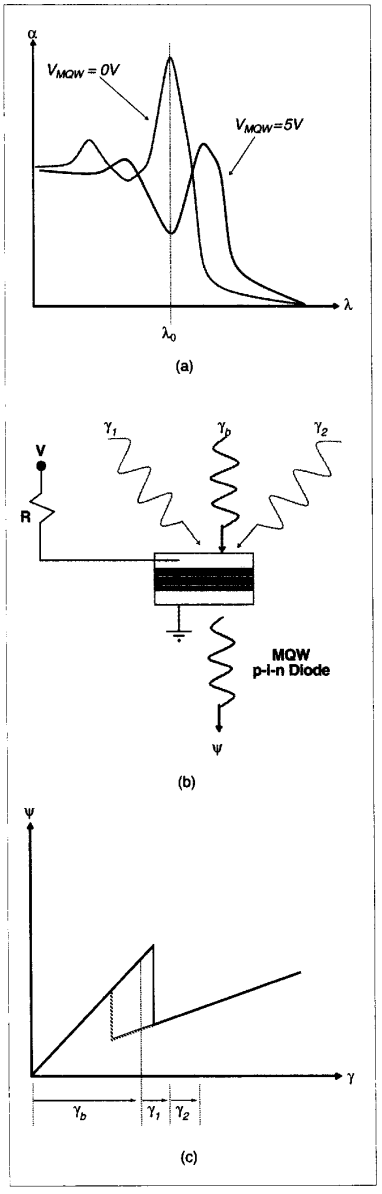
Self-electro-optic effect devices consist of one or more detectors and one or more optical modulators, such that the devices have optical inputs and outputs. Even though the devices are in some sense electronic, the devices can have low energies provided they are integrated [5]. In this article, we will review the progress in the development of these devices, beginning with the Resistor-SEED (R-SEED) device [6-8], which can be viewed as a simple NOR gate. The symmetric SEED (S-SEED) [9, 10] and the logic-SEED (L- SEED) [11, 12], are devices with improved features, functionality, and performance. Further along, the integration of FETs with MQW modulators (FET-SEED) [13-15], enables optical interconnections of electronic circuits. We'll also discuss where the SEED technology can be used, and describe an experimental optical switching fabric made using these devices.

SEED Technology

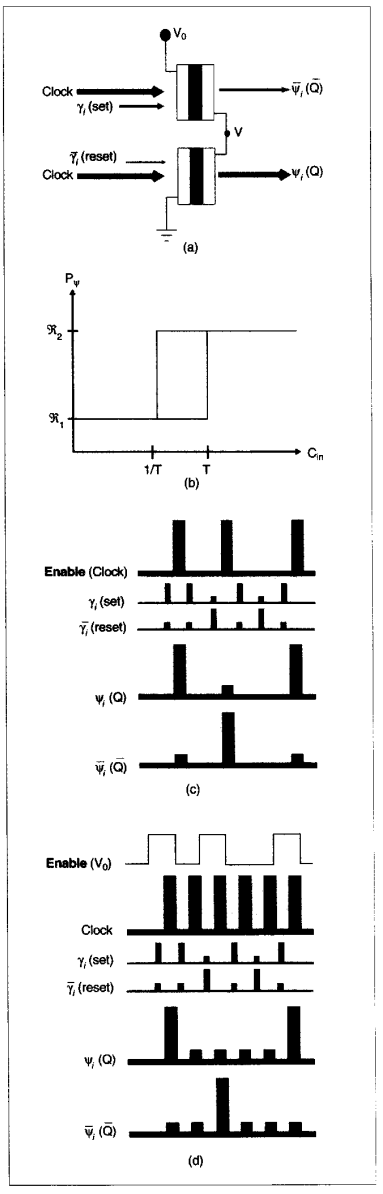
Resistor-SEED

The characteristic curve of the resistor-SEED device (Fig. 1a) results when this MQW material is placed in the intrinsic region of a p-i-n diode and electrically connected to a resistor (Fig 1b). When the incident intensity, γ_i, is low there is no current flowing through the p-i-n diode or resistor, thus the majority of the voltage is across the p-i-n diode. If the device is operating at the wavelength λ_o, the device will be a low absorptive state. As the incident intensity increases, so does the current flowing in the p-i-n diode. This current, in turn, reduces the

8755-3996/93/$3.00©1993 IEEE



1. Absorption spectra of MQW material for both 0 V and 5 V (a). Schematic of MQW p-i-n diode (b). Input/output characteristics of MQW p-i-n diode (c).



2. Symmetric-self-electro-optic effect device (SEE). S-SEED with inputs and outputs (a). Power transfer characteristics (b). Optically enabled S-SEED (c). Electrically enabled S-SEED (d).

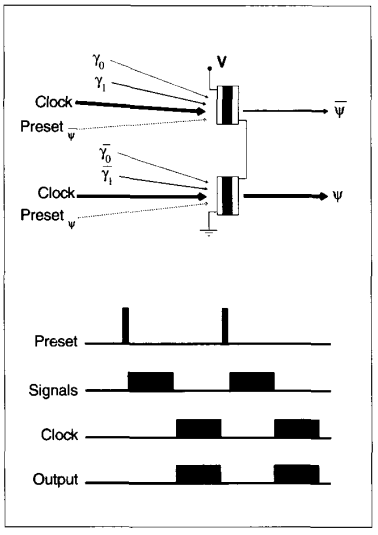
voltage across the diode. As a result, the absorption and current flow increases. This state of increasing absorption creates the nonlinearity in the output signal, ψ (Fig. 1c). Optical logic gates can be formed by biasing the R-SEED close to the nonlinearity, γ_b, and then applying lower level data signals γ_1 and γ_2 to the device.

Symmetric-SEED

The S-SEED, which behaves like an optical inverting S-R latch, is composed of two electrically connected multiple quantum well (MQW) pin diodes (Fig. 2a). The device inputs include signals γ (set), $\bar{\gamma}_i$ (reset), and the clock. To operate the S-SEED, the γ_i and $\bar{\gamma}_i$ inputs are also separated in time from the clock inputs (Fig. 2c, 2d). The γ_i and $\bar{\gamma}_i$ inputs, which represent the incoming data and its complement, are used to set the state of the device. When $\gamma_i > \bar{\gamma}_i$, the S-SEED enters a state where the lower MQW p-i-n diode will be transmissive, forcing the upper diode to be absorptive. When $\gamma_i < \bar{\gamma}_i$, the opposite condition will occur. Low switching intensities are able to change the device's state when the clock signals are not present. After the device has been put into its proper state, the clock beams are applied to both inputs. The ratio of the power between the two clock beams should be approximately one, which will prevent the device from changing states. These higher energy clock pulses will transmit the state of the device to the next stage of the system. Since the γ_i and $\bar{\gamma}_i$ inputs are low intensity pulses and the clock signals are high intensity pulses, a large differential gain may be achieved. This type of gain is referred to as time-sequential gain.

The operation of an S-SEED is determined by the power transfer characteristic (Fig. 2b) [10]. Here, the optical reflected power, ψ_i, is plotted against the ratio of the total optical signal power impinging on the set (when the clock is applied) and reset windows (when the clock is not applied). Assuming the clock power is incident on both signal windows, the output power is proportional to the reflectivity, $\Re_1$. The ratio of the input signal powers is defined as the input contrast ratio, $C_{in} = P\gamma/P\bar{\gamma}$. As C_{in} is increased from zero, the reflectivity of the lower diode switches from a low value, $\Re_1$, to a high value, $\Re_2$, at a G_{in} value approximately equal to the ratio of the absorbances of the two optical windows: $\tau = (1-\Re_1)/(1-\Re_2)$. Simultaneously, the reflectivity of the upper diode switches from $\Re_2$ to $\Re_1$. The return transition point (ideally) occurs when $C_{in} = (1-\Re_2)/(1-\Re_1) = 1/\tau$. The ratio of the two reflectivities, $\Re_2/\Re_1$, is the output contrast, C_{out}. Typical measured values of the preceding parameters include: C_{out} = 3.2, τ = 1.4, $\Re_2$ = 50% and $\Re_1$ = 15% [16].

The operation of an S-SEED as a 2-Module (switching node) can be accomplished by either optically or electrically enabling the individual S-SEEDs. To optically enable an S-SEED array, a spatial light modulator can be used to select which S-SEED receives clock pulses. If an S-SEED receives a clock pulse, the information previously latched



γ_0	γ_1	$\bar{\gamma}_0$	$\bar{\gamma}_1$	$Preset_\psi$	$Preset_{\bar{\psi}}$	ψ	$\bar{\psi}$	
0	0	1	1	0	1	0	1	
0	1	1	0	0	1	0	1	AND / NAND
1	0	0	1	0	1	0	1	
1	1	0	0	0	1	1	0	
0	0	1	1	1	0	0	1	
0	1	1	0	1	0	1	0	OR / NOR
1	0	0	1	1	0	1	0	
1	1	0	0	1	0	1	0	

3. Logic using S-SEED devices.

into the device will be transferred to the next stage of the network. If no clock is received the information cannot be transferred (Fig. 2c). On the other hand, the S-SEEDs can also be electrically enabled by controlling the voltage applied to the devices. If the appropriate voltage is present, the S-SEED behaves as previously described, and the information will be transferred. If no voltage is present, both MQW p-i-n diodes will become absorptive, preventing the stored information from transferring to the next stage.

The S-SEED is also capable of performing optical logic functions such as NOR, OR, NAND, and AND. This allows S-SEEDs to be used to implement more complex switching building blocks such as 2 x 1 and 2 x 2 switching nodes. The inputs will also be differential, thus still avoiding any critical biasing of the device. A method of achieving logic gate operation is shown in Figure 3. The logic level of the inputs will be defined by the ratio of the optical power on the two optical windows. When the power of the signal incident on the γ_1 input is greater than the power of the signal on the $\bar{\gamma}_1$ input, a logic "1" will be present on the input. On the other hand, when the power of the signal incident on the γ_1 input is less than the power of the signal on the $\bar{\gamma}_1$ input, a logic "0" will be incident on the input.

For the noninverting gates, OR and AND, we can represent the output logic level by the power of the signal coming from the $\bar{\psi}$ output relative to the power of the signal coming from the ψ output. As before, when the power of the signal leaving the ψ output is greater than the power of the signal leaving the $\bar{\psi}$ output, a logic "1" will be represented on the output. To achieve AND operation, the device is initially set to its "off" or logic "0" state (ψ = low and $\bar{\psi}$ = high), with the preset pulse, $Preset_{\bar{\psi}}$, incident on only one p-i-n diode (Fig. 3). If both input signals have logic levels of "1," (set = 1, reset = 0), then the S-SEED AND gate is set to its "on" state. For any other input combination, there is no change of state, resulting in AND operation. After the signal beams determine the state of the device, the clock beams are then set high to read out the state of the AND gate. For NAND operation, the logic level is represented by the power of the ψ output signal relative to the power of the $\bar{\psi}$ output signal. That is, when the power of the signal leaving the $\bar{\psi}$ output is greater than the power of the signal leaving the ψ output, a logic "1" is present on the output.

The operation of the OR and NOR gates is identical to the AND and NAND gates, except that preset pulse, $Preset_\psi$ is used instead of the preset pulse $Preset_{\bar{\psi}}$. Thus, a single array of devices can perform any or all of the four logic functions and memory functions with the proper optical interconnections and preset pulse routing.

An approximation of the optical switching energy required by S-SEEDs is given by [17]

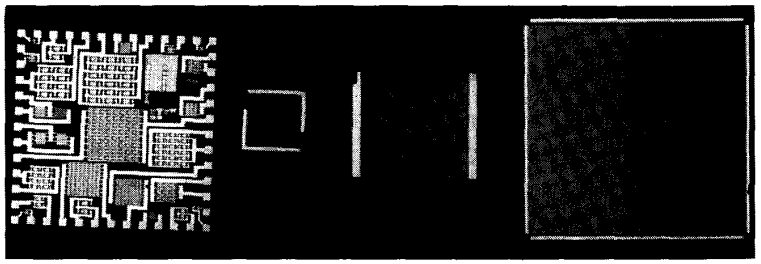
$$E_{opt} = \frac{2C(V_o + 2V_f)}{S_{avg}}$$

where C is the diode capacitance, assumed to be 115 aF/μm^2; V_o is the supply voltage (in this case, 15 V); V_f is the forward bias voltage (1 V); and S_{avg} is the average responsivity of the two diodes (0.33). The calculated value of optical switching energy density, 5.9 fJ/μm^2, agrees reasonably well with the measured data, although the smallest devices have slightly higher energy densities. A summary of the measurements of the different device sizes is shown in the Table. There was some contrast ratio degradation at power levels greater than 200 μW because of saturation of the quantum well material.

There have been four generations of fabricated S-SEED arrays (Fig. 4). These include a 16 x 8 array (1988), 64 x 32 (1989), 128 x 64 (1990), and a 256 x 128 array (1991) [18]. These four generations are illustrated in Fig. 4.

Table: Summary of S-SEED Parameters

			Calc.	*Measured*	
Device Size (μm)	**Power** (μW)	Δt (ns)	**E/μm^2** (fJ)	**E** (pJ)	**E/μm^2** (fJ)
100 x 100	200	750	5.9	149	7.5
	400	361		142	7.1
60 x 60	200	357		71	9.8
	400	145		56	7.7
30 x 30	100	130		12.5	6.9
	200	63		11.6	6.5
13.5 x 14	50	80		3.7	9.7
	100	39		3.4	8.9
	200	24		3.8	10.5
	400	14		3.6	9.5



4. Generations of S-SEED arrays using 16 x 8; 64 x 32; 64 x 128; and 128 x 256.

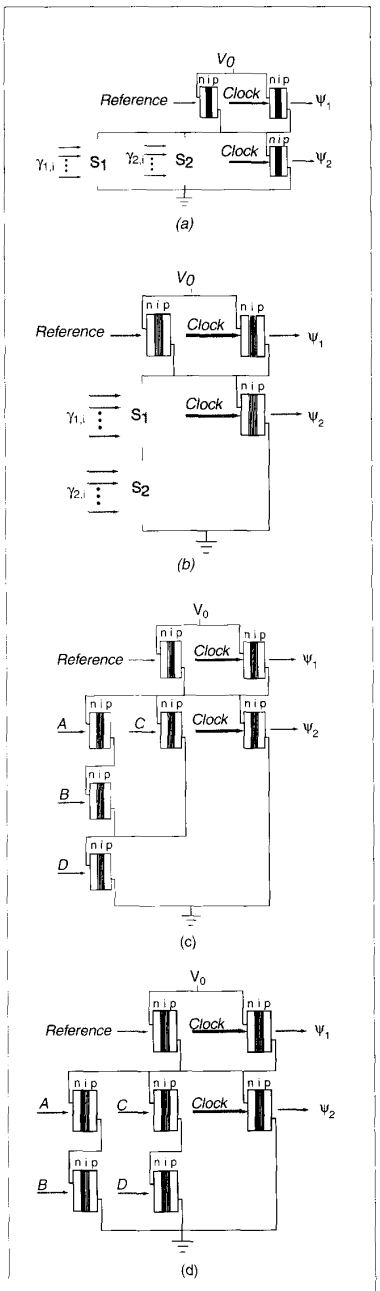
Logic-SEED

Logic-SEEDs (L-SEEDs) allow each effective pixel in a 2D-OEIC to possess more intelligence or functionality. These "smart pixels" have the capability to perform any Boolean logic function. Two classes of L-SEED smart pixels have been demonstrated: single-ended logic and differential logic. The first class of L-SEEDs, single-ended logic, has configurations of quantum well diodes that are similar to the transistor configuration in NMOS circuits. In these circuits, optical signals are routed individually and compared to a locally generated reference beam. If the reference beam is generated using the same laser that supplies the signal beams, critical biasing can be avoided. These devices also utilize time-sequential gain. The basic structure of these single-ended devices consists of a reference diode, the desired logic circuitry, and an S-SEED output driver (Fig. 5). An OR/NOR of two subfunctions, S_1 and S_2, can be implemented by connecting the two subfunctions in parallel (Fig. 5a). The output of the OR gate function is ψ, where $\psi = S_1 + S_2$; the NOR gate output is ψ_2, where $\psi_2 = \overline{S_1 + S_2}$. AND/NAND functions can be created by connecting the subfunctions serially (Fig. 5b). For this case $\psi_1 = S_1 S_2$ and $\psi_2 = \overline{S_1 S_2}$. Two examples of the single-ended circuit are $\psi_1 = (AB + C)D$ (Fig 5c); and $\psi_1 = AB + CD$ (Fig 5d).

In the second class of L-SEEDs, the signals are routed as differential pairs. These circuits have diode connections similar to transistor connections in CMOS. Unfortunately, these L-SEEDs are more complex than the first class, but they do not require a reference beam to be generated. Thus, the optical systems required to use these devices may be easier to build than the comparable single-ended systems.

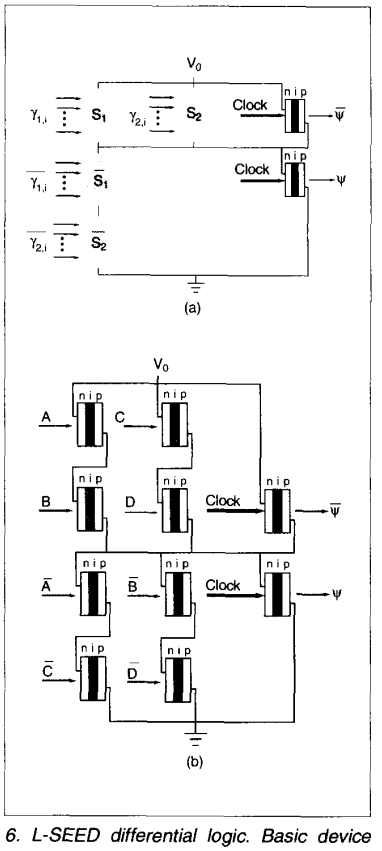
The method of realizing arbitrary Boolean functions is similar to the single-ended gates previously discussed. In an arbitrary logic gate (Fig. 6a), each logical input, consisting of two complementary beams, is incident upon a subfunction divided into complemented, S_j, and uncomplemented, $\overline{S}_j$, sections. The input diodes accept the incident input signals $\gamma_{j,i}$ for S_j, and $\overline{\gamma}_{j,i}$ for $\overline{S}_j$. Instead of connecting the subfunctions S_j in series with a diode biased by an incident reference beam, S_j and $\overline{S}_j$ are now connected in series. The diodes in $\overline{S}_j$ are electrically interconnected in a manner known as the conduction complement of the connections of the diodes in S_j. For example, if S_j consists of serially connected diodes, $\overline{S}_j$ requires parallel connected diodes. The voltage at the interconnecting node between S_j and $\overline{S}_j$ is connected to the center node of an output S-SEED and, thus, determines the output state of the device. For inverting functions (ANDs and ORs), ψ is the uncomplemented output, and $\overline{\psi}$ is the complemented output. For inverting functions (NANDs and NORs), the outputs are reversed. Figure 6b illustrates the implementation of the function $\psi = AB + GD$.

Another functional operation that can be performed with the SEED technology is the "transmission gate." These devices consist of back-to-back quantum well photodiodes, which transfer the voltage from the center tap of one S-SEED to another. An example of the application of this device is an S-SEED based (2,2,1) node smart "pixel" (Fig. 7). Neighboring S-SEEDs (SS_1, SS_2, and SS_3, are connected by optoelectronic transmission gates, TG_1 and TG_2, consisting of a pair of back-to-back quantum well photodiodes. These photodiodes transfer the voltage from one S-SEED to another. Input signals, γ_i and $\overline{\gamma}_i$, set the states of

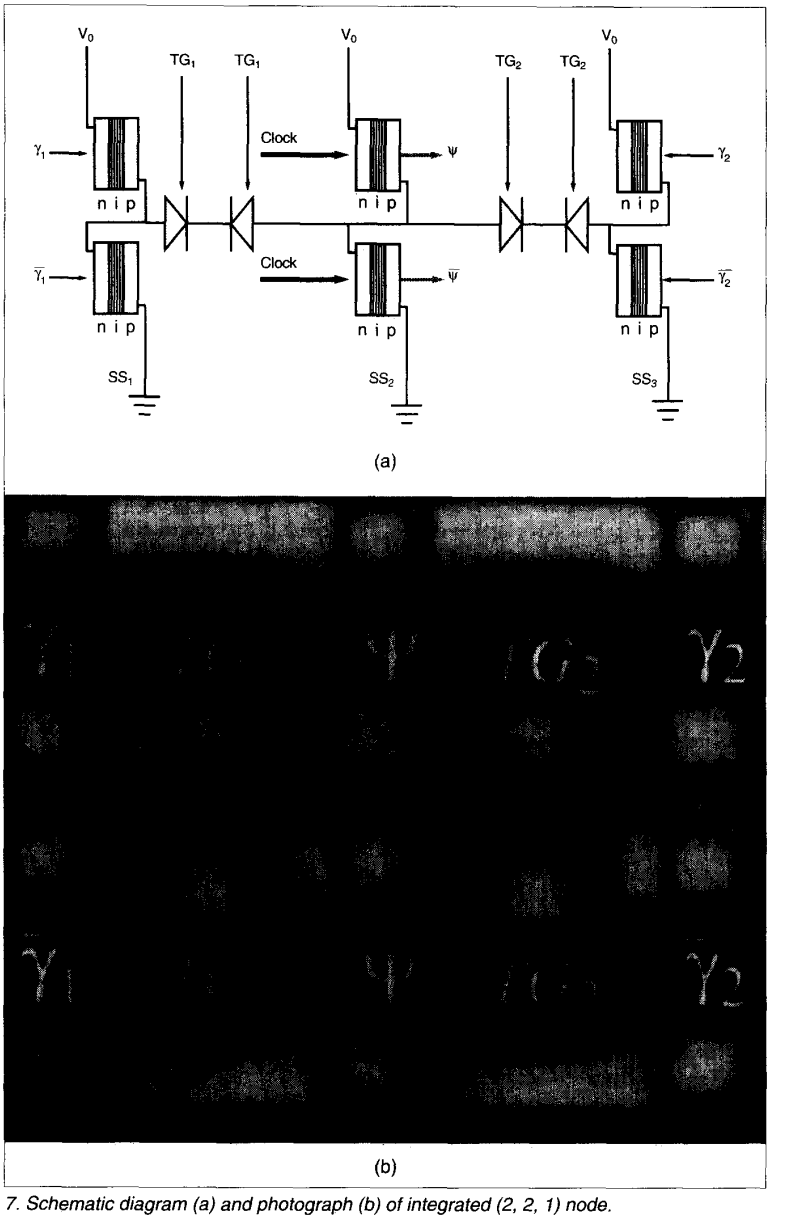


5. Single-ended L-SEEDs. OR function provided parallel subgroups (a); AND function provided by serially connected subgroups (b); $\psi_1 = (AB + C)D$ (c); $\psi_1 = AB + CD$ (d).

S-SEEDs SS_1 and SS_3. Transfer of the information from these S-SEEDs to the output S-SEED SS_2 is accomplished by



6. L-SEED differential logic. Basic device structure (a); logic gate with $\psi = AB + CD$.



7. Schematic diagram (a) and photograph (b) of integrated (2, 2, 1) node.

applying an enable signal to the appropriate transmission gate. For example, to transfer the information from S-SEED SS_1 to SS_2 requires the application of enable TG_1. A 10 x 16 array of switching these integrated switching nodes has been fabricated and demonstrated. A shift register using these devices has also been demonstrated.

FET-SEEDs

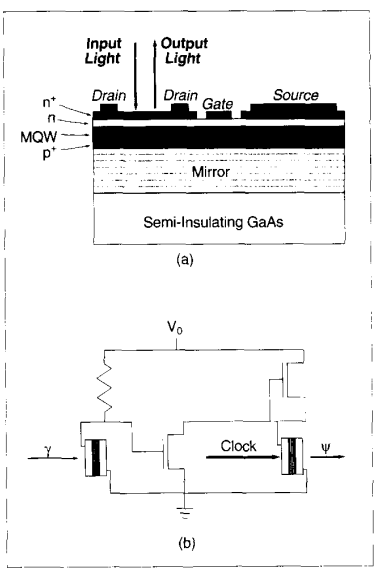
To take further advantage of the spatial bandwidth available in the optical domain, integrated electronic circuits could be integrated with optical detectors (inputs) and modulators or microlasers (outputs). This mixture of the processing capabilities of electronics and the communications capabilities of optics will allow connection intensive architectures with more complex nodes to be implemented. In addition, the gain provided by the electronic devices should allow high speed operation of the nodes. In the simplest case, the two-dimensional optoelectronic integrated circuits (2D-OEIC) could be arranged into a large 2-D array of "smart pixels" such as 2 x 1, 2 x 2, or even 4 x 4 switching nodes [2]. All the nodes in the 2-D array are electrically independent from each other, with the exception of a common ground and power supply. These "smart pixels" could also be developed to include the more complex circuitry necessary for self-routing nodes.

There are several advantages to a monolithically integrated electronic "smart pixel" technologies compared to L-SEEDs. The most important of these is that the required optical energies of electronic smart pixels may be less. This is because electronic gain may be able to reduce the required input voltage swing of the detectors from the 5-10 volts required by SEEDs, to perhaps a few tenths of a volt. This translates somewhat indirectly into reduced required optical switching energies, provided intelligent cir-

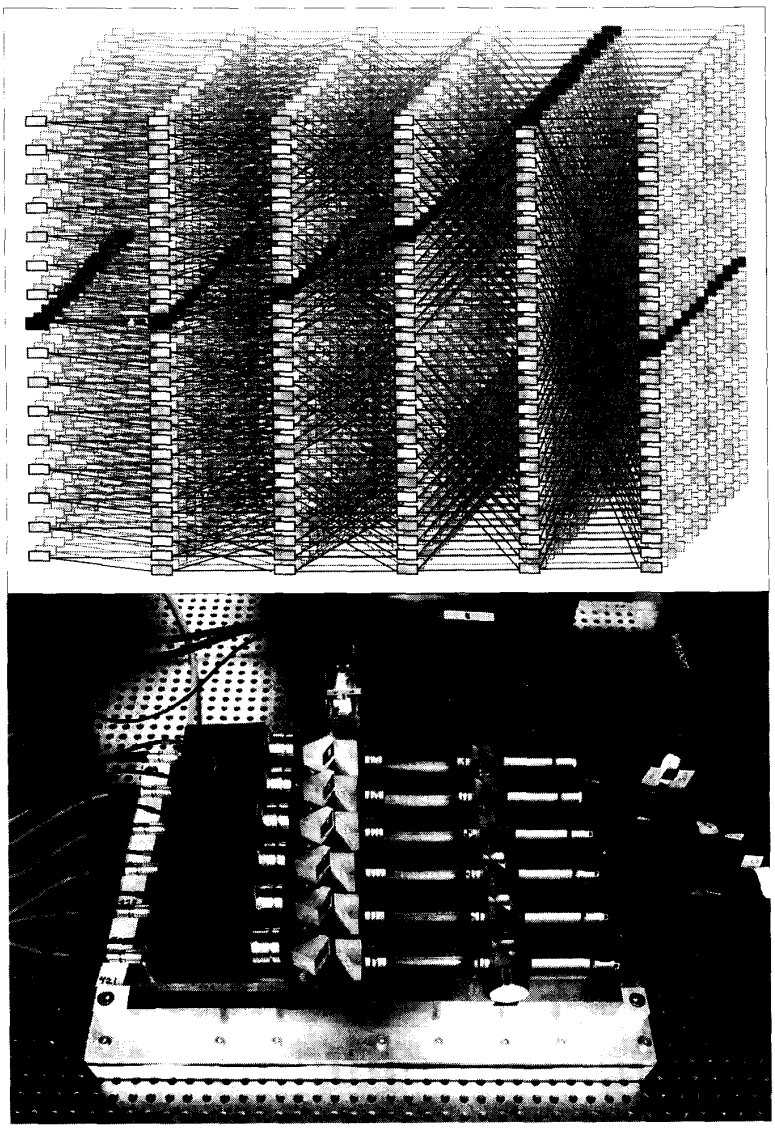
cuit designs are used. This is not true in a hybrid electronic smart pixel technology without integrated detectors, because the capacitance of a bonding pad (even with bump-bonding) would be much larger than the detector capacitance and would negate any energy advantage a reduced input voltage swing would have. A second advantage of transistor based smart pixels is that the complexity of the node could be greater in optically interconnected electronic smart pixels.

Integrated quantum well modulators with GaAs field effect transistors (FETs) have been demonstrated. The GaAs FETs were fabricated on top of a p-i-n diode structure grown p-side down (Fig. 8). Optical switching energies on the order of picojoules were observed for devices with 15-by-15 μm optical windows.

Promising results have also been achieved by integrating quantum well modulators with heterojunction bipolar transistors (HBTs). All of the devices made to date use the transistors as phototransistors. In this mode, the recovery of the device when the light is removed is rather long (at least a few ns), so the devices in their present configurations are probably not suited to high speed smart pixel applications. Also, the devices tend to operate at much higher currents than FETs and have greater capacitances. However, there is no fundamental reason why a smart pixel technology cannot be implemented using quantum well modulators and HBTs.



8. F-SEEDs. Layer structure (a); simple demonstrator circuit (b).



9. 16 x 32 (32-bit wide) free-space extended generalized shuffle network. Network topology (a); photograph of hardware (b).

Although promising results have been shown growing quantum well modulators on silicon substrates [19], the integration of quantum well devices with silicon VLSI has not been done. Integration of MQW modulators and detectors with silicon VLSI has advantages over integration with GaAs electronic circuitry, because higher density electronic circuits have been achieved on silicon. However, higher performance optoelectronic devices may be possible using MQW modulators integrated with GaAs electronics.

Interconnection Networks

The main objective of the free-space technology is to exploit the spatial bandwidth (pin-outs or connections) available in the optical domain [20]. This has allowed system designers to apply this technology to

connection intensive multistage interconnection networks (MIN). Using an S-SEED as a simple 2 x 1 switching node, several prototype switching fabrics have been successfully demonstrated [14]. A digital 2-module stores information, a single bit, from one of two 2-modules located in the previous stage in the network, then passes that information to the next stage in the network when the optical clock signal is applied to it. To set up a path through the network, represented by thick lines, clock signals are allowed to transfer information from the active nodes in a given stage to the next stage. Since the nodes are 2-Modules, only one of the two inputs present on each node can be active at any given time. To prevent corruption of the data entering the 2-Modules (S-SEEDs), the outputs of the undesired nodes are disabled electrically, thus preventing a transfer of the information they contain. One path through the 3-D network is shown as a thick line in Figure 9a. The first six stages of a 16 x 32 network is shown in Figure 9b. A 32 x 32 EGS network would require 13 stages to be strictly nonblocking [21]. The potential advantage of these fine-grained switching fabrics is that large dimensional fabrics could be possible in the future. As an example, a 1024 x 1024 nonblocking EGS fabric could be demonstrated using 19 S-SEED (64 x 128) arrays and their associated optical hardware.

Conclusion

Flexibility is the earmark of the SEED technology. For several years, a manufacturable technology has existed that allows SEEDs to be made with a variety of functions. Symmetric-SEEDs and Logic-SEEDs are two examples of this technology. The current trend is to incorporate electronic transistors into the SEED technology, for increased functionality and reduced optical power requirements. The integration of electronic and photonic components allows optics and electronics to do what they do best: electronics to process information, and photonics to communicate information. We expect rapid progress to continue in the coming years.

H. Scott Hinton received a B.S.E.E. degree in 1981 from Brigham Young Unviersity and a M.S.E.E. from Purdue in 1982. In 1981, he joined AT&T Bell Laboratories as a Member of Technical Staff. From 1985-89 he was supervisor of the Photonic Switching Technologies Group, and from 1989-92, Head of the Photonic Switching Department. He is currently the BNR-NT/-NSERC Chair in Photonic Systems at McGill University.

Anthony L. Lentine received his B.S. and M.S. degrees in Electrical Engineering from the University of Illinois in Urbana in 1979, and 1980, respectively. He is currently enrolled in an external Ph.D. program at Heriot-Watt Univrsity, Edinburgh, U.K. In 1980, he joined AT&T Bell Laboratories, Naperville IL, as a Member of Technical Staff. Since 1985, he has been working on photonic switching and optical computing applications of quantum well opteoelectronic devices. He is the co-inventor of many of the SEED devices used for prototype optical processing systems.

References

1. H. S. Hinton and D. A. B. Miller, "Free-space photonics in switching," *AT&T Technical Journal*, pp. 84-92, January/February, 1992.

2. J. E. Midwinter, "A novel approach to the design of optically activated wideband switching matrices," *Proceedings of the IEE* Part J, Optoelectronics, **134**, pp. 261-268, 1987.

3. D. A. B. Miller et al, "Bandedge electro-absorption in quantum well structures: the quantum confined stark effect," *Physical Review Letters*, **53**, pp. 2173-2177, 1984.

4. D. A. B. Miller et al, "Electric field dependence of optical absorption near the bandgap of quantum well structures," *Physical Review*, **B32**, pp. 1043, 1985.

5. D. A. B. Miller, "Optics for low-energy communication inside digital processors: quantum detectors, sources, and modulators as efficient impedance converters," *Optics Letters*, **14**, 2, Jan 1989.

6. D. A. B. Miller et al, "Novel hybrid optically bistable switch: The quantum well self-electrooptic effect device," *Applied Physics Letters*, **45**, pp. 13-15, 1984.

7. D. A. B. Miller et al, "The quantum well self-electrooptic effect device: optoelectronic bistability and oscillation, and self-linearized modulation," *IEEE Journal of Quantum Electronics*, **QE-21**, 9, pp. 1462-1476, September 1985.

8. D. A. B. Miller, "Quantum well self electro-optic effect devices," *Optical and Quantum electronics*, **22**, pp. 561-598, 1990.

9. A. L. Lentine et al, "Symmetric self-electro-optic effect device: Optical set-reset latch," *Applied Physics Letters*, **52**, 17, pp. 1419-1421, April 25, 1988.

10. A. L. Lentine, H. S. Hinton, D. A. B. Miller, I. E. Henry, I. E. Cunningham, and L. M. F. Chirovsky, "Symmetric self-electro-optic effect device: optical set-reset latch, differential logic gate, and differential modulator/detector," *IEEE Journal of Quantum Electronics*, **QE25**, 8, August, 1989, pp. 1928-1936.

11. A. L. Lentine et al, "Logic self electro-optic effect devices: Quantum well optoelectronic multiport logic gates, multiplexers, demultiplexors and shift registers," *IEEE Journal of Quantum Electronics*, **QE-28**,, 6, pp. 1539-1553, June 1992.

12. A. L. Lentine, T. J. Cloonan, and F. B. McCormick, "Photonic switching nodes based on self electro-optic effect devices," *Optical and Quantum Electronics*, **24**, pp. 5443-5464, 1992.

13. D. A. B. Miller, M. D. Feuer, T. Y. Chang, S.C. Chunk, J. E. Henry, D. J. Burrows, and D. S. Chemla, "Field-effect transistor self-electrooptic effect device: integrated photodiode, quantum well modulator and transistor," *IEEE Photonics Technology Letters*, **I**, 3, pp. 62-64, March 1989.

14. T. K. Woodward, L. M. F. Chirovsky and A. L. Lentine, "Operation of integrated GaAs-AlGaAs BET-SEEDs: modulators with gain," IEEE LEOS Annual Meeting, Postdeadline paper PD10 (1991).

15. L. A. D'Asaro, L. M. F. Chirovsky, E. J. Laskowski, S. S. Pei, and F. Ren "Batch fabrication and structure of integrated GaAs-AlGaAs FET-SEEDs," IEEE LEOS Annual Meeting, Postdeadline paper PD9 (1991).

16. F. B. McCormick, F. A. P. Tooley, T. J. Cloonan, J. L. Brubaker, A. L. Lentine, et al., "Experimental Investigation of a Free-Space Optical Switching Network Using S-SEEDs," *Applied Optics* **31**, pp. 5431-5446, 1992.

17. A. L. Lentine, L. M. F. Chirovsky, L. A. D'Asaro, C. W. Tu, and D. A. B. Miller, "Energy scaling and subnanosecond switching of symmetric self-electrooptic effect devices," *IEEE Photonics Technology Letters*, **I**, 6, pp. 129-131, June 1989.

18. L. M. F. Chirovsky et al., "Large Arrays of symmetric self-electro-optic effect devices," *OSA Proceedings on Photonic Switching*, H. S. Hinton and J. W. Goodman, eds. (Optical Society of America, Washington, DC, 1991), **8**, pp. 56-59.

19. K. W. Goosen, G. D. Boyd, J. E. Cunningham, W. Y. Jan, D. A. B. Miller, et al., "GaAs-AlGaAs multiple quantum well reflection modulators grown on GaAs and Silicon substrates," *IEEE Photonic Technology Letters*, **1**, pp. 304-306, 1989.

20. H. S. Hinton, "Architectural considerations for photonic switching networks," *Journal of Selected Areas of Communications*, **6**, pp. 1209-1226, August 1988.

21. T. J. Cloonan, G. W. Richards, A. L. Lentine, F. B. McCormick, and J. R. Erickson, "Free-space photonic switching architectures based on extended generalized shuffle networks," *Applied Optics*, **31**, pp. 7471-7492 (1992).