Progress in the Smart Pixel Technologies

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(Invited Paper)

***Abstract*— The purpose of this paper is to review the recent progress in the developing smart pixel technologies. This paper will begin by reviewing some of the rapidly evolving smart pixel terminology. It will then describe several of the smart pixel technologies that have recently emerged. Finally, it will outline the performance of these technologies in both device complexity and aggregate capacity.**

I. Introduction

A smart pixel is an optoelectronic structure composed of electronic processing circuitry (CMOS, BiCMOS, bipolar, etc.) enhanced with optical inputs and/or outputs [1]. The optical signals entering and/or leaving the smart pixels are typically arranged into two-dimensional (2-D) arrays that can be supported by the free-space optical interconnection of different smart pixel arrays (SPA's). In the simplest case, a SPA is formed by creating a 2-D array of similar smart pixels (uniformly distributed) as shown in Fig. 1.

The input optical signals to these smart pixels are detected by optoelectronic devices such as p-i-n or metal-semiconductor-metal (MSM) photodetectors. These detected signals are then amplified to the required (digital) electrical levels by analog electrical amplifiers [2].

Once the signals have been amplified to the appropriate electrical level they can be processed by the specific electrical circuitry of the smart pixel. The functionality of the smart pixels can range from one or two transistors providing some type of nonlinear gain to a smart pixel composed of several thousand transistors processing an ATM packet header. For this uniformly distributed type of SPA, the electronics in each smart pixel are localized to the area of the smart pixel preventing long, across-chip lines that can lead to reduced electrical performance because of skew, crosstalk, and the special drivers required to drive the longer electrical interconnects

Finally, after the input signals, both optical and electrical, have been processed, they can be directed to the optoelectronic outputs. These can be either sources, such as LED's or VCSEL's, or modulators such as MQW p-i-n diodes.

II. Smart Pixel Definitions

As the smart pixel technology continues to evolve, there needs to be a basic understanding and acceptance of key performance metrics including connection density, complexity, and aggregate capacity.

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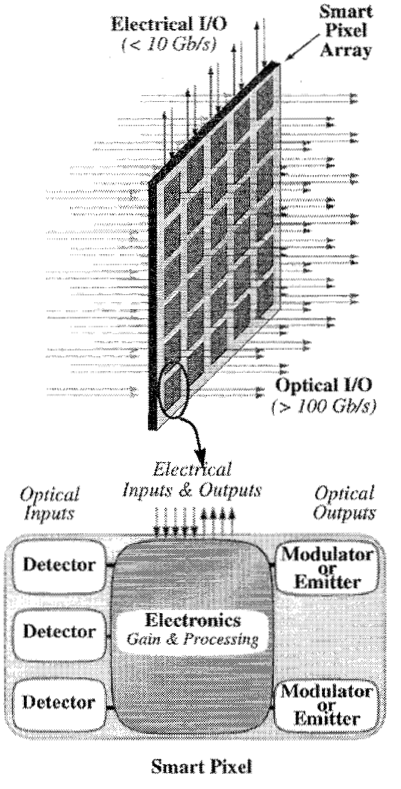

Fig. 1. Smart pixel array.

A. Connection Density

Since optical interconnection is the prime advantage of SPA's [3], the number of optical inputs and outputs of a SPA becomes an important parameter. The connection density refers to the number of optical connections per cm^2 (input + output) supported by a SPA and its associated optical interconnect. As an example, if there are 1000 smart pixels in a 1-cm^2 SPA and each smart pixel requires two signal inputs and two signal outputs, then the connection density that would need to be supported by the interconnect optics would be 4000 connections/cm^2. If the signals are differential, then the connection density would need to be 8000 connections/cm^2.

B. Complexity

The second major advantage of SPA's is the intelligence provided through the electronic processing circuitry. It is this intelligence that allows the smart pixels to perform complex operations on the data entering/exiting the SPA. It is this

intelligence that separates SPA's from photonic integrated circuits (PIC's) where PIC's refer to monolithically integrated optical and optoelectronic devices (lasers, detectors, optical waveguides, gratings, couplers, etc.) but do not include electronic structures. The complexity of the SPA's will be defined as the average number of transistors per optical I/O. It will be calculated by dividing the total number of transistors in the SPA by the total number of optical I/O.

C. Aggregate Capacity

To exploit the connectivity advantage of free-space optics, each SPA should have an aggregate optical throughput or capacity that is much larger than the electrical aggregate capacity. The aggregate optical capacity refers to the sum of all the optical inputs and/or outputs multiplied by their associated bit rates. On the other hand, the aggregate electrical capacity refers to the sum of all the electrical inputs and outputs multiplied by their associated bit rates. As an example, if there are 1000 optical inputs and 1000 optical outputs, each operating at 100 Mb/s, then the aggregate optical capacity is 200 Gb/s.

III. Smart Pixel Partitioning

The physical architecture or partitioning of the optical I/Os in SPA's is constrained by the type of optical interconnect employed in the system. There are three basic partitioning approaches, including: 1) uniformly distributed smart pixels, 2) concentrated I/Os, and 3) clustered smart pixels. Each is described below.

A. Uniformly Distributed

For the case of uniformly distributed smart pixels (Fig. 1), there are two major interconnection methodologies. The first is to use a large, complex, and bulky multi-element imaging system that will support a large field of view to cover the entire SPA and at the same time have a low enough f/# to collect the light emitted from the SPA sources and also image the received input information onto the SPA photodetectors. Despite the tremendous amount of progress in developing these systems, they tend to be both bulky and expensive. Examples of this approach include both AT&T System_4 architecture, which imaged 32×32 optical channels between six uniformly distributed SPA chips [4], and System_6, which provides the interconnection of $\sim 10\,000$ optical channels on/off a single uniformly distributed SPA [42].

A second approach is to provide each optical input and/or output with its own μchannel through the use of lenslet arrays [5] as illustrated in Fig. 2. These lenslet arrays have the potential of being mass produced and inexpensive. In this particular configuration, the separation between the optical I/O is equal to the size of the lenslet arrays. Thus, the total number of optical connections that can be supported by the μchannel approach is relatively small. Despite this limitation, this type of optical interconnect could be effective for complex SPA's that require a large area per smart pixel (a large number of transistors per optical I/O).

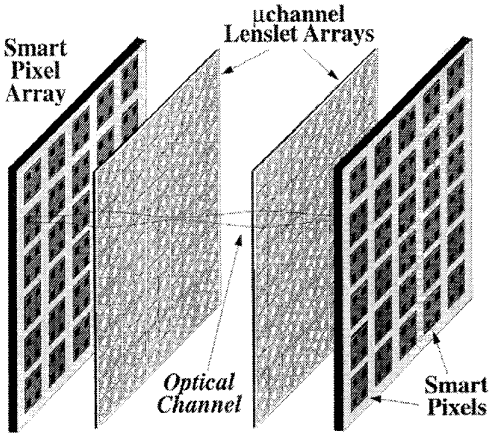

Fig. 2. Microchannel interconnected SPA's.

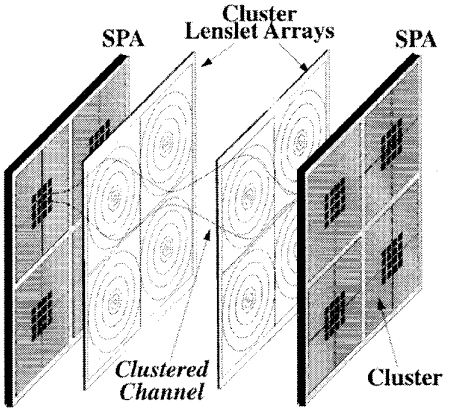

Fig. 3. SPA clustered interconnects.

B. Centralized I/O

To reduce the field of view required by the interconnection optics, the SPA's can be partitioned such that the optical I/O for all the smart pixels is concentrated together in the center of the SPA. The advantage of this partitioning is that the optical I/O can be tightly packed, thus reducing the field of view of the interconnection optics, which reduces the complexity and cost of the optics. The disadvantage is that the centralization of the optical I/O creates an electrical interconnection bottleneck in routing the electrical signals from the surrounding SPA electronics to the tightly packed optoelectronic I/O devices. This electrical connectivity issue is the same problem faced by large spatial light modulators.

C. Clustering

Clustering is a combination of both of the previous partitioning methods [6]. In this approach, the optical I/O for a small group of the smart pixels is clustered together as shown in Fig. 3. The size of the cluster is linked to the size of the lenslet that will support each cluster. In this case, the lenslet will support multiple channels instead of the single channel per lenslet supported in the μchannel approach. This approach can provide a significant connection density when

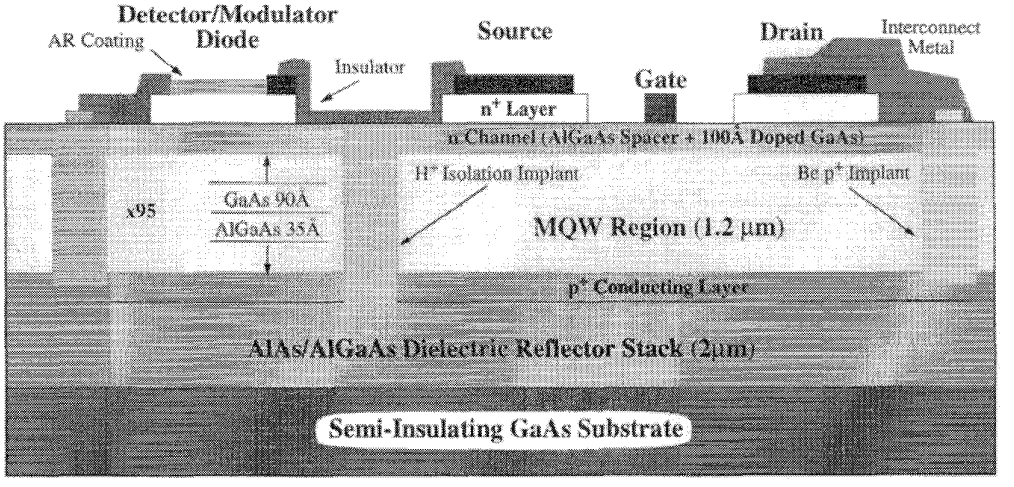

Fig. 4. Cross section of the AT&T FET-SEED technology.

the distance between the SPA's is small [6]. It also builds on the inexpensive lenslet technologies and avoids the use of expensive bulk lenses.

This approach has been recently used in McGill's Phase II Hybrid CMOS-SEED system demonstrator [7].

IV. Smart Pixel Technologies

There are several rapidly evolving SPA technologies approaching the point where they can be used in full-scale optoelectronic systems. These SPA technologies can be categorized as either modulator-based or source-based smart pixels. The modulator-based SPA's were the first to be developed and have been included in several demonstration systems. The source-based SPA's are rapidly evolving as the characteristics of VCSEL's are improving. Both of these categories of SPA's will be discussed in the section below.

A. Modulator-Based Smart Pixels

The first SPA technologies to be developed were based on the monolithic integration of photodetectors, electronics, and modulators into a single functional device. There are two major advantages of modulator-based SPAs: 1) they are simple devices and should be reliable, manufacturable, and uniform, and 2) the input light (power supply) can be centrally controlled, thus simplifying system synchronization. The major disadvantage is that the required interconnect optics are significantly more difficult. The three major SPA technologies discussed in this section are the FET-SEED Hybrid CMOS-SEED and liquid-crystal-on-silicon technologies.

1) FET-SEED Smart Pixels: The FET-SEED technology was the first smart pixel technology to monolithically integrate: 1) multiple-quantum-well (MQW) reflection modulators [8] based on a GaAs–$Al_xGa_{1-x}As$ stack, 2) p-i-n photodetectors using the same MQW stack as the modulators, 3) doped-channel MIS-like field effect transistors (DMT), and 4) optional integrated resistors [9]. The cross section of the FET-SEED technology is shown in Fig. 4.

A single molecular-beam epitaxial (MBE) growth sequence is used to provide the DMT channel, the quantum well absorbing region for both the modulators and photodetectors, the doped n- and p-type contact layers, and the dielectric mirrors required by the reflection modulators. Reflection modulators were used to provide both a structure suitable for batch fabrication and to enable heat sinking on the back side of the chip. Heat sinking is necessary in order to insure a stable excitonic absorption wavelength. These basic circuit elements were then stitched together using the buffered FET logic (BFL) to form larger and more complicated functional circuits. As an example of the general functionality of this technology, below is a list of the circuits that were designed at the AT&T/ARPA FET-SEED workshop [10].

- Time-integrating correlator
- Transceiver arrays
- Crossbar switch array
- Address decoders
- Smart spatial light modulator arrays
- Shift registers
- Wavelet transformer self-routing switching nodes
- Serial-to-parallel converters
- Exchange/bypass switching nodes
- Pulse-arithmetic neural network
- Test circuits

Fig. 5 is a photograph of one of the smart pixels in the 4×4 FET-SEED SPA used in the AT&T $System_5$ photonic switching system demonstrator [11]. Each smart pixel included 24 FET's, 17 diodes, four MQW photodetectors, and four MQW modulators and was able to operate at 400 Mb/s.

The FET-SEED technology has also been employed in demonstration systems at McGill University (16-channel optical backplane) [12], Optivision (16-channel optical interconnect) [13], and the University of Southern California (network application circuits) [14].

2) Hybrid CMOS-SEED Smart Pixels: The Hybrid CMOS-SEED technologies were pursued based on the philosophy that individual optical logic gates will not be able to compete with the existing or future silicon electronics technology platforms

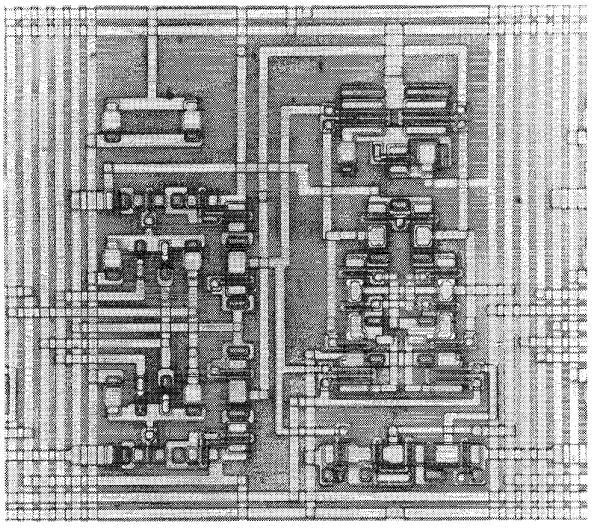

Fig. 5. AT&T System$_5$ smart pixel.

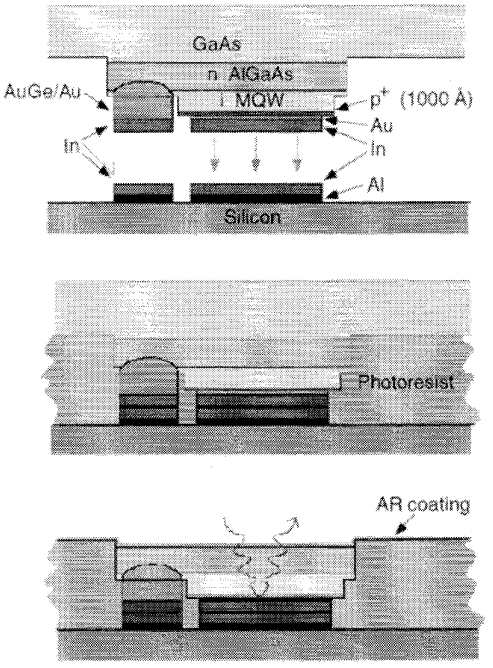

Fig. 6. Hybrid CMOS-SEED process.

with respect to power consumption, device size, and system complexity. It has also become obvious that silicon electronics is going to continue to increase in both performance and complexity while its cost will continue to decrease. Rather than compete with this rapidly growing technology, the objective of the smart pixel technology is to complement it. Since the added value of optics in the digital electronic domain is interconnection, providing optical inputs and outputs for the existing electronic integrated circuit platforms became the technologies' driving force. The first approach at integrating modulators/photodetectors onto silicon circuits was to put InGaAs modulators on silicon CMOS chips [15]. This use of GaAs–$Al_xGa_{1-x}As$ modulators/photodetectors on silicon CMOS was then pursued by AT&T [16]. In this process, MQW modulators/photodetectors are grown on GaAs chips such that the n and p contacts are coplanar (see Fig. 6). A Ti–Au pad is then deposited at the location of the optical windows of the MQW modulators/photodetectors to act as a 40% reflector. A lead–tin alloy is then deposited on the electrical contacts of the modulators/photodetectors to be used for the flip-chip bonding between the two substrates. The silicon CMOS chips have been obtained from the MOSIS foundry (both 1.2-μm and 0.8-μm line rules have been used). The aluminum bonding pads on the CMOS chip are then coated with a thin Ti–Pt–Au to provide a solder-wetable surface for the solder bump bonding later in the process. The two chips are then flip-chip solder-bonded together. Prior to removing the GaAs substrate, a silica-filled epoxy is wicked between the chips to protect both the GaAs and silicon chips. The GaAs substrate is then etched off, leaving only the small MQW modulators/photodetectors in the desired locations on the chip. An antireflection coating is then applied across the chip. A close-up of a CMOS-SEED SPA is shown in Fig. 7. It should be pointed out that this technique is not limited exclusively to silicon CMOS but could be used with other silicon circuit families such as ECL, bipolar, BiCMOS, etc.

As an example of the general functionality of this technology, below is a list of the circuits that were designed at the AT&T/ARPA Hybrid-SEED Workshop [17].

- Half-tone imaging
- Shared memory processor interconnect
- Multi-access interconnect architecture
- Digital cellular
- Imaging processor
- Optical A/D converter
- Optical permutation network
- Programmable logic smart pixel devices
- Crossbar switch
- Sorting switching nodes
- ATM switching nodes
- ATM-based optical backplane
- Focal plane processor
- Field programmable smart pixel arrays
- High-performance bus interface
- Linear fringe detector
- FFT nodes
- Wavelength meter
- Position-tolerant array sensor
- Cellular neural network
- Detector arrays
- Multidimensional interchanger

An example of a complete CMOS-SEED SPA is shown in Fig. 8. It is a 4 × 9 SPA for a buffered *HyperPlane* ATM backplane-based switching fabric. It includes ~60 transistors per smart pixel with a total of ~20 600 transistors in a 4-mm^2 area. It also includes 144 optical inputs and outputs and can store up to three concurrent ATM cells [18]. This technology has operated at bit rates greater than 1 Gb/s [19].

3) Liquid Crystal on Silicon: Finally, the liquid-crystal-on-silicon (LCOS) smart pixel technology provides optical out-

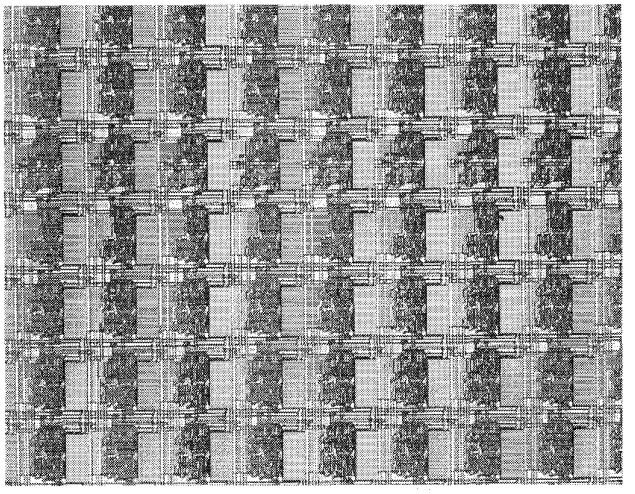

Fig. 7. Close–up of a CMOS–SEED smart pixel

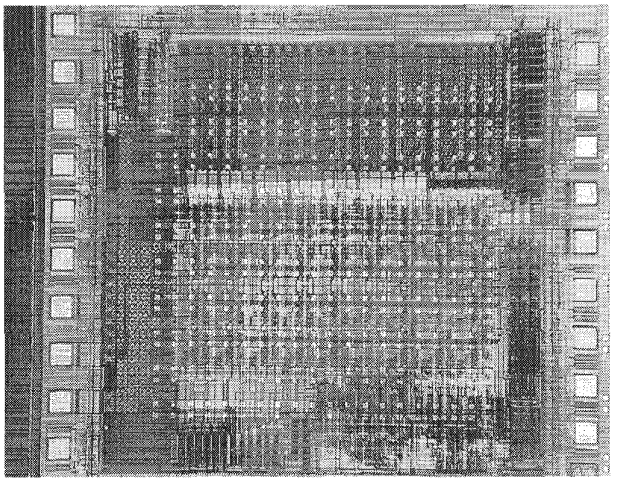

Fig. 8. Buffered *HyperPlane*SPA.

puts for any standardized electronic platform through the use of integrated arrays of liquid-crystal modulators [20]. The majority of this effort has focused on the integration of the high-birefringence and low-voltage operation of ferroelectric liquid-crystal (FLC) modulators on preprocessed silicon CMOS circuits. The cross section of an experimental LCOS device is shown in Fig. 9 [21]. The construction of this device begins with a silicon substrate that provides both the mechanical support for the assembly as well as the general electrical interconnect for the electrical signals entering and leaving the SPA. The silicon CMOS integrated circuit is first solder bonded to the silicon substrate and then the electrical connections between the CMOS chip and the substrate are made using standard wire-bonding techniques. The next step is to mount the SPA cover glass, which is composed of: 1) optically flat glass, 2) ITO coating, 3) FLC alignment layer, 4) mechanical polyimide spacers, 5) solder pads, and 6) a four-sided trench with a hole drilled through the front surface. This is accomplished with a solder reflow process that allows the solder joints to self-align and provide the necessary force to

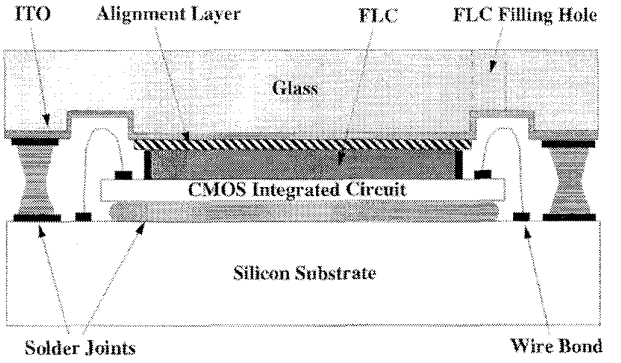

Fig. 9. Liquid-crystal-on-silicon.

maintain the desired spacing for the FLC. An FLC paste is the place in the hole where it will become a liquid when the structure is heated in a vacuum chamber. The liquid FLC will then fill the gap between the cover glass and the silicon CMOS integrated circuit by capillary action.

Although this technology is limited to modulator response times in the microseconds regime, it has found many applications that require massive optical interconnection. Examples include spatial light modulators, displays, and optical neural networks [20].

B. Source-Based Smart Pixels

An alternate to the modulator-based SPA's described above is a smart pixel technology based on the use of optical sources for the SPA outputs instead of modulators. The simplest, and most near-term, approach is to bring together, in a hybrid package, an electronic processing platform such as CMOS, an array of optical detectors, an electronic processing platform such as CMOS, and/or an array of optical sources such as VCSEL's. A second approach is to place the optoelectronic components on the electronic platform via thin-film integration techniques. A third approach is to flip-chip bond the detector and VCSEL arrays directly onto the electronic platform. Finally, the fourth approach is to monolithically integrate the detectors, electronics, and sources all onto a single substrate. Each of these approaches is described below.

1) Hybrid MSM/VCSEL Smart Pixels: The VCSEL/MSM hybrid technology is based on the hybrid integration of VCSEL's, MSM photodetectors, and a standard electronic integrated circuit platform such as ECL, bipolar, CMOS, BiCMOS, etc. into a common electronic package [22]. An example of this approach is shown in Fig. 10 where a 4×4 VCSEL array, a 0.8-μm CMOS chip fabricated through the MOSIS process, and a 4×4 array of MSM detectors were packaged together in the same PGA package [23]. Due to manufacturing costs, this is a short-term solution and will eventually be replaced by one of the other source-based approaches.

2) ELO-Based Smart Pixels: Using a technique referred to as epitaxial lift off (ELO) [24], high-quality, single-crystal thin-film materials and devices can be separated from a lattice-matched growth substrate using selective etching and then aligned and bonded to a host substrate such as preprocessed

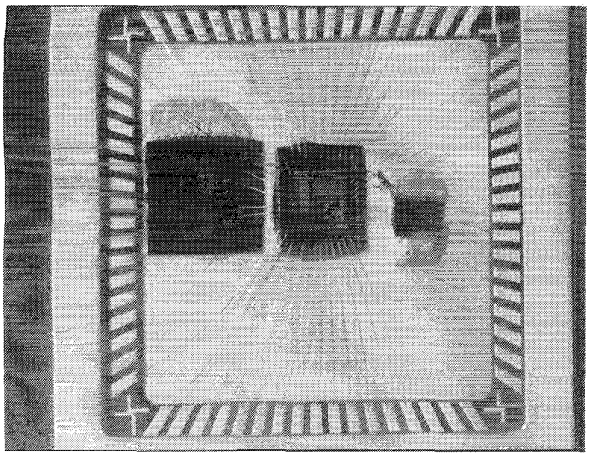

Fig. 10. Hybrid MSM/CMOS/VCSEL smart pixel array.

silicon CMOS substrates. The devices to be bonded to the host substrate are removed from the growth substrate through stop-etch layers. These epitaxial thin-film devices are then handled manually using a thick (100 μm) wax handling layer. Using this handling layer, the devices are then attached to a transparent transfer diaphragm constructed of either polyimide or mylar and supported by a ring of silicon on the outer edge. The diaphragm is then inverted with the thin-film devices facing the host substrate. The optoelectronic devices are then visually aligned and bonded to the host substrate using a pressure probe [25]. The performance of these devices has been shown to be comparable to that of devices that have not been separated from the growth substrate [26].

This technology has been able to demonstrate the placement of 64 AlGaAs detectors on a single silicon substrate [27] (see Fig. 11), thin-film LED-based transmitters that operate at 155 Mb/s [28] and receivers that operate at 250 Mb/s [29]. It has also become driving SPA technology in a through-wafer systems effort [30], [31]. This technology is not limited to source-based outputs but could also be applied to modulator-based SPA's.

3) Monolithic MSM/MESFET/VCSEL Smart Pixels: The GaAs MSM/MESFET/VCSEL smart pixel is based on the monolithic integration of VCSEL's, MSM detectors, and MESFET transistors. This smart pixel technology, pioneered by NTT, uses optical sources instead of modulators as the output device in each smart pixel [32]. Smart pixels based on this technology have demonstrated 3-dB bandwidths of 220 MHz. Fig. 12 is a picture of a simple monolithically integrated MSM/MESFET/VCSEL smart pixel.

4) Flip-Chip Bonded VCSEL/MSM Smart Pixels: A natural extension of the Hybrid-SEED technology is to flip-chip bond VCSEL's to an electronic platform instead of modulators.

V. SPA Performance

Over the past five years, there has been tremendous progress in the development of the smart pixel technology. This section will review the progress in device aggregate capacity, SPA complexity, and the performance of the SPA demonstrators.

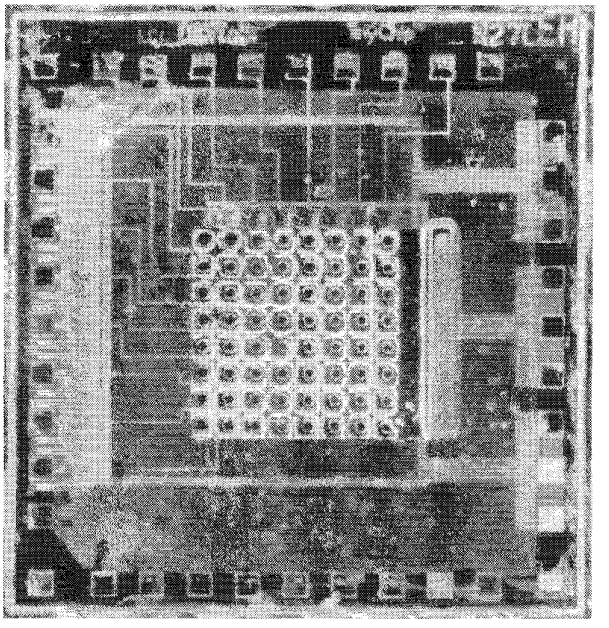

Fig. 11. ELO ALGaAs–based p–i–n detectors on silicon neural network circuitry.

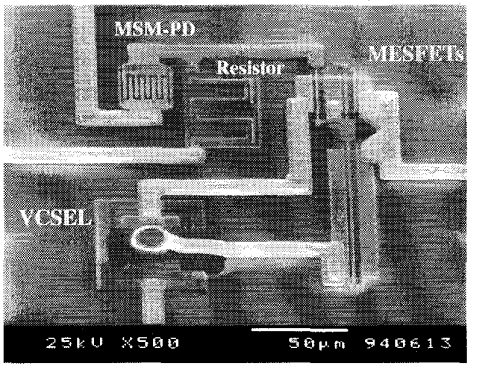

Fig. 12. NTT monolithic GaAs MSM/MESFET/VCSEL smart pixel [32].

A. SPA Aggregate Capacity

Fig. 13 illustrates the progress in aggregate capacity of single SPA's as a function of connectivity (pin-outs per chip) and per channel data rate (bits per second). The upper right corner of the figure (shaded) is the desired high-performance region supporting greater than a terabit aggregate capacity. The performance of several of the SPA device demonstrators representing the different SPA technologies have been mapped onto the figure. In this figure, the S-SEED devices represent the progress associated with simple optical logic gates. Despite the progress in developing optical logic gates, it became obvious that more speed and intelligence was needed. The first generation of these high-performance SPA's (HP-SPA) were primarily 4 × 4 arrays with bit rates ranging from 10–500 Mb/s. The next generation will be targeting 8 × 8 SPA's (or larger) as the device demonstrators for the 1996–1997 timeframe.

Another class of SPA's, the high-density SPA's (HD-SPA), targeting the high-connection density applications such as

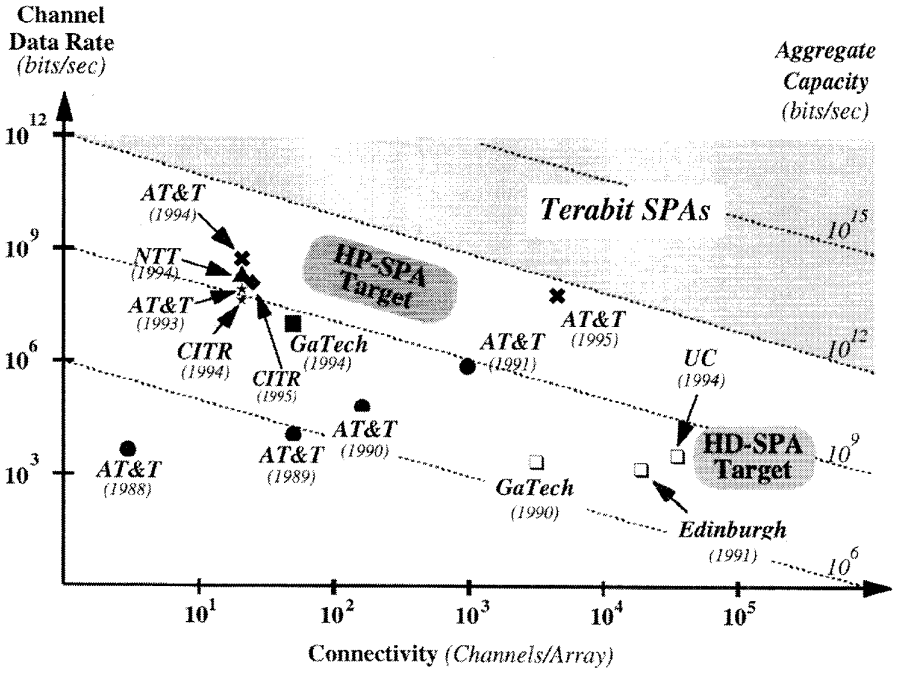

Fig. 13. The smart pixel array connectivity versus the individual optical channel bit rate with the following demonstrated SPAs: 1) AT&T (1988) [33], 2) AT&T (1989) [34], 3) AT&T (1990) [35], 4) AT&T (1991) [36], 5) GaTech (1994) [37], 6) CITR (1994) [38], 7) CITR (1995) [39], 8) AT&T (1993) [40], 8) NTT (1994) [41], 9)AT&T (1994) [16], 10) AT&T (1995) [42], 11) GaTech (1990) 12) Edinburgh (1991) [43], and 13) UC (1994) [44]. The smart pixel technologies represented include: ×—Hybrid CMOS-SEED, ▲—Monolithic MSM/MESFET/VCSEL, ♦—Hybrid MSM/VCSEL, ★—FET-SEED,●—S-SEED,■, and □–FLC-LCOS

smart spatial light modulators has also made significant progress. This progress is illustrated in the lower right corner of the figure. The target devices for this type of smart pixel include large arrays greater than 512 × 512 with modulator switching speeds in the 100-μs range.

B. SPA Complexity

Fig. 14 shows the trends in SPA intelligence. Since SPA's are based on the electronic integrated circuit technologies, they will be directly linked to the evolution of the semiconductor industry. The Semiconductor Industry Association's semiconductor roadmap, partially listed in Table I, illustrates the projected evolution of both the semiconductor electronic and the smart pixel technologies to the year 2010 [46].

Based on these SIA projections, it is conceivable that by the year 1998, 32 × 32 SPA's will be using 0.25-μm CMOS with each smart pixel containing up to 4000 transistors and operating in excess of 450 Mb/s per channel. This would provide greater than 450 Gb/s aggregate capacity per SPA! Further extrapolation leads to the year 2007 when 32 × 32 SPA's will be using 0.1-μm CMOS with each smart pixel containing up to 12 000 transistors and operating in excess of 1 Gb/s per channel. This would realize the technology design objective of 1 Tb/s aggregate capacity per SPA.

C. SPA Demonstrator Performance

There have been several SPA-based systems that have been successfully constructed and demonstrated within the past few years. These demonstrators include photonic switching systems, optical computing systems, and free-space optical backplanes. The performance of these systems is shown in Fig. 15. The total systems connections is the sum of the individual SPA connectivities. As an example, the 1993 AT&T System included five 4 × 4 FET-SEED SPA's. Each SPA had 32 optical inputs (32 optical channels comprised of 64 differential optical signals) and 32 optical outputs (64 differential optical signals) for a total of 640 system optical connections (this does not include the optical power supply inputs, 64 per SPA, required for this type of modulator-based

TABLE I
SIA SEMICONDUCTOR ROADMAP

First DRAM Shipment *Minimum Feature Size*	1995 *0.35 μm*	1998 *0.25 μm*	2001 *0.18 μm*	2004 0.13 μm	2007 *0.1 μm*	2010 *0.07 μm*
Memory						
Bits/Chip (DRAM/Flash)	*64M*	*256M*	*1G*	*4G*	*16G*	*64G*
Logic (High Volume μP)						
Transistors/cm² *(packed)*	*4M*	*7M*	*13M*	*25M*	*50M*	*90M*
Logic (Low Volume ASIC)						
Transistors/cm² *(auto layout)*	*2M*	*4M*	*7M*	*12M*	*25M*	*40M*
Number of Chip I/O						
High Performance	*900*	*1350*	*2000*	*2600*	*3600*	*4800*
Chip Frequency (MHz)						
On-chip (cost performance)	*150*	*200*	*300*	*400*	*500*	*625*
On-chip *(high performance)*	*300*	*450*	*600*	*800*	*1000*	*1100*
Chip-to-board	*150*	*200*	*250*	*300*	*375*	*475*
Chip Size (cm²)						
DRAM	*1.9*	*2.8*	*4.2*	*6.4*	*9.6*	*14.0*
Microprocessor	*2.5*	*3.0*	*3.6*	*4.3*	*5.2*	*6.2*
ASIC	*4.5*	*6.6*	*7.5*	*9.0*	*11.0*	*14.0*
Power Suppy Voltage (V)						
Desktop	*3.3*	*2.5*	*1.8*	*1.5*	*1.2*	*0.9*
Battery	*2.5*	*1.8-2.5*	*0.9-1.8*	*0.9*	*0.9*	*0.9*
Maximum Power						
HP with heatsink (W)	*80*	*100*	*120*	*140*	*160*	*180*
Logic w/o heatsink (W/cm²)	*5*	*7*	*10*	*10*	*10*	*10*
Battery (W)	*2.5*	*2.5*	*3.0*	*3.5*	*4.0*	*4.5*

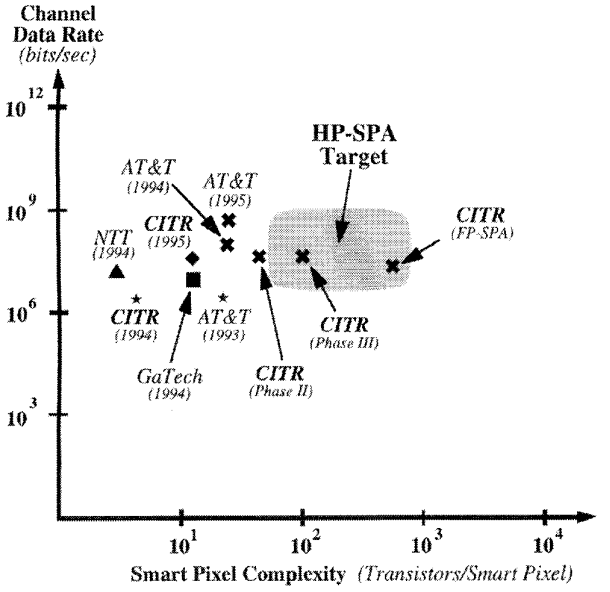

Fig. 14. The smart pixel array complexity versus the individual optical channel bit rate for the following SPAs: 1) NTT (1994) [41], 2) CITR (1994) [39], 3) CITR (1995) [39], 4) GaTech (1994) [37], 5) AT&T (1993) [40], 6)AT&T (1994) [16], 7) AT&T (1995) [42], 8) CITR (*Phase II*)[39], 9) CITR (*Phase III*) [39], and 10) CITR (*FP–SPA*) [45]. The smart pixel technologies represented include: ×—Hybrid CMOS-SEED, ▲—Monolithic MSM/MESFET/VCSEL, ♦—Hybrid MSM/VCSEL, ★—FET–SEED, and ■—ELO.

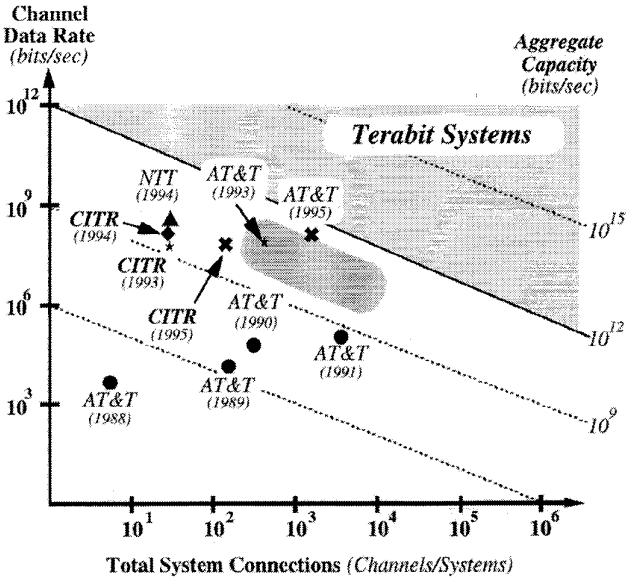

Fig. 15. SPA system connectivity versus the individual optical channel bit rate with the following demonstrated SPAs: 1) AT&T (1988) [33], 2) AT&T (1989) [34], 3) AT&T (1990) [35], 4) AT&T (1991) [36], 5) CITR (1993) [38], 6) CITR (1994) [39], 7) CITR (1995) [39], 8) AT&T (1993) [40], 9) NTT (1994) [41], and 10) AT&T (1995) [42]. The smart pixel technologies represented include: ×—Hybrid CMOS–SEED, ▲—Monolithic MSM/MESFET/VCSEL, ♦—Hybrid MSM/VCSEL, ★—FET—SEED, and •—S–SEED.

system). This figure also shows the performance targets for SPA-based systems to be demonstrated in the 1996–1997 timeframe.

VI. Applications

There are two main classes of applications that match the capabilities of the smart pixel technologies: high-performance intelligent interconnects and high-density interconnects. High-performance intelligent interconnects refer to applications that require a modest number (10–10 000) of high-performance interconnects (>100 Mb/s) supported by a significant amount of intelligence (>50 transistors per optical I/O). This application class includes optical backplanes, switching networks, and high-performance computers. The second class of applications, high-density interconnects, focuses more on connectivity (1000–100 000) than performance (<100 Mb/s) and/or intelligence (<50 transistors per optical I/O). Specific applications include: advanced displays, optical storage, analog optical processing, optical neural networks, etc. Fig. 16 illustrates the potential application space of the smart pixel technology.

Perhaps the most critical aspect in the evolution of applications based on the SPA technology will be the development of a low-cost, high-reliability packaging technology. The optomechanical tolerances required to optically interconnect successive SPA's will require modular, manufacturable optical hardware modules (OHM) that can transfer optical information from the transmitting SPA to the photodetectors of the receiving SPA. In addition, for the case of modulator-based systems, the OHM will also have the responsibility to deliver optical power to the modulators. In order to integrate SPA's

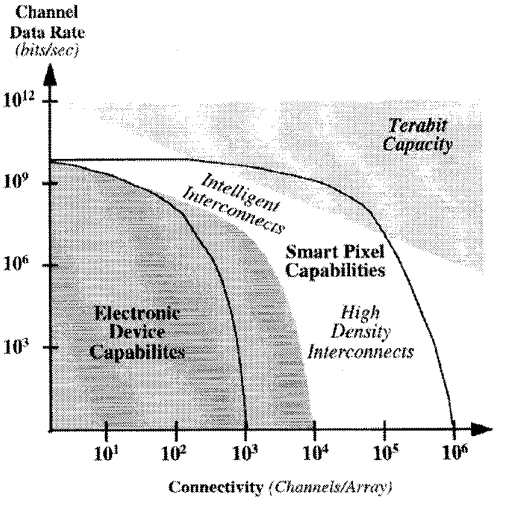

Fig. 16. Smart pixel application space.

into the existing digital electronic infrastructure, it is necessary that a compact and durable optical system be designed and developed that is compatible with current computer packaging. This implies the following OHM requirements.

1) Support a smart pixel density of 1000 smart pixels/cm^2
2) Fit in a standard electrical rack: $\sim 1''$ spacing between SPA's and a 1-in^3 optomechanical volume per SPA pair.
3) Support a SPA size of 1 cm × 1 cm.
4) For modulator-based systems, keep the loss between the optical power supply and the detector less than 10 dB, and for the source-based systems, keep the loss between the VCSEL's and the detector less than 3 dB.

5) Use only elements which are potentially cost-effective in mass production.
6) Minimize the number of critical alignments.
7) Maintain optomechanical stability over a 100° temperature range.
8) Modular OHM's that can operate in a "plug and play" environment.

The push to decrease optical system size has dramatically changed the methods for system packaging. Previous free-space digital optics systems typically used nearly all 32 ft^2 of an optical table [4]. The large system size was due to the large size of the off-the-shelf optical components and their mounting mechanisms. With the shrinking of optical components and the availability of high-power laser diodes, new optical system packaging methods are evolving which are compatible with the physical conventions of current electronic systems. The current optomechanical approaches include: slotted baseplates [4], barrels [39], glued optics [41], and, finally, active alignment [47].

VII. Conclusion

This paper has described the major SPA technologies that are currently evolving toward manufacturable device platforms. The reviewed SPA technologies included both the modulator-based FET-SEED, Hybrid CMOS-SEED, and LCOS smart pixels and the source-based Hybrid VCSEL/MSM, ELO, flip-chip-bonded VCSEL/MSM, and monolithic MSM/MESFET/VCSEL smart pixels.

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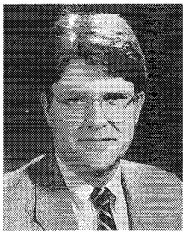

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