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A PIPELINE ANALOG-TO-DIGITAL CONVERTER FOR A PLASMA IMPEDANCE PROBE

by

Mohamad A. EL Hamoui

A thesis submitted in partial fulfillment
of the requirements for the degree

of

MASTER OF SCIENCE

in

Electrical Engineering

Approved:

Dr. Chris Winstead Major Professor	Dr. Edmund A. Spencer Committee Member
Dr. Brandon Eames Committee Member	Dr. Byron R. Burnham Dean of Graduate Studies

UTAH STATE UNIVERSITY
Logan, Utah

2009

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Abstract

A Pipeline Analog-to-Digital Converter for a Plasma Impedance Probe

by

Mohamad A. EL Hamoui, Master of Science

Utah State University, 2009

Major Professor: Dr. Chris Winstead
Department: Electrical and Computer Engineering

Space instrumentation technology is an essential tool for rocket and satellite research, and is expected to become popular in commercial and military operations in fields such as radar, imaging, and communications. These instruments are traditionally implemented on printed circuit boards using discrete general-purpose Analog-to-Digital Converter (ADC) devices and other components. A large circuit board is not convenient for use in micro-satellite deployments, where the total payload volume is limited to roughly one cubic foot. Because micro-satellites represent a fast growing trend in satellite research and development, there is motivation to explore miniaturized custom application-specific integrated circuit (ASIC) designs to reduce the volume and power consumption occupied by instrument electronics. In this thesis, a model of a new Plasma Impedance Probe (PIP) architecture, which utilizes a custom-built ADC along with other analog and digital components, is proposed. The model can be fully integrated to produce a low-power, miniaturized impedance probe.

(67 pages)

To my Habiba....

Acknowledgments

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Mohamad A. El Hamoui

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Acronyms

LP	Langmuir Probe
SIP	Sweeping Impedance Probe
PFP	Plasma Frequency Probe
PIP	Plasma Impedance Probe
GPS	Global Positioning System
DDS	Direct Digital Synthesizer
PLD	Programmable Logic Device
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
RF	Radio Frequency
FPGA	Field Programmable Gate Array
FFT	Fast Fourier Transform
LSB	Least Significant Bit
OPAMP	Operational Amplifier
INL	Inregral Nonlinearity
DNL	Differential Nonlinearity
SNR	Signal-to-Noise Ratio
ENOB	Effective-Number-Of-Bits
THD	Total Harmonic Distortion
SINAD	Signal-to-Noise-And-Distortion
SFDR	Spurious Free Dynamic Range
ROM	Read-Only Memory
PLL	Phase-Locked Loop

Chapter 1

Introduction

1.1 Motivation

Plasma instrumentation has been an active field of research over the last four decades. Most of this work was developed for sounding rockets and satellites launched into the ionosphere. The ionosphere is a region that exists in the upper atmosphere. It ranges from roughly 50 km to 1500 km in altitude. Plasma in this region is formed because of the collection of ionized molecules and free electrons due to high intensity radiation generated from the sun. Plasma activity in the ionosphere has a significant impact on telecommunication systems, power grids, and is important to space scientists and meteorologists.

Plasma impedance measurement is critically important to study the plasma characteristics and its behavior in the ionosphere. Several in situ techniques have been designed for this specific task. The Langmuir Probe (LP) [1–4] functions by applying a fixed DC bias (power supply) to an electrode in contact with plasma. The Standing Wave Impedance Probe (SWIP) technique [5, 6] utilizes a transmission line that connects the dipole antenna to a crystal frequency oscillator. The Sweeping Impedance Probe (SIP) [7, 8] uses a phase detection scheme to measure the magnitude, phase, and impedance of a probe by sweeping the frequency across a desired range. The Plasma Frequency Probe (PFP) [9] determines the electron density and temperature by measuring the resonance frequencies of the impedance probe.

This thesis will present a new integrated design for a Plasma Impedance Probe (PIP). The PIP is a type of SIP instrument that can also provide PFP information. It is mainly used to analyze the electron density and several plasma characteristics in the ionosphere. There has been various forms and methods of using the PIP. Chapter 2 will give a brief history of the traditional PIP instrument and the improved proposed integrated PIP, respectively.

1.2 Thesis Outline

This work explores a custom application-specific integrated circuit (ASIC) approach to design an ADC that is uniquely optimized for the PIP instrument. In general-purpose ADCs, the typical performance characteristics need to be optimized across different operating conditions; however, in our case, we need to analyze which characteristics are critical and noncritical for the PIP instrumentation. This gives the opportunity to improve on key performance characteristics for our application, and relax the requirements of other characteristics. Error tolerances for a pipeline ADC designed as part of a PIP system will be considered. The research contributions to this work include:

1. Modeling of the ADC and characterizing it to fit the PIP system's requirements;
2. Introducing a method for modeling nonlinear distortion caused by the plasma environment for a pipeline ADC, and comparing it to the quadratic nonlinearity found in CMOS transistors; and
3. Modeling and analyzing the whole PIP chip to verify its functionality.

Chapter 2 begins with an overview of the PIP instrument. A brief literature survey of previous and current state-of-the-art PIP technologies are presented, along with their disadvantages. This chapter also presents the architecture of the proposed integrated PIP system. It demonstrates the functionality of the instrument, and outlines the advantages of the system, which can overcome some serious limitations of previous PIP designs.

Chapter 3 gives a background introduction to pipeline ADCs. It describes the 1.5-bits/stage topology and illustrates its advantages compared to other topologies. It also characterizes the specifications for the ASIC ADC. Errors and nonlinearity are inserted to a 16-bit 100 MHz pipeline ADC behavioral Simulink model to study their effects on the impedance calculation, and to determine maximum tolerance for component errors and variations.

Chapter 4 provides a comprehensive description and modeling of all the components associated with the PIP chip. The components are also modeled in Cadence using Verilog-AMS to obtain more realistic circuit models. Absolute impedance magnitude across the operating frequency range is presented using Simulink and Cadence.

Chapter 5 summarizes the work presented in this thesis. It outlines the advantages of the proposed PIP architecture and discusses future work that may be implemented.

With this analysis, design specifications driven by the accuracy needs of the plasma instrument can be determined. This enables the creation of a new generation of plasma measurement, instrumentation, and research.

Chapter 2

Overview of the Plasma Impedance Probe and the Proposed System

2.1 Plasma Theory

The plasma antenna probe is a half-wave dipole antenna formed by two conductors and a 75 Ω coax cable feed-line, or an infinitesimal monopole antenna whose length is very small compared to the wavelength λ of the signal. In our case, the probe is a dipole antenna, in which both conductor ends are immersed in plasma where one side is connected to ground and the other is fed to the input voltage on the generator end. Because of the low frequency of operation compared to a wavelength, the antenna can be regarded as a simple capacitor. The current in the dipole varies linearly from maximum at the midpoint of the antenna to zero towards the conductors. Also, in free space, when there is no material medium, the relative dielectric permittivity $\varepsilon_r = 1$. In plasma, the ε_r of the medium changes and the capacitance will then be

$$C_p(\omega) = \varepsilon_r(\omega) C_{fs,} \tag{2.1}$$

where ω is the applied input frequency in rads/sec, $C_p(\omega)$ is the capacitance when immersed in plasma, C_{fs} is the empty free space capacitance (see fig. 2.1), and $\varepsilon_r(\omega)$ is defined as

$$\varepsilon_r(\omega) = 1 - \frac{\omega_{pe}^2}{\omega^2 + \upsilon^2} - j\frac{\omega_{pe}^2 \left(\frac{\upsilon}{\omega}\right)}{\omega^2 + \upsilon^2}, \tag{2.2}$$

where ω_{pe} is the plasma electron frequency, and υ is the electron-neutral collision frequency. A complex plasma permittivity indicates that the plasma stores and dissipates energy within

its medium. In a cold plasma, plasma with partially ionized gas molecules, ω_{pe} is given as

$$\omega_{pe} = \sqrt{\frac{\eta_e q_e^2}{m_e \varepsilon_0}}, \tag{2.3}$$

where η_e is the plasma electron density, q_e is the electron charge, m_e is the electron mass, and ε_0 is the free-space permittivity.

Impedance resonances occur at three major frequencies. A small impedance resonance from the free space capacitance occurs at ω_{pe}, when the electric field is parallel to the magnetic field. A series-like RLC resonance, sharp minimum impedance with zero phase, occurs at the electron cyclotron frequency ω_{ce}. The term cyclotron (cycloid motion) comes from the orbital movement of a plasma electron in a magnetic field. For a given magnetic field B, the cyclotron frequency is given by

$$\omega_{ce} = \frac{q_e B}{m_e}. \tag{2.4}$$

A parallel-like RLC resonance, with maximum impedance, occurs at the upper hybrid frequency ω_{uh} and is defined as

$$\omega_{uh} = \sqrt{\omega_{pe}^2 + \omega_{ce}^2}. \tag{2.5}$$

The antenna impedance characteristics explained above are well-modeled by Balmain [10]. Balmain's model gives the impedance magnitudes and resonances across the frequency range, as depicted in fig. 2.1, where most ionospheric plasma characteristics take place. These frequencies are in the range of 100 KHz to 20 MHz. The PIP has to measure impedance magnitudes ranging from 100 to 160 $k\Omega$.

2.2 PIP Instrument History

The PIP instrument has been studied by numerous researchers, who contributed many improvements over the last forty years. A wide variety of designs have been circulated in the literature. Steigies [11] described a design that uses a digitally controlled impedance probe for fast and accurate measurement of the absolute electron density in the ionospheric plasma.

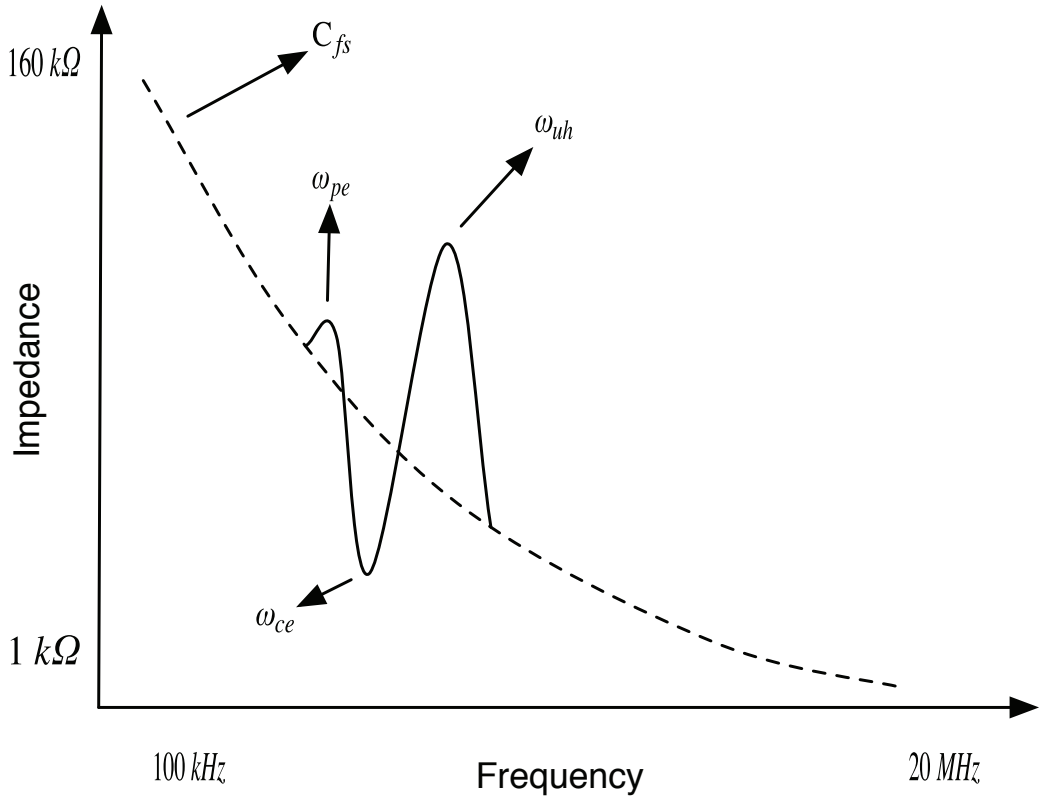

Fig. 2.1: Plasma characteristics across the operating frequency range.

A block diagram of the instrument is shown in fig. 2.2. The Direct Digital Synthesizer (DDS) generates a sine wave output signal that is sensed by the sensor box, which consists of a capacitance bridge, amplifiers, rectifiers, and a differential amplifier. A Programmable Logic Device (PLD) is used to control the frequency synthesis of the DDS signal. The Sensor Box output is sampled by an Analog-to-Digital Converter (ADC). Sampled data is communicated to a ground station via the digital telemetry link (TM). Plasma electron density was found by generating a resonance curve over a wide range of frequencies. It was measured with an uncertainty of less than 5%. However, the upper limit of the frequency sweep (12.5 MHz) was limited by the DDS clock frequency of 25 MHz. Resonance frequencies could exceed 12.5 MHz and appear up to 20 MHz.

Blackwell [12] generated plasma impedance curves in a controlled plasma environment using a network analyzer and a spherical RF probe as shown in fig. 2.3. Tungsten filaments are used to create a uniform and ionized plasma in the vessel. The main drawback of

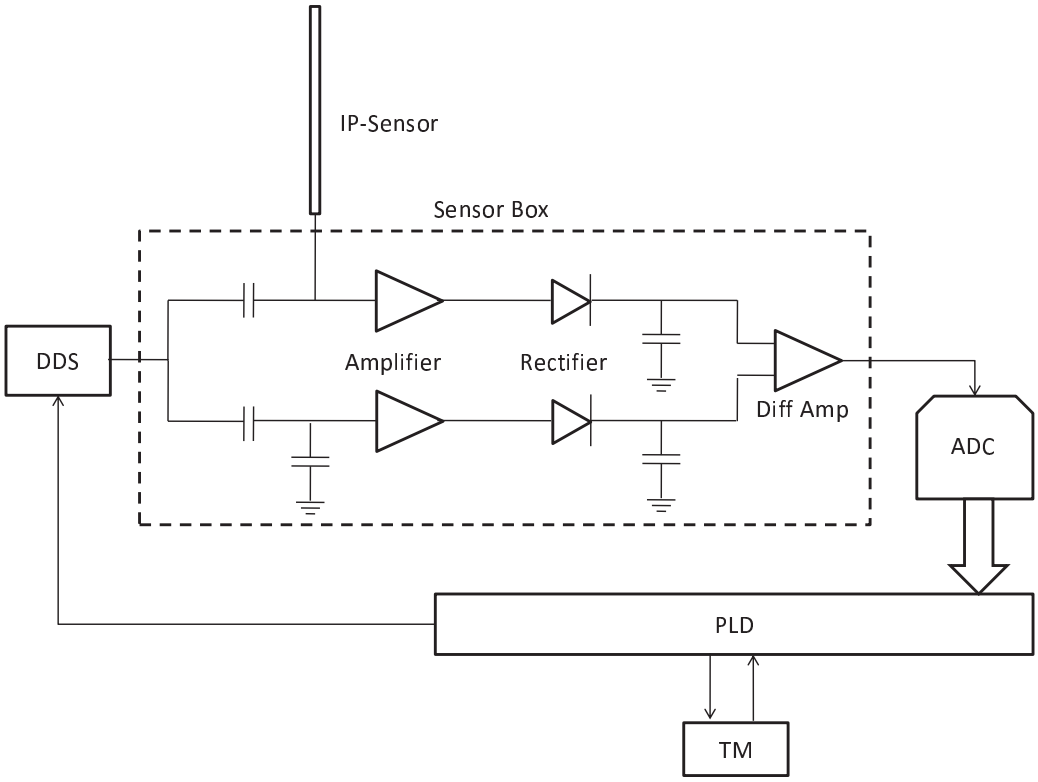

Fig. 2.2: Stegies's PIP instrument.

using this technique is that it requires intensive calibration of the network analyzer. Several trials of different coax cables and matched loads had to be tested carefully to generate the expected results. Also, errors in impedance measurement were introduced by reflected radiation from objects near the probe and generation of standing waves at high frequencies.

Hummel [13] described a quadrature detection technique, depicted in fig. 2.4, that measures the real and imaginary parts of an impedance to extract its magnitude and phase. In-phase and quadrature sampling are performed by two ADCs driven by a sine and cosine DDS signals, respectively. The transimpedance amplifier, with a feedback resistor R_f, and a difference amplifier construct the signals

$$v_p \approx v_c, \tag{2.6}$$

$$v_x \approx v_c + R_f i_p, \tag{2.7}$$

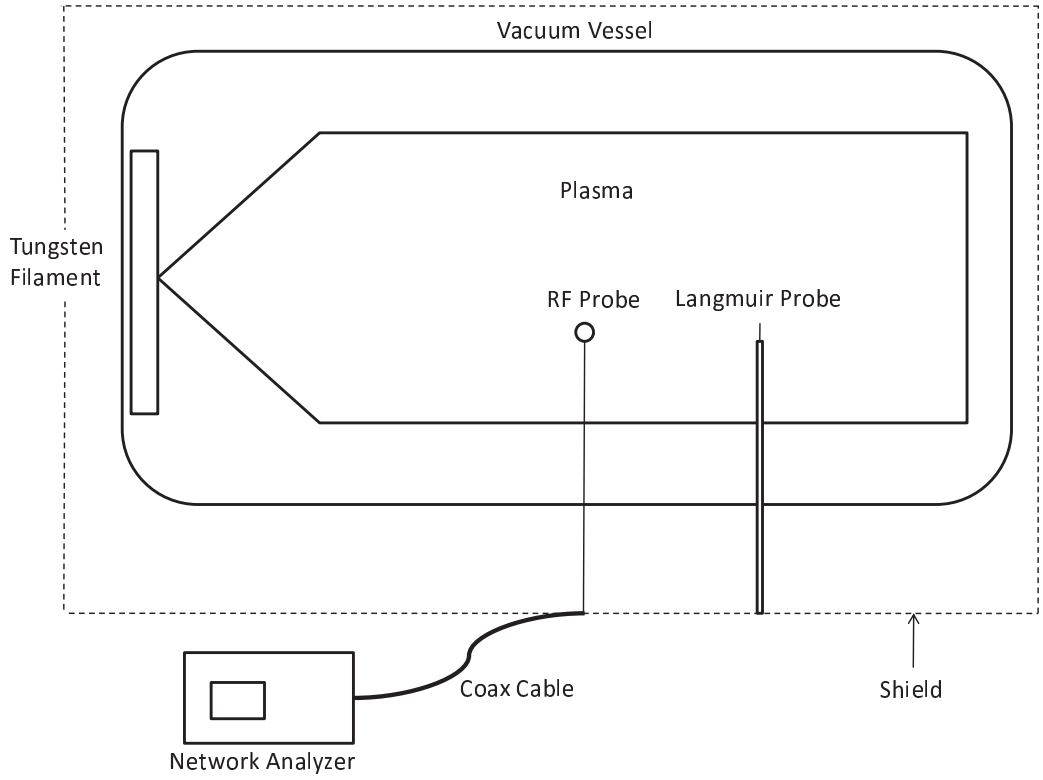

Fig. 2.3: Blackwell's PIP instrument.

$$v_z \approx R_f i_p = R_f \left(\frac{v_c}{Z_a} \right), \tag{2.8}$$

where v_p is the stimulated plasma voltage, v_c is the DDS cosine signal, v_x is the transimpedance output, i_p is the plasma current, v_z is the difference amplifier output, and Z_a is the antenna impedance. The comparator creates a square wave that serves as the clock of the ADCs. Clock dividers are used to ensure that the sampling rate does not exceed the ADC's specs. Frequency synthesis and clock division are both controlled by the Field Programmable Gate Array (FPGA). This technique, however, requires two precise and accurate DDS units that should generate signals with 90 degrees phase difference. Also, note that clocking the ADC at a sampling rate lower than the maximum tends to degrade its performance by losing resolution. A thorough analysis of the quadrature PIP instrument was performed by Sanderson [14]. He reported that the instrument reliability was limited by transient errors and imperfections in the probe's sinusoidal stimulus produced by the

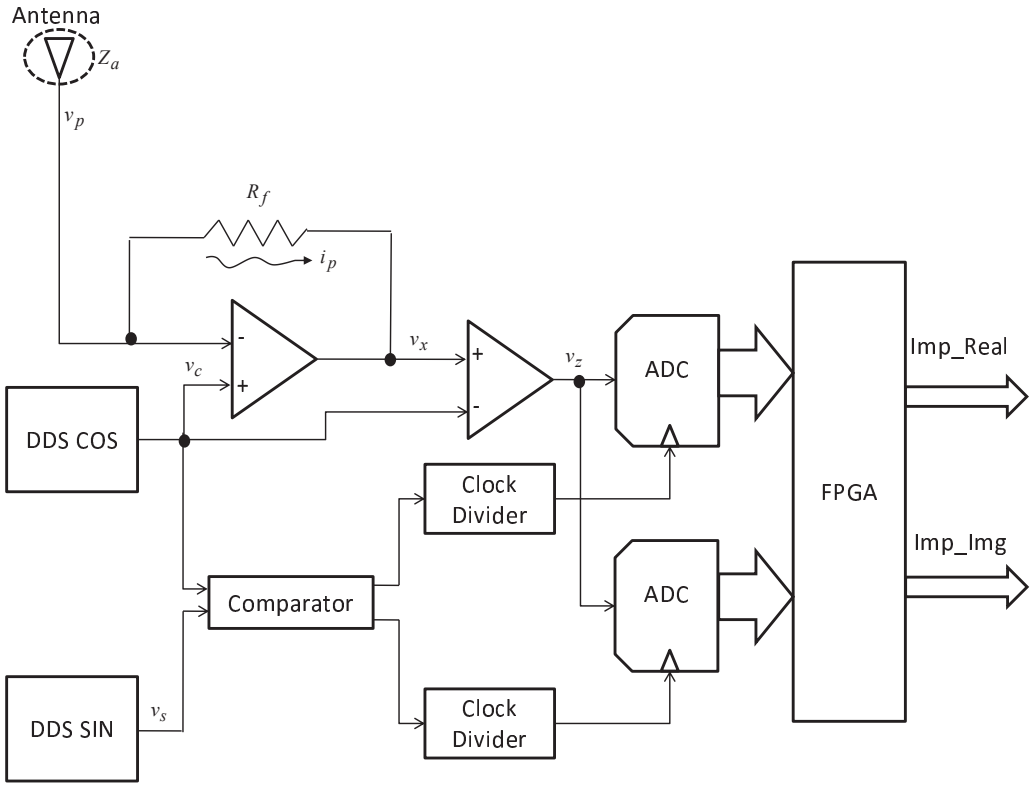

Fig. 2.4: Hummel's quadrature PIP instrument.

DDS. This affected the accuracy and stability of the quadrature PIP.

2.3 Proposed Integrated PIP System

The proposed PIP architecture is shown in fig. 2.5. The impedance probe's potential is driven by a sinusoidal stimulus generated by a DDS at a specified frequency. The resulting probe current is sensed by using a transimpedance amplifier. The governing equations describing the system are

$$v_p \approx V_{DDS,} \tag{2.9}$$

$$v_x \approx V_p + i_p Z_f, \tag{2.10}$$

$$v_z \approx Z_f i_p = \left(\frac{Z_f}{Z_a}\right) V_{DDS}, \tag{2.11}$$

where V_{DDS} is the DDS output voltage, and Z_f is the transimpedance feedback impedance which consists of a parallel RC circuit. The amplifier's output voltage is subtracted from the

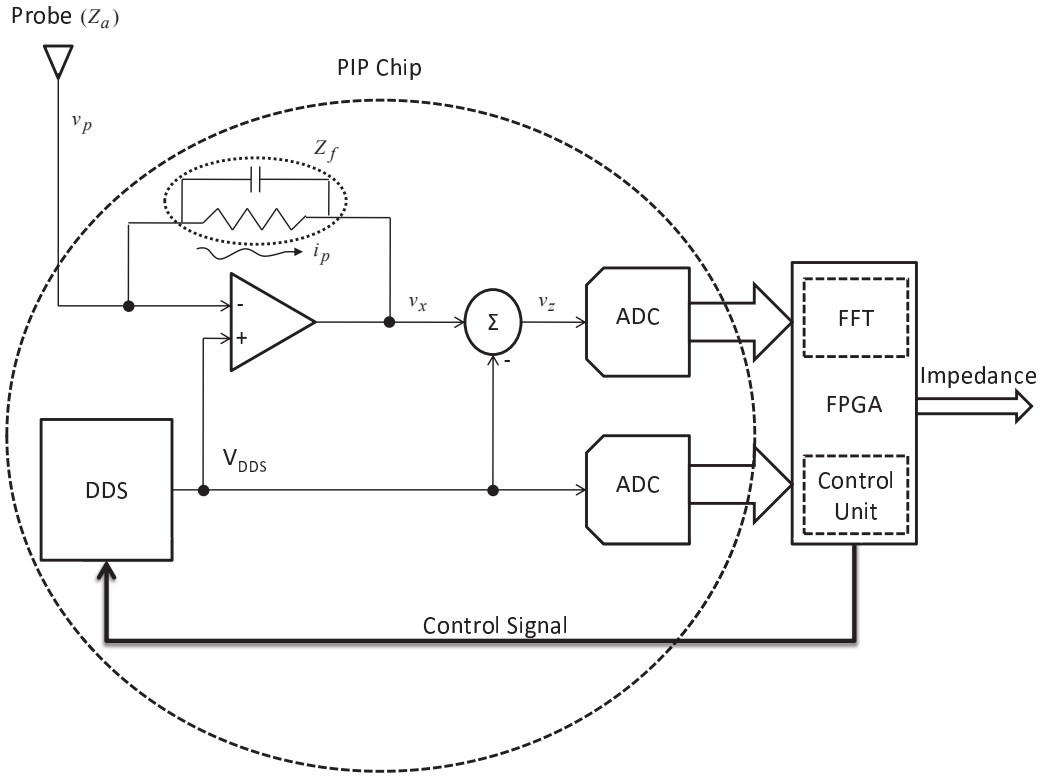

Fig. 2.5: Proposed PIP instrument.

DDS voltage through a difference amplifier to isolate $i_p Z_f$ at the ADC input. This signal as well as the DDS signal are both sampled by matched ADCs, and are then passed to the FPGA for further signal processing. In contrast to previous PIP designs, the integrated PIP samples the probe's current and voltage directly. This procedure relaxes error tolerances and eases the requirement of pure sinusoidal waveforms from the DDS. This allows us to tolerate low resolution and moderate jitter in the DDS design. The off-chip FPGA performs a Fast Fourier Transformation (FFT) operation on both of the signals at the fundamental frequency (DDS output frequency). The two outputs are then divided to generate the corresponding plasma impedance and phase. The FFT operation is insensitive to transient spikes and suppresses noise introduced by the system and its surrounding circuitry. The whole operation is then repeated by sweeping the DDS frequency from 100 KHz to 20 MHz. This operation is performed by a control logic unit that is programmed on the FPGA.

To quantify the error tolerances in the proposed design, a model of the ADC and the

FFT were designed using Matlab and Simulink. Monte Carlo simulations were applied to predict the impact of the ADC component errors on the overall instrument's accuracy. The ADC characterization will differ from conventional approaches in that performance and accuracy are measured with respect the instrument's final output, i.e. the fundamental component measured by the FFT. Conventional, general-purpose ADCs are concerned with the device's behavior across the whole frequency spectrum. Because we are only interested in the fundamental, we can relax some of the system's error tolerances while tightening others. Our analysis will focus on errors in the impedance measurement at a specific input frequency, while disregarding distortion appearing at other frequencies. Distortion effects caused by glitches and transient spikes are filtered out by the FFT operation.

The complete PIP system was modeled and integrated with the ADC model. The overall modeled system included the physical plasma and probe model, the transimpedance amplifier, the DDS, the ADCs, the FFT operation, and the control logic unit. A whole frequency sweep was applied, and the errors' effect on the impedance calculation was evaluated. A Verilog-AMS model of the PIP chip was implemented and then cross-linked with Simulink to verify the whole instrument design at a detailed level of abstraction.

Chapter 3

Pipeline ADC Characterization

An ADC is a mixed-signal device that is used in various applications, such as radar, imaging, and communications. Its main role is to convert real-world analog data (input voltage or current) into the digital domain (binary representation) for digital signal processing. There are several ADC architectures which include: flash, successive approximation, pipeline, cyclic, two-step, and sigma-delta to name a few. Each has its advantages and disadvantages when it is evaluated against speed, accuracy, latency, area, and resolution [15–17]. For our PIP implementation, a pipeline ADC has been chosen. The reason for this choice is that the PIP needs to operate at input frequencies up to 20 MHz while still maintaining high accuracy. Pipeline ADCs are known to achieve medium-to-high resolution (in excess of 8 bits) at a conversion rate of several hundreds of megahertz [18–21]. Resolution can be increased by simply increasing the number of pipeline stages. In contrast to exponential area growth when scaling flash and other parallel architectures, pipeline ADC chip area grows linearly. Moreover, power consumption and some of the system accuracy requirements can be reduced by using a special technique known as Digital Error Correction, which will be discussed in the following section.

3.1 Pipeline ADC Overview

The pipeline ADC is a cascaded array of N individual stages where each stage consists of a Sample-and-Hold (S\H) block, an m-bit low-resolution stage-ADC, an m-bit low-resolution stage Digital-to-Analog Converter (DAC), an analog subtractor, and a 2^m gain amplifier. Figure 3.1 shows a block diagram of the pipeline architecture and of a single pipeline stage. The S\H samples the input voltage V_{in} at each clock cycle, holds the final sampled value, and then passes it to the input of the stage-ADC to produce a low-resolution

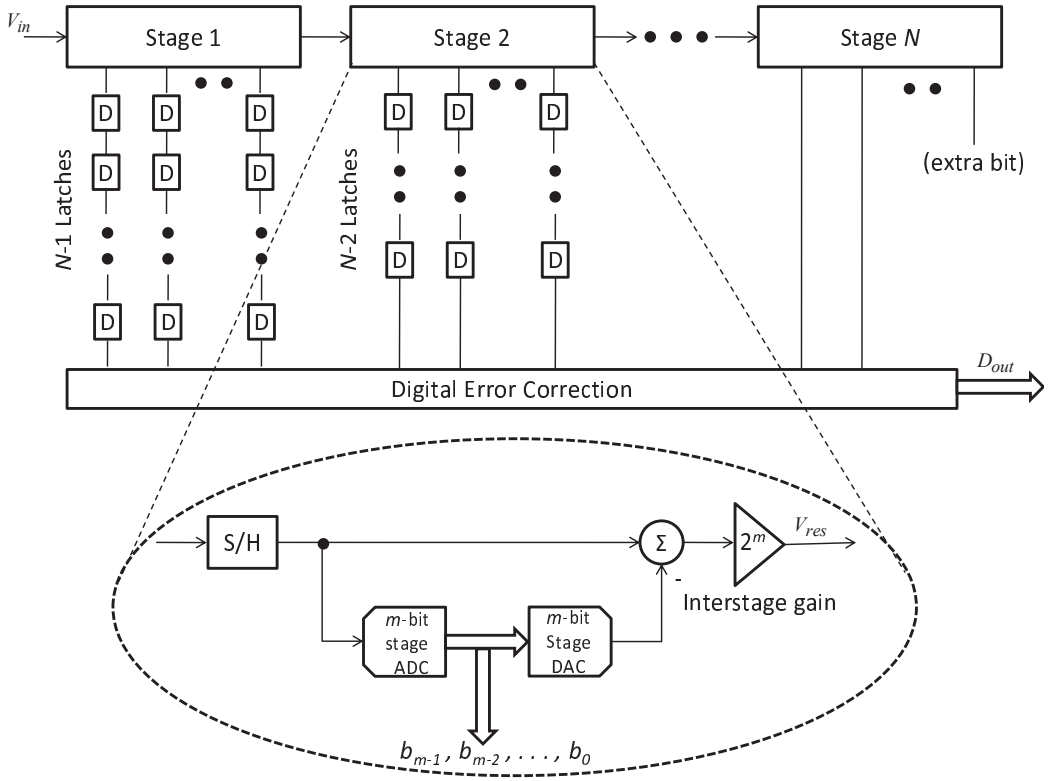

Fig. 3.1: N-bit pipeline ADC showing m-bits/stage implementation.

digital output word. The stage-DAC converts the digital output back to analog and subtracts it from V_{in} to yield the residue.

The output *residual voltage* is defined as

$$V_{res} = (V_{in} - V_{DAC})2^m, \tag{3.1}$$

where the gain of the interstage amplifier is set by the bit resolution of the stage-DAC. The amplifier restores the residue to $\pm V_{ref}$ (full-scale range), where V_{ref} is the reference voltage against which is compared the analog input. This ensures that all stages use the same input voltage range. On the next clock cycle, the residue of each stage is applied to the next stage for further quantization. This process continues until full quantization of the sampled voltage is achieved. Then the digital outputs from each stage are passed to the digital error correction algorithm, which performs addition by using a series of full adders to form the final digital output word D_{out}. Since no digital correction can be done after the last stage,

the least significant bit is ignored. Note that the stage-ADC outputs are delayed through digital latches (D blocks) so that D_{out} corresponds to the sampled input. The drawback of this architecture is that it initially generates D_{out} only after a specific latency, depending on the resolution or number of stages implemented. Ideally, the ADC should detect changes in the analog input voltage within one LSB (least significant bit).

$$LSB = \frac{V_{ref}}{2^N} \tag{3.2}$$

Thus, as the resolution increases, the ADC will still need to produce an accuracy that is capable to resolve very small possible changes (low LSB value) in the analog input voltage. For example, assume that the reference voltage is set to 1 V, then for a 16-bit converter the ADC has to resolve a 15.25 uV change in the input voltage. To achieve this specification, the first stage should be N-bit accurate, the second stage should be $N-1$ bit accurate, and the requirement for accuracy decreases linearly down the pipeline chain [22].

The speed and resolution of the pipeline ADC is heavily dependent on the settling time of the S/H and stage-DAC units. This means a high gain and fast operational amplifier (opamp) will be required. However, the need for high accuracy is required at the first stage, and the requirements can be relaxed for subsequent stages. The possibility of the need of less accuracy is because the following stage components' errors are scaled down by the previous interstage gain.

3.2 1.5-Bits/Stage Topology

Figure 3.2 shows the systematic flow for the 1.5-bits/stage implementation [23,24]. This topology is widely used in pipeline ADCs, because it relaxes the accuracy requirements on the stage-ADCs by introducing redundant bits. It can also achieve higher speed, since a lower interstage amplifier gain is used. The stage-ADC is composed of two comparators with ideal thresholds of $\frac{-V_{ref}}{4}$ (V_{ref-}) and $\frac{+V_{ref}}{4}$ (V_{ref+}). It supplies two output bits ($b_1 b_0$) for digital correction and code conversion. The stage-DAC acts as a multiplexor which selects whether to add or subtract V_{ref} from the input signal or take no action. The extra 0.5-

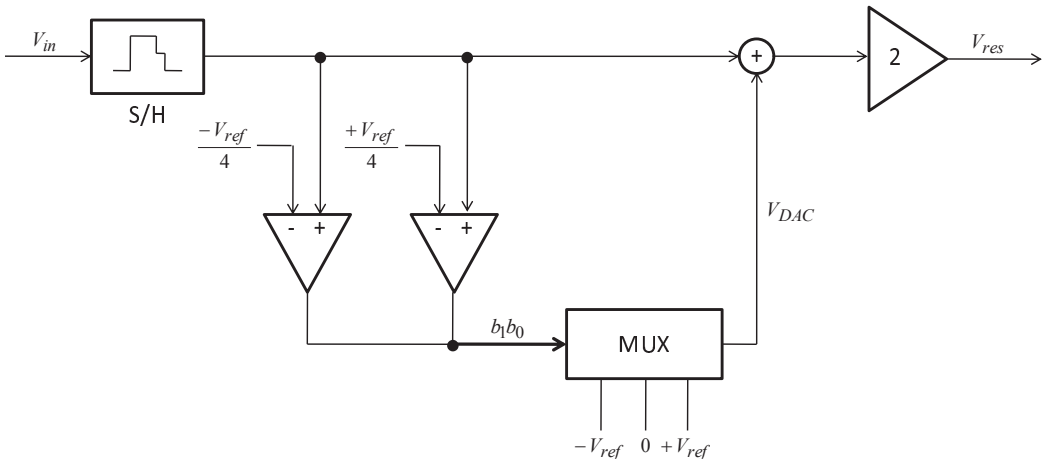

Fig. 3.2: 1.5-bits/stage system architecture.

bit redundancy is used to compensate for tolerances and imperfections in the comparators, which will be illustrated subsequently. This redundancy is later canceled out by digital error correction. Therefore, the 1.5-bits/stage can be thought of as a super 1-bit/stage, where the gain of the amplifier is kept at 2. A lower gain interstage amplifier increases the speed of the converter, because it maximizes bandwidth due to the gain-bandwidth trade-off. Table 3.1 summarizes the 1.5-bits/stage functionality.

An example, adapted from a presentation by Sanchez-Sinencio [25], graphically illustrating the 1.5-bits/stage architecture for an 8-bit pipeline ADC along with digital correction is shown in fig. 3.3. Symmetrical reference voltages of ± 1 V represent the full-scale range. Ideal comparator thresholds of $\pm 0.25\ V$ are chosen. A sampled input voltage of $V_{in} = 0.6\ V$ is considered. At the first stage, since $V_{in} > V_{ref+}$, the output bits are 10 and V_{in} is multiplied by 2 and then subtracted from V_{ref} to yield a residue voltage of $0.2\ V$. The rest of the procedure can be easily understood by following table 3.1. Bit addition is performed by using the ripple-carry adder algorithm, where each addition operation should wait for the

Table 3.1: 1.5-bits/stage truth table.

Condition	Digital Outputs (b_1b_0)	V_{DAC}	V_{res}
$V_{in} > V_{ref+}$	10	$+V_{ref}$	$2V_{in} - V_{ref}$
$V_{ref-} \leq V_{in} \leq V_{ref+}$	01	0	$2V_{in}$
$V_{in} < V_{ref-}$	00	$-V_{ref}$	$2V_{in} + V_{ref}$

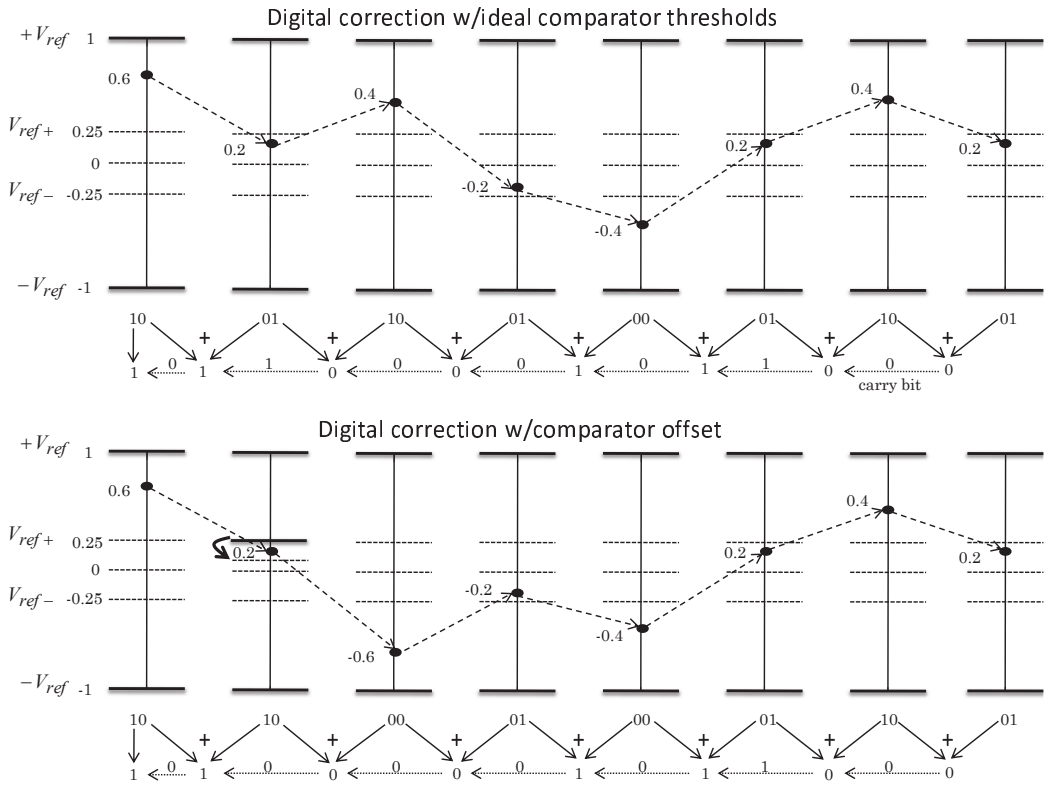

Fig. 3.3: An 8-bit 1.5-bits/stage example showing how digital correction corrects the final digital output for a comparator offset in the second stage. Refer to table 3.1 to understand the transitions from stage to stage.

carry bit calculated from the previous addition. For the nonideal case, a negative voltage shift to V_{ref+} at the second stage gives an incorrect two-bit output. However, this error is corrected by the third stage, and following that the residue voltage takes on the same path as in the ideal case. Both cases generate the same output word. Hence, this architecture relaxes the requirements of the stage-ADC to a maximum offset of $\frac{V_{ref}}{4}$, since any additional offset will cause the residue voltage to exceed the V_{ref} rails. This entitles us to use low-precision comparators to reduce power consumption and complexity.

3.3 AC and DC Specifications

In order to fully characterize the pipeline ADC for the proposed PIP instrument, it is necessary to outline what specifications set the benchmark and measure the performance of an ADC. These specifications (specs) are divided into two categories: AC (dynamic) and

DC (static) domains. As will be explained soon, INL and DNL are DC specs, while SNR, THD, SINAD, and SFDR are AC specs. These are the primary specs, but various less significant specs exist [26].

3.3.1 Integral Nonlinearity (INL)

INL describes the linearity of a realistic transfer curve by measuring the difference between its digital output transition points and a reference straight line. The two most common methods for INL testing are the "best-fit" method and the "end point" method. The latter measures INL by drawing a straight line between the end points of the ADC transfer curve, and calculating the deviation from the midpoint of each digital output to the output value of the straight line at that same point. The two points are at 0.5 LSB before the first output transition and 0.5 LSB after the last output transition. This method is shown for a 3-bit ADC in fig. 3.4. As for the best-fit method, the straight line is constructed so that it best fits the transfer curve by passing it through most output codes. Therefore, this method minimizes INL error and is less stringent than the end point method, which reports worst or maximum INL measured. Thus, the end point is more widely used because it is considered to be a more reliable measurement. The INL standard unit is stated in $LSBs$.

3.3.2 Differential Nonlinearity (DNL)

DNL is the deviation between the code-code step size transitions (width of each transition) of a real converter transfer curve and an ideal one. In an ideal ADC converter, the transitions occur exactly 1 LSB apart. If a DNL of ≥ 1 LSB or ≤ -1 LSB is measured, then a code transition is missing and it is identified as a missing code. In other words, a missing code appears when no output code corresponds to an input voltage. For example, a datasheet stating that it guarantees no missing codes for an N-bit ADC should have 2^N code transitions across the whole full-scale operating range. DNL measurement of a 3-bit ADC is shown in fig. 3.4. It can be seen that with a DNL of 2.1 LSB, a missing code appears at 100. To ensure a true N-bit resolution, a converter should exhibit an INL and

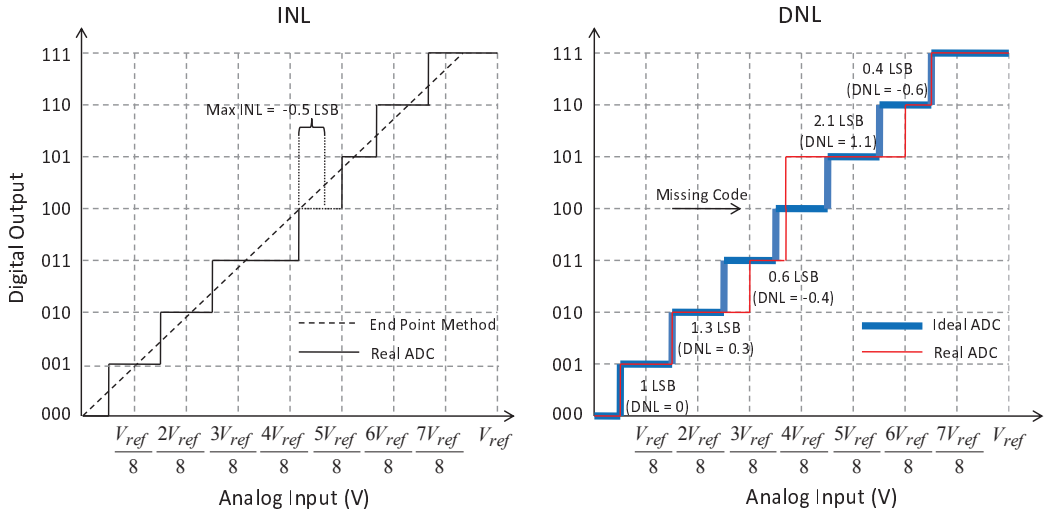

Fig. 3.4: INL and DNL for a 3-bit ADC.

DNL of no more than $\pm 0.5\ LSB$ [26].

Because of the complex phenomena of ionospheric plasma, the PIP instrument has to measure abrupt changes in the plasma impedance; therefore, a high resolution ADC is needed to detect these sudden and small impedance deviations. Hence, special care should be taken when setting the INL and DNL specs, so that we do not lose bit resolution.

3.3.3 Signal-to-Noise Ratio (SNR)

SNR is defined as the ratio of the sinusoidal input signal power to the effective input-referred noise power level. It is expressed in dB and represented by the function

$$SNR = 10 \log \left(\frac{P_{sig}}{P_{noise}} \right), \tag{3.3}$$

where P stands for the average power integrating over a period of the input sinusoid. The output noise in an ADC is generally generated by the quantization process and clock jitter. Quantization error result from the process of assigning an accurate analog input voltage to a discrete limited precision digital output code. However, this type of error can be reduced by increasing the converter's resolution, since a smaller LSB value is used. As the value of LSB decreases, the full-scale voltage is divided into smaller increments achieving better

accuracy and precision. In ideal ADCs, the SNR is typically estimated using the following equation:

$$SNR = 6.02N + 1.76 \ [dB] \,. \tag{3.4}$$

It is evident from (3.4), that the resolution of the ADC is related to SNR. For example, an ideal 10-bit ADC would have an optimum SNR of 61.96 dB. Also, it can be used to find the Effective-Number-of-Bits (ENOB), which specifies the true-bit resolution of an ADC. And so, if the same 10-bit ADC had a real SNR value of 56 dB instead of 61.96 dB, then its ENOB is 9 bits. Hence, the real 10-bit ADC performs as an ideal 9-bit ADC. Since a low SNR would increase the noise floor seen at the FFT spectrum output [27] and eventually corrupt the fundamental signal, it is of critical importance to assure reliable measurement. A high SNR ratio would make the device less sensitive to variations in temperature, wind, and gravitational force found in the ionosphere.

Clock jitter is the time variation in the rising and falling edges of the clock signal. Since an analog input is sampled at every clock rising edge, with a timing error we could end up sampling the incorrect input voltage. This uncertainty degrades the overall ADC performance. Clock jitter is usually caused because of improper clock routing and layout. A poor clock signal trace might couple with other electrical sources that modulates the timing of the signal. Also, noise from other analog sources can couple into the clock path. That is why the digital clock line is usually shielded in a mixed-signal chip. The maximum tolerable peak-to-peak (or cycle-to-cycle) jitter (ΔT_{pp}) allowed in ADCs is determined by using

$$\Delta T_{pp} \leq \frac{V_{in}}{2^{N+1} V_{FS} \pi f_{in}} \ [secs] \,, \tag{3.5}$$

where V_{FS} is the full-scale voltage, and f_{in} is the input sinusoidal frequency. If we assume the input voltage is equal to the full-scale voltage ($V_{in} = V_{FS}$), then as f_{in} increases, ΔT_{pp} decreases and becomes more of a concern. Therefore, SNR performance degrades at higher frequencies. This is the reason why most datasheets report measurement performances for several input frequencies. If (3.5) is violated, the SNR would degrade significantly, since its

performance at high frequencies is dominated by the clock jitter of the system clock. SNR and clock jitter are illustrated in fig. 3.5.

Other sources of noise can contribute to degrade the SNR performance. The quantization noise and the effective input noise are considered to be the most critical. The following equation [28] relates the clock jitter, quantization noise, and effective input noise to SNR:

$$SNR = -20\log\sqrt{(2\pi f_a \Delta T_{pp})^2 + \frac{2}{3}\left(\frac{1+\epsilon}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_{noise}}{2^N}\right)^2}, \tag{3.6}$$

where f_a is the input sinusoidal frequency at full-scale input voltge, ϵ is the average DNL in $LSBs$, and V_{noise} is the effective input noise of the ADC. If $\Delta T_{pp} = 0$, $\epsilon = 0$, and $V_{noise} = 0$, (3.6) will reduce to (3.4).

3.3.4 Total Harmonic Distortion (THD)

THD is the ratio of the total root-mean-square (RMS) value of the first k harmonic components to the RMS value of the input signal amplitude. It is expressed as

$$THD = \sqrt{\frac{A_{2k}^2 + A_{3k}^2 + ... + A_{nk}^2}{A_k^2}}\ [dB], \tag{3.7}$$

where A_k is the RMS amplitude of the fundamental frequency component, and $A_{2k} - A_{nk}$ are the RMS amplitudes of the 2^{nd} through n^{th} harmonic components. The amplitudes are measured by using a spectrum analyzer. These harmonic components are caused by the nonlinearity existing in an ADC system; thus, it indicates the level of linearity associated with the converter. Since the input to the pipeline ADC is a sine wave, harmonics appear at integer multiples of the fundamental input frequency, as depicted in fig. 3.5. Ideally, the sine wave has one fundamental component centered at the input frequency. Most commercial ADCs take into account the first six harmonic spurs in calculating THD.

In our PIP design, the FFT operation filters out all frequency components above the fundamental. Since the harmonic components appear away from the fundamental, THD requirements can be relaxed significantly.

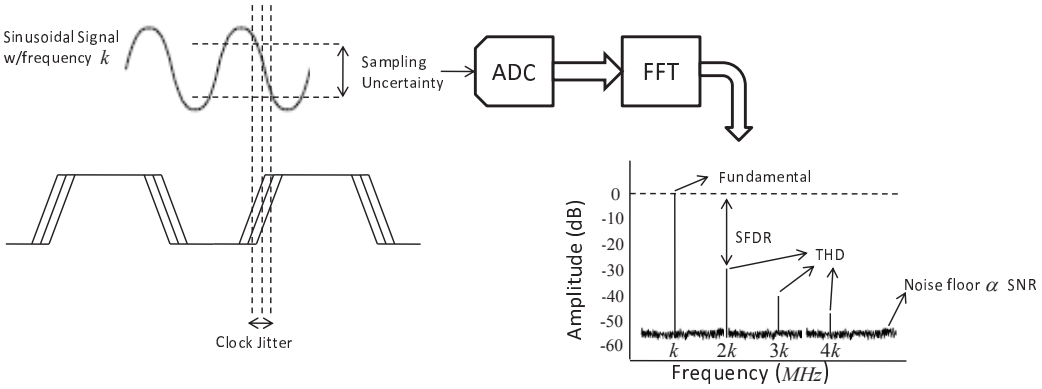

Fig. 3.5: Systematic signal flow showing clock jitter, SFDR, THD, and SNR.

3.3.5 Signal-to-Noise-And-Distortion (SINAD)

SINAD is the ratio of the RMS fundamental input value to the RMS value of all spectral components (noise and distortion) below the Nyquist frequency, including harmonics but excluding DC. Accordingly, SINAD measures the degree of quality of the output signal. It can be determined by either of the two following formulas:

$$SINAD = 10 \log \frac{P_{sig}}{P_{noise+distortion}} \; [dB] \,, \tag{3.8}$$

or

$$SINAD = 20 \log \sqrt{\left(10^{-\frac{SNR}{20}}\right)^2 + \left(10^{-\frac{THD}{20}}\right)^2} \; [dB] \,. \tag{3.9}$$

As can be seen from (3.9), SNR and THD are directly related to SINAD. Then, we can conclude that SINAD gives an overall measure of the quality of an ADC in the AC domain.

In general ADCs, SINAD is of vital importance. However, in our case, since the frequency distortion adds unequal degrees of amplification across all spectral components other than the fundamental, SINAD is not critical for the performance of the PIP's ADC.

3.3.6 Spurious-Free Dynamic Range (SFDR)

SFDR, as represented in fig. 3.5, is the difference between the fundamental signal amplitude and the amplitude of the highest spectral tone. The highest tone can be a

harmonic or a nonharmonic spur. Also, it can be expressed as

$$SFDR = 20 \log \frac{A_{signal}}{A_{highest\ tone}}\ [dBc\ or\ dBFS]\,, \tag{3.10}$$

where dBc is measured with respect to the fundamental amplitude, and $dBFS$ is measured with respect to the full-scale voltage range. The spurious signal has no effect on the fundamental, and the SFDR spec can be made less stringent. Nevertheless, it should be emphasized that the amplitude of the spurious component should not exceed that of the fundamental, resulting in a negative SFDR, since the FFT captures the highest amplitude at its output.

3.4 Pipeline ADC Model

A 1.5-bits/stage 16-bit ADC at a sampling frequency (f_{sample}) of 100 MHz was modeled using Matlab/Simulink. This behavioral model was developed by modifying a 10-bit ADC Simulink model [29]. It will be used to analyze the effect of pipeline ADC nonidealities on the fundamental component, which will be illustrated in sec. 3.5 and sec. 3.6, and it will serve as a key building block of the PIP instrument model. The model of each pipeline stage is based on the 1.5-bits/stage systematic architecture shown in fig. 3.2.

A Simulink comparator model with thresholds of $-0.25\ V$ and $+0.25\ V$ was used to model the stage-ADC, a three terminal switch with reference values of -1, 0, and 1 was used to model the stage-DAC, and a multiplier was used to multiply the output of the adder by 2. The S/H block was modeled using a zero-order hold block, and the digital error correction block is composed of delay blocks and an adder which combines the digital output of all 16 stages. V_{ref} is set to $\pm 1\ V$. A Matlab m-file is used to run the simulation and modify component parameters or add nonidealities to the system. Figures 3.6 and 3.7 show the FFT output for an ideal and a nonideal ADC, respectively. It is evident that by adding errors and variations to the ADC components, the power of the fundamental gets disturbed, and the noise floor along with the harmonic spectras increase significantly.

Post-processing data manipulation to obtain FFT, SNR, and other ADC specs is done

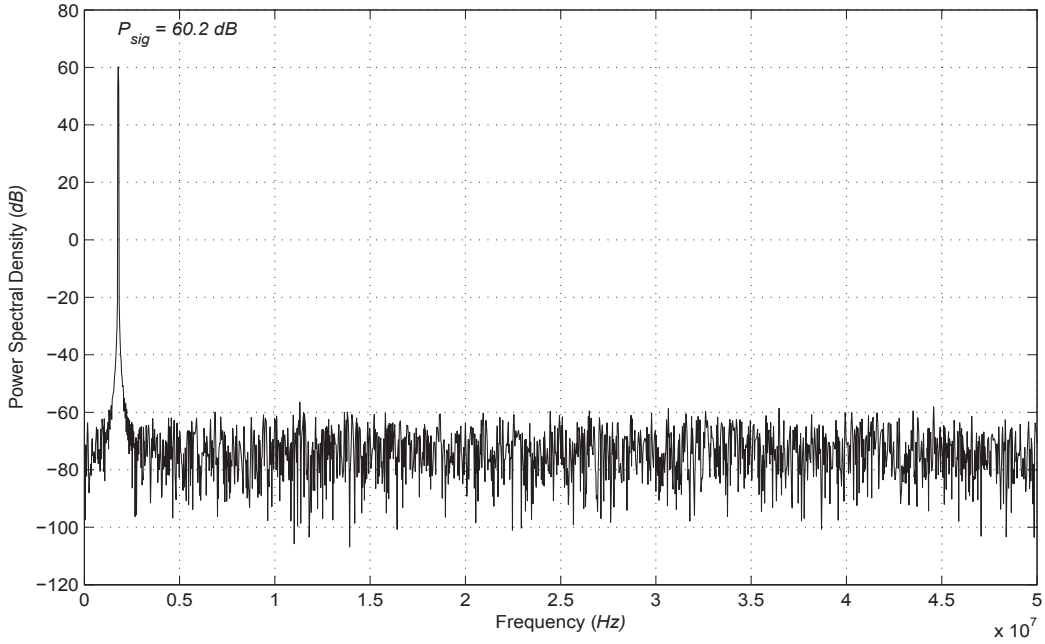

Fig. 3.6: FFT of the ADC output signal in the ideal case.

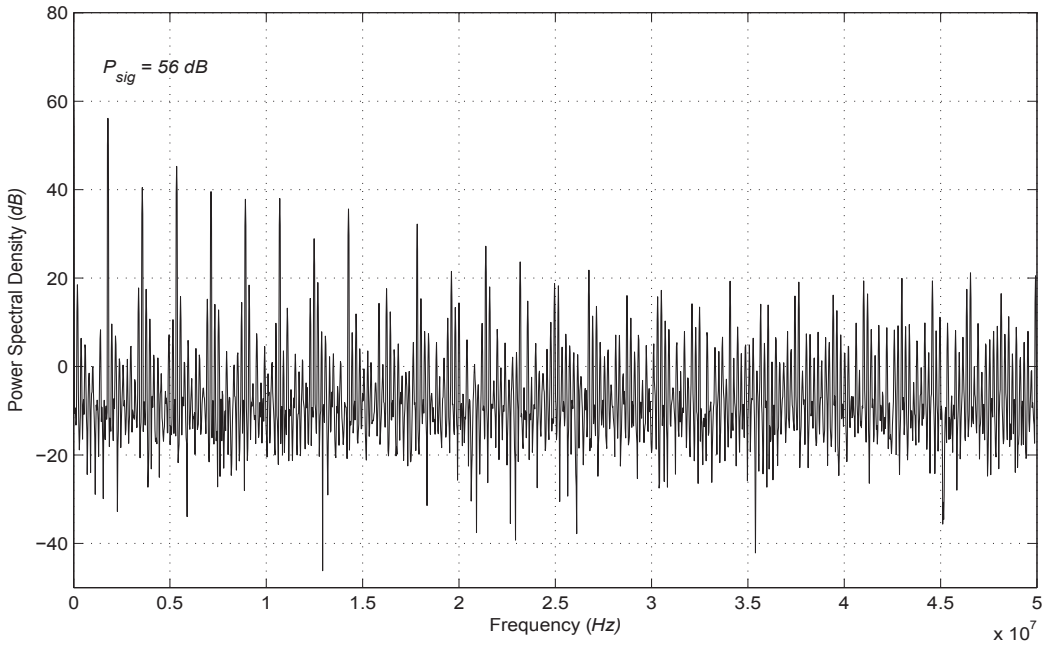

Fig. 3.7: FFT of the ADC output showing effect of errors on the fundamental component and on other frequencies.

using the SD toolbox [30]. Figure 3.8 shows the transfer characteristics of the residue at the output of the first stage. The dynamic range of the residue does not exceed the allowed limit, $\pm V_{ref}$, even with errors introduced to the comparators. Because of the half-bit redundancy in a 1.5-bits/stage architecture, low-precision comparators may be used, which alternately would save power and space.

3.5 Nonlinear Distortion

High speed ADCs are highly susceptible to nonlinear distortion. It is mainly caused by the switching mechanism at the S/H block, the pre-amplifier at the input of the ADC, the differencing amplifier, and by other sources of nonlinearity introduced at the ADC input. Since transistors are used as switches, their nonlinear resistance and parasitic capacitance introduce nonlinearity to the system. In sec. 3.7, THD is defined as a measurement of an ADC linearity. However, in contrast to THD, harmonics are unimportant for our design specs, since only the fundamental component is captured at each digitally swept frequency. This enables us to modify our design to boost its performance in one criterion, while loosening requirements in another. Our interest is focused on how much nonlinear distortion has an impact on the fundamental output magnitude.

A suitable method of modeling nonlinear distortion for a pipeline ADC is the sigmoid function. It is defined as

$$sig = \frac{1}{1 + e^{-\alpha x}}, \tag{3.11}$$

where x is the input, and α is a factor which controls the linearity of the sigmoid S shape curve. The S shape closely resembles a nonlinear behavior, yet modification is needed in order to have it centered around the origin and normalized between $\pm V_{ref}$. Modifying (3.11) will result in the following equation.

$$sig^{'} = \frac{\frac{2}{1+e^{-\alpha x}} - 1}{\frac{2}{1+e^{-x}} - 1} \tag{3.12}$$

A plot of the function $sig^{'}$ for $\alpha = 0.5$, 2 and 5 is shown in fig. 3.9. It can be visualized

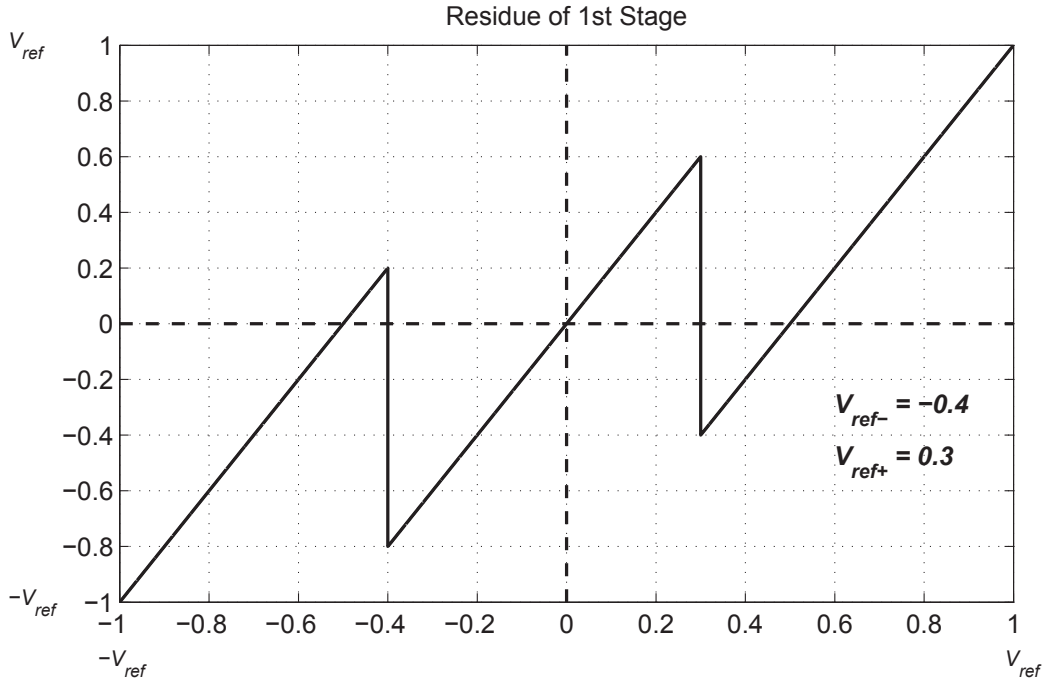

Fig. 3.8: Transfer curve of first stage with comparator threshold offset.

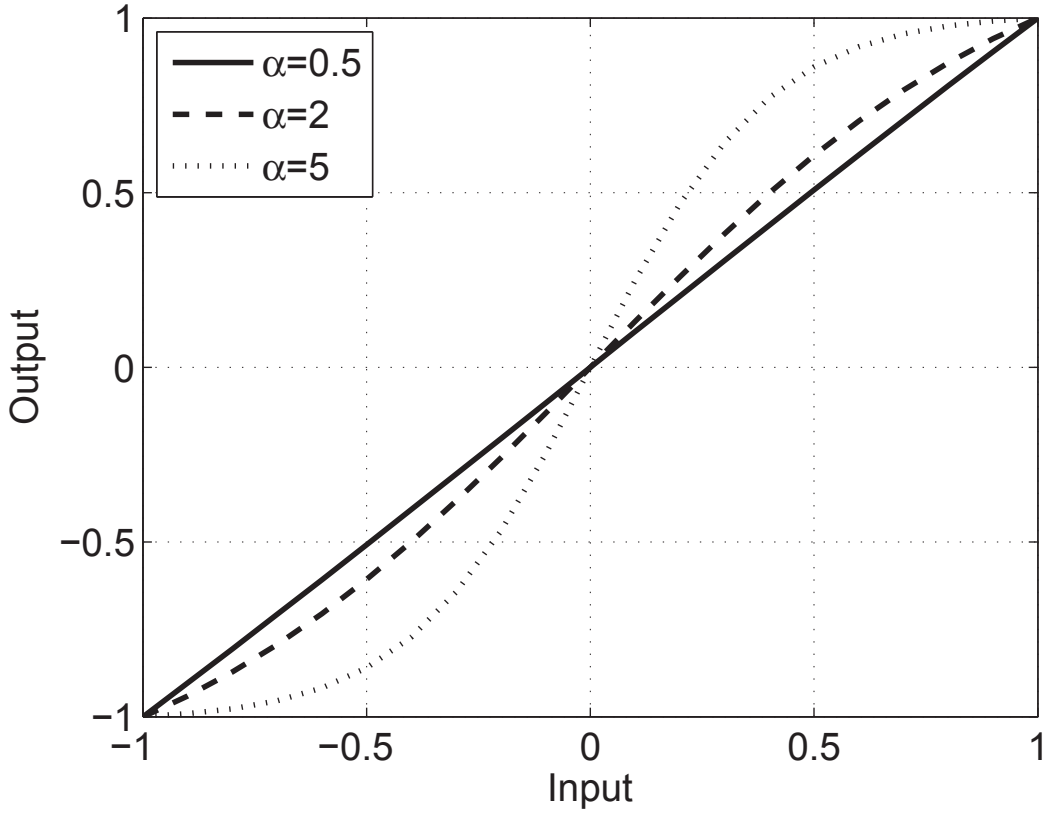

Fig. 3.9: Modified sigmoid curve for α= 0.5, 2, and 5.

that as α increases, the curve becomes more threshold-like at 0. Thus, we can use $sig^{'}$ to model the nonlinearity at the ADC input by passing a sinusoidal signal through it. We also consider an alternative quadratic model of nonlinearity. The S/H, DAC, and gain circuitry are mainly composed of CMOS switches and opamps. Both components are designed in a fully differential configuration, since it eliminates common-mode voltage offsets and corrects mismatches in the circuit [31]. The differential pair configuration has a quadratic dependence on the input differential voltage, and it can be represented by a nonlinear quadratic function of the form

$$Q = \frac{\alpha x}{\sqrt{1 + (\alpha x)^2}}. \tag{3.13}$$

Figure 3.10 shows the percentage error of the magnitude of the fundamental with respect to α for the sigmoid and quadratic methods. A jittered sinusoidal signal with an amplitude (A) of 1 V at a frequency (f_{in}) of 5 MHz and a clock jitter (ΔT_{pp}) of 10 ps was used. Random offsets within 1% standard deviation (σ) of the nominal value were applied to the ADC thresholds, DAC reference levels, and the gain amplifier at each stage.

The digital output word was passed through an FFT block, and then the magnitude of the fundamental was recorded for each α as it was swept from 0.001 to 5, meaning from highly linear to nonlinear. It is evident that as α increases, the percentage error increases in a similar manner for both models. The quadratic model represents the nonlinearity of a differential pair operating in strong inversion. The sigmoid model applies to a pair operating in weak inversion. Depending on the bias current, the actual nonlinearity is expected to shift between these two models.

In practice, we could get a close approximation by choosing either one of the models and selecting a best-fit α value. By using this method, the induced error is predictable and can be removed by calibration. Also, since the nonlinearity model of the differential pair proved to have the same effect as the sigmoid function, we can use the sigmoid function as a reference when measuring how much nonlinearity is exhibited by the system.

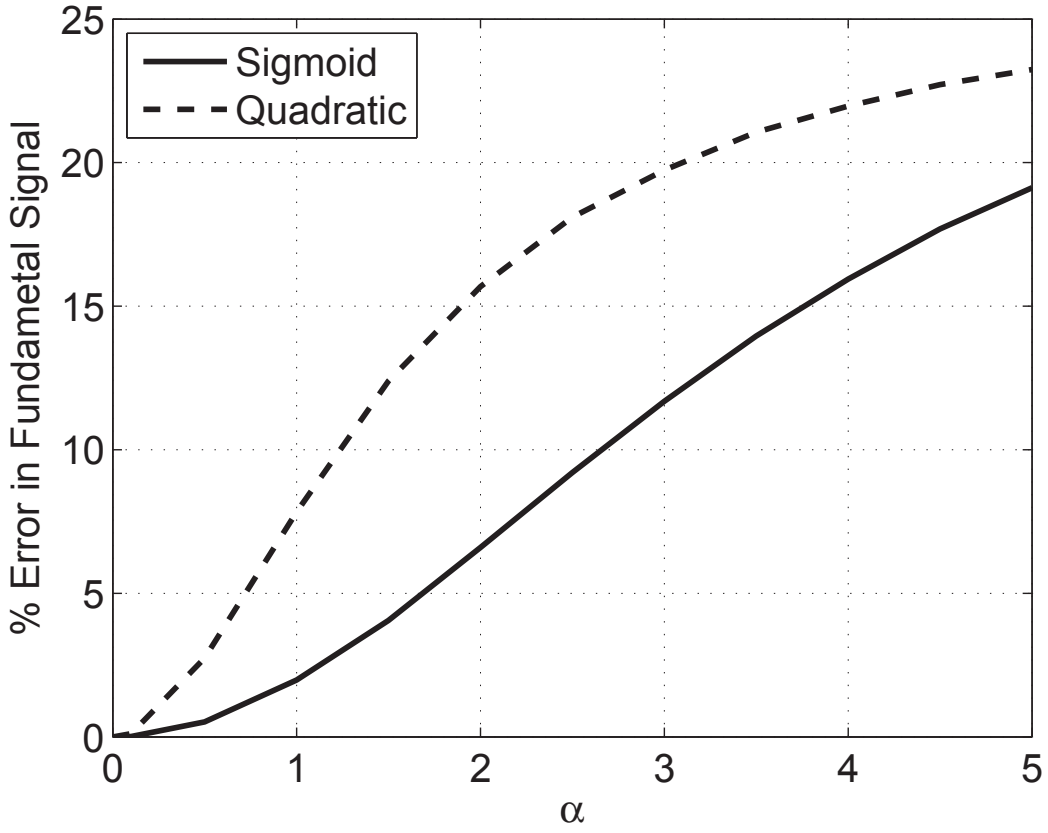

Fig. 3.10: Percentage error of fundamental signal w.r.t to α for the sigmoid and quadratic function.

3.6 Issues with Nonideality and Instrument Accuracy

The previous section focused on how nonlinear distortion at the input of the ADC affects the fundamental signal. The next step is to examine which ADC components have a large impact on the fundamental signal. In a pipeline ADC, most errors occur at the comparator, DAC, and interstage gain units. These variations might contribute to incorrect output. Also, unpredictable parametric variations resulting from the fabrication process might have an impact on the output magnitude as well. Both sets of nonidealities will be studied shortly.

3.6.1 Yield

CMOS device fabrication is a complex process, which consists of multiple steps and procedures. Thus, there is a high chance that the manufactured chip will have some de-

ficiencies. Therefore, it is important to estimate the probability that the manufactured test chips will fail to meet the required specs. Parametric variation due to the fabrication process will be modeled as random offsets added to the comparator thresholds, DAC reference levels, and the gain amplifier at each stage. These offsets result from transistor and capacitor layout mismatch.

A Monte-Carlo simulation of 100 runs, equivalent to 100 test chips, was performed. A sine wave with $A = 1\ V$, $f_{in} = 1.5\ MHz$, and $\Delta T_{pp} = 10\ ps$ were applied to the input of the ADC. The histogram of Δ_{out}, percentage output error, is shown in fig. 3.11 for all 100 test chips. The random offsets were generated by a Gaussian random-number generator, where σ of each error is fixed at 1%. For $V_{ref} = \pm 1\ V$, a 1% standard deviation accounts for a ± 10 mV voltage variation. The output distribution shows that 85 of the custom-built chips lie from and below the 5% error region, and that all chips lie below the 25% error region. This procedure allows the designer to predict the probability that the output magnitude will lie outside its maximum tolerable value, due to fabrication deficiencies or design inaccuracies. This analysis can be extended to any ADC architecture.

3.6.2 Offset Effect on Fundamental Output

Stage-ADC, DAC, and gain nonidealities are the main factors that cause performance limitations of the pipeline ADC. As discussed at the beginning of sec. 3.6, it is essential to study the effects of each of the nonidealities on the accuracy and precision of the fundamental output. This is critical to the overall reliability and performance of the PIP system.

A Monte-Carlo simulation was performed by varying σ for each nonideality separately. For this test, the pipeline ADC was fed a sinusoidal signal with $A = 0.1\ V$ and $f_{in} = 1.5$ MHz. A low input voltage was chosen because the PIP instrument may need to resolve input signals below the full-scale range. Hence, it will be beneficial to know how precisely the pipeline ADC measures the fundamental output under this condition with random offsets being added.

Figure 3.12 shows the effect of varying the standard deviation of each of the nonidealities, varying one while keeping the others fixed, on the fundamental output. σ_{out} is the

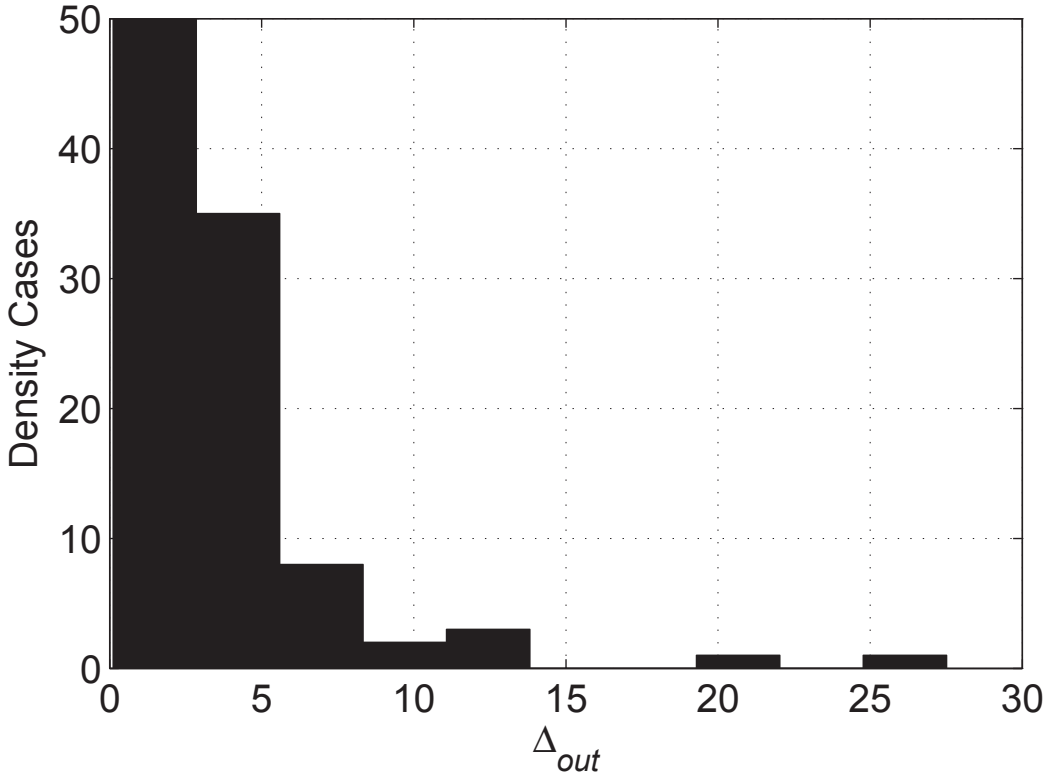

Fig. 3.11: Distribution of percentage errors of the fundamental output for all 100 test chips. σ for random offsets is set at 1%.

standard deviation of the fundamental output from its ideal value, and $\sigma_{relative}$ is the relative standard deviation of the nonideality being simulated. The figure shows that the DAC has the highest influence on the fundamental error, which increases as its standard deviation increases. The gain amplifier stage has a less effect on the fundamental output, but increases in the same manner as for the DAC. Notice that offsets added to the comparator thresholds do not affect the fundamental output at all. The reason for this is related to the 1.5-bits/stage architecture. As discussed previously in sec. 3.2, the extra half-bit redundancy relaxes the requirements for accurate comparators. Mismatched capacitors in the DAC and the gain stage are the main cause of offset errors. Therefore, it is important to try to match these capacitors as accurately as possible using techniques such as capacitor error averaging [22] in the schematic design phase, and common-centroid for the layout.

Since the PIP system might operate across the full input voltage range, a study is needed to examine the effect of errors on the fundamental output throughout that range.

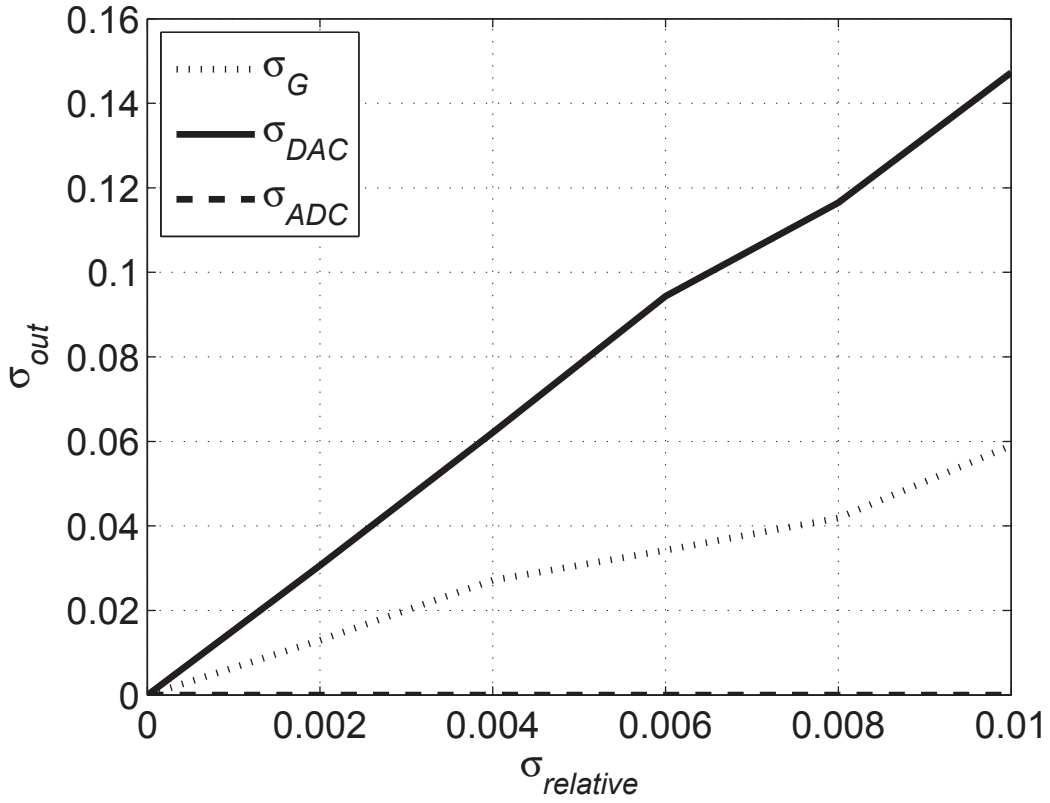

Fig. 3.12: Output standard deviation versus relative standard deviation for offsets at stage-ADC, DAC, and gain stages.

Figure 3.13 shows the output error as a function of the input signal amplitude A against the fundamental output. Clearly it is visible that a high impedance deviation occurs at very low input voltages and decreases exponentially as A increases. Note that as A exceeds 0.1 V, the percentage error becomes very close to zero. Moreover, the results showed again that DAC offsets affect the fundamental output mostly followed by the interstage gain error. The sub-ADC still has no influence on the fundamental output at any input voltage level. Much consideration is needed if our PIP system will operate below 100 mV.

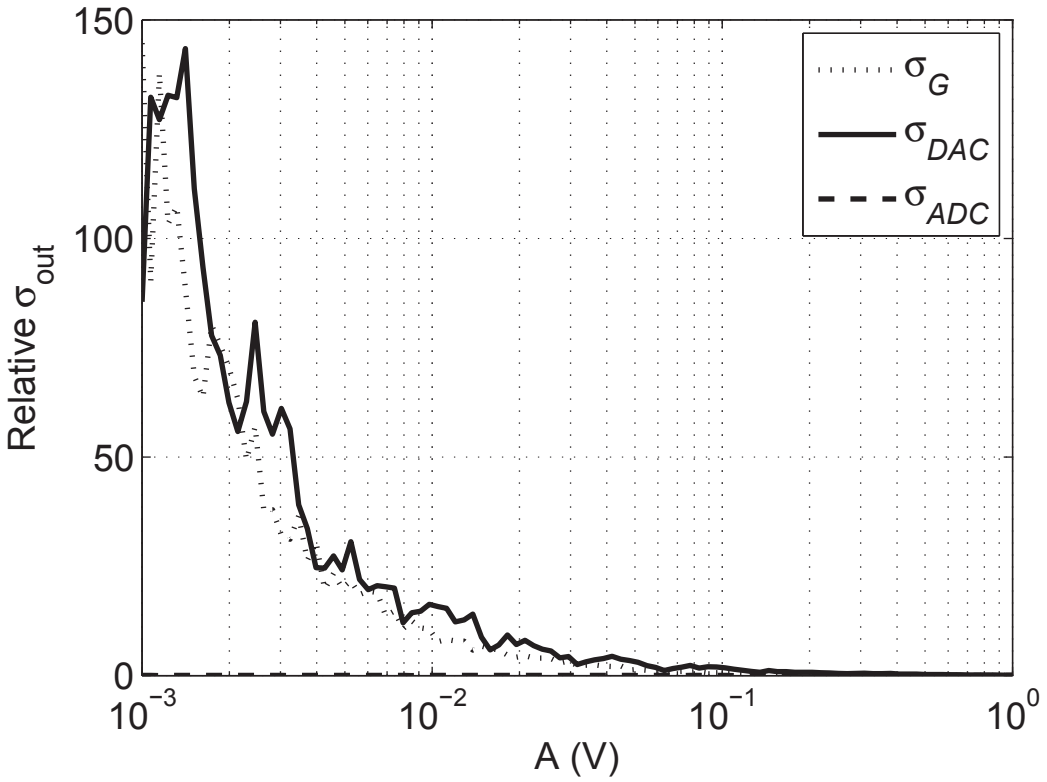

Fig. 3.13: Normalized output standard deviation versus input amplitude for offsets at stage-ADC, DAC, and gain stages with $\sigma = 1\%$.

Chapter 4

PIP Instrument Implementation

In Chapter 3, the effects of the pipeline ADC nonidealities on the fundamental output have been studied thoroughly. In this chapter, behavioral models of the building blocks of the rest of the PIP instrument will be described and built. These blocks are the DDS, control unit, plasma antenna probe, and the transimpedance amplifier. These sub-systems will then be integrated with the pipeline ADC model to form the PIP instrument model.

4.1 Plasma Antenna Probe Model

The plasma antenna model [32] is implemented in Simulink in the Laplace transform domain as

$$Z_a(s) = \frac{1}{s}\left(\frac{s^2 + as + b}{s^2 + cs + d}\right), \tag{4.1}$$

where s is the Laplace transform complex argument, and a, b, c, and d are the model's coefficients. The term $\frac{1}{s}$ models the free-space capacitance curve. The coefficients are made complex by setting $c^2 - 4d < 0$ and $a^2 - 4b < 0$. The complex conjugate poles set by a and b represent the electron cyclotron frequency, and the complex conjugate zeros set by c and d represent the upper hybrid frequency. The plasma electron frequency was neglected because of its negligible impedance deviation; a, b, c, and d were chosen through a least mean square fitting procedure against the Balmain impedance formula. As a result, (4.1) evaluates to

$$Z_a(s) = \frac{5.5e^{11}s^2 + 7.873e^{17}s + 6.854e^{24}}{s^3 + 4.969e^6 s^2 + 6.256e^{13}s}. \tag{4.2}$$

The magnitude and phase of $Z_a(\omega)$ across the operating frequency range is shown in fig. 4.1. As expected, the magnitude of the antenna impedance, $\|Z_a\|$, is capacitive at frequencies below $\omega_{ce} \approx 0.55\ MHz$ and above $\omega_{uh} \approx 1.3\ MHz$ with a phase $\theta_a \approx -90^o$.

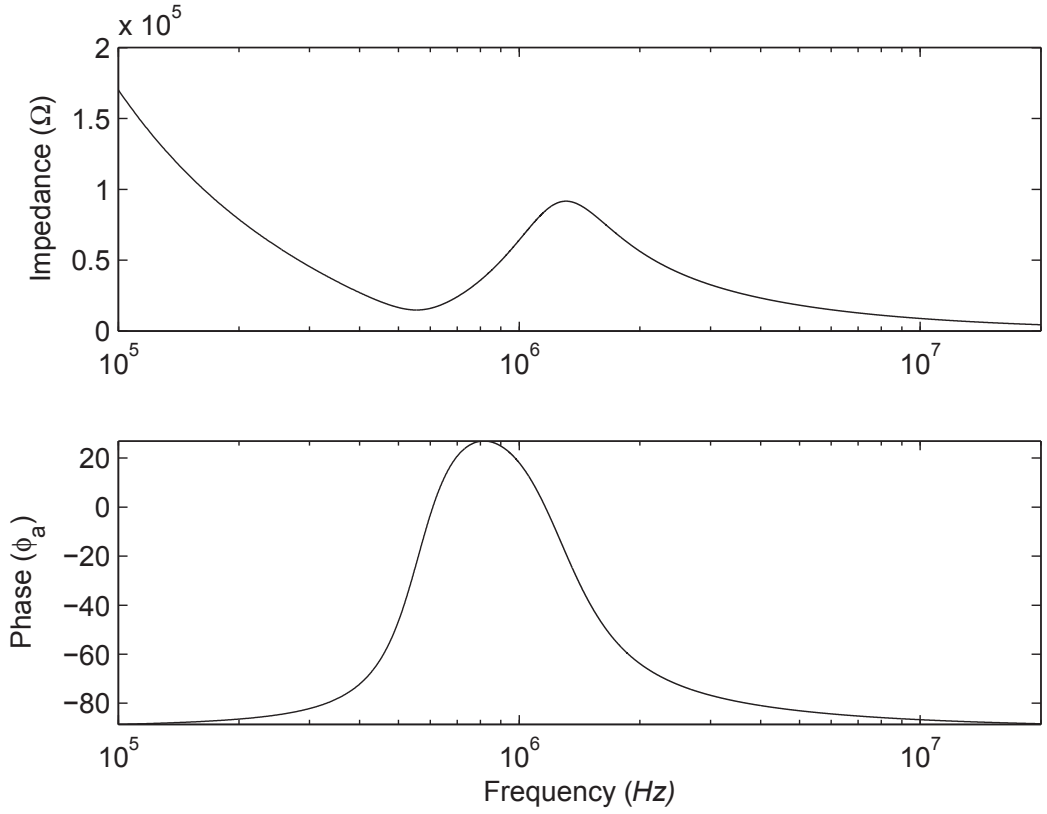

Fig. 4.1: Frequency response of Z_a as described in (4.2) showing the resonance regions.

4.2 Direct Digital Synthesizer (DDS) Model

The DDS system shown in fig. 4.2 consists of a clock divider, a digital counter, a read-only memory (ROM), a DAC, and a smoothing filter. The DDS is a digitally-programmable electronic device that generates digitized arbitrary waveforms such as square, sine, triangle, and sawtooth. These signals are generated from a stable and accurate clock source. This referenced clock can be generated using a crystal oscillator or a Phase-locked loop (PLL) [33]. Crystal oscillators are used when the main clock source frequency ranges from several KHz to 1-10 MHz. Frequencies in the tens and hundreds of MHz and up to the GHz region are usually generated using a PLL, because it is controlled through a feedback loop to provide a stable, low jittered output. Also, PLLs can generate multiple clock sources by simply fanning-out its output. This is beneficial in electronic circuits such as our PIP, which requires clock distribution to the two pipeline ADCs and the DDS.

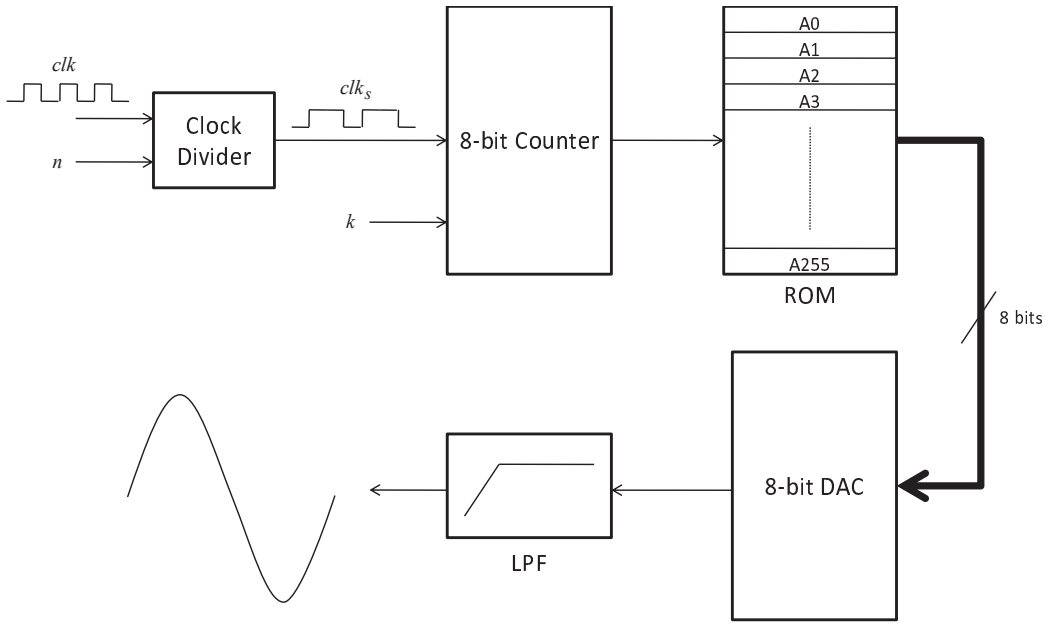

Fig. 4.2: DDS block diagram.

The sinusoidal waveform is generated by stepping through the ROM samples in increments of k, at the rate $\frac{f_{clk}}{n}$; k and n are determined by the control unit in the FPGA, and the procedure is explained in sec. 4.4; clk is the referenced clock source, and $A0 - A255$ are an array of memory addresses where the amplitudes for one period of a waveform are stored. Because the PIP's output voltage is insensitive to harmonic distortion, a low-resolution DDS is sufficient.

4.2.1 Clock Divider

A Simulink block of the clock divider is shown in fig. 4.3. It takes a referenced clock and divides it by an even number n to generate a 50% duty cycle clock output (clk_s) with a frequency of $\frac{f_{clk}}{n}\ Hz$. A binary counter will count up to $\frac{n}{2}$, because we need to only pull clk_s to logic 1 for half of its period. Since a maximum value of $n = 10$ is set by the control unit, a 4-bit up-counter built-in model is used in this design. A comparator outputs a logic 1 once it detects the count value reached $\frac{n}{2}$. When this occurs, the counter will reset to the initial count (set to 0 in this case), and the D flip-flop will toggle its output to 1. An inverter is placed at the output of the flip-flop to set clk_s to be high initially, since the

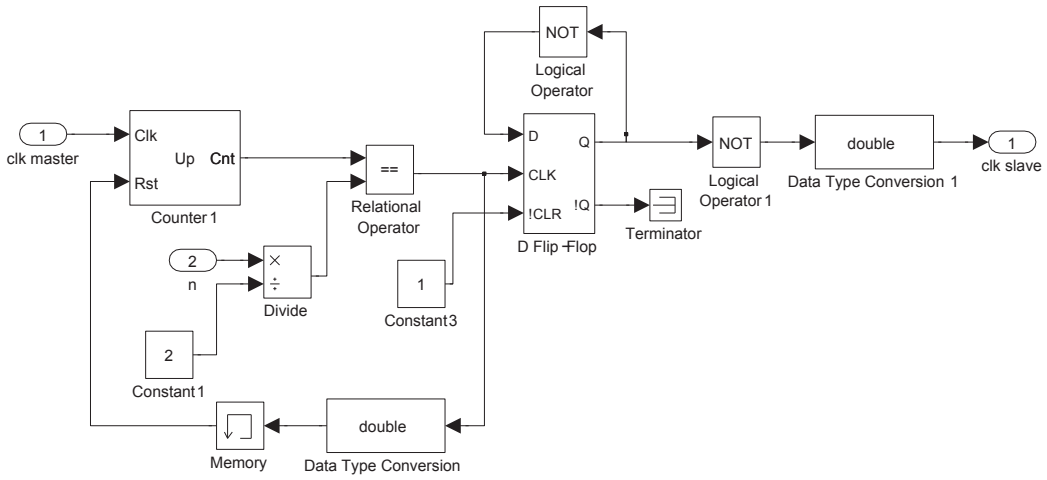

Fig. 4.3: Clock divider Simulink model.

flip-flop's initial state is at 0. Another inverter is placed in the feedback path between the flip-flop's output and input, because when the comparator outputs a 1 again, the flip-flop has to toggle its previous logic 1 to 0 in order to generate a whole periodic cycle. Since two high logic levels are required by the comparator to produce one period, n has to be divided by 2, as discussed previously. A memory delay block is added between the comparator's output and the reset port of the counter to break algebraic loops reported by Simulink. An algebraic loop occurs when the output of a direct feed-through block (comparator) is driven by its input, either directly or through other blocks (counter) in the feedback path. Note that a memory block is not needed in the feedback loop of the flip-flop, since it is not a feed-through block. Notice the use of a data type conversion block at the input of the memory block and the output port. This is used to convert any data type value to the specific input data type required by the destination block.

4.2.2 Binary Counter

A built-in Simulink model of an 8-bit counter is used to increment the count value depending on the frequency of the clock signal generated by the clock divider. The increment occurs at each positive rising edge of clk_s. According to Simulink, a rising edge is triggered when a value rises from zero to a positive value, and not from a negative to a positive value. For example, the rising edge of a clock pulse centered at zero with peaks of ± 1 would not

be detected by the counter model. Thus, it is imperative to feed the counter with a clock signal where its lower limit is set at 0. The output count value is multiplied by k to select the appropriate address in the ROM unit. As k increases, the counter will run through the ROM faster by skipping k memory allocations at each increment. This results in a higher frequency periodic signal compared to the referenced periodic signal that has its values stored in the ROM. The counter is switched back to its initial count once the output of the multiplier reaches the last memory address.

4.2.3 Read-Only Memory (ROM)

Since the PIP requires only a sinusoidal DDS to stimulate the probe, a ROM with stored samples of one period of a sine wave can be used in this case. The ROM is modeled as a 1-dimensional look-up table with 256 rows. The look-up table uses zero-based indices, where, as an example, an input of 10 would access the 11^{th} row. The data stored in each row is an 8-bit binary word. Once a specific row is selected, the data output is passed through a serial-to-parallel binary converter. The bits has to be pipeline out in parallel, since all of them need to be processed by the DAC at each clock pulse. Since an 8-bit binary counter is used to access the memory, a ROM with $2^8 = 256$ memory addresses is needed. This means the sine wave has a period of 256 points, where the amplitude of each point is stored in its corresponding memory slot. For example, the amplitude at point 100 would be stored at $A100$.

The amplitudes are found by using the following function

$$y_{sin} = V_{ofs} + A_{\text{peak}}(\sin(wt)), \tag{4.3}$$

where V_{ofs} is the dc component, A_{peak} is the highest amplitude, and w is the frequency in rads/sec. For a 256-point sine wave, (4.3) is represented in Matlab format as

$$y_{sin} = 128 + 127(\sin(2 * pi * (\frac{1}{256}) * (1 : 256))). \tag{4.4}$$

However, since the amplitudes have to be stored in binary format, y_{sin} needs to be rounded to the next lower integer. This is easily done by applying the floor function, and then the binary conversion process is achieved by using the $dec2bin()$ function.

4.2.4 Digital-to-Analog Converter

The Simulink model of the 8-bit DAC is shown in fig. 4.4. The model is based on the following mathematical expression

$$V_{out} = \sum_{i=0}^{N_{DAC}-1} D_i 2^{i-N_{DAC}}, \tag{4.5}$$

where N_{DAC} is the number of bits of the DAC unit, and D_i is the i^{th} bit of the input digital word. So for an 8-bit DAC, (4.5) is expanded to get

$$D_0 2^{-8} + D_1 2^{-7} + D_2 2^{-6} + \cdots + D_7 2^{-1}, \tag{4.6}$$

where D_0 and D_7 are the least-significant bit and the most-significant bit, respectively. So a 10000110 binary word will yield an analog output voltage of $(1 \times 2^{-1}) + (0 \times 2^{-2}) + (0 \times 2^{-3}) + (0 \times 2^{-4}) + (0 \times 2^{-5}) + (1 \times 2^{-6}) + (1 \times 2^{-7}) + (0 \times 2^{-8}) = 0.5234375\ V$. The DAC in this case assumes that the maximum output voltage is 1 V. If a higher maxima is set, the DAC analog output has to be scaled up by multiplying it with that maxima.

One interesting issue regarding this architecture is that it generates a sinusoidal signal with peaks of 0 and 1 V. However, the pipeline ADC requires a full-scale sinusoidal input of $\pm 1\ V$. Therefore, the sine wave output has to be centered at 0 by subtracting it by $\frac{1}{2}$, and then amplifying it to full-scale by multiplying it by 2.

4.2.5 Smoothing Filter

Since the DAC sinusoidal output is digitized, we need to smooth the transition steps to create a clean sine wave. This is achieved by using a smoothing filter, which is a low-pass filter that passes low-frequency components (pass-band), but suppresses frequencies

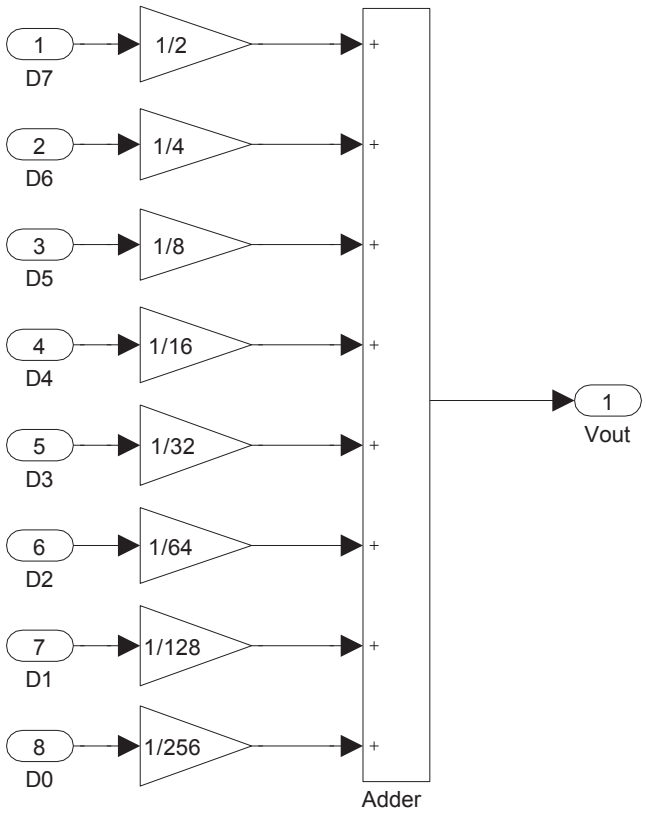

Fig. 4.4: Simulink model of an 8-bit DAC.

above the cut-off frequency (stop-band). A first order RC (a series resistor R and a parallel capacitor C) filter is considered because of its circuit simplicity. Its cut-off frequency is determined by

$$f_c = \frac{1}{2\pi\tau_{RC}}, \tag{4.7}$$

where τ_{RC} is the RC time constant. The filter can be modeled in frequency domain as

$$H(s) = \frac{1}{1 + s\tau_{RC}}, \tag{4.8}$$

where $H(s)$ is the transfer function $\left(\frac{output}{input}\right)$. Equation (4.8) has a pole at $s = -\frac{1}{RC}$ and a magnitude of 1 at DC. This means the unity gain magnitude will start to roll-off at $-6\ dB$ per decade or $-20\ dB$ per octave once the input frequency reaches the pole frequency.

To avoid aliasing, f_c should not exceed half the sampling rate of the digitized sine wave, which is the clock period of clk_s. Also, it should be larger than the signal bandwidth

to allow perfect smoothing of the signal. We have chosen f_c to be in the middle of the two. As illustrated in sec. 4.2.1, the generated clock period is determined by the divisor n. Consequently, for every integer that n takes, a different cut-off frequency is required. This can designed using a switched-capacitor filter, where one of an array of pre-determined capacitors is connected to a series fixed resistor using a switch. The capacitance values are found by assuming a fixed resistor and a known cut-off frequency. For example, for $n = 2$, $f_c = \frac{f_{sample}}{2n} = \frac{100}{4} = 25\ MHz$ and, assuming $R = 1\ k\Omega$, $C \approx 6.4\ pF$. Capacitances for all possible values of n set by the control unit are shown in table 4.1.

The Simulink model of the DDS unit is shown in fig. 4.5. Two smoothing filters are cascaded to give a smoother output. The choice of two filters is based on experimental analysis. The switching mechanism is processed by the control unit.

4.3 The Transimpedance and Difference Amplifiers Model

In order to measure the impedance of the probe, we need to measure the current through the probe and the applied DDS voltage. Since the matched ADCs accept only voltage inputs, we need to convert the current i_p at the probe's terminal to a voltage using a current-to-voltage converter. As shown in fig. 4.6, this is achieved using a transimpedance amplifier with a feedback impedance Z_f, and a difference amplifier to subtract off the DDS voltage. The output of the difference amplifier, $i_p Z_f$, is sampled by the ADC and then calibrated by the FPGA by dividing the sampled data by Z_f to acquire the measured current. The FPGA stores the values of Z_f for each swept frequency and performs the division accordingly.

Table 4.1: Smoothing filter time constant and capacitance for all possible $n's$, where $R = 1$ $k\Omega$ and $f_{clk} = 100\ MHz$.

n	$f_c\ (MHz)$	$\tau_{RC}\ (ns)$	$C\ (pF)$
2	25	6.3662	6.4
4	12.5	12.732	12.8
6	8.3333	19.1	19.1
8	6.25	25.468	25.5
10	5	31.831	31.9

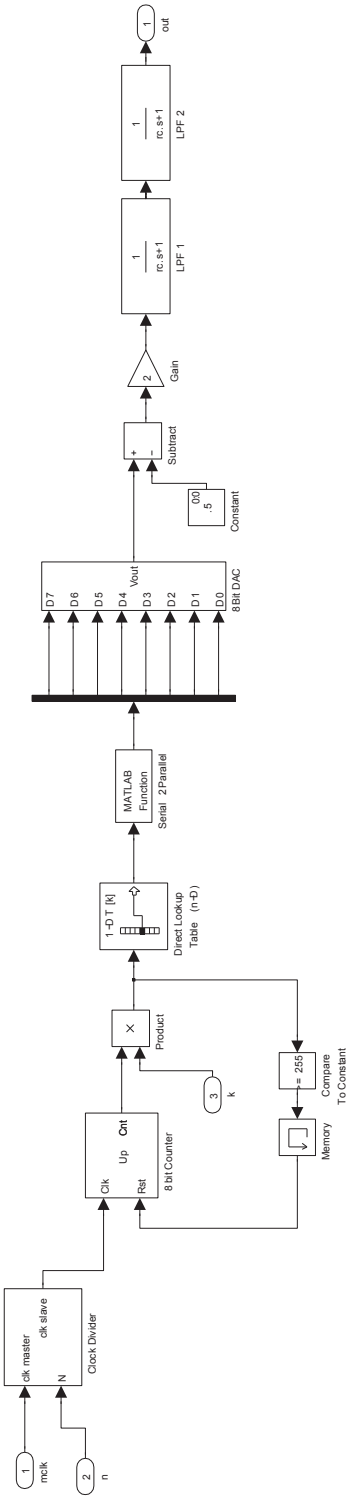

Fig. 4.5: Simulink model of the DDS system.

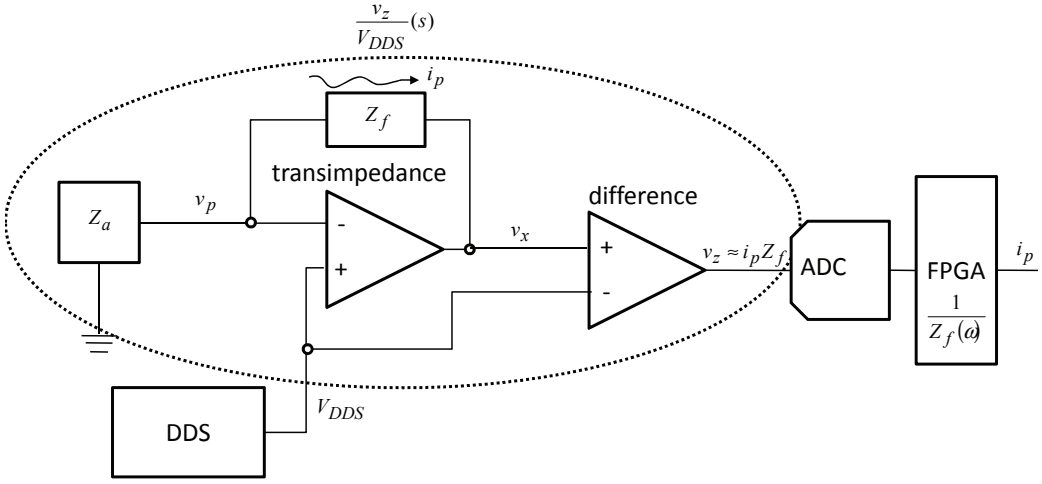

Fig. 4.6: Transfer function model of the plasma probe and the transimpedance and difference amplifers.

The feedback impedance in the s-domain is represented as

$$Z_f(s) = \frac{R_f}{1 + sC_f R_f}, \tag{4.9}$$

where C_f is described as

$$C_f = \sqrt{\frac{C_{in}}{2\sqrt{2}\pi f_{GB} R_f}}, \tag{4.10}$$

where C_{in} is the transimpedance amplifier's input capacitance, and f_{GB} is the unity-gain frequency. Equation (4.10) gives the optimum value for C_f, as to suppress ringing and to maximize the amplifier's bandwidth while maintaining stability [34]. For $R_f = 15\ k\Omega$ and $C_f = 4\ pF$, (4.9) becomes

$$Z_f(s) = \frac{15e^3}{1 + s6e^{-8}}. \tag{4.11}$$

The transfer function $\left(\frac{v_x}{V_{DDS}}\right)$ describing the relation between the input DDS voltage and the transimpedance amplifier's output is defined as

$$\frac{v_x}{V_{DDS}} = 1 + \frac{Z_f}{Z_a}. \tag{4.12}$$

Substituting equations (4.2) and (4.11) into (4.12) yields

$$\frac{v_x}{V_{DDS}}(s) = \frac{48000s^6 + 9.103e^{11}s^5 + 8.478e^{18}s^4 + 5.95e^{25}s^3 + 1.677e^{32}s^2 + 4.287e^{38}s}{33000s^6 + 7.612e^{11}s^5 + 6.23e^{18}s^4 + 5.017e^{25}s^3 + 1.09e^{32}s^2 + 4.287e^{38}s}. \tag{4.13}$$

By subtracting the DDS voltage from (4.13), we retrieve the overall transfer function describing the ratio of the difference amplifier's output and the DDS input, which is expressed as

$$\frac{v_z}{V_{DDS}}(s) = \frac{15000s^6 + 1.491e^{11}s^5 + 2.248e^{18}s^4 + 0.933e^{25}s^3 + 0.587e^{32}s^2}{33000s^6 + 7.612e^{11}s^5 + 6.23e^{18}s^4 + 5.017e^{25}s^3 + 1.09e^{32}s^2 + 4.287e^{38}s}. \tag{4.14}$$

4.4 The Control Logic Unit

The control unit serves as the brain of the whole PIP instrument. Its main role is to control the frequency synthesis, and to allocate enough processing time (PIP transient start-up and FFT operation) to obtain correct impedance values. As illustrated in sec. 4.2, the desired frequency (f_d) is generated by providing the DDS the incrementer k and the clock divisor n. The following derivation will set the basis for determining the lowest and highest swept frequency:

$$f_d = \left(\frac{1 \text{ period}}{256 \text{ samples}}\right)\left(\frac{k \text{ samples}}{1 \text{ point}}\right)\left(\frac{1 \text{ point}}{n \text{ cycles}}\right)\left(\frac{100e^6 \text{ cycles}}{\text{second}}\right), \tag{4.15}$$

$$f_d = \frac{100e^6 k}{256n}\ \left(\frac{\text{periods}}{\text{second}}\right), \tag{4.16}$$

$$f_d = 0.390625\left(\frac{k}{n}\right)\ MHz. \tag{4.17}$$

Equation (4.17) illustrates that for $k = 1$ and $n = 1$, the DDS output frequency is 390.625 KHz. Since the PIP has to operate across a wide frequency range (100 KHz to 20 MHz), the control unit has to adjust k and n appropriately to generate the desired output

frequency. The method for obtaining these parameters is given in Algorithm 4.1. Note that the maximum value that k or n can be assigned is $\frac{2^{N_{DDS}}}{2} = \frac{2^8}{2} = 128$. Any value on top of that would exceed the look-up table's dimensions after the first increment. For example, if $k = 130$, then at the 2^{nd} increment the pointer will try to access address $A260$, which does not exist since the maximum is at $A256$. The enclosed CD contains the Matlab code for the frequency synthesis.

The timing of the FFT operation (T_{FFT}) is related to the desired frequency by the following equation:

$$T_{FFT} = \left(\frac{\text{FFT Points}}{4}\right) T_d, \tag{4.18}$$

$$T_{FFT} = 1024 \left(\frac{k}{n}\right) f_{clk}, \tag{4.19}$$

where T_d is the period of the desired frequency, and a 4096 point FFT is utilized. Also, the Hann algorithm is used as the windowing function. The transient start-up time is set to disregard the first 20 samples.

4.5 PIP Simulink Model and Results

The top level of the PIP chip Simulink model is shown in fig. 4.7. This model is controlled by a Matlab file, which serves as the brain of the system. It provides the frequency synthesis, and processes the FFT operation on the sampled current (I) and voltage (V) at each frequency step. The pulse generator generates a 100 MHz clock, and is considered as an off-chip clock signal.

The resulting impedance magnitude across the full operating range for the ideal and nonideal simulink models, compared to the Balmain's model, is shown in fig. 4.8. The simulation results prove to be superior to previous design results [13, 14]. It is evident that both the ideal and nonideal systems exhibit a magnitude curve that closely matches the analytical model. Observe that the parallel-like and series-like resonances of the Simulink simulations are accurately estimated. The jittery behavior observed at frequencies above f_{uh} can be explained by the limitation of the FFT frequency resolution. The frequency

Algorithm 4.1 Frequency synthesis.

Input:
Start sweeping frequencies (*sweep*),
Minimum frequency f_{min},
Maximum frequency f_{max},
Step frequency f_{step},
DDS bit resolution N_{DDS},
Accurancy α

Output:
Inceremenier, k
Divisor, n

Begin
If (*sweep*)
Begin
For $m = f_{min} : f_{step} : f_{max}$
Begin
$frac = (2^{N_{DDS}} m)/(f_{sample})$
For $i = 1 : 1 : 2^{N_{DDS}}/2$
Begin
For $j = 1 : 2 : 2^{N_{DDS}}/2$
Begin
If $abs(frac - (k/n)) \leq \alpha$
Begin
$k_{temp} = i$
$n_{temp} = j$
break
End
End
If $abs(frac - (k/n)) \leq \alpha$
break
End
$k[m] = k_{temp}$
$n[m] = n_{temp}$
End
End
End

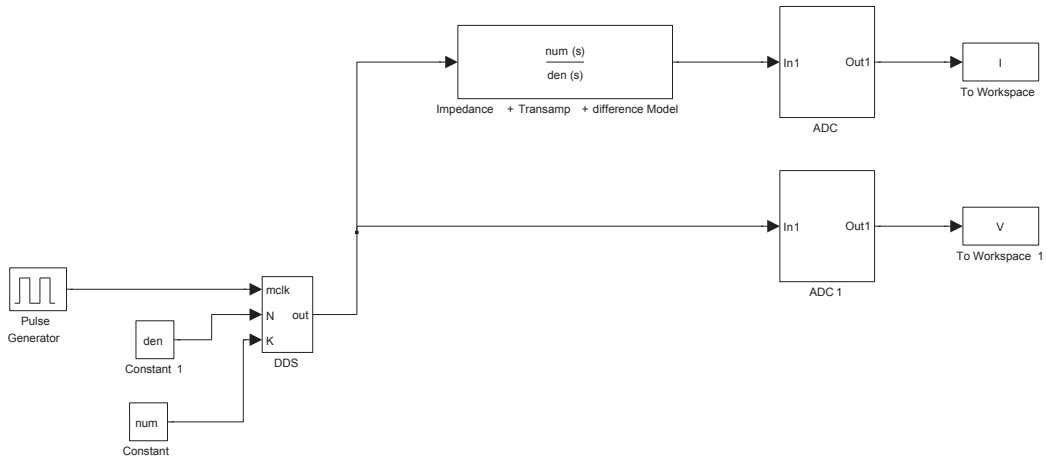

Fig. 4.7: Simulink model of the PIP chip.

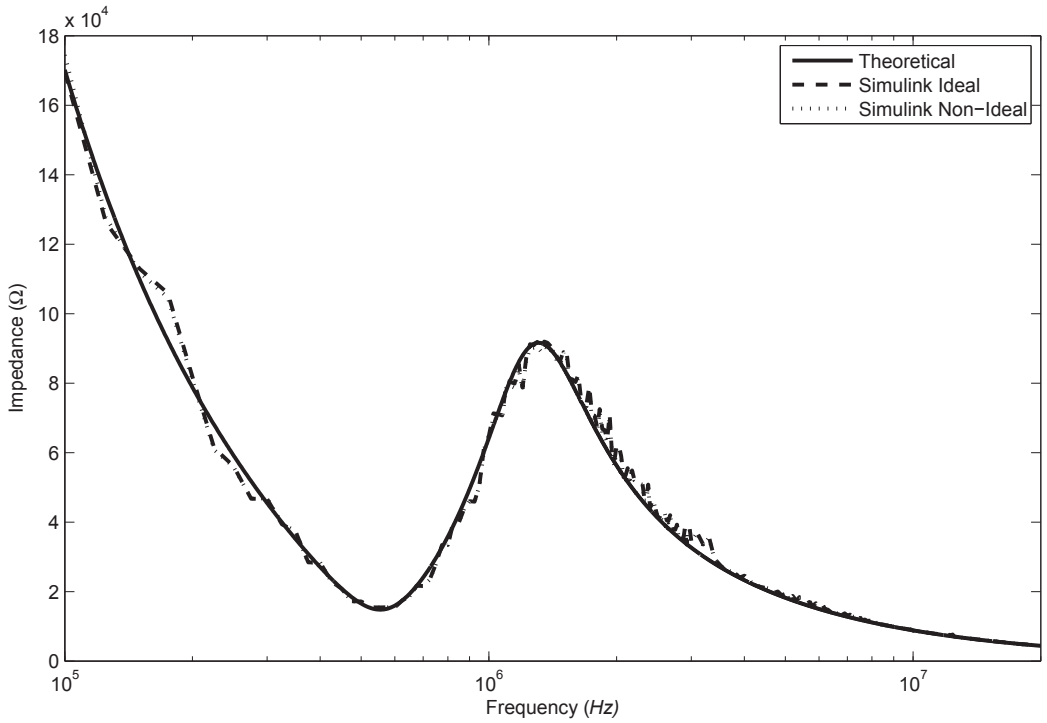

Fig. 4.8: Impedance magnitude measurements of ideal and nonideal Simulink models. $\sigma = 1\%$ is inserted into the error model of the nonideal Simulink system.

resolution is defined as

$$\text{Frequency Resolution} = \frac{f_{clk}}{\text{FFT Points}}. \tag{4.20}$$

Thus for a 4096 point FFT and a 100 MHz sampling rate, a frequency resolution of 24.414 KHz is achieved. This means that each FFT spectrum bin is represented by this resolution. For a fixed sampling frequency, the resolution can be increased by decreasing the FFT points. However, in this case the filling time buffer will be shorter.

4.6 Design Verification Using Simulink/Matlab and Cadence Co-simulation Capability

A Verilog-AMS [35] model of the PIP chip within Cadence was developed by Magathi Jayaram [36]. Verilog-AMS is a hardware description language that models analog and mixed signal systems. It is widely used in industry, since it allows designers to model systems and components at a high-level of abstraction. Its main advantage is its ability of processing continuous time and discrete event signals. Also, a Verilog-AMS model would provide the engineer performance and functionality verification before going into the actual transistor design. This ensures that all functional failures are solved initially, which saves time and cost.

The design methodology chosen is a top-down design approach. This approach is broken down into three phases:

- behavioral block-level model,
- semi-ideal transistor model,
- and physical transistor model.

The behavioral level models only the functionality of the system blocks. A Verilog-AMS model of each block is developed. In this phase we are mainly looking for system verification and testability. It also allows us to optimize the architecture and explore the parametric

specifications of each component. At this point, a rough idea of the expected performance can be concluded, and suggestions and feedback from the customer can still be implemented.

After verifying the behavioral models and developing the test-benches needed for system testing, the next stage is to replace critical and complex blocks in the system with a semi-ideal transistor model, which models second order effects. Noncritical circuits, such as bias circuitry and digital logic, will be kept in the behavioral model form. Verilog-AMS has the capability of simulating behavioral models with transistor level models. This type of simulation is referred to as mixed-level simulation. It allows the simulation of complex circuits to run at a much faster speed than the transistor-level simulations. This allows for more extensive tests to be conducted. The results of this phase illustrate how much do second order effects impact the system's performance.

The last design phase includes substituting the semi-ideal transistor model file with a physical device model that is provided by the foundry. Every component should be simulated at the actual transistor level within a mixed-level simulation. The outcome of this phase is a first look at the actual electronic chip. By implementing this top-down design strategy, an accurate, efficient, and verified design can be implemented, which greatly reduces the tendency of chip failures.

Our design and verification strategy is shown in fig. 4.9. As illustrated, a co-simulation capability between Cadence and Matlab/Simulink allows the integration of analog/mixed-signal components within the top system level simulation for ASIC development [37]. In our case, Verilog-AMS models of the DDS and ADC components within Cadence are co-simulated and verified within the Matlab/Simulink framework. The implementation of the co-simulation is done using coupler modules on both ends of the simulators. Both couplers communicate with each other using a TCP/IP socket-based approach.

The co-simulation schematic in the Simulink framework is shown in fig. 4.10. Inputs to the simcoupler include the system clock, the output of the transimpedance amplifier, and the values of k and n. Notice that k and n are converted to binary format, since the Verilog-AMS model of the DDS does not accept inputs in integer format. The Simulink coupler's

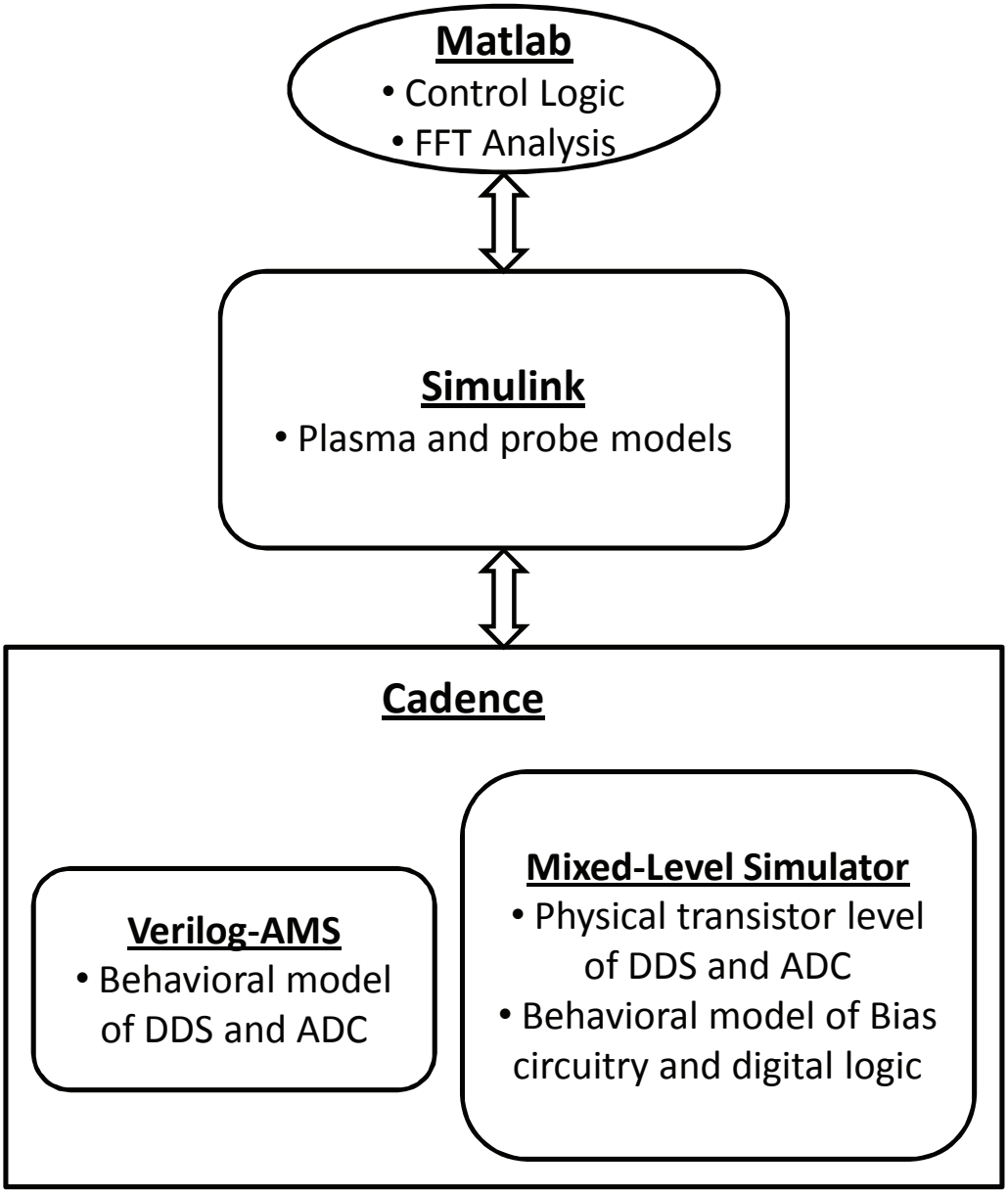

Fig. 4.9: Top-level functional unit abstraction and verification of the PIP chip.

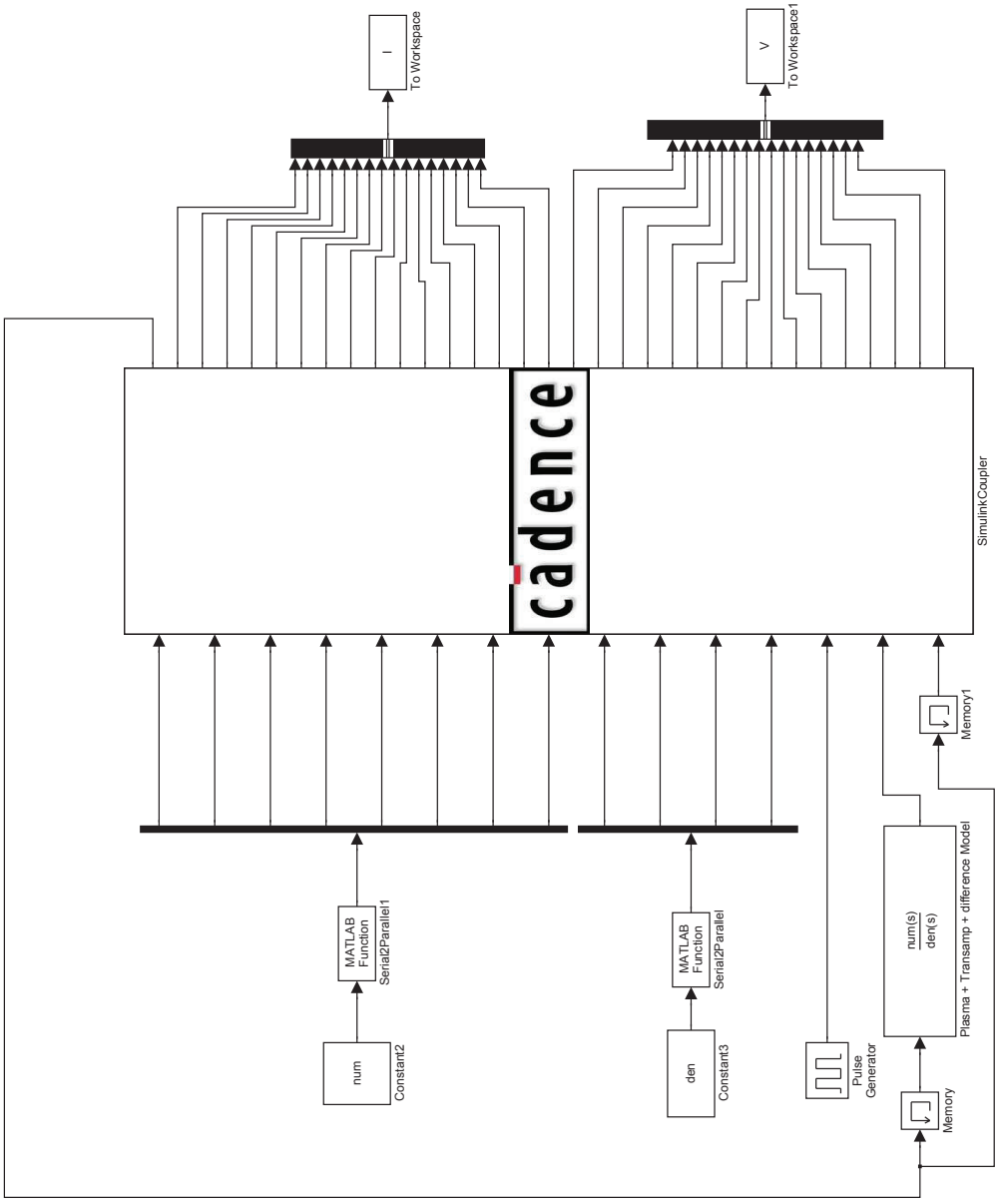

Fig. 4.10: Top-level system design showing co-simulation in the Simulink framework.

outputs include the outputs of the matched ADCs and the DDS output. The DDS signal is fed back to the plasma probe and transimpedance amplifier, and the sampled current and voltage from the ADC is sent to the Control unit (Matlab file) for post-processing analysis. Memory blocks are added on each feedback path to break algebraic loops.

There are three types of co-simulation flows [38] that the user can select from. The Cadence Virtuoso Analog Design Environment (ADE) flow is intended for users that are familiar with the ADE, and if most of the debugging is done in the Virtuoso environment. This flow runs the co-simulation by launching Matlab automatically from the ADE. The Simulink flow is for users who do not want to use the ADE, but who would rather visualize the results using Simulink. This flow requires a script to run the simulation of the ADE from Matlab/Simulink. The Analog-Mixed Signal (AMS) environment flow can be used to run simulations separately. This type of flow is for users who are experienced in both tools, and who want to have more control on the co-simulation functionality. Since the frequency sweep and the FFT procedure for the PIP chip is controlled by Matlab/Simulink, the co-simulation should be a Simulink flow.

The resulting impedance magnitude across the full operating range for the theoretical Balmain model against the nonideal Simulink model and the co-simulation output is shown in fig. 4.11. It follows that, with even more realistic Verilog-AMS models of the ADC and the DDS, the impedance magnitude is precisely measured with slight deviation at some frequencies. Only 11 co-simulation points were considered because of limited memory and processor clock speed exhibited by the lab Linux machine. The points chosen were more concentrated at the resonance frequencies, since they are of vital importance. With these results, we fully quantified the precision of the PIP's impedance measurement across its entire frequency operating range.

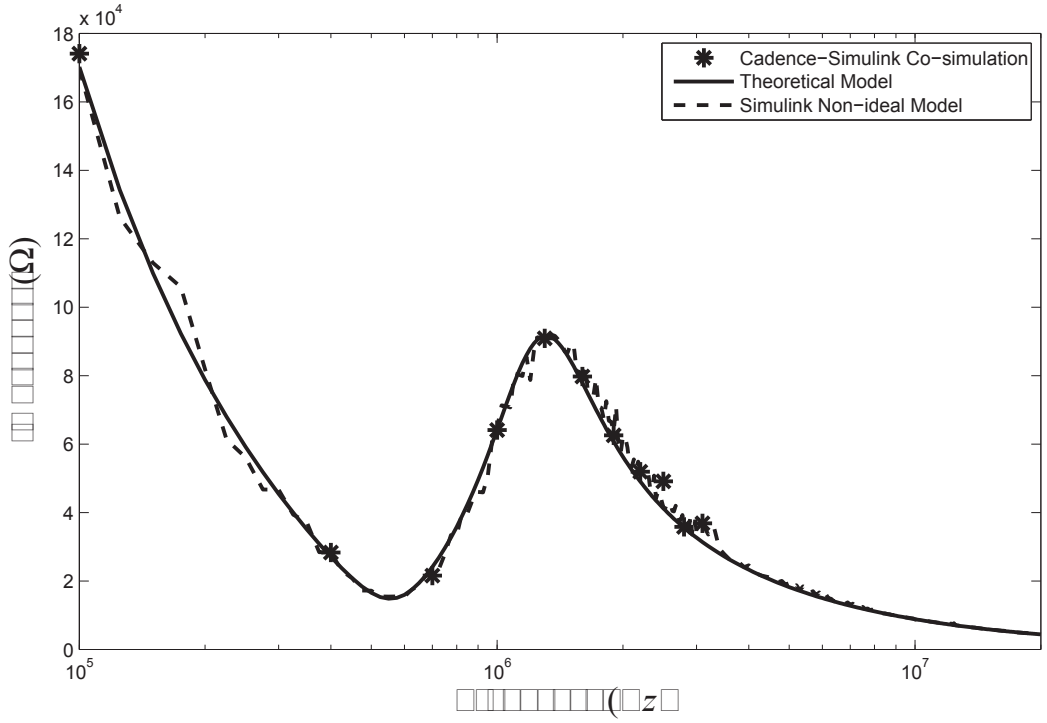

Fig. 4.11: Impedance magnitude measurement of the nonideal Simulink model and the co-simulation implementation.

Chapter 5

Conclusion

5.1 Summary

The need for miniaturizing space environment instrumentation is emerging as a key function for micro-satellite research. The PIP instrument has undergone numerous improvements and modifications, and various techniques on measuring the characteristics of the lower-altitude ionospheric plasma have been reported in the literature [11–14]. However, these designs lacked accurate impedance measurements, where the main focus was aimed to pinpoint precisely the resonance frequencies. Moreover, the hardware implementations introduced are not feasible for micro-satellite deployment, due to high power consumption and large volume occupied.

The aim of this thesis is to outline and customize the design of the fully-integrated PIP instrument. To accomplish this task, the author has characterized the pipeline ADC for optimum performance and accuracy in measuring the fundamental component at the FFT's output. Analog errors such as nonlinear distortion, clock jitter, finite bandwidth, and transient spikes were inserted to agitate the critical components of the ADC. The impact of these errors on each component of the ADC is evaluated to identify the most critical error. Statistical variance in the impedance measurement was calculated to determine the variation's effect. Furthermore, the proposed PIP system presented in fig. 2.5 was modeled in the Matlab/Simulink framework. Full system Monte Carlo simulations with random component parametric variations were performed. The design was then verified using a co-simulation capability between Cadence and Matlab/Simulink, where the ADC and the DDS were modeled in Verilog-AMS and all other components were left at the system-level. The extracted absolute impedance magnitude was in close proximity with the theoretical impedance curve.

To conclude, the proposed PIP system offers tremendous advantages over previous PIP designs. The prevailing advantages include:

1. by using matched ADCs to sample directly the probe's voltage and current, the system reduces the requirement of pure sinusoidal signals;

2. by using the FFT technique, we can eliminate harmonic effects (transient spikes) that appear away from the fundamental component;

3. by integrating the PIP parts on one single chip, we can customize the analog components to yield high reliability and efficiency.

5.2 Future Work

The Simulink model of the transimpedance amplifier assumed an ideal infinite gain opamp. Practically, real opamps suffer finite gain, bandwidth, input impedance, and a nonzero output impedance. The issues of these nonideal effects should be carefully considered in the Simulink model. In addition, to achieve a rigid functional verification of the PIP design, a transimpedance Verilog-AMS model has to be included in the Cadence design hierarchy. In this case, all major analog and mixed-signal components can be simulated and tested within the Matlab/Simulink framework.

This thesis took into account the behavioral verification of the PIP instrument. To fully verify the functionality of the design, a transistor-level component design has to be implemented. This design phase has to follow the top-down design methodology illustrated in sec. 4.6. By accomplishing this, a less error-prone physical chip could be fabricated.

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