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Architecture, Modeling, and Analysis of a Plasma Impedance Probe

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ARCHITECTURE, MODELING, AND ANALYSIS OF A PLASMA IMPEDANCE PROBE

by

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Abstract

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Variations in ionospheric plasma density can cause large amplitude and phase changes in the radio waves passing through this region. Ionospheric weather can have detrimental effects on several communication systems, including radars, navigation systems such as the Global Positioning Sytem (GPS), and high-frequency communications. As a result, creating models of the ionospheric density is of paramount interest to scientists working in the field of satellite communication.

Numerous empirical and theoretical models have been developed to study the upper atmosphere climatology and weather. Multiple measurements of plasma density over a region are of marked importance while creating these models. The lack of spatially distributed observations in the upper atmosphere is currently a major limitation in space weather research. A constellation of CubeSat platforms would be ideal to take such distributed measurements. The use of miniaturized instruments that can be accommodated on small satellites, such as CubeSats, would be key to acheiving these science goals for space weather.

The accepted instrumentation techniques for measuring the electron density are the Langmuir probes and the Plasma Impedance Probe (PIP). While Langmuir probes are able to provide higher resolution measurements of relative electron density, the Plasma

Impedance Probes provide absolute electron density measurements irrespective of spacecraft charging.

The central goal of this dissertation is to develop an integrated architecture for the PIP that will enable space weather research from CubeSat platforms. The proposed PIP chip integrates all of the major analog and mixed-signal components needed to perform swept-frequency impedance measurements. The design's primary innovation is the integration of matched Analog-to-Digital Converters (ADC) on a single chip for sampling the probes current and voltage signals. A Fast Fourier Transform (FFT) is performed by an off-chip Field-Programmable Gate Array (FPGA) to compute the probes impedance. This provides a robust solution for determining the plasma impedance accurately.

The major analog errors and parametric variations affecting the PIP instrument and its effect on the accuracy and precision of the impedance measurement are also studied. The system clock is optimized in order to have a high performance ADC. In this research, an alternative clock generation scheme using C-elements is described to reduce the timing jitter and reference spurs in phase locked loops. While the jitter performance and reference spur reduction is comparable with prior state-of-the-art work, the proposed Phase Locked Loop (PLL) consumes less power with smaller area than previous designs.

(97 pages)

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Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
CP	Charge Pump
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DDS	Direct Digital Synthesizer
DFT	Discrete Fourier Transform
ENOB	Effective Number of Bits
FD	Frequency Divider
FFT	Fast Fourier Transform
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
IP	Impedance Probe
IS	Impedance Spectroscopy
LP	Low Pass
LSB	Least Significant Bit
MIP	Mutual Impedance Probe
PC	Personal Computer
PD	Phase Detector
PFD	Phase frequency Detector
PIP	Plasma Impedance Probe
PISA	Plasma Impedance Spectrum Analyzer
PLL	Phase Locked Loop
RF	Radio Frequency
ROM	Read Only Memory
RPC	Rosetta Plasma Consortium
SFDR	Spurious Free Dynamic Range
S/H	Sample and Hold
SINAD	Signal-to-Noise-and-Distortion
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
TM	Telemetry
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator

Chapter 1

Introduction

The central goal of this dissertation is to develop an integrated architecture for the Plasma Impedance Probe (PIP) that will enable space weather reserach from CubeSat [1] platforms. The PIP is an instrument that belongs to the broad domain of impedance spectroscopy and uses the swept-frequency technique. It measures the impedance of a probe immersed in an ionospheric plasma environment. Studying these impedance curves help in determining ionospheric plasma characteristics like the upper hybrid frequency, electron-neutron collision frequency, and the plasma's electron density [2, 3].

The closest, naturally occurring plasma to the surface of the earth is the ionosphere. Although the ionosphere contains only a fraction of the atmospheric material, it is crucial to study its characteristics due to its influence on the radio waves passing through them. Most of the ionosphere is electrically neutral, but when solar radiation strikes the chemical constituents of the atmosphere, electrons are dislodged from atoms and molecules to produce the ionospheric plasma [4–6]. At high latitudes there is another source of ionization called the aurora. The aurora is a display of light caused by electrons and protons striking the atmosphere at high speed [4–6]. The presence of these charged particles makes the upper atmosphere an electrical conductor, which supports electric currents and affects radio waves.

1.1 Need for Spatially Distributed Measurement

The ionosphere varies greatly due to the changes in the two sources of ionization and because it responds to changes in the neutral part of the upper atmosphere in which it is embedded. This region of the atmosphere is known as the thermosphere. Since it responds to solar radiation, the ionosphere varies over the 24-hour period between daytime and night time and over the 11-year cycle of solar activity. During a geomagnetic storm

the auroral source of ionization becomes much more intense and variable, and expands to lower latitudes. Further, the energy input at high latitudes produces waves and changes in thermospheric winds and composition. This produces both increases and decreases in the electron concentration. Hence, the ionosphere varies significantly over an hourly basis. These variations in ionospheric plasma density can cause large amplitude and phase changes in the radio waves passing through this region [4–6]. Ionospheric weather can have detrimental effects on several communication systems, including radars, navigation systems such as the Global Positioning System (GPS) and other high-frequency communication systems. As a result, creating models of the ionospheric density is of paramount interest to scientists working in the field of satellite communication [6].

Numerous empirical and theoretical models have been developed to study the upper atmosphere climatology and weather. These models range from capturing climatological behavior from historical data to real-time estimators that reconstruct the ionosphere from live measurements in specific locales. The accuracy of these empirical models largely depend on the quality and quantity of the observations with which they are driven. Hence, multiple measurements of plasma density over a region is of marked importance while creating these models. The lack of spatially distributed observations in the upper atmosphere is currently a major limitation in space weather research [7,8]. A constellation of CubeSat platforms would be ideal to take such distributed measurement [9]. The use of miniaturized instruments that can be accomadated on nano satellites, such as CubeSats, would be key to acheiving these science goals for space weather.

1.2 CubeSat Specifications

The term "CubeSat" represents nano-satellites that adhere to the standards described in the CubeSat design specification [1]. The $10 \times 10 \times 10$ cm, 1kg CubeSat standard has evolved to become the basis for nanosatellite designs. The $10 \times 10 \times 10$ cm basic CubeSat is often called a "1U" CubeSat, meaning one unit. CubeSats are scalable in 1U increments and larger CubeSats such as a "2U" CubeSat ($20 \times 10 \times 10$ cm) and a "3U" CubeSat ($30 \times 10 \times 10$ cm) can also be built.

Power is the next primary consideration after launch restrictions. CubeSats are primarily powered by solar cells mounted on the external faces of the satellite. As surface size is the primary factor in solar power collection, physical size of the CubeSat defines the maximum power collection ability of the system. Most CubeSats are placed in sun-sync orbit allowing them to constantly collect solar power. The power subsystem also includes a battery to stabilize the power generated by the solar collectors. The total power available for the necessary performance of the electric system and the scientific payload of a CubeSat varies based on the type of solar cells mounted and the type of secondary power provided.

Solar panels are currently made of Silicon (Si), Gallium-Arsenide (GaAs), or Gallium-Arsenide triple junction cells. Only a limited number of cells can fit on the CubeSat. Nickel Cadmium (NiCd), Nickel Hydrogen (NiH2), and Li-Ion batteries are becoming more and more common in space applications to provide the secondary power. The reported power available for a 1U CubeSat varies from 5W to 20W and the estimated power available for the payloads varies from 0.5 W to 4 W [1, 10–12]. Consequently, the number of payloads on each CubeSat depends on the power consumed in each payload.

1.3 Background

Recent research in Impedance Spectroscopy (IS) has led to the development of compact, fully-integrated impedance spectroscopy systems [13–19]. These circuits are based on the frequency response analyzer approach for IS, which are best suited to the slow changing parameters measured by many sensors. These existing fully-integrated systems are unsuitable for the rapid changes in the ionospheric plasma density and the ionospheric frequency range (100 KHz to 20 MHz) under consideration. Existing PIPs are made from off-the-shelf components and/or bench-top instruments. Their volume and power requirements inhibit them from being used in the tightly constrained CubeSats.

1.3.1 Impedance Spectroscopy

Impedance Spectroscopy is a versatile tool used to characterize the intrinsic properties of any material and its interface. It is used in many macro-scale applications such as

monitoring electrochemical reactions [20–22], testing batteries [23], geological mapping [24, 25], testing coatings [26] and many other applications [27, 28]. Recently, IS is being applied to micro-scale applications across a wide variety of applications. It is especially gaining popularity for biological and medical applications [29–36].

Applications

IS is being used extensively for investigating human tissue. Kun et al. have published a series of papers [29–33] on detecting tissue ischemia (lack of oxygen and nutrients eventually resulting in the death of the tissue). Although, their work is not on the micro-scale, the ability to implement on-chip IS might greatly expand the applications of this work. For example, Othman et al. [34] shows that IS can detect ischemia leading to organ failure in the intestine. For this to be a practical application, an embedded sensor with a low power, compact impedance spectrometer would be necessary. Additionally, IS has been applied for the detection of skin cancer [35] and skin irritation [36].

IS has been coupled with on-chip fluidics for particle detection. This helps in differentiating different particle types [37], monitor particle position [38], and measure the size of the particles [39]. One unique application is the testing of neural probes. IS is used to inspect the probes and detemine the state of their coatings [40]. The use of IS in on-chip fluidics leads to the need for on-chip IS instrumentation circuitry.

IS has also been used to detect and sort blood cells [41] based on abnormalities in the cell. This can be used for cancer screening [42, 43]. Work has been published showing the ability to inspect cell's membrane and cytoplasm [44] and detecting bacterial viability [45] using IS. Yotter and Wilson [46] state that IS will become an important technique in impedance-based single cell measurements. Some of the issues restricting the use of IS is the size and sensitivity of the IS instruments. Hence, on-chip IS instrumentation circuitry would help address these issues.

Biological sensors are a key application area for IS. It has been used for DNA sensors, immunosensors, and biocatalytic enzyme-based biosensors [47–49]. Another vital biosensor application is the use of proteins bonded to electrodes. As the proteins react to specific

chemicals, the reactions can be measured using IS [50–52]. An on-chip IS system would be applicable for all of the above applications.

1.3.2 Existing IS Instrumentation

Nearly all of the applications described above attach on-chip probes to bench-top instruments (either a PC with a DAQ or some sort of network analyzer) to do the actual impedance measurement. While this could prove useful for initial research, it presents some serious limitations as well. Bench-top equipment can be expensive and severely limits large scale production and deployment of IS systems. Some of the applications listed above present exciting possibilities for in-vivo or portable applications, however the size and power requirements make this impossible.

There have been a number of IS systems that have been developed that rely on computers for most of the computation, while using discrete components on a PCB to perform measurements [53]. Computer-based solutions suffer from all the same limitations of bench-top instruments listed above. Some more compact solutions have also been presented. Carullo et al. [26] replace the computer with a commercial digital signal processor. Using off-the-shelf components on a PCB will still not allow these instruments to be used for in-vivo or portable applications where the power and size are tightly constrained.

Arnold and Manck [13] discuss a fully on-chip system but give very few details as to the implementation. Hassibi and Lee [14] discuss an on-chip sensor array system for biomolecular detection, however the system only has programmable amplifiers and no IS is actually done. On-chip IS is a relatively new field and recently a fully on-chip system capable of computing complete impedance data has been developed by Yang, Rairigh, Liu, and Mason [15–18]. Their on-chip IS system targets detecting impedance information in the 1mHz to 100kHz frequency range in gas sensors. Analog Devices has made available AD5933 [19], a new system-on-chip fully integrated electrical impedance spectrometer, which might allow the implementation of minimum-size instrumentation for electrical bioimpedance measurement in the 1mHz to 100kHz frequency range. Some of the disadvantages of using this chip in the configuration suggested by the manufacturers are the need for additional mea-

surement for calibration, the lack of constant output resistance and possibility of spectrum leakage while determining the Discrete Fourier Transform(DFT) [54]. Thus existing on-chip IS systems are unsuitable for measuring the ionospheric plasma impedance as the frequency range under consideration is 100KHZ to 20 MHz.

1.3.3 Previous PIP Instruments

The PIP instruments have undergone numerous design iterations and changes over the last fifty years. In the 1960s, Oya and Obayashi [55] applied a bridge circuit to the impedance probe and realized an accurate measurement of the absolute electron density. Since then, the impedance probe technique has been applied to many sounding rockets and satellite observations [56].

Steigies et al. [57] reported a design in 2000 that measured the magnitude of the plasma impedance while sweeping over a wide range of frequencies. A schematic diagram of the instrument used is shown in Figure 1.1.

The signal is generated by the Direct-Digital Synthesizer (DDS). The sensor box contains a capacitance bridge, wide-band amplifiers, and signal detection. The Impedance Probe (IP) sensor represents one component of the capacitance bridge and the output signal is proportional to the impedance of the sensor. The instrument is controlled by a programmable logic device (PLD) that also reads the analog-to-digital (A/D) converter and communicates with the telemetry (TM). Although the IP is digitally programmed to give fast, accurate results, the upper limit of the accessible electron density in this approach is limited by the DDS clock frequency of 25MHz. The IP sensor unit consists of a base plate on which the strip antenna connected to the pre-amplifier and release mechanisms are mounted. Figure 1.2 shows the IP sensor unit. The sensor circuit is also made from surface mount components. This severely restricts large scale development. Though the power consumed is not reported, it is unlikely that it would satisfy the tightly constrained power budget of CubeSats.

Blackwell et al. [3] described a plasma impedance probe in 2005 to measure absolute electron density. A small spherical probe was used in conjunction with a network analyzer,

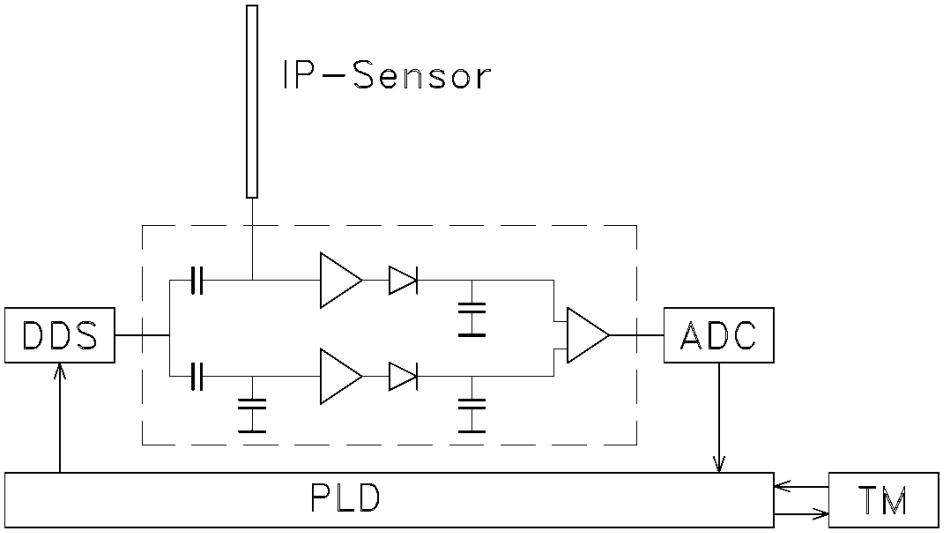


Fig. 1.1: Block diagram of the impedance probe instrument.

as shown in Figure 1.3, to determine the impedance of the probe-plasma system over a wide range of frequencies. Impedance curves were in good agreement with accepted circuit models but several sources of errors were listed by Blackwell et al. [3]. The use of a network analyzer to determine the impedance restricts the large scale production and deployment of this instrument. It is also unsuitable for CubeSat platforms.

Rowland et al. [58] developed a plasma impedance spectrum analyzer (PISA) at NASA GSFC in 2006 that included a white noise generator that stimulated a wide range of frequencies simultaneously, allowing the instrument to send down the entire impedance frequency spectrum every few milliseconds. This allows identification of all resonance frequencies, including the series resonance which depends on temperature. The PISA, as shown in Figure 1.4, weighs about 3kg and was developed for FASTSAT, a microsatellite which is 39.5 inches in diameter and weighs 90 Kg. Hence, the PISA would not conform to the CubeSat specifications described in Section 1.2.

Trotignon et al. [59] reported a Mutual Impedance Probe (MIP) design in 2007 that relies entirely on the capacitive coupling of two antennas, to gain insight into the plasma characteristics around comets. The MIP was designed to measure the plasma density,

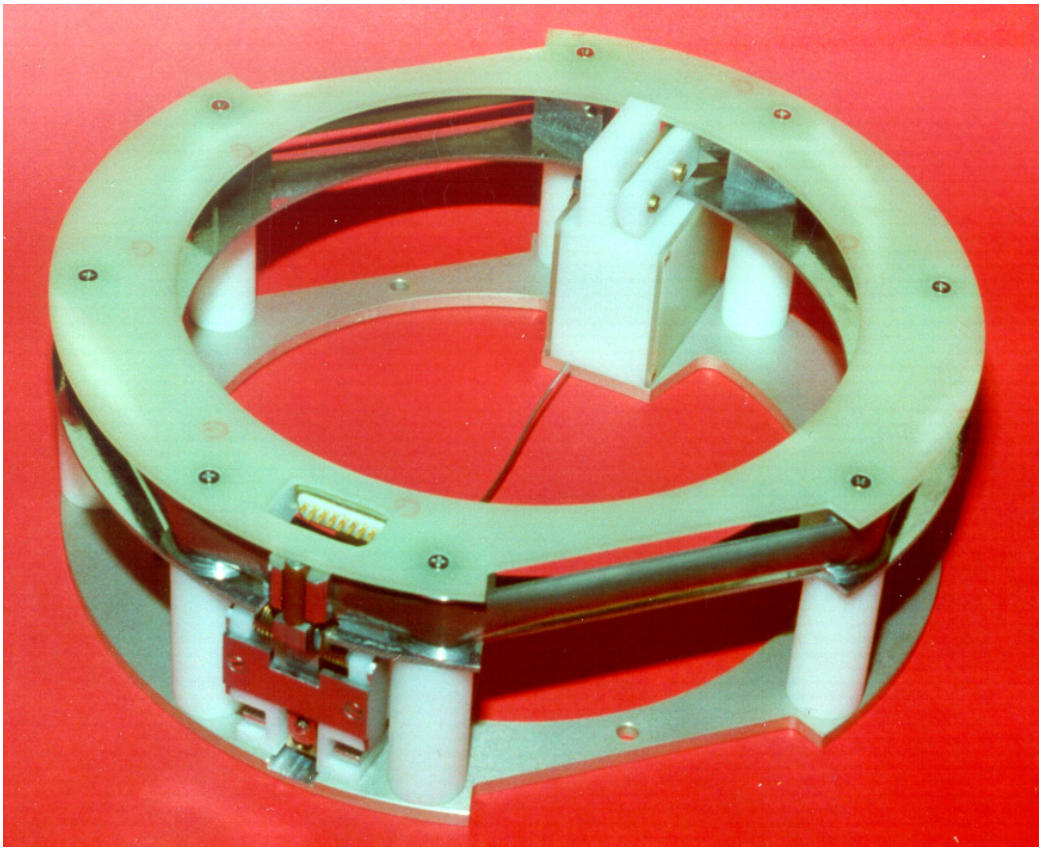


Fig. 1.2: Impedance probe sensor unit.

temperature and drift velocity, and also act as a receiver for high-frequency waves (above 10 kHz). The MIP is part of the Rosetta Plasma Consortium (RPC) which consists of four additional instruments. An alternating current, I, with a frequency lying in the range that contains the plasma frequency resonance, was driven through a transmitting electrode. The induced difference in voltage, V, measured on open circuit between two receiving electrodes is fed into a high-input impedance amplifier. The mutual impedance, Z, which is then computed on-board, is equal to the ratio of V to I. As Z depends essentially on the properties of the surrounding plasma, the frequency response of the mutual impedance probe is used for plasma diagnosis. The mutual impedance probe instrumentation consists of an electronics board for signal processing in the 7 kHz to 3.5 MHz range and a sensor unit of two receiving and two transmitting electrodes mounted on a 1-m long bar. The RPC instrument schematic is shown in Figure 1.5. The MIP sensor has a mass of 0.370 kg and the MIP electronics,

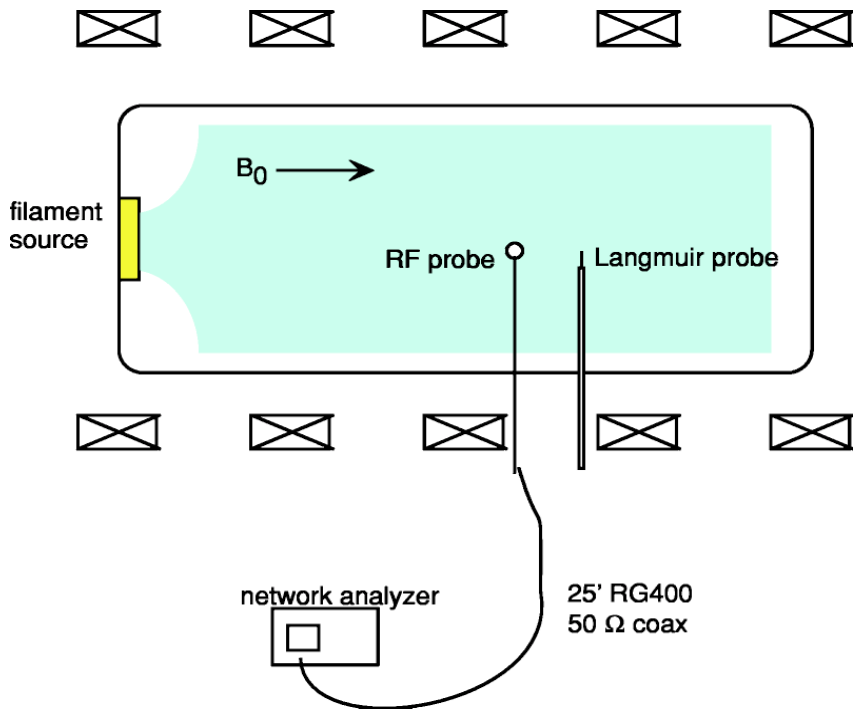


Fig. 1.3: Experimental setup used to measure the plasma impedance.

which are shared with the other instruments have a mass of 3.291 kg. This instrument suffers from all the same drawbacks listed above for the design developed by Steigies et al. [57].

In 2006, Hummel [60] reported a PIP instrument that used the quadrature technique to measure both the magnitude and phase of the probes impedance. In this method, two high speed analog-to-digital converters were used to sample the current signal and the drive voltage signal at the frequency of the drive signal, but one quarter of the period delayed from each other. The magnitude and phase were extracted using an envelope detector and a phase-locked loop, respectively. Figure 1.6 depicts the block diagram of the quadrature PIP and the quadrature PIP electronic board.

In 2007, Sanderson [61] performed a detailed analysis of the quadrature PIP design and its performance on sounding rocket flights. The instruments reliability was limited by various transient errors that upset the stability of the quadrature design. The quadrature

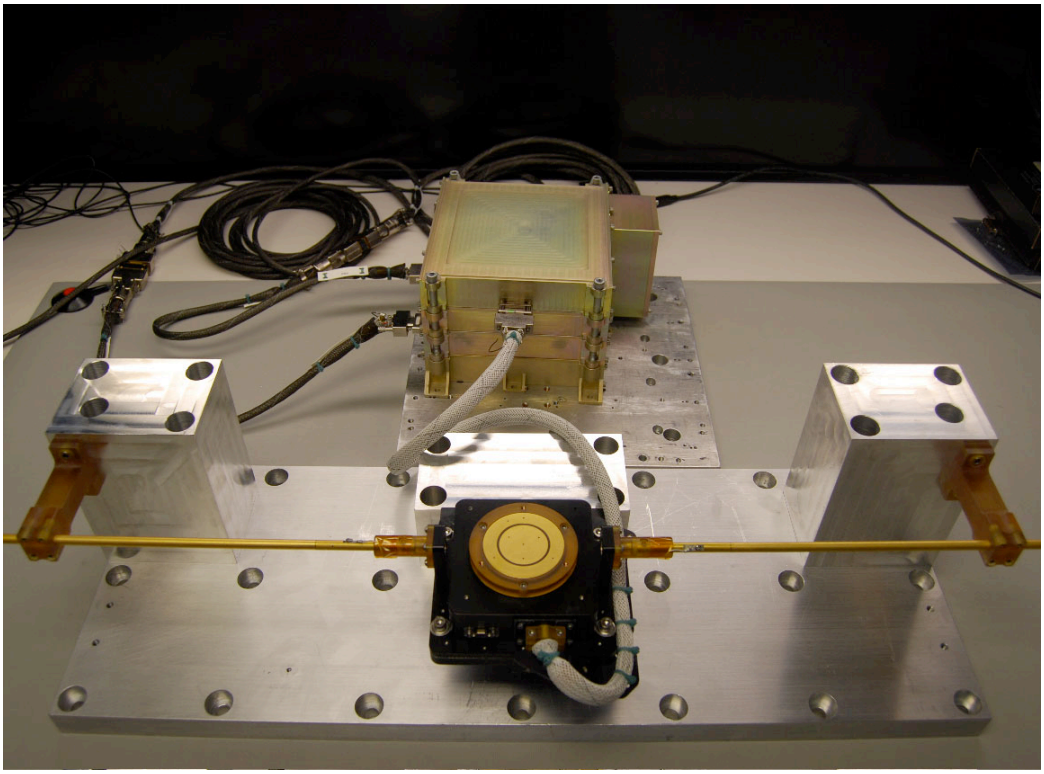


Fig. 1.4: The PISA instrument.

design also relied on the DDS to produce a precise sinusoidal stimulus for the probe. The quadrature PIP's accuracy and stability were adversely affected by the timing and delay errors generated by imperfections in the DDS oscillator and noise and stability problems associated with the wide band trans-impedance amplifier. The instrument was made from off-the-shelf components. Maximum power was consumed by the DDS. The power dissipated by each DDS was about 650mW at 5V supply and 180 MHz clock. Further, the peak-to-peak (p-p) output jitter of the DDS was measured to be 250 ps, when a 40 MHz 1V p-p input sine wave clock generation configuration was used. The dimensions and the power consumption along with the other disadvantages listed above make the quadrature PIP ill-suited for CubeSats.

Several commercial probe systems [62–64] are also available to measure a wide range of plasma parameters such as plasma density, uniformity, and electron temperature distribution. Nearly, all of them attach probes to bench-top instruments like a computer to do

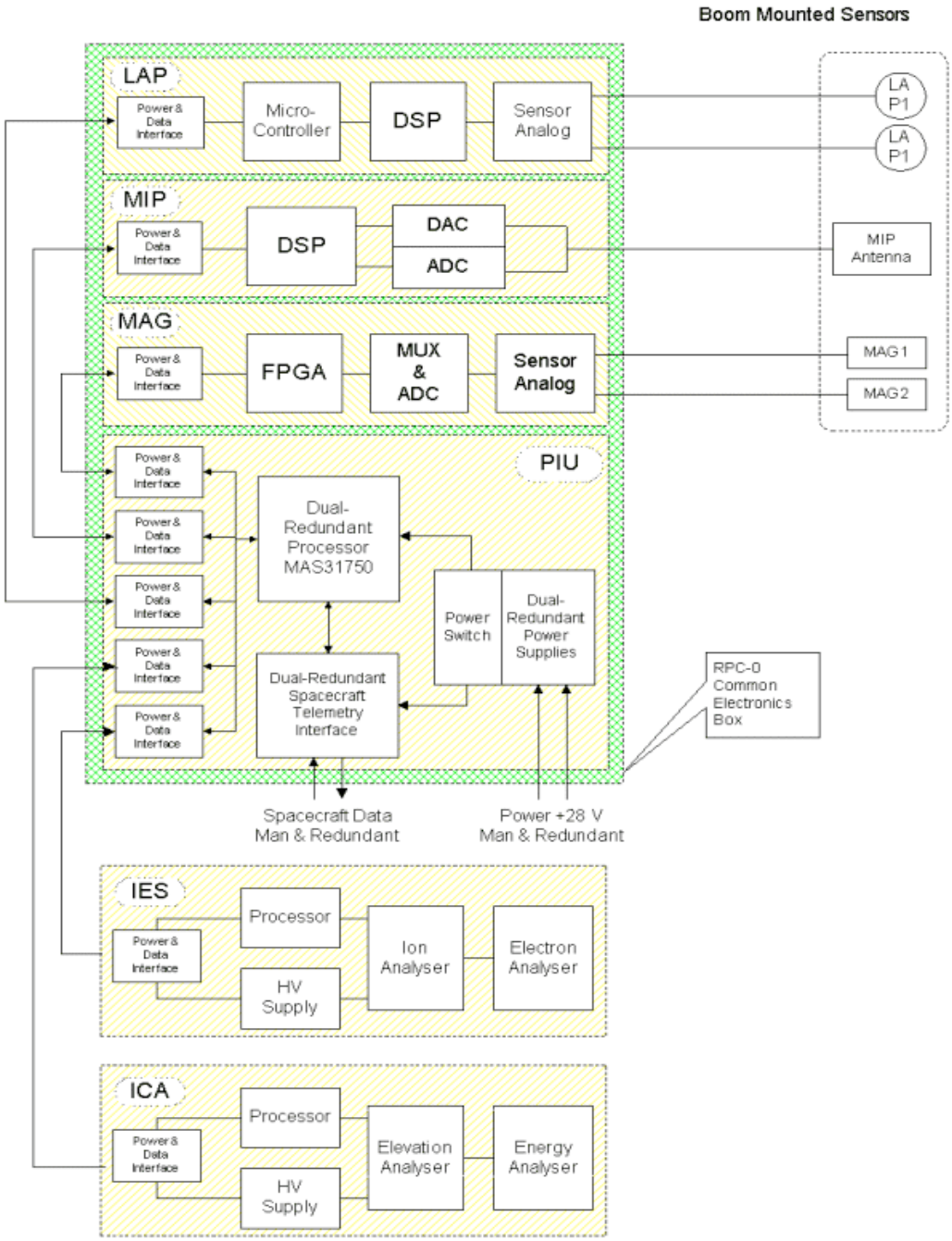
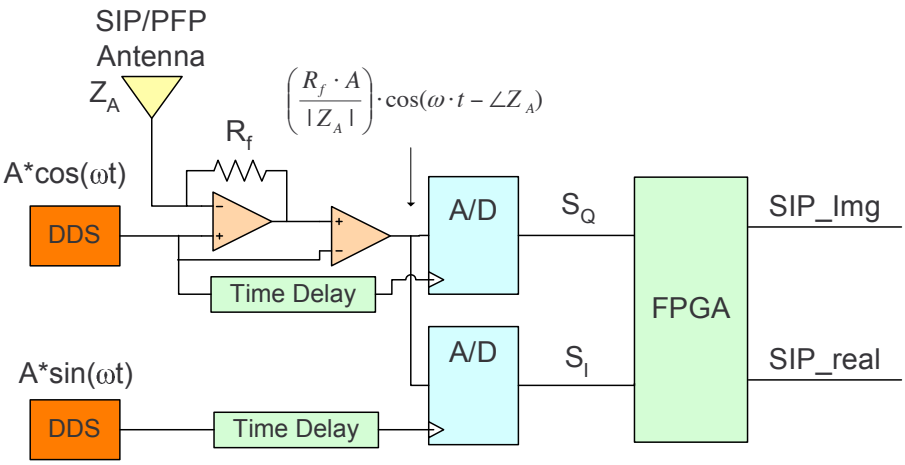


Fig. 1.5: RPC instrument schematic.



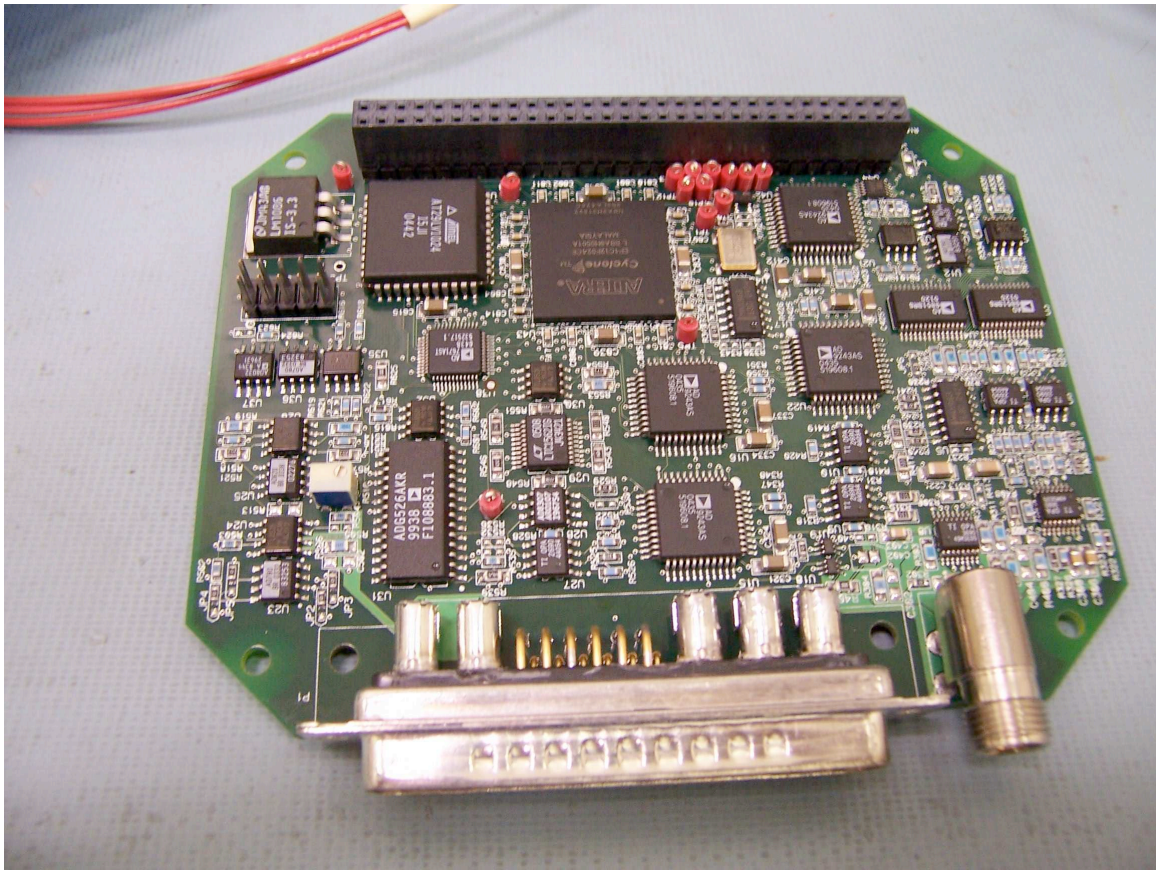


Fig. 1.6: Quadrature PIP.

the actual impedance measurement. These existing commercial systems are inadequate for the highly constrained dimensions and power budget of nanosatellites.

1.4 Motivation for the New PIP Instrument

Most of the PIP and IS instruments currently available attach on-chip probes to bench-top instruments (either a PC with a DAQ or some sort of network analyzer) to do the actual impedance measurement. While this could prove useful for initial research, it presents some serious limitations as well. Bench-top equipments are expensive and severely limits the large scale production and deployment of these systems. Further, the few existing on-chip impedance spectrometers are unsuitable for the frequency range under consideration while the existing PIP instruments are unsuitable for CubeSat applications due to the power, bandwidth, and volume requirements of the CubeSat platform. Hence a miniaturized, low-power solution is required. In this dissertation, an integrated architecture for the PIP that will enable space weather research from CubeSat platforms is developed. The PIP chip integrates all of the major analog and mixed-signal components needed to perform swept-frequency impedance measurements. By integrating these components onto a single chip, the weight and volume of the PIP instrument is drastically reduced. This resulting instrument will be capable of long-term, low-cost, multi-point deployments in nanosatellite applications.

1.5 Contributions of This Thesis

A new integrated electronic design for the PIP, suitable for CubeSat platforms, is presented in Chapter 2. To the author's knowledge, no other fully integrated PIP has been explicitly reported in literature. The major analog errors and parametric variations affecting the PIP instrument and its effect on the accuracy and precision of the impedance measurement are studied. A novel behavioral verification methodology is also presented in Chapter 2. In Chapter 4, a new low-power, low-jitter clock generation circuit is proposed. Performance comparisons between the author's custom phase locked loop (PLL) and existing PLLs for clock generation are examined in Chapter 4. The advantages and viability of the

new design for CubeSat platforms are also analyzed in Chapter 4.

The new integrated PIP instrument developed for CubeSats, would help in realizing an accurate ionospheric plasma density model with spatially distributed measurements. Though this instrument is mainly developed for measuring the plasma impedance, the system architecture could be extended to develop a fully on-chip IS system that could be used for a wide variety of biological and medical applications. The novel clock generation circuit though ideal for the integrated PIP instrument can be optimally used in general purpose analog-to-digital converters (ADCs) to provide a low- jitter clock.

1.6 Outline of This Thesis

Chapter 2 describes the system architecture for the integrated PIP and its advantages over existing systems. The top-down design methodology adopted is discussed in detail. The behavioral verification strategy and the impedance curves generated are also presented. Finally, the custom ADC developed for the PIP and the need for ADC clock optimization are summarized.

In Chapter 3, the need for a new clock generation circuit is presented. The PLL system operation is explained briefly. The sources of noise in the PLL are discussed and the relationship between integrated phase noise and jitter is defined. Various existing methods for reducing jitter and reference spurs are also presented.

Chapter 4 presents an introduction to Muller C gates. A novel PLL using Muller C elements to reduce jitter and reference spurs is proposed. The theory and implementation details are discussed. Finally, a performance metric for the PLL is defined and the Muller C PLL is compared with other existing PLL designs.

Chapter 5 summarizes the main contributions of this dissertation.

Chapter 2

Proposed PIP Design: Architecture, Modeling, and Results

In this chapter, a single-chip electronic system for a PIP suitable for nanosatellite instrumentation will be described. The PIP chip integrates all of the major analog and mixed-signal components needed to perform swept-frequency impedance measurements. Unlike previous PIP designs described in Section 1.3, the integrated PIP performs direct voltage current sampling on the probes terminal. A Fast Fourier Transform (FFT) is performed by an off-chip FPGA to compute the impedance of the probe and plasma. By performing analog-to-digital conversion as early as possible in the signal flow chain, the design is made less sensitive to variability in analog components. By using an FFT operation, the PIP instrument is made less sensitive to transient spikes that proved disruptive in previous PIP designs [60]. Further, integrating all the analog/mixed signal components onto a single chip, drastically reduces the weight and volume of the PIP instrument.

2.1 Proposed PIP Design

The new electronic PIP design samples the probes current and voltage signals directly. This approach eliminates the PIPs requirement for a pure sinusoidal stimulus, and greatly relaxes the error tolerance for the DDS. The new design eliminates analog signal processing wherever possible, thereby eliminating several sources of error and instability from the system. The impedance magnitude and phase are extracted by a FFT, which is performed off chip in a complementary FPGA device. The FFT operation is insensitive to transient errors and increases the noise immunity of the system.

2.1.1 System Architecture

The proposed system architecture is shown in Figure 2.1. The probe is simulated by a

sinusoidal voltage waveform generated by the DDS. A transimpedance amplifier replicates the DDS signal on both of its terminals. The probes current passes through the feedback impedance, Z_F, so that the op amps output signal is $V_{DDS} + IZ_F$. The DDS voltage signal is then subtracted from the amplifiers output to produce a signal proportional to the probes current.

A pair of matched ADCs are used to sample the DDS voltage signal and the signal proportional to the probes current. The sampled V_{DDS} and IZ_F signals are then sent to the FPGA for digital signal processing. The FPGA performs a FFT operation on each of the sampled signals at a frequency corresponding to the fundamental frequency of the DDS voltage signal. The two FFT outputs are then divided to produce the impedance. The FPGA contains control logic which coordinates a frequency sweep from 100 kHZ to 20MHZ, and delivers impedance data to other system components (e.g. a telemetry data transmitter).

2.1.2 Advantages

The system has a high tolerance to common analog errors such as nonlinear distortion, clock jitter, and transient spikes or glitches. The spectral effects of these errors tend to appear away from the fundamental component. So they can be effectively filtered out by the FFT operation. For the same reason, the DDS signal can be any periodic waveform, not necessarily a sinusoid. This decreases the instruments sensitivity to imperfections in the probes stimulus waveform. In addition, the use of symmetric differential sampling helps in eliminating nonlinear distortions. This increases the noise immunity of the system.

The use of matched ADCs to sample the probes current and voltage signals decreases the instruments sensitivity to variations in the probes stimulus waveform. Since precise sinusoids are not required, a low-power, low-resolution DDS design can be used. After eliminating most of the analog signal processing, the proposed system requires only two precision components, the transimpedance amplifier and the ADC.

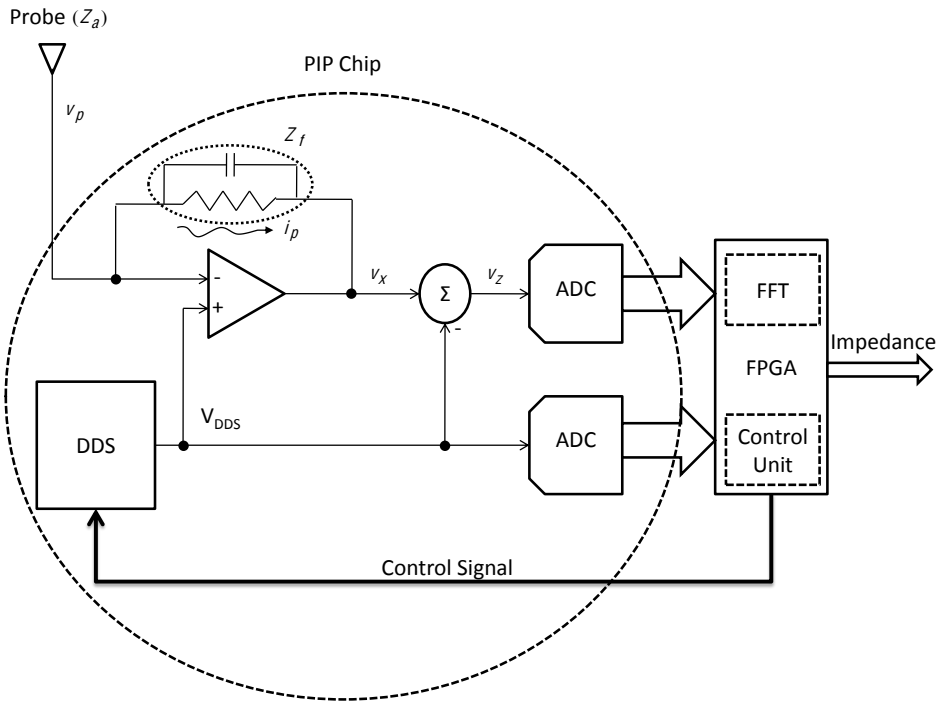


Fig. 2.1: Proposed PIP system architecture.

2.2 Design Methodology

Our design approach for the new PIP system is strongly focused on analog errors and variations. Revisions are costly in fully-integrated designs, so the design must be thoroughly characterized and verified before fabricating any prototypes.

To evaluate the error tolerances in the PIP chips integrated parts, we ask two fundamental questions for each component.

- What are the major errors and parametric variations associated with the component?
- For each error or variation, what is its effect on the accuracy and precision of the impedance measurement?

These questions are addressed using a top-down design strategy in which every effect is evaluated within the context of a full system simulation. A complete system framework is created using Matlab/Simulink [65]. This framework includes physical probe/plasma

models, the DDS, transimpedance amplifier, ADCs, FFT, impedance computation, and control logic.

To evaluate the impact of errors and variations, the Simulink framework is disturbed by inserting a component error model. We then evaluate the errors effect on the impedance calculation. For random parametric variations, Monte Carlo simulations are performed. The variations impact is quantified by calculating the statistical variance in the measured impedance.

By evaluating each error and variation, design effort can be focused on reducing the most significant error sources. The top-down strategy also allows us to simulate errors and variations in groups, so that we can quantify the accuracy and precision of the PIP under the influence of all errors and variations. This assessment reveals the value and limitations of the PIP as a scientific instrument.

2.3 Transistor-level Design

The top-down design strategy is useful for system modeling and for transistor-level component design.The central problem in integrated system design is behavioral verification: the entire design hierarchy must function together as a cohesive instrument.

Our component design/verification strategy is illustrated in Figure 2.2. For integrated component design, we use the Cadence chip design tools. Within Cadence, the PIP chipss complete design hierarchy is built using the Verilog-AMS language. Verilog-AMS is a behavioral language for modeling analog/mixedsignal components. Verilog-AMS simulations allow for a mixture of models at several levels of abstraction, including:

- Intermediate level: semi-ideal circuit models, including timing behavior, parasitics and other electrical characteristics;
- Transistor level: actual circuit simulation with physical device models;
- Post-layout: extracted circuit models from a physical chip layout.

Cadence and Matlab recently introduced a cross-link capability that allows Cadence components to be simulated within Simulink models. Consequently, all Verilog-AMS models

are tested within the Simulink system framework. By maintaining a top-down environment throughout the design process, we can fully quantify the precision of the PIPs impedance measurements across its entire spectral range.

2.4 Behavioral Verification of the PIP Instrument

The PIP instrument is heterogeneous in nature as it integrates analog, digital, and RF hardware, as well as software components. Hence, its design, verification, and modeling is complicated. Further, each top-level circuit simulation can consume CPU time ranging from hours to days to weeks. This invariably means speeding up the top-level verification with the help of behavioral models written using a higher level language. These models can be either basic models that are used to verify the functionality or complex models that are used to predict the system performance. This section describes the modeling of the PIP instrument performed using various languages and tools.

2.4.1 Modeling with Matlab/Simulink

A complete PIP framework was built using Matlab/Simulink by Hamoui [65]. This frame work included the physical probe/plasma models, the DDS, transimpedance amplifiers, ADCs, FFT, impedance computation, and control logic. Further details about this work can be found in Hamoui [65].

2.4.2 Modeling with Verilog-AMS

Behavioral modeling and simulation, using Verilog-AMS for the PIP chip makes system level analysis much more efficient and accurate [66]. The key challenge faced during verification was in ensuring that the behavioral Verilog-AMS model represents the functional as well as parametric (when desired) behavior of the block being modeled. Apart from this, it is also critical to ensure that the connectivity of the analog blocks matches between circuit schematics and behavioral models.

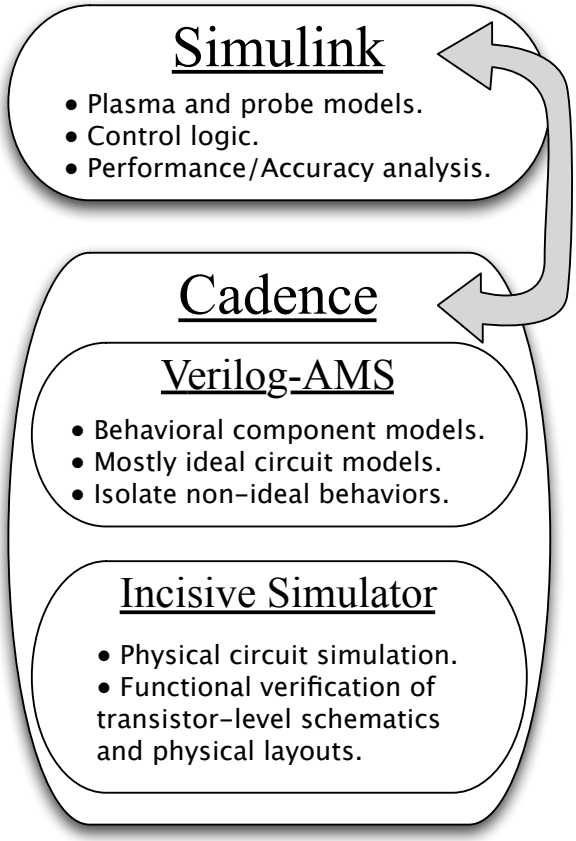


Fig. 2.2: Levels of abstraction and tools used for the functional verification of the PIP chip design.

Verilog-AMS Features

Verilog-AMS hardware description language (HDL) defines a behavioral language that can be used for analog as well as mixed-signal systems. Since Verilog-AMS combines Verilog-HDL as well as Verilog-A, as shown in Figure 2.3, it inherits the ability to process both digital and continuous time analog signals. It also processes analog discrete-event signals.

Verilog-AMS makes it more straightforward to write behavioral models for mixed-signal blocks and brings strong event-driven capabilities to analog simulation, allowing analog event-driven models to be written that perform with the speed and capacity inherited from the digital engines [67].

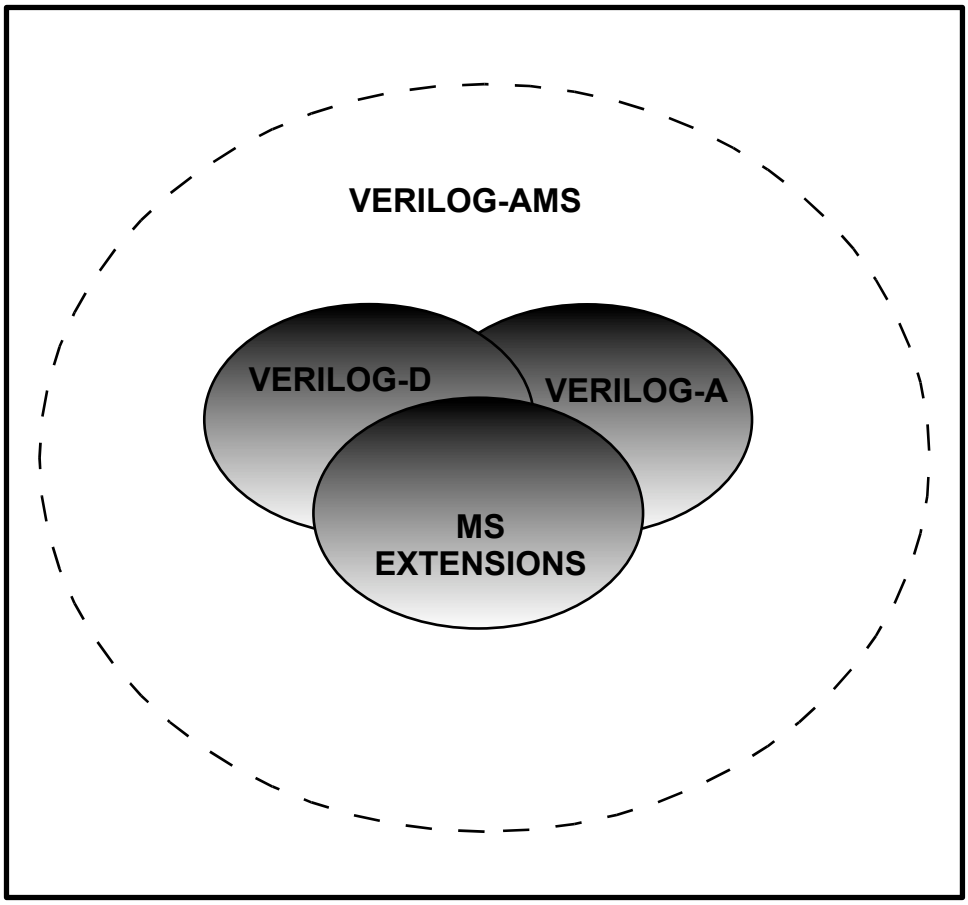


Fig. 2.3: Verilog-AMS architecture.

Applied Modeling Methodology

Verilog-AMS supports multi-level and multi-domain simulation as shown in Figure 2.4. Hence, it was used to model various components of the PIP-chip, including the ADC, the transimpedance amplifier and the PLL used in the DDS. The methodology used was based on the following elements:

- The use of Verilog-AMS to describe the functionality of the analog/mixed signal blocks including the transimpedance amplifier, the ADC and the PLL;
- The use of Cadence Virtuoso environment to combine analog and digital signals in a single environment;

- The use of Virtuoso AMS Design Simulator as the mixed abstraction level simulator.

When using the top-down methodology for developing the PIP chip, there are various needs for mixed-signal models. Initially during the architectural phase, the blocks were represented abstractly, a single block describing the complex analog and digital functionality. Verilog-AMS was used to describe this complex system. As the design is specified in more detail, it can be partitioned into analog only, digital only or mixed-signal. Figure 2.5 shows the proposed mixed-signal modeling framework.

Modeling Implementation

Transimpedance Amplifier: The operational amplifier configured as a transimpedance amplifier, exhibits analog behavior. The non-ideal opamp model is straightforward and was modeled using Verilog-AMS. Figure 2.6 shows the well-commented Verilog-AMS code used to model the opamp.

PLL: The DDS system consists of a clock divider, a digital counter, a read only memory (ROM), and a digital-to-analog converter (DAC). These signals are generated from a stable and accurate clock source. This referenced clock is generated using a phase-locked loop (PLL). The PLL block diagram is shown in Figure 2.7. The Phase-Frequency Detector (PFD) detects the difference between the input reference frequency and the output frequency of the Voltage Controlled Oscillator (VCO). This voltage signal proportional to the difference is exported and drives the charge pump (CP) circuit. The output current of the CP is converted into smooth voltage by the loop filter (LP). This voltage controls the VCO, and eliminates the frequency error. The CP, VCO, and loop filter are all circuits that exhibit analog behavior while the PFD and frequency divider are purely digital. The CP, VCO, and LP were modeled using Verilog-AMS while Verilog HDL was used to model the PFD and the frequency divider(FD). The top-level PLL design was modeled using Verilog-AMS.

ADC: There are several well-known ADC architectures [68]. For our PIP design, a 1.5 bits/stage, 16-bit pipelined ADC was chosen, as the PIP needs to operate at input frequencies up to 20 MHz while still maintaining high accuracy. In addition, system accuracy

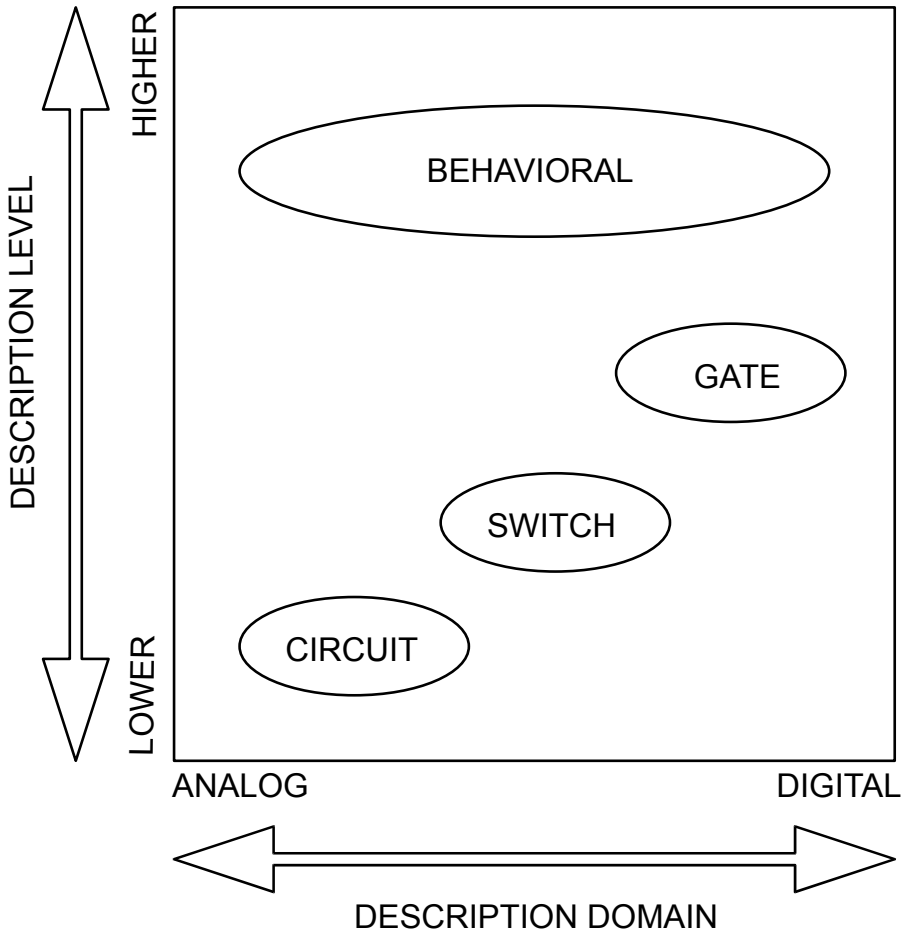


Fig. 2.4: Verilog-AMS: Scope for description.

requirements can be relaxed by using digital error correction. Figure 2.8 shows the block diagram for the modeled pipelined ADC and the ADC description domain.

The pipeline ADC is a cascaded array of N individual stages where each stage consists of a Sample-and-Hold (S/H) block, an m-bit low-resolution stage-ADC, an m-bit low-resolution stage Digital-to-Analog Converter (DAC), an analog subtractor, and a 2m gain-amplier. The S/H, samples the input voltage Vin at each clock cycle. It then holds the final sampled value. This sampled value is passed on to the input of the stage-ADC to produce a low-resolution digital output word. The stage-DAC then converts the digital output word to its

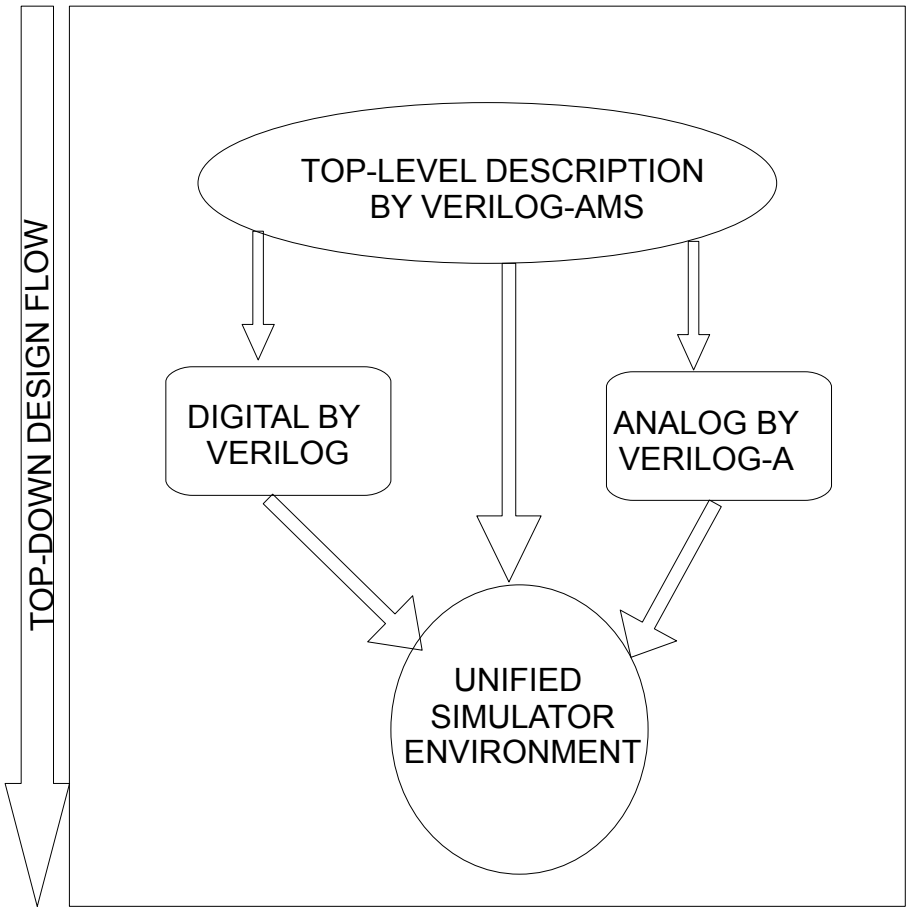


Fig. 2.5: Proposed mixed-signal modeling framework.

equivalent analog voltage. This voltage is then subtracted from Vin to yield the residue. This is done in order to ensure that all stages of the pipelined ADC use the same input voltage range.

On the next clock cycle, the residue of each stage is applied to the next stage for further quantization. This process continues until full quantization of the sampled voltage is achieved. Then the digital outputs from each stage are passed to the digital error correction algorithm, which performs addition by using a series of full adders to form the final digital output word Dout. Since no digital correction can be done after the last stage, the least

```
`define dB2dec(x) pow(10,x/20)
module opamp(vinp,vinm,vdd,vss,voutp,voutm);
 inout vinp,vinm,vdd,vss;
 inout voutp,voutm;
 electrical vinp,vinm,vdd,vss,voutp,voutm;

 parameter real gain = 100 from (0:inf),      // open loop gain in dB
        three_dB_freq  = 1M from (0:inf), // 3dB frequency
        rin  = 1M from (0:inf),           // input resistance
        cin  = 1n from [0:inf),           // input capacitance
        iout_max = 100n from (0:inf), // max. output current
        vout_offset = // output dc offset,
        rout = 80 from (0:inf),         // output resistance

 real vin,vout,voutmax,voutmin,vout0,iout;

 analog
 begin
  vin  = V(vinp,vinm);
  vout = V(voutm,voutm);
  voutmax = V(vdd);
  voutmin = V(vss);

  // input stage
  I(vinp,vinm) <+ vin / rin + cin * ddt(vin);

  // dominant pole
vout0 =laplace_nd(vin*`dB2dec(gain),{1{1,1,(`M_TWOPI*three_dB_freq)}})
      + vout_offset;

  // output current
  iout = (vout0 - vout) / rout;

  // output current limitation
  case (1)
   iout >  iout_max : iout =  iout_max;
   iout < -iout_max : iout = -iout_max;
  endcase

  /* slewrate applied is only an estimation to smooth out
    the discontinuity introduced by the output voltage limitation
    it is not the slew rate of a real opamp !!!
  */
  I(voutp,voutm) <+ slew(iout,iout_max*three_dB_freq);
 end
endmodule
```

Fig. 2.6: PLL block diagram and description domain.

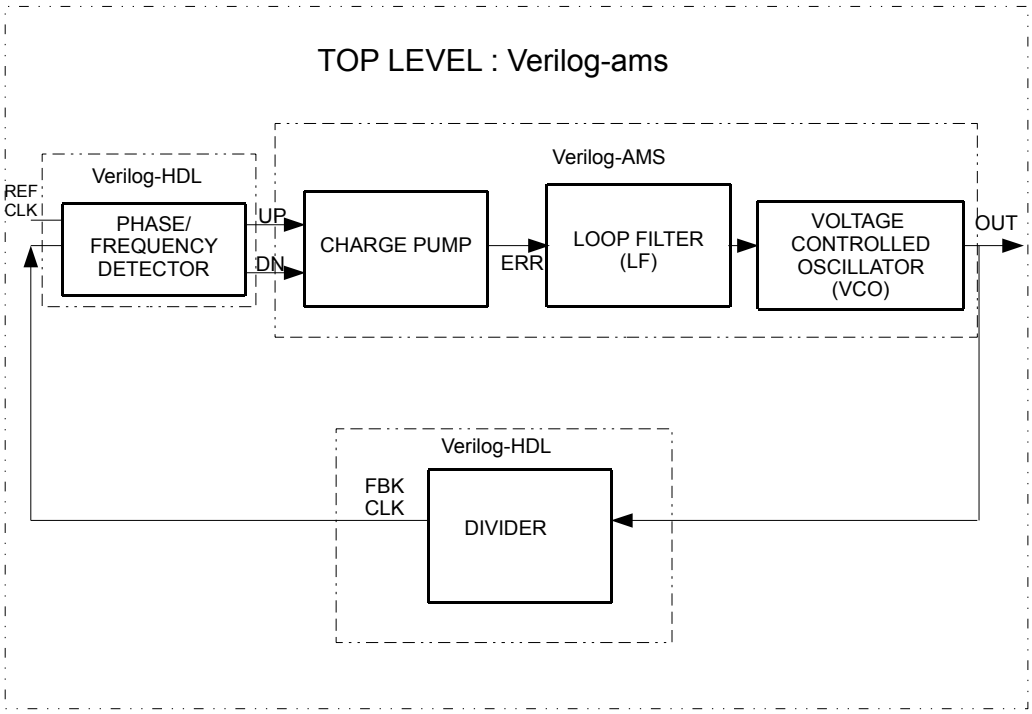


Fig. 2.7: PLL block diagram and description domain.

signicant bit is ignored. Further, the stage-ADC outputs are delayed through digital latches (D blocks) such that Dout corresponds to the sampled input.

The 1.5-bits/stage can be thought of as a super 1-bit/stage, where the gain of the amplier is kept at 2. The stage-ADC supplies two output bits (b1 b0) for digital correction and code conversion. The stage-DAC acts as a multiplexor which selects whether to add or subtract Vref from the input signal or take no action. The extra 0.5-bit redundancy is used to compensate for tolerances and imperfections in the comparators. This redundancy is later canceled out by digital error correction.

The individual stages containing the S/H, stage-ADC, stage-DAC, gain amplifier, and analog subtractor are all circuits exhibiting analog behaviour while the digital correction circuit consisting of the adders and latches are purely digital. Hence, Verilog-AMS was used to model each stage of the ADC while Verilog-HDL was used to model the digital correction

circuit. The top-level ADC was then simulated using the unified Cadence Virtuoso AMS designer.

2.4.3 System C and Cadence NCSim

System C was used to implement the DDS using Cadence NCSim. The DDS system consists of a clock divider, a digital counter, a read-only memory (ROM), and a DAC. The FFT operation performed by the FPGA was also modeled using the Cooley-Tukey FFT algorithm [69] in System C. System C supports all the data types supported by C++, and hence, the FFT operation becomes easier to model using System C. Figure 2.9 and Figure 2.10 show the functional block diagram of the DDS and the FFT operation in Cadence NCSim environment, respectively.

2.5 Cadence-Simulink Co-Simulation

The co-simulation capability between the Cadence Virtuoso AMS Designer simulator and MATLAB/Simulink (AMS-MATLAB/Simulink co-simulation), allows the design and simulation of analog and mixed-signal subsystems in system-level simulations. The Verilog-AMS models of the DDS and ADC components developed in Cadence were co-simulated and verified within the Matlab/Simulink framework. The co-simulation was performed using coupler modules on both ends of the simulators. Both couplers communicate with each other using a TCP/IP socket-based approach.

Cadence/Simulink co-simulation supports different flows that support different groups of users.

- ADE Flow: Run co-simulation by starting MATLAB/Simulink from the Virtuoso Analog Design Environment (ADE). This is for users who want most of the debugging to be done in the Virtuoso environment.

- Simulink Flow: Run the co-simulation from MATLAB/Simulink (without starting ADE) using the runSimulation script that comes from the ADE flow. This is for users who would rather visualize the results using Simulink.

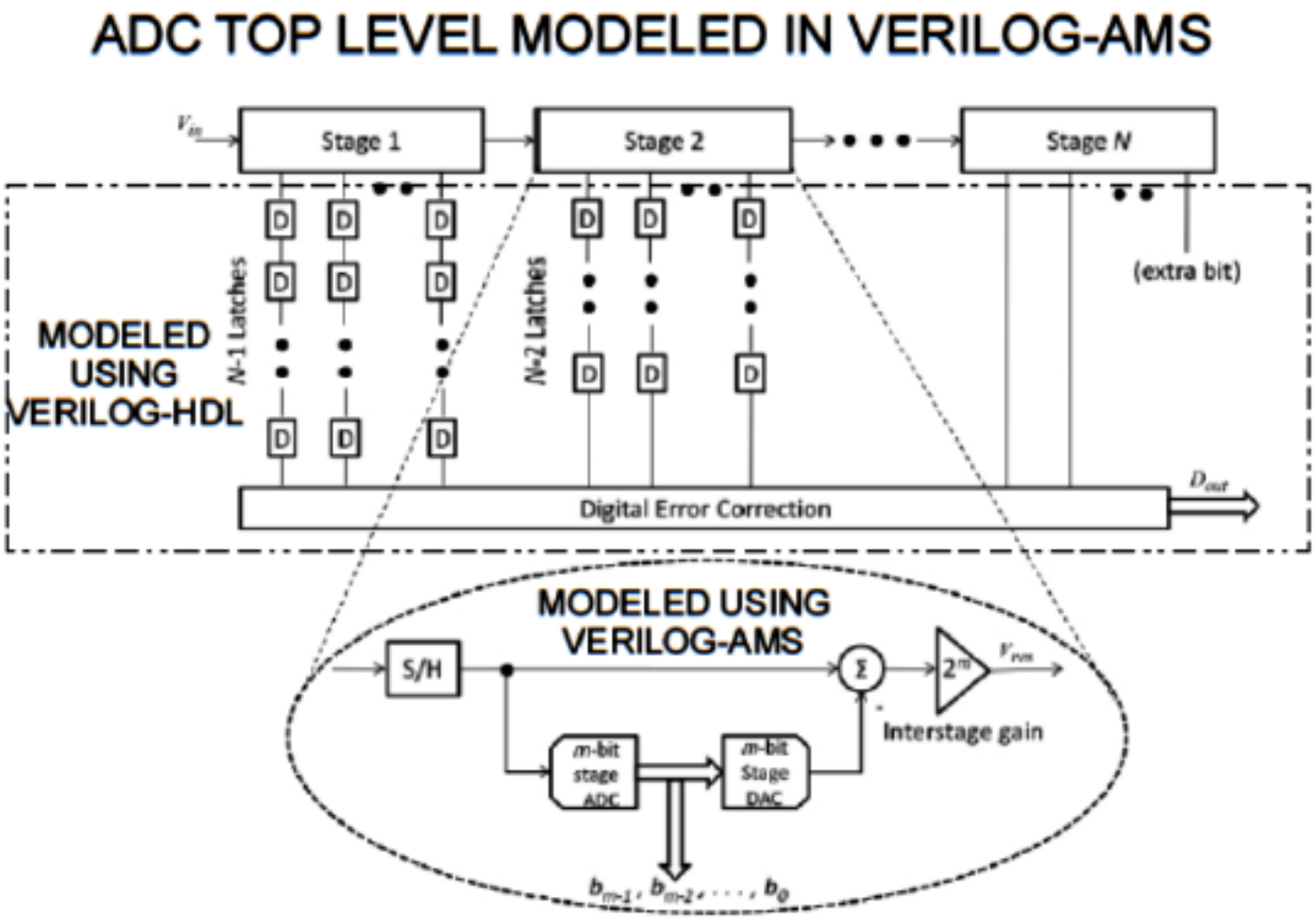


Fig. 2.8: Pipelined ADC block diagram and description domain.

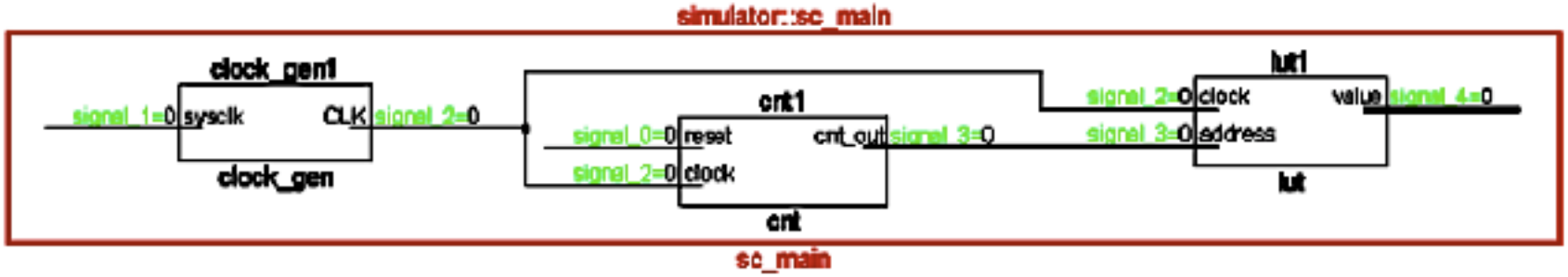


Fig. 2.9: DDS block diagram generated using System C and Cadence NCSim.

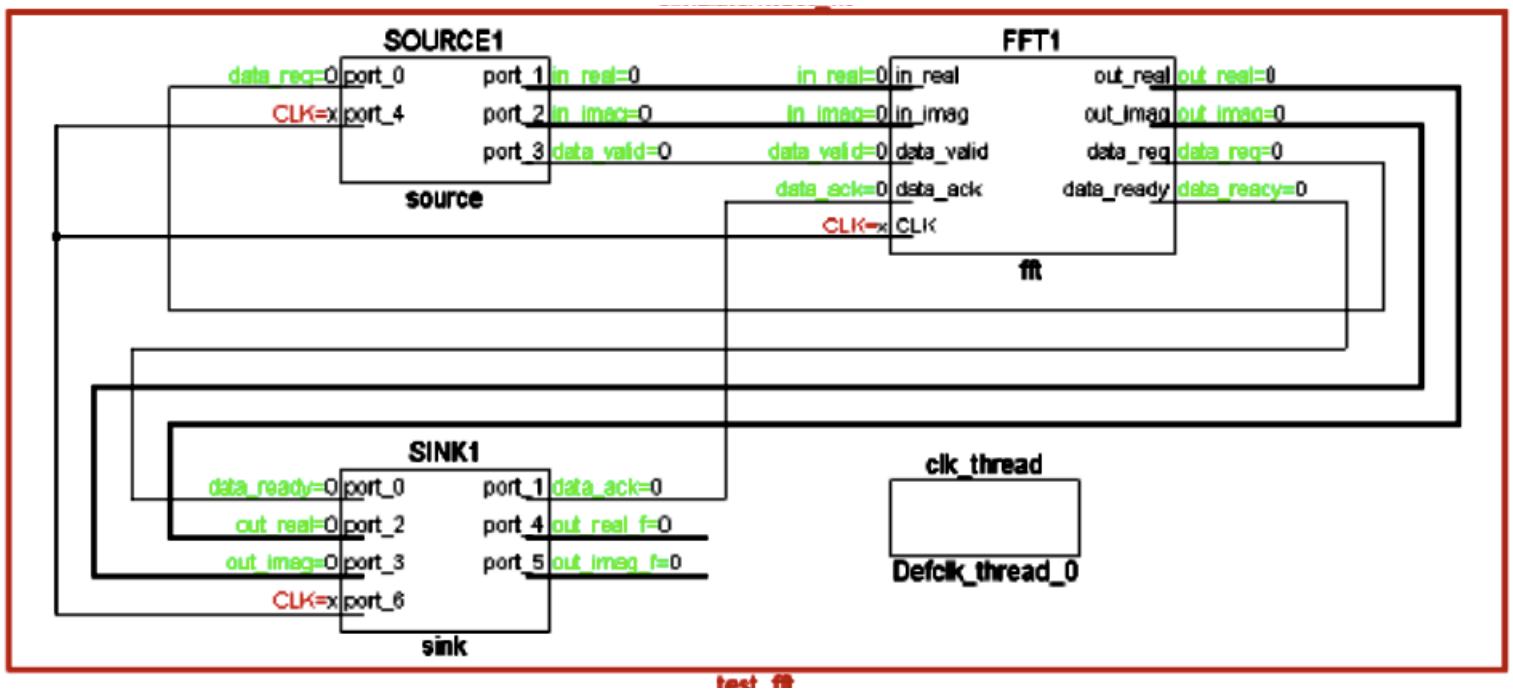


Fig. 2.10: FFT operation block diagram generated using System C and Cadence NCSim.

- AMS Environment Flow: Start MATLAB first, then start the AMS environment from the Virtuoso hierarchy editor (HED), and run simulations separately using each of these programs. This type of flow is for users who are experienced in both tools, and who want to have more control on the co-simulation functionality.

Since the frequency sweep and the FFT operation for the PIP chip is controlled by Matlab/Simulink, the Simulink co-simulation flow was chosen. The co-simulation schematic in the Simulink framework is shown in Figure 2.11 and the co-simulation schematic in the Cadence framework is shown in Figure 2.12. Inputs to the simcoupler include the system clock, the output of the transimpedance amplifier, the inputs to the DDS namely the clock divider ratio (k), and the counter increment (n). The Simulink coupler's outputs include the outputs of the matched ADCs and the DDS output. The DDS signal is fed back to the plasma probe and the sampled current and voltage from the ADC are sent to the control unit for further processing.

The resulting impedance curves from the theoretical Balmain model, the non-ideal Simulink model and the Cadence-Simulink co-simulation are shown in Figure 2.13. From Figure 2.13, we see that with a more realistic Verilog-AMS model of the ADC and the DDS, the impedance magnitude is precisely measured with a slight deviation at some frequencies. Only eleven co-simulation points were considered because of limited memory and processor clock speed exhibited by the lab Linux machine. The frequencies at which the co-simulations were performed were chosen so at to be more concentrated at the resonance frequencies.

Thus, by maintaining a top-down environment throughout the design process, the precision of the PIPs impedance measurements across its entire spectral range is fully quantified. Precise impedance measurements were not necessarily the primary goal of previous PIP instrument designs, which were typically interested in locating resonance frequencies and could tolerate uncertainty in the absolute impedance magnitude (e.g. [57]). Our PIP design is intended to support a new generation of plasma instrumentation and research in which precise impedance measurements will be essential for studying an expanded set of plasma characteristics.

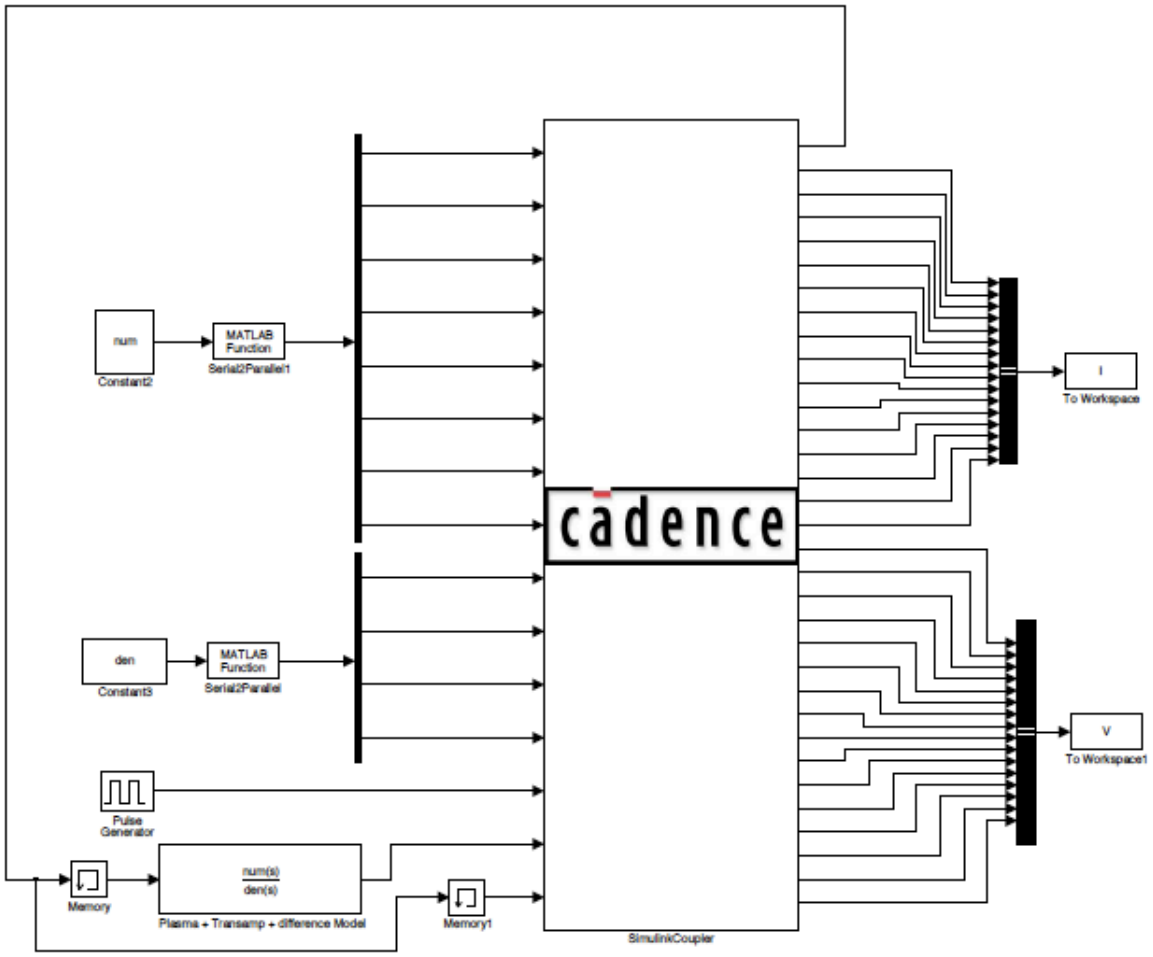


Fig. 2.11: Top-level system design showing co-simulation in the Simulink framework.

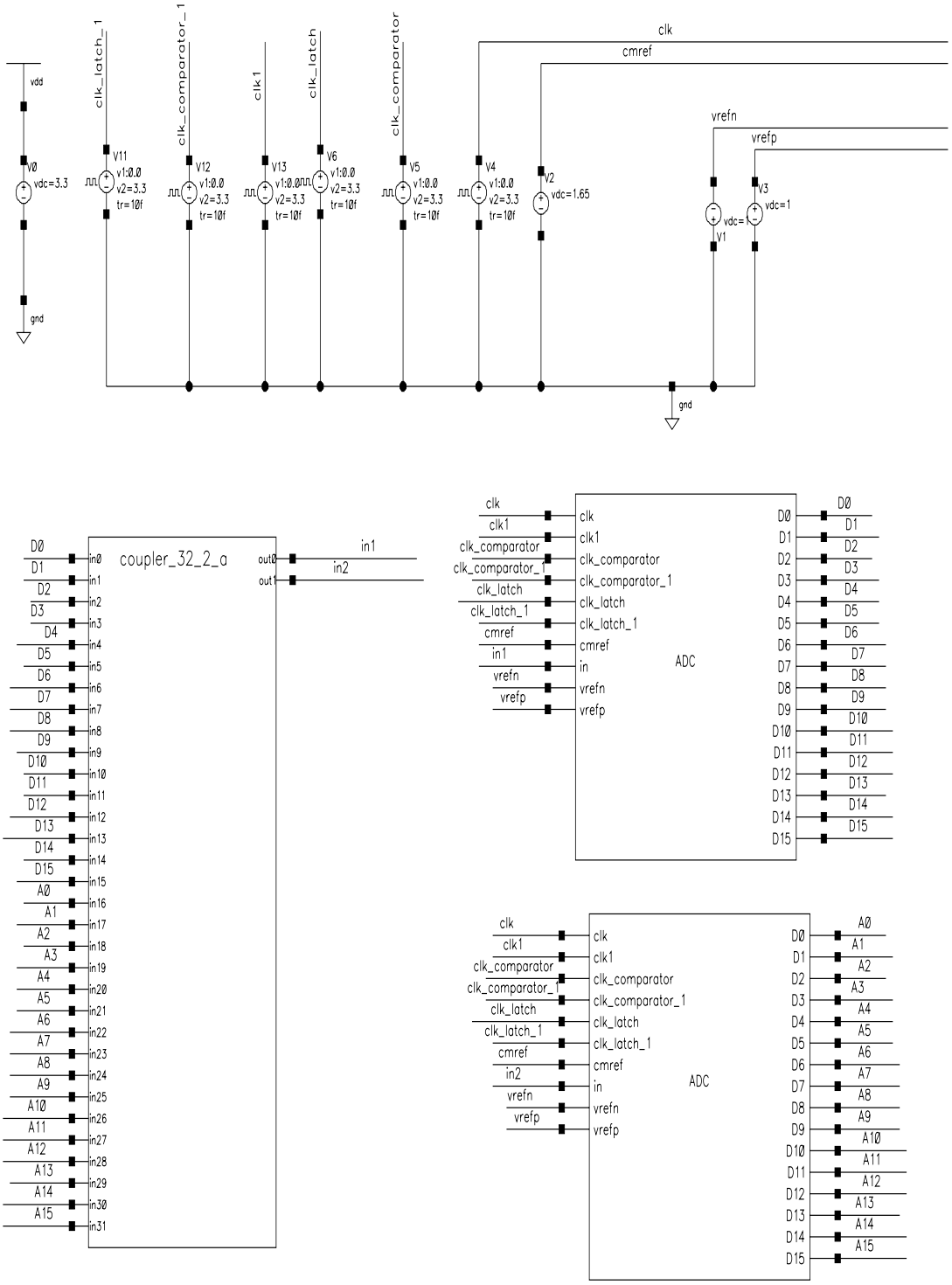


Fig. 2.12: Top-level system design showing co-simulation in the Cadence AMS framework.

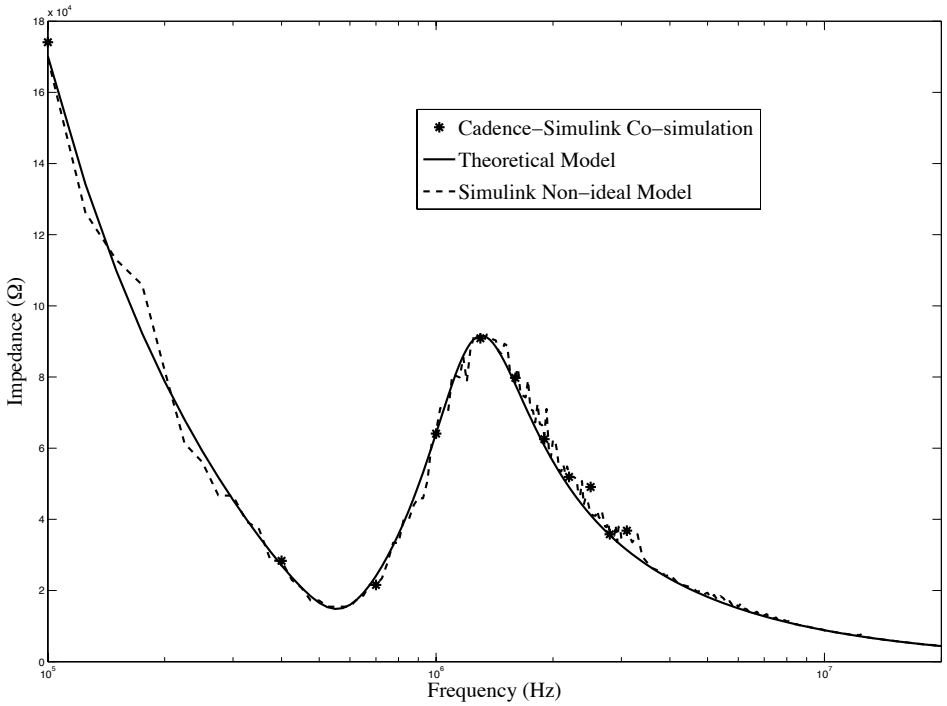


Fig. 2.13: Theoretical, Matlab/Simulink, and Cadence/Simulink co-simulation, plasma impedance curves.

2.6 Custom ADC for the PIP

An ADC that is uniquely optimized for our PIP chip was designed. Error tolerances for the ADC and its effect on the impedance measurement were considered. There are several well-known ADC architectures [68]. For our PIP design, a 1.5 bits/stage, 16-bit pipelined ADC was chosen, as the PIP needs to operate at input frequencies upto 20 MHz while still maintaining high accuracy. Pipeline ADCs are known to achieve medium-to-high resolution (in excess of 8 bits) at conversion rates of several hundreds of megahertz [68]. An increase in resolution mostly involves increasing the number of pipelined stages. Hence, the chip area would grow linearly in contrast to exponentially for flash and other parallel architectures. In addition, system accuracy requirements can be relaxed by using digital error correction techniques.

2.6.1 Characterization of the ADC

In order to fully characterize the pipelined ADC for the proposed PIP, it is necessary to determine which specification has the highest impact on the performance of the custom ADC for the PIP. The PIP instrument has to measure abrupt changes in the plasma impedance. Therefore, a high resolution ADC is required to detect the sudden, small variations in the impedance measurements. The resolution of an ADC and the Effective Number of Bits (ENOB) depends on its Signal-to-Noise ratio (SNR). A low SNR would increase the noise floor seen at the FFT output and may corrupt the fundamental signal. Hence, it is critical to have a high SNR for reliable impedance measurements.

In our PIP design, the FFT operation filters out all frequency components above the fundamental. Since the harmonic components appear away from the fundamental, common spectral requirements, such as THD, can be ignored for the purposes of our design. Signal-to-Noise-and-Distortion (SINAD) is of vital importance in general purpose ADCs. However, in our case, since the frequency distortion adds unequal degrees of amplification across all spectral components other than the fundamental, SINAD is not critical for the performance of the PIPs ADC. The Spurious-Free Dynamic Range (SFDR) can be made less stringent for our PIP design as the spurious signal has no effect on the fundamental.

2.6.2 Non-Idealities in the ADC and Instrument Accuracy

A 1.5-bits/stage 16-bit ADC, at a sampling frequency of 100 MHz, was modeled using Matlab/Simulink by Hamoui [65]. This model was used to analyze the effect of the non-idealities of the pipelined ADC on the fundamental component. High-speed ADCs are highly susceptible to nonlinear distortion. It is mainly caused by the switching mechanism at the S/H block, the pre-amplifier at the input of the ADC, and by other sources of nonlinearity introduced at the ADC input. A sigmoid function F(x) normalized to the reference voltage and centered about the origin was used to model the nonlinear distortion of the pipelined ADC by Hamoui [65]. Figure 2.14 depicts the errors and variations added to each stage of the pipelined ADC.

Figure 2.15 shows the FFT output for an ideal and a non-ideal ADC. It is evident that

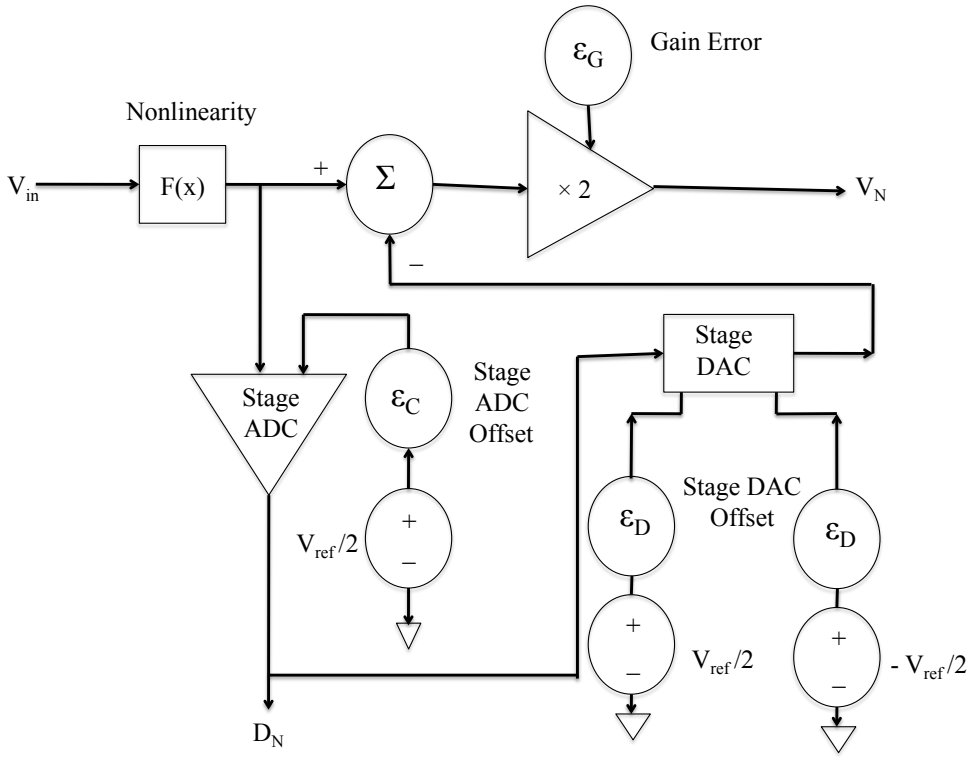


Fig. 2.14: Single stage of the pipelined ADC depicting the errors and variations added to the various components.

by adding errors and variations to the ADC components, the power of the fundamental gets disturbed, and the noise floor along with the harmonic spectral components increase significantly. Stage ADC, DAC, and gain non-idealities are the main factors that limit the performance of the pipelined ADC.

Figure 2.16 shows the effect of varying the standard deviation of each of the non-idealities, varying one while keeping the others fixed, on the fundamental output. σ_{out} is the standard deviation of the fundamental output from its ideal value, and $\sigma_{relative}$ is the relative standard deviation of the non-ideality being simulated. The non-idealities in the DAC have the highest influence on the fundamental output, which increases as its standard deviation increases. The gain amplifier stages have less of an impact on the fundamental component, but increases in the same manner as that of the DAC. The comparator offsets

had no effect on the fundamental output.

2.7 Analog-to-Digital Converter Clock Optimization

Jitter is probably the most important parameter in developing a good system clock circuit. Jitter is the variation in the placement of a clock edge. It produces a timing error, leading directly to errors in conversion amplitude accuracy as shown in Figure 2.17. From Figure 2.17, we see that increasing the analog input frequency increases the slope of the input signal, which magnifies the conversion error.

Equation 2.1 gives the relationship between the SNR(dB) and frequency of a perfect ADC having infinite resolution, while Equation 2.2 defines the SNR(dB) of a perfect ADC with N- (10, 12, 14, or 16) bit resolution.

$$SNR_{ideal} = 20 \log \left(\frac{1}{2\pi f t_{jitter}} \right) \tag{2.1}$$

$$SNR_{bits} = 6.02N + 1.76 \tag{2.2}$$

Figure 2.18 combines these two equations. Equation 2.1 represents the diagonal lines in Figure 2.18 while Equation 2.2 represents the horizontal lines in Figure 2.18. The intersections is the amount of total clock jitter that can be tolerated for a given analog input frequency [70]. At low frequencies, the accuracy is limited by the resolution of the converter. However, as the input frequency increases, the performance of the ADC is dominated by the total clock jitter of the system. Hence, the system clock has to be optimized in order to have a high performance ADC.

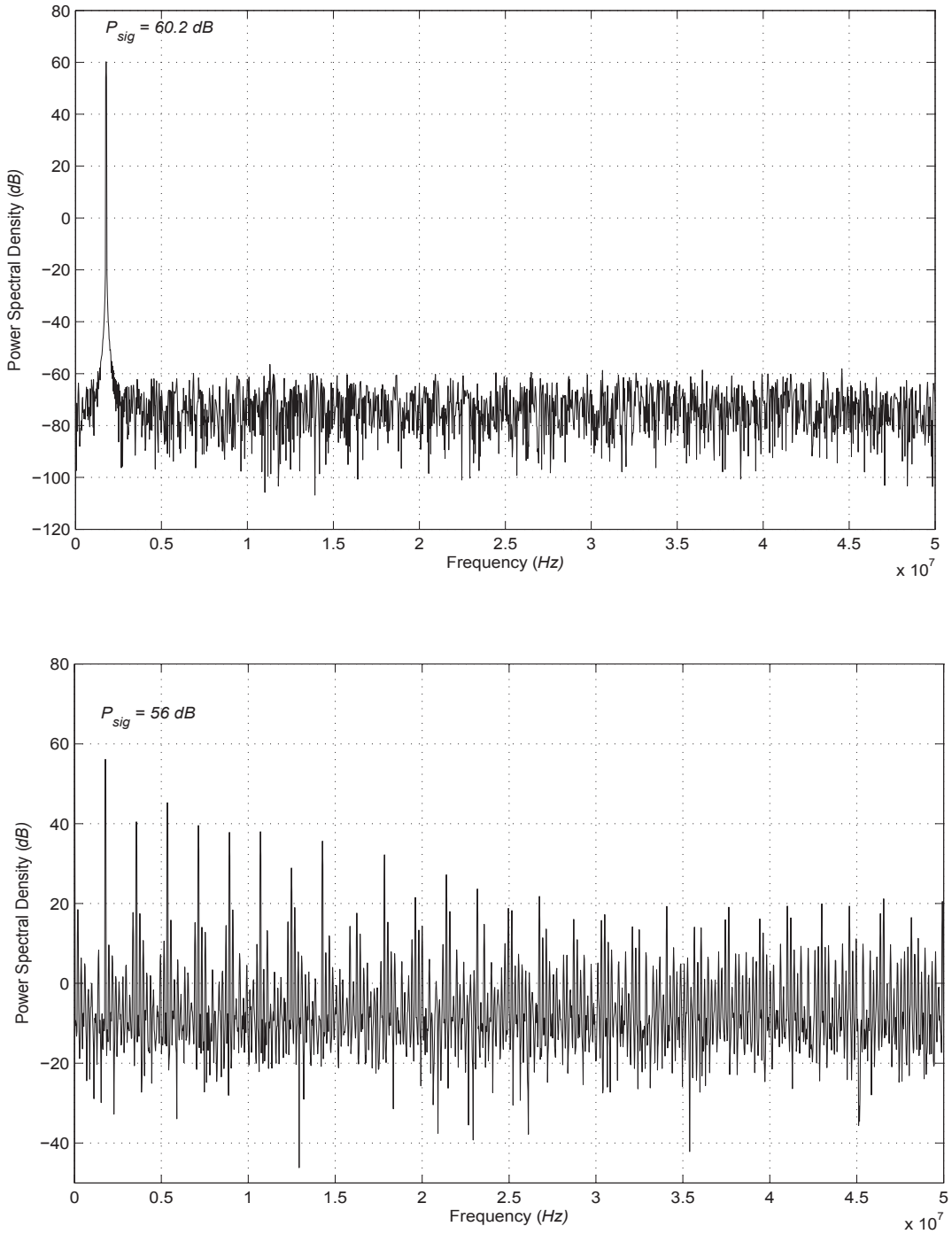


Fig. 2.15: FFT outputs showing the ideal and the effect of errors on the fundamental component.

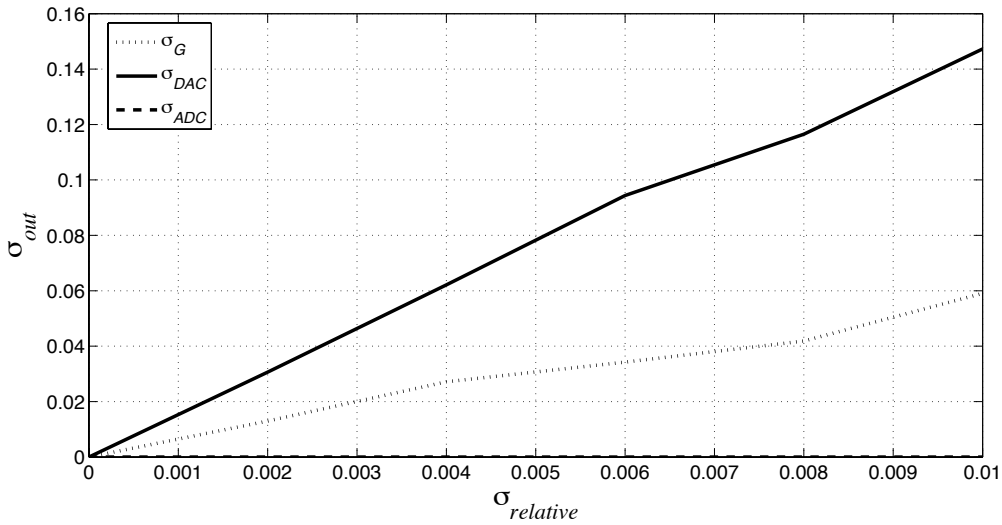


Fig. 2.16: Output standard deviation versus relative standard deviation for offsets at stage ADC, DAC, and gain stages.

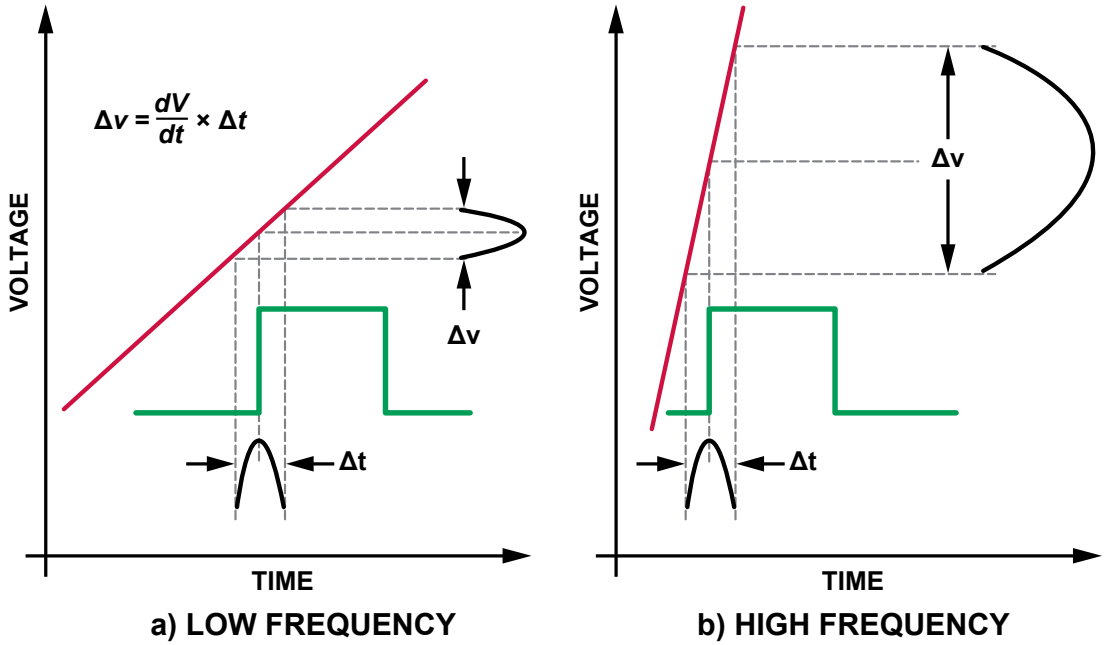


Fig. 2.17: Conversion error as a function of clock jitter and analog input frequency.

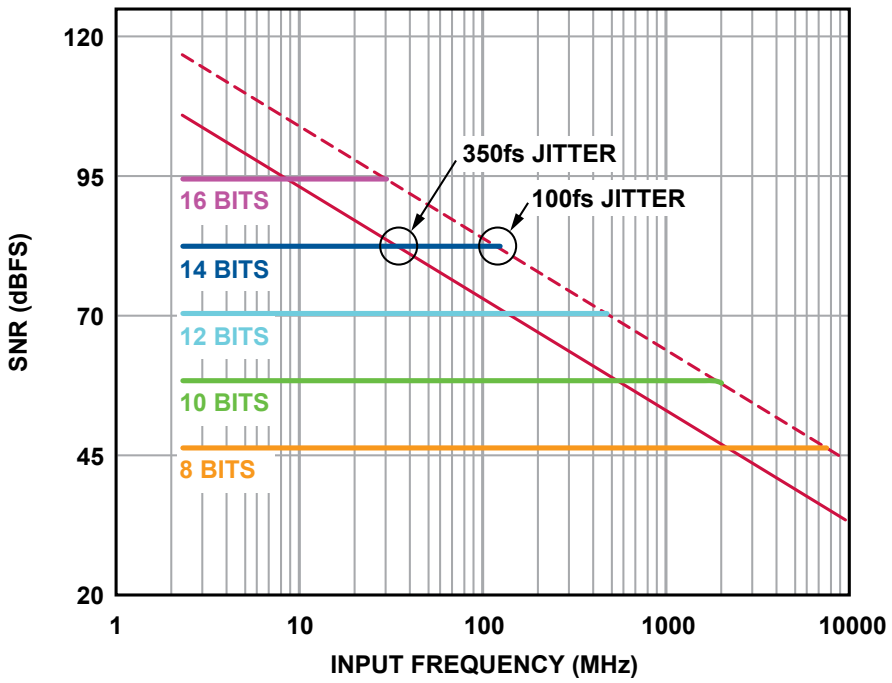


Fig. 2.18: SNR of an ideal ADC vs. analog input frequency and jitter.

Chapter 3

Clock Generation Using Phase Locked Loops

One of the most important sub-circuits in high speed data converters is the clock generation circuit. This is because the timing accuracy of the clock signal directly affects the dynamic performance of the ADC as seen in Section 2.6. To minimize this dependency, the clock signal should exhibit low levels of timing jitter or phase noise. If this factor is not considered while designing the clock circuit, the system will exhibit low dynamic performance irrespective of the quality of the front-end analog circuitry or ADC.

Timing jitter introduces uncertainty in sampling time which directly correlates to uncertainty in sampled values [71]. As a result, the SNR of the sampled waveform is compromised during the data conversion process. The maximum clock jitter that can be tolerated from all sources before the noise due to jitter exceeds the quantization noise (1/2 LSB) is given by Equation 3.1

$$T_{j-rms} = \frac{V_{in(P-P)}}{V_{inFSR}} \times \frac{1}{2^{(N+1)} \times \pi \times f_{in}}, \tag{3.1}$$

where T_{j-rms} is the total rms-jitter, $V_{in(P-P)}$ is the peak-to-peak input voltage, V_{inFSR} is the full-sacle input voltage, N is the resolution, and f_{in} is the input frequency. Hence, if the input voltage (V_{in}) is optimized to equal the full scale range of the ADC (V_{inFSR}), then the jitter requirement becomes a factor of the ADCs resolution (N bits) and the input frequency being sampled (f_{in}). T_{j-rms} represents the total jitter from all the sources. A source of jitter that can be accounted for within the ADC itself is the aperture jitter. This is a timing uncertainty associated with the input sample and hold circuit of the ADC and should be considered when determining the maximum allowable clock jitter of the clock

source. Hence, the clock circuit jitter (T_{clkj}) can be determined by Equation 3.2.

$$T_{clkj} = \sqrt{\left((T_{j-rms})^2 - (T_{j-aperture})^2\right)}, \tag{3.2}$$

where $T_{j-aperture}$ is the ADC aperture jitter.

Most mixed-signal circuits typically use a phase locked loop (PLL) to generate a stable clock for the ADC. Designing the PLL to simply match the requirement specifications may not yield the expected results when used in a data conversion system. This is because the frequency components that exist alongside the fundamental play a significant role. It is therefore important to examine the clock signal with a spectrum analyzer and make sure that the energy associated with the fundamental frequency is not spread over too wide a range. Reference spurs that extend to higher frequencies may be visible and will have a direct impact on the jitter performance characteristics. Spurious Free Dynamic Range (SFDR) is a crucial specification that is used to characterize the dynamic performance of an ADC. For ADC characterization, it is important to measure the harmonic imperfections of the ADC. Thus, it is crucial that the clock provided to the ADC be as spectrally pure as possible.

One of the major sources of power consumption in Hummel's quadrature design [60] described in Section 1.3 was the DDS. The power dissipated by each DDS was about 650 mW at 5V supply and 180 MHz clock. Further, the peak-to-peak (p-p) output jitter of the DDS was measured to be 250 ps, when a 40 MHz, 1V p-p input sine wave clock generation configuration was used. Texas Instruments provides a series of clock generation circuits (CDC421AXXX) [72], that typically consume power in the range of 330 mW to 396 mW and have a total jitter in the range of 29 ps - 42 ps and rms jitter of 0.5 ps for a 100 MHz clock. Analog devices AD9958/AD9959 [73–75], are low jitter clock generators whose rms jitter is about 1.5 ps and power consumption is around 330 mW-660 mW for a 100 MHz clock. As seen in Section 1.2, the CubeSats have a very stringent power budget and the total power allocated for all the payloads ranges between 0.5 W to 4 W. Hence, an alternative low-power clock generation circuit needs to be developed.

3.1 PLL: System Operation and Analysis

A PLL synchronizes the output phase and frequency of a controllable oscillator to match the output phase and frequency of a reference oscillator. Ideally, the steady state condition will show zero difference in phase and frequency between the controlled oscillator and the reference oscillator. The simplest PLL consists of four basic building blocks:

- Voltage-controlled Oscillator (VCO);
- Phase detector (PD) or Phase Frequency Detector (PFD);
- Loop Filter;
- Feedback Divider.

A phase comparison by the phase detector of the outputs of the reference and controlled oscillators generates an error signal. This error signal is then processed by the loop filter to control the controllable oscillator for minimum phase error. An increase in phase error produces a control voltage that changes the controllable oscillator to decrease the phase error and vice versa. Consequently, the loop tracks the changes in the phase and frequency of the reference oscillator. The phase detector provides a phase comparison for each rising edge of the reference oscillator. The output of the phase detector produces a pulsed error voltage that has a pulse width equal to the difference in phase between the two signals. Equation 3.3 shows the mathematical description for the ideal phase detector.

$$V_{pdavg} = K_d \Theta_e, \tag{3.3}$$

where K_d is the phase detector gain (V/rad) and Θ_e is the phase error (rad). The loop-filter then smooths the pulsed error voltage to produce a slowly varying voltage for controlling the VCO. Depending on the control voltage, the VCO changes the frequency in a direction that reduces the phase difference. Equation 3.4 shows a mathematical description of the ideal VCO transfer function:

$$\omega_{out} = \omega_{off} + K_v V_{tune}, \tag{3.4}$$

where $\omega_{out} = \frac{\Delta\theta_{out}}{\Delta t}$, ω_{off} is the offset frequency of the VCO(rad/s) and K_v is the VCO gain (rad/s/V).

The next cycle begins again with a phase detector comparison with the reference rising edge. The cycle repeats for each reference oscillator period until the phase difference is minimized. When a PLL is locked, the output frequency should follow the input frequency. The tune voltage or current input to the VCO should also vary smoothly with changes in the input frequency. One of the most common applications of a PLL is the multiplication of the reference frequency. To accomplish this, a frequency divider is placed in the feedback loop between the VCO output and the phase detector input.

There are numerous PLL architectures. PLL architecture decisions affect the system requirements that will be met. Single PLL, multiple PLL, direct digital synthesis with a PLL, multivibrator VCO, ring oscillator VCO, phase frequency detector and XOR phase detector are some example choices. Several noteworthy introductory books [76–82], articles [83–86], and websites [87–90] have been published on PLL system architecture, understanding PLL requirements, feedback theory, and detailed component design.

3.2 Noise in PLL

Noise plays a major role in the design of high performance PLL based systems. Noise is best described as a signal that is relatively unpredictable over a specific observation time period [76]. In this section, the primary noise sources that arise in time and frequency control systems are described briefly.

3.2.1 Semiconductor Noise Sources

There are five primary types of noise mechanisms that arise in semiconductor characterization and modeling. These primary sources combine to construct noise models for larger macro-devices like the oscillators. The five primary noise sources are discussed in this subsection.

Thermal Noise

Thermal noise is present in all conductors that have a temperature above absolute zero. Thermal noise results from the Brownian motion of electrons due to temperature and limits the achievable noise floor of highly sensitive systems. This random motion of free electrons within the conductor creates an equivalent open circuit voltage across the ends of the conductor. This voltage has a Gaussian distribution and for frequencies below 1THz ($f << 1THZ$), the mean square value of thermal noise ($E\left\{e_n^2\right\}$) can be given by

$$E\left\{e_n^2\right\} = 4k_B T_A R\left(f_2 - f_1\right) = 4k_B T_A R B_n, \tag{3.5}$$

where k_B is the Boltzamann's constant (1.38×10^{-23}) Joules/Kelvin, T_A is the resistors ambient temperature in Kelvin, R is the resistance in Ohms, E is the statistical expectation. Equation 3.5 is known as the Nyquist theorem for thermal noise where B_n is the equivalent noise bandwidth of the circuit under consideration. Since the noise power is a linear function of bandwidth, the power spectral density is uniform, and hence called a white noise spectrum.

Shot Noise

Shot noise consists of random fluctuations of the electric current in many electrical conductors, due to the current being carried by discrete charges (electrons) whose number per unit time fluctuates. This is often an issue in pn-junctions. Shot noise and thermal noise are differentiated by the physics that exists in the pn-junctions of diodes and bipolar transistors where the passage of each carrier across each junctions depletion region is an independent random number characterized by a Poisson distribution. The barrier potential across each pn-junction restricts the flow of current in a single direction which is required for shot noise to be present. According to Schottky's theorem, the power spectral density (PSD) of the shot noise is uniform (white) having a density of

$$S_{shot}\left(f\right) = 2q\left\langle I\right\rangle, \tag{3.6}$$

with units of ampere-squared per hertz, where q is the charge of an electron (1.6×10^{-19}), and $\langle I \rangle$ is the direct current flowing through the junction. The spectral level falls of for frequencies greater than roughly τ_o^{-1} where τ_o corresponds to the mean transit-time for the carriers to traverse the depletion region of the junction.

Flicker $(1/f)$ **Noise**

The term $1/f$ noise applies to the noise shape of the power spectral density with respect to frequency for the observed noise rather than to an underlying physical mechanism or process. Flicker noise is present in all active devices and some passive devices. In bipolar transistors, it is primarily caused by carrier traps associated with crystalline defects or contamination of the emitter-base depletion region. In MOSFET devices, there is no universally accepted model for $1/f$ noise, but two primary schools of thought have emerged. In Mc Whorter model [76], the $1/f$ noise is attributed to the random trapping and de-trapping of charge carriers with different relaxation times near the silicon-insulator interface within the device. The Hooge model [76] attributes the $1/f$ noise on charge scattering that occurs within the device due to lattice vibrations.

Flicker noise is always associated with direct current flow and its PSD is given by

$$S_{1/f}(f) = K \frac{\langle I \rangle^a}{f^b} A^2/Hz, \tag{3.7}$$

where K is a device-dependent constant, $\langle I \rangle$ is the direct current in amperes, f is the frequency of interest in Hertz, a is a device dependent constant whose value is normally within the range of 0.5 to 2, and b is a device dependent constant ($\approxeq 1$).

The amplitude distribution of Flicker noise is frequently non-Gaussian. $1/f$ noise is difficult to accurately simulate, and hence a number of numerical methods have been developed for creating $1/f$ noise.

Generation-Recombination Noise

Generation-Recombination noise occurs whenever free charge carriers are generated and

recombine in a semiconductor material. The effects at room temperature is very small. This noise does not appear if there is no direct current flow but is not produced by the current. Its a low-frequncy noise phenomenon having a gaussian distribution and its Lorentzian PSD is given by

$$S_{gr}(f) = K_2 \frac{\langle I \rangle^2 \tau}{1 + (2\pi f \tau)^2} A^2/Hz, \tag{3.8}$$

where K_2 is a device-dependent constant, $\langle I \rangle$ is the direct current in amperes, f is the frequency of interest in Hertz, and τ is the device-dependent time constant.

Burst (Popcorn) Noise

Burst or Popcorn noise is a special kind of generation-recombination effect that is related to the presence of heavy-metal ion contamination within a semiconductor. The spectral density of burst noise has the form given by

$$S_{pop}(f) = K_3 \frac{\langle I \rangle^c}{1 + \left(\frac{f}{f_{bc}}\right)^2} A^2/Hz, \tag{3.9}$$

where k_3 is a device-dependent constant, $\langle I \rangle$ is the direct current in amperes, f is the frequency of interest in Hertz, c is a device dependent constant whose value is normally within the range of 0.5 to 2, and f_{bc} is the frequncy corner for a particular noise process. It is possible to have more than one burst noise process to be present within a device, with each process having its own characteristic parameters. The amplitude distribution of Burst noise is generally non-Gaussian.

3.2.2 Other Sources of Noise

Other sources of noise also exist such as hot-electron noise, avalanche noise produced in Zener diodes, and quantum 1/f noise. These noise sources will not be addressed here. Many other potential noise problems may also be introduced during system design due to the complexity of modern systems. Extensive digital signal processing, switching, dc-dc power supplies, and switched capacitor techniques are a few of the many noise sources that

may need to be considered.

3.3 Phase Noise

Phase noise is characterized by a small phase (and hence frequency) perturbation or jitter on the signal. It manifests itself as noise spreading out on either side of the main carrier. Synthesizers, especially those based around phase locked loops, can have significant amounts of phase noise if they are not carefully designed. Each component of the PLL contributes to the overall noise that appears at the output, but the actual way in which the noise is contributed by any element depends upon where it is produced. For example, noise generated by the VCO will affect the output in a different way to the noise generated in the phase detector. To illustrate this, lets look at the noise generated by the VCO. This noise will pass through the divider chain and appear at the input of the phase detector. It will then pass through the loop filter which will allow only the components of noise below the loop cut-off frequency to pass through. This noise will then appear on the error control voltage and have the effect of canceling out the noise on the VCO. As this effect takes place only within the loop bandwidth, it will reduce the level of noise within the loop bandwidth, but will have no impact on noise outside the loop bandwidth.

Noise generated by the phase detector is altered in a different way. Again, only the components of noise below the loop bandwidth passes through the low pass filter. This means there will be no noise outside the loop bandwidth appearing on the tune voltage at the control terminal of the VCO. The noise components within the loop bandwidth will appear at the input of the VCO and appear as a phase noise at the output of the VCO.

Noise generated by the reference undergoes the same treatment as noise generated by the phase detector. Further, the division ratio(N) of the divider has the effect of multiplying the noise level. This is due to the fact that the PLL effectively multiplies the reference frequency. Consequently, the noise level is also multiplied by a factor of N. Hence, a reference oscillator having a good phase noise performance can be degraded significantly if the division ratio is high.

Dividers normally do not produce significant noise contribution. Any noise produced

by the divider can be grouped with the noise produced by the phase detector. The combined noise profile of the loop is shown in Figure 3.1. Hence, the noise within the loop bandwidth primarily arises from the reference and the phase detector while the noise outside the loop bandwidth is due to the VCO. Consequently, the noise profile is heavily dependent on the choice of loop bandwidth. A number of measures used to characterize the phase noise performance of frequency sources have been published in Crawford [76]. In oscillators, phase noise performance is frequently summarized by specifying the total integrated phase noise in rms-rad which is related to the Lorentzian PSD. In the discussion that follows, a relationship between the total integrated phase noise and the Lorentzian PSD is defined.

One of the most prevalent phase noise measures used is $\mathcal{L}(f)$. $\mathcal{L}(f)$ is the normalized frequency-domain representation of phase fluctuations. It is the ratio of the power spectral density in one phase modulation sideband, referred to the carrier frequency on a spectral density basis, to the total signal power, at a frequency offset f. The units for this quantity are Hz^{-1}. The frequency range for f ranges from $-v_o$ to ∞ where v_o denotes the nominal carrier frequency. $\mathcal{L}(f)$ is therefore a two-sided spectral density and is also called single-sideband phase noise.

Another quantity of importance is the one-sided power spectral density of the phase fluctuations, $S_\theta(f)$. The two-sided version is represented by $P_\theta(f)$. $S_\theta(f)$ is measured by passing the signal through the phase detector and measuring the PSD at the detector output. Normally the approximation

$$\mathcal{L}(f) = \frac{1}{2} S_\theta(f)\, rad^2/Hz \tag{3.10}$$

is made, but is only valid as long as $\int_{f_1}^{\infty} S_\theta(f)\, df \lll 1 rad^2$ is satisfied for an appropriate lower frequency bound f_1. In many communication systems, the total amount of phase noise present is more important than the close in-phase noise spectrum details. The total phase noise is called the total integrated phase noise and is usually specified as a root-mean-square

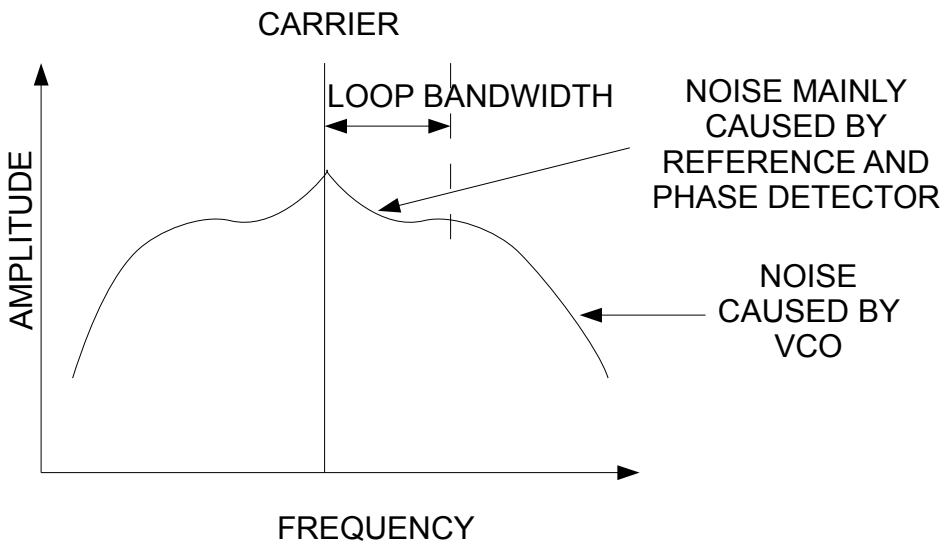


Fig. 3.1: Noise profile of a typical synthesizer.

quantity defined as

$$\sigma_\theta = \sqrt{\int_{f_1}^{f_2} S_\theta\left((f)\, df rms - rad.\right.} \tag{3.11}$$

A reasonable first-order approximation for any PLL source is the Lorentzian PSD given by Equation 3.12. This is a two-sided spectrum centered around the carrier frequency f_c. The total integrated phase noise from Equation 3.12 is then given by Equation 3.13.

$$\mathcal{L}\left(f\right) = \frac{L_o}{1 + \left(\frac{f}{f_c}\right)^2} \tag{3.12}$$

$$\sigma_\theta = \sqrt{\left(\int_{-\infty}^{\infty} \frac{L_o}{1 + \left(\frac{f}{f_c}\right)^2} df\right)} = \sqrt{\pi L_o f_c} rms - rad \tag{3.13}$$

3.4 PLL Performance: Jitter and Reference Spurs

Jitter is extremely important in systems using PLL based clock drivers. The effect of

jitter ranges from not having an affect on the system operation to completely rendering the system non-functional. In this section, the reader is introduced to various kinds of jitter in PLL-based frequency synthesizers, their causes and their effects, the relationship between phase noise and jitter, and various reported methods of reducing jitter. We will also look at the causes and effects of reference spurs and briefly enumerate the reported methods for reducing reference spurs.

3.4.1 Clock Jitter

Clock jitter can be defined as the deviations in a clock's output transitions from their ideal positions. The deviations can either be leading or lagging to the ideal position. Jitter measurements can be classified into three categories: cycle-cycle jitter, period jitter, and long-term jitter.

Cycle-Cycle Jitter

Cycle-cycle jitter is the change in a clock's output transition from its corresponding position in the previous cycle. Figure 3.2 shows a graphical representation of cycle-cycle jitter. J_1 and J_2 are the jitter values measured. The maximum of such values measured over multiple cycles is the maximum cycle-cycle jitter.

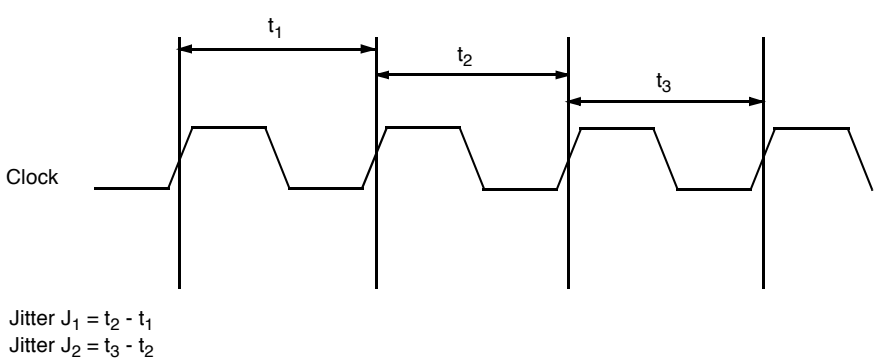


Fig. 3.2: Cycle-cycle jitter.

Period Jitter

Period jitter measures the maximum change in the clock's output transition from its ideal position. Figure 3.3 shows period jitter.

Long-Term Jitter

Long-term jitter measures the maximum change in the clock's output transition from its ideal position, over many cycles. The number of cycles depends on the application and the frequency. Figure 3.4 shows a graphical representation of long-term jitter.

3.4.2 Causes of Jitter

There are four primary causes of jitter as listed below.

- Power supply noise on a PLLs supply input, which appears as jitter on the output. Power supply noise manifests itself through Ground Bounce and V_{dd} Noise. When there is a surge of current through the output drivers, the inductance of the leads of the supply have a voltage drop across them. This causes the ground potential to either raise or lower. Hence, in an oscillator where the output frequency is dependent on the effective supply voltage, the frequency changes due to the ground bounce. Further, the threshold voltage of the transistors within the oscillator changes causing a change in the frequency. This change appears on the output as jitter.

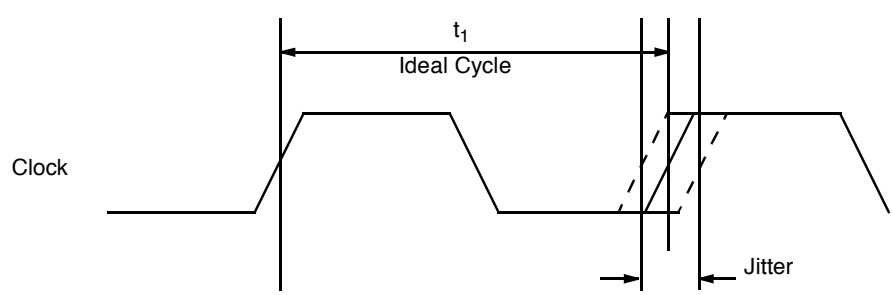


Fig. 3.3: Period jitter.

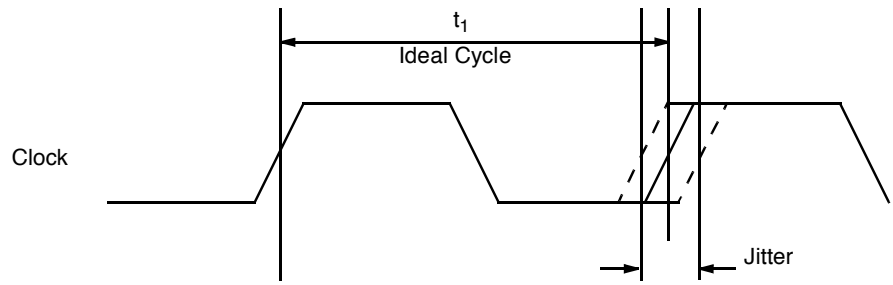


Fig. 3.4: Long-term jitter.

- The PLL has a dead-band associated with it, during which the phase-frequency detector does not detect small changes in the input phase. Since these changes are not corrected, they appear on the output in the form of jitter.
- Random thermal noise from the crystal reference as well as random mechanical noise from the vibrations of the crystal reference.
- Inherent noise present in the active and passive devices as described in Section 3.2.

3.4.3 Jitter-Phase Noise Relationship

The output of the oscillator can be represented by a sine wave given by Equation 3.14.

$$V(t) = [A_o + \varepsilon(t)] \sin[2\pi f_o t + \Delta\phi(t)], \tag{3.14}$$

where A_o is the nominal peak voltage, $\varepsilon(t)$ is the deviation of the amplitude from its nominal value, f_o is the fundamental frequency, and $\delta\phi(t)$ is the deviation of the phase from its nominal value. $\varepsilon(t)$ is negligible and Equation 3.14 can be simplified to

$$V(t) = A_o \sin\left[\frac{2\pi}{T_o}\left(t + \frac{\Delta\phi(t)}{2\pi f_o}\right)\right], \tag{3.15}$$

where $T_o = \frac{1}{f_0}$. The $\sin(x)$ function equals zero for $x = 2\pi$. Therefore, from Equation 3.15 we get,

$$t = T_o + \Delta T = T_o\left(1 - \frac{\Delta\phi(t)}{2\pi}\right). \tag{3.16}$$

Consequently, jitter (J) can be expressed as

$$J = \frac{\Delta T}{T_o} = \frac{\Delta\phi\,(t)}{2\pi}. \tag{3.17}$$

3.4.4 Methods for Reducing Jitter

Several different techniques have been reported for the design and implementation of low jitter clock circuits. Methods reported include modifying the filter design to narrow the PLL bandwidth [91–94] and to make the phase noise at the VCO as low as possible [95, 96], reducing power supply noise [97–99], eliminating ground bounce [100], using a voltage controlled crystal oscillator (VCXO) [101–103], employing a dual-phase frequency detector [104], and adopting a ferroelectric capacitor as a VCO timing element [105].

Techniques for modifying the filter design include :

- Using a fourth order filter to improve the attenuation obtained at wide frequency offsets, without compromising the in-band performance of the loop [91].
- Designing an active loop filter with adaptive biasing technique [92]. Using the new loop filter, the PLL can automatically adjust the loop bandwidth and damping factor to the frequency of the reference clock.
- Using nonlinear filters [93].
- Using delta operator-based lowpass filters [94].

Comer [95] proposes the addition of a bandpass filter following the VCO in a conventional PLL as a means of reducing jitter. He provides an analysis to verify and quantify this approach and concludes that jitter may be reduced by a factor $\frac{\pi}{2Q}$, where Q is related to the selectivity of the bandpass filter employed. Comer [96] clarifies that the analysis is valid only when the dominant noise source is the "injection noise," or more simply, the crosstalk from other digital signals on the chip.

Power supply noise can be mainly reduced by bypassing and filtering the power supply appropriately. Further, using a regulated power supply with the bypassing and filtering

technique ensures better power supply rejection [97–99]. A PLL that is highly robust to supply/substrate noise is described by Park et al. [106]. To achieve this, a new type of VCO based on pseudo-differential delay elements is presented.

Ground bounce can be reduced by an effective combination of two methodologies based on shaping the supply current:

- Introducing intentional skews to the synchronous clock network, and
- Frequency modulation of the system clock.

The former technique reduces the time-domain peaks as well as the spectral power of the supply current by spreading the simultaneous switching activities. The latter technique reduces the power contained in the clock harmonics by spreading this power into the side lobes formed around the clock harmonics without any change in the spectral power of the supply current [100].

Pauls and Kalkur [105] used a ferroelectric capacitor as the VCO timing element. Polarization reversal within ferroelectric capacitors creates a high nonlinear dielectric constant along with a hysteresis profile. Due to these attributes, a PLL, when based on a ferroelectric capacitor, has the advantage of reduced cycle-to-cycle jitter.

3.4.5 Reference Spurs

Discrete spurious contamination that occur during frequency synthesis result from periodic modulation of the carrier. If multiple-tone modulation is present, the individual modulation frequencies as well as cross modulation terms will be seen if the modulation indices are sufficiently high. In this case, the phase modulated signal can be represented by

$$s(t) = Real\{\exp[j\omega_o t + j\sum_{k=1}^{p} \Delta\Theta_k sin(\omega_k t)]\}, \tag{3.18}$$

where ω_o is the radian carrier frequency, and the phase modulation amplitude indices, and modulation frequencies are given by $\Delta\Theta_k$ and ω_k, respectively.

In PLL-based systems that incorporate digital logic elements such as phase-frequency detectors and dividers, introduce frequency-domain aliasing. This aliasing can cause frequency terms that were originally not a concern. If only one modulation tone is present in Equation 3.18, the discrete sideband spurious levels that will be observed relative to the carrier level can be closely approximated by

$$L_{spur} = 20\log\left(\frac{\Delta\Theta}{2}\right) \approx 20\log\left(\frac{\Delta f}{f_m}\right) dBc, \tag{3.19}$$

where $\Delta\Theta$ is the peak-phase (sinusoidal) deviation and equivalently Δf and f_m represent the peak frequency (sinusoidal) deviation and frequency modulation rate, respectively. If the modulation is not sinusoidal, but is either square wave, sawtooth, or exponential in form, then the resulting spurious levels can be estimated by first expressing the modulation signal as a Fourier series and then applying Equation 3.19 for each individual Fourier component.

3.4.6 Causes of Reference Spurs

Reference spurs occur due to the presence of a small AC component on the VCO tuning voltage. Since the output frequency of the VCO is directly proportional to the tuning voltage, the output can be viewed as an FM modulated signal. This produces a series of harmonics. This AC component on the VCO tuning line may arise due to current leakage in the charge pump or due to mismatched currents in the charge pump.

- **Effect of charge pump leakage on reference spurs**: When the PLL is in the locked state, the charge pump is off for majority of the time. In the off state, any current that leaks from the charge pump causes spurs. This leakage causes the VCO tuning voltage to drop and can cause an undesired AC signal on the tuning line.

- **Effect of current mismatch on reference spurs**: In the locked state, there are also fast alternating current pulses. The width of these pulses are larger for lower charge ump currents and higher charge pump mismatches. The width of this correction pulse is directly related to causing an undesired AC signal on the VCO tuning line.

3.4.7 Methods for Reducing Reference Spurs

For low reference spur, lowering the gain of the VCO [107] and increasing the frequency of the control line ripple in the VCO help the PLL suppress the reference spurs at the cost of increased settling time. Other methods to suppress the reference spurs involve shifting the reference spur to a higher frequency using a double sampling phase detector [108] or using an adaptive PLL with two tuning loops: a main loop for locking the PLL frequency synthesizer that operates all the time and an auxiliary loop for reducing the reference spur, that operates only when the PLL is closely locked [109].

A spur-reduction technique was presented by Kuo et al. [107], to achieve low reference spurs for a 5-GHz frequency synthesizer. A dual-path control scheme incorporated with a pair of varactors reduces the gain of voltage-controlled oscillator to less than 15 MHz/V, and attenuates the spurious tones. In addition, a digital frequency-calibration circuit is used to enlarge the tuning range to overcome process variations.

Low reference spurs are accomplished for a fully integrated 5-GHz frequency synthesizer by Sun and Siek [110]. The proposed synthesizer architecture adapts the loop parameters according to different operating modes, so as to reduce the loop bandwidth in the locked state and to further attenuate the reference spurs. In addition, a high-performance charge pump circuit is incorporated with the adaptive synthesizer to reduce non-ideal effects that cause spurs.

Tai-Cheng Lee and Wei-Liang Lee [111] propose using distributed phase-frequency detectors and charge pumps to move spurious tones to higher frequencies and reduce the spur levels. Huh et al. [112] reduce the reference spurs by reducing the charge pump (CP) mismatch. A digital controller calibrates the replica CP to improve the current matching. Although, the main CP and the replica CP are matched to reduce the ripple, it is hard to compensate for the current mismatch due to channel-length modulation.

Chapter 4

Proposed PLL Design Using Muller C-Gates

The VCO has the largest effect on the overall noise performance of the PLL. Noise in oscillators arises from the inherent noise in active and passive devices as well as noise coupled into the oscillator through the substrate or power supply. Currently, most efforts to minimize timing jitter in VCO focus on reducing power supply noise and ripple as seen in Section 3.4. In this chapter, an alternative method using C-elements is proposed to reduce the timing jitter and reference spurs, and can be used concurrently with these standard methods. A brief introduction to Muller C-Gates is given in Section 4.1. Section 4.2 explains our proposed approach and how it reduces the timing jitter and reference spurs of the PLL. Section 4.3 covers the design and implementation details of key components. Results are presented in Section 4.4. A Figure of Merit (FOM) for PLL designs is defined in Section 4.5 and various existing designs are compared with our method.

4.1 Muller C-Gates or C-Element

The Muller C-gate or C-element originally developed by David E. Muller, is a widely used asynchronous logic gate. The C-element's output reflects the inputs when the states of all the inputs match. The output then remains in this state until all the inputs transition to the other state [113]. Figure 4.1 shows the gate-level and transistor-level implementations and the symbol for the C-element.

To understand the functionality of the C-element, consider the transistor level implementation in Figure 4.2. The C-element consists of two cross-coupled inverters that act as a latch and stores its previous states. Consider the C-element when both the inputs are 0. In this case, the pull-up network comes into play and changes the state of the latch. The C-element would then output a 0. If both inputs are 1, the pull down network changes the

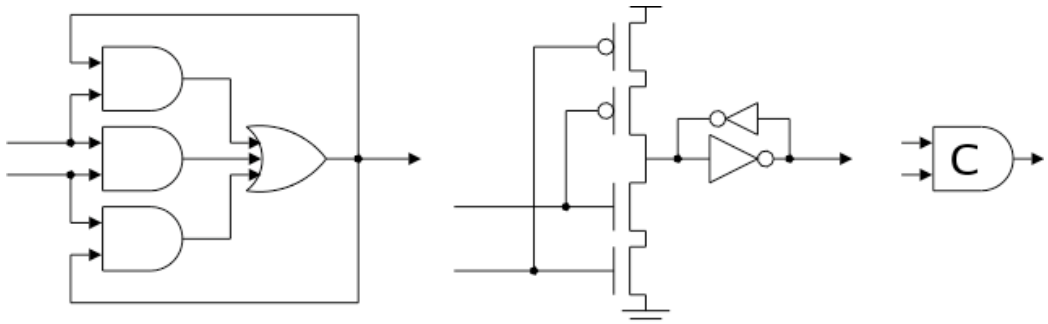


Fig. 4.1: Muller C-Gate.

state of the latch and the C-element outputs a 1. Otherwise, the input of the latch is not connected to either Vdd or ground and the latch outputs its previous state. The truth table for a two input C-gate is listed in Table 4.1, where A and B are the inputs, Y the output and Y_{n-1} denotes the previous output state.

4.2 Jitter and Spur Reduction Scheme

Noise performance of a PLL is the combination of low-pass filtered input reference clock jitter and high-pass filtered VCO jitter [105]. Winstead and Hamoui [114] proved that a Muller-C gate can be used to significantly reduce the jitter of clock signals, as long as multiple clock sources were available with independent phase noise.

Now, consider two independent clock sources generated by two PLLs. The jitter can be significantly reduced by passing these clocks through a C-element. In order to reduce the reference spurs, the ripple voltages on the control lines for the two VCOs are designed to be by π radians out of phase with one another. This causes the VCO output signals to destructively interfere when passed through the C element and consequently reduces the amplitude of the reference spurs.

Table 4.1: Truth table for a 2-input C-Element.

A	B	Y
0	0	0
0	1	Y_{n-1}
1	0	Y_{n-1}
1	1	1

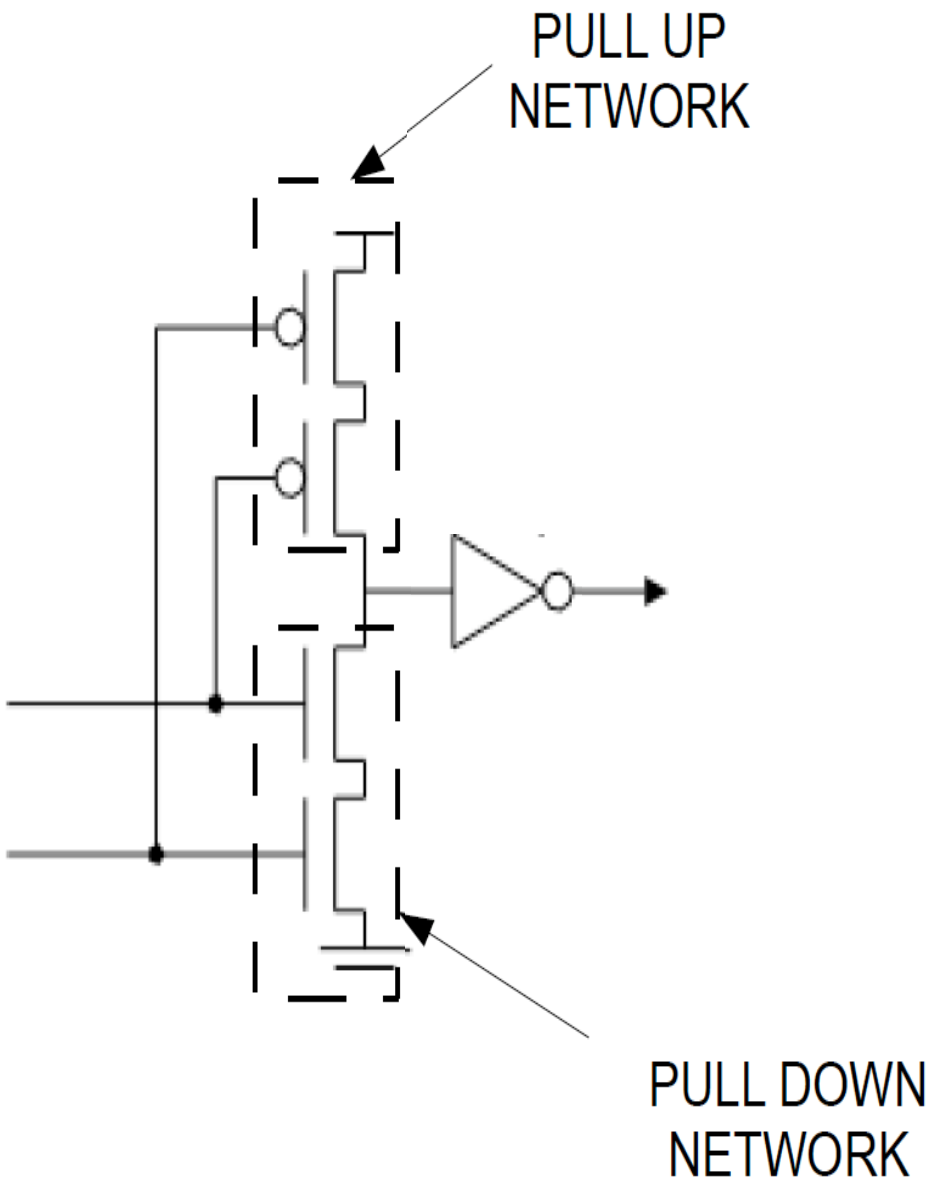


Fig. 4.2: Muller C-Gate: Transistor level implementation.

Conventionally, the phase detector is implemented using a charge-pump and a digital phase frequency detector. The non-ideal effects, mismatch and leakage in the charge pump and timing error of the phase frequency detector create periodic ripples on the control line of the VCO as explained in Section 3.4. These periodic ripples modulate the VCO to generate the reference spur around the carrier. The amplitude ratio between the reference spur and the carrier can be calculated using a narrow band frequency modulation approximation [115]. This ratio is given by

$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2}\frac{K_{VCO} \times A_m}{2\pi f_{ref}}, \tag{4.1}$$

where $K_{VCO}Hz/V$ is the VCO gain, A_m is the amplitude of the control line ripple and f_{ref} is the reference frequency.

Now consider the two VCOs: VCO1 and VCO2, in Figure 4.3 that are identical except for a π radian phase mismatched ripple. When the outputs of the VCO are passed through the C-element, the C-element finds the maximum of the two VCO outputs at every point in time. Consequently, as seen from Figure 4.3, the average peak-to-peak amplitude of the output ripple from the C element is halved. From Equation 4.1, we see that the magnitude of the spur is directly proportional to the magnitude of the control line ripple. Hence, by reducing the magnitude of the ripple, the magnitude of the reference spurs are reduced.

4.3 Design, Modeling, and Implementation

A conventional Phase Frequency Detector (PFD) PLL architecture is used. The PLL is composed of five fundamental blocks as depicted in Figure 4.4.

Operational blocks of the PLL consist of PFD, charge pump, analog filter, VCO, and feedback frequency divider. The operation of the PLL can be understood by examining the loop depicted in Figure 4.4. The PFD generates pulses (UP and DOWN) corresponding to the phase/frequency difference between the reference signal (REF_CLK) and the feedback signal from the divider (FBK_CLK). The charge pump provides positive and negative current pulses based on the pulses from the PFD. The PLL without a loop filter is inherently

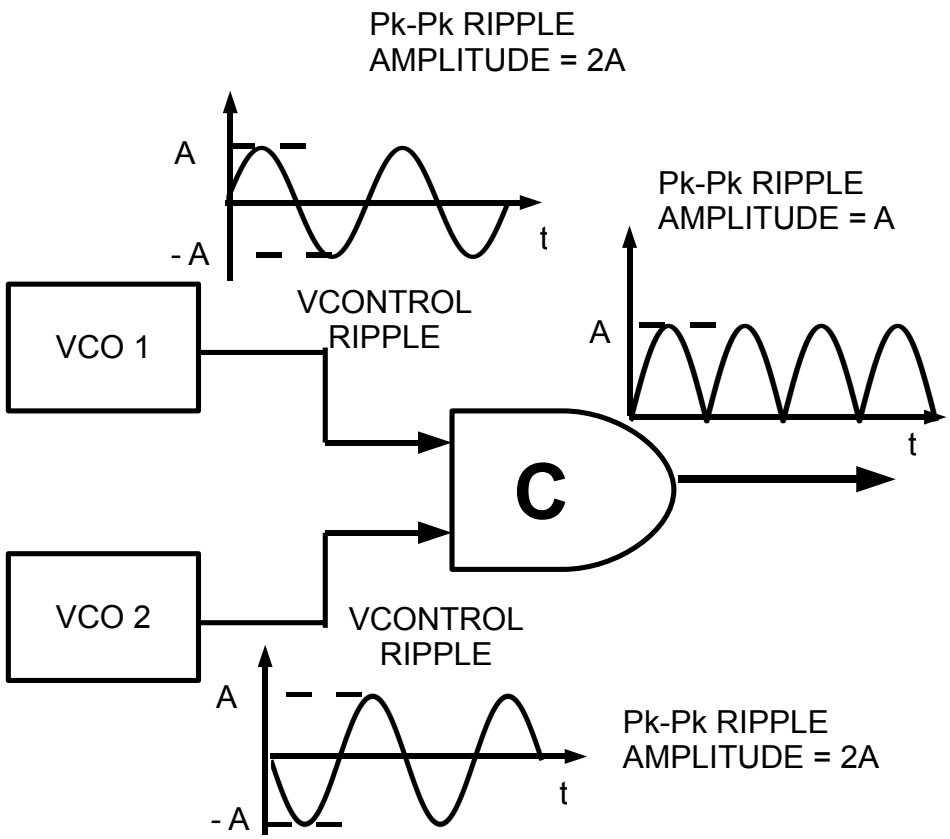


Fig. 4.3: Reduction in peak-to-peak amplitude of the ripple voltage from the C element.

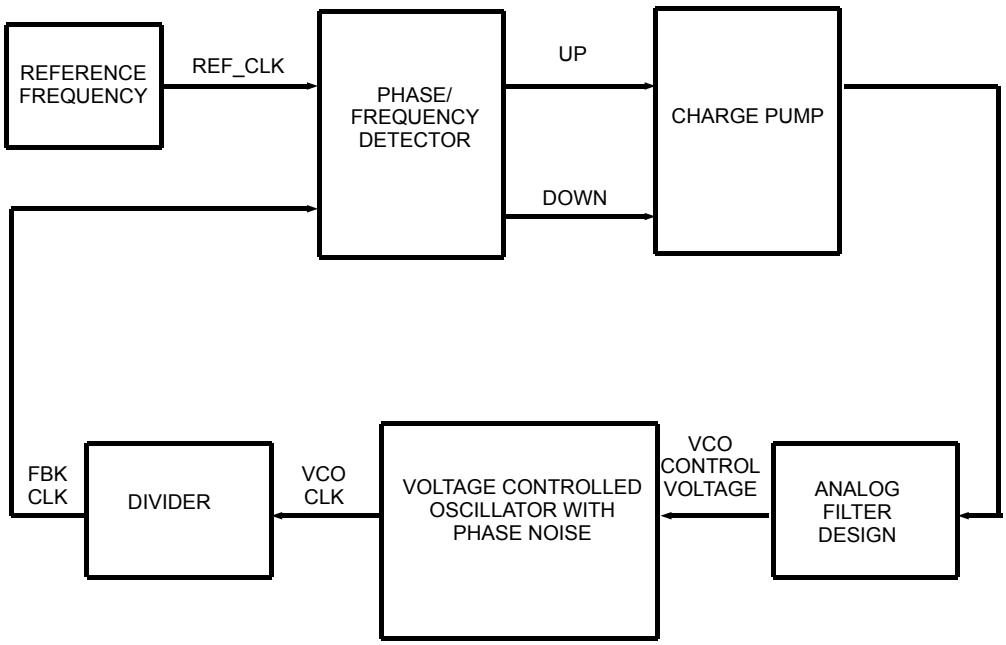


Fig. 4.4: Block diagram of the PLL.

stable, but an analog loop filter is required to convert the current pulses from the charge pump into a smooth output voltage for the VCO. The VCO generates an output voltage that oscillates at a frequency determined by the control voltage and the divider divides down the VCO output frequency by N, to bring it down to the reference frequency. When the loop is designed correctly, the PLL adjusts the VCO control voltage until the reference clock (REF_CLK) and the feedback divider clock (FBK_CLK) are equal in phase and frequency. Once this alignment is achieved the loop is said to be locked. Since

$$REF\_CLK = FBK\_CLK,$$

we have

$$REF\_CLK = \frac{VCO\_CLK}{N}.$$

Hence, the VCO clock is N times larger than the reference clock. By changing N, the PLL generates different VCO frequencies from a single input clock frequency.

The PLL is implemented using Matlab's m-files and Simulink models which are controlled by a Graphical User Interface (GUI) to ease the usage of the program. The Simulink model of the PLL is based on the models and examples developed by Benson [116]. I have used these models as a reference to create a model that fit our needs.

The phase frequency detector is implemented by two digital flipflops and a NAND gate as seen in Figure 4.5.

The charge pump and loop filter are implemented using blocks from the SimPower-System blockset. This extension to Simulink makes it possible to draw electrical circuits directly in Simulink as seen in Figure 4.6.

The PLL model multiplies the reference frequency of 1 MHz by a factor of 50 using the PLL. It uses a spectrum analyzers to monitor the VCO control voltage and VCO output signal. A down converter is used before the analyzer monitoring the VCO output to improve the frequency resolution of the analysis The VCO has a band limited phase noise generator with a 1/f spectral shape, set by an FIR filter. Generation of the 1/f noise can be done using recursive digital filtering in which the filtering is applied to a white Gaussian noise [76]. The total integrated phase noise can also be specified in the model. Non-idealities are added to the charge pump and timing mismatches between the UP and DOWN signals from the PFD are also taken into account using the "Variable transport delay" unit in Simulink

The model described above is modified (Figure 4.7) to verify our jitter and reference spur reduction scheme explained in Section 4.2. The independent clocks are generated by two PLLs (PLL1 and PLL2). Gain and phase mismatches as well as independent random noise sources are added to the two VCOs. The reference signal is inverted before feeding it to PLL2. This provides us with a ripple voltage on the control signal of VCO2 that is π radians out of phase with the the ripple voltage on the control signal of VCO1. The output clock signal from VCO1 and the inverted clock signal from VCO2 are then passed through the Muller C element. The output of the Muller C element is monitored using a spectrum analyzer and the jitter is measured on the rising edge.

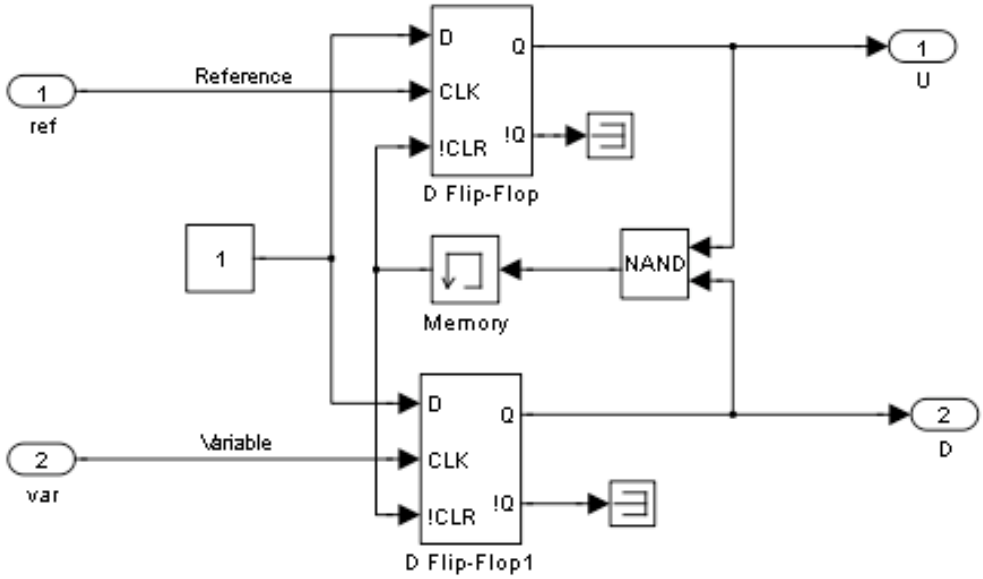


Fig. 4.5: Simulink implementation of the phase frequency detector.

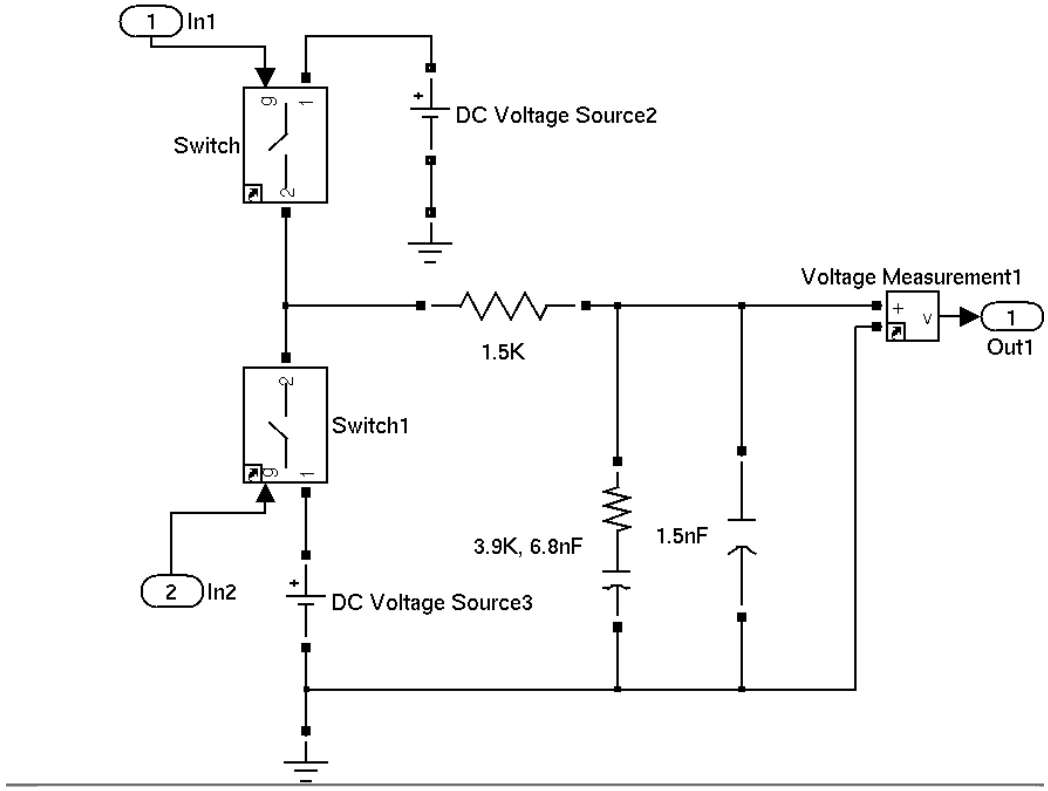


Fig. 4.6: Charge pump modeling using the SimPower blockset.

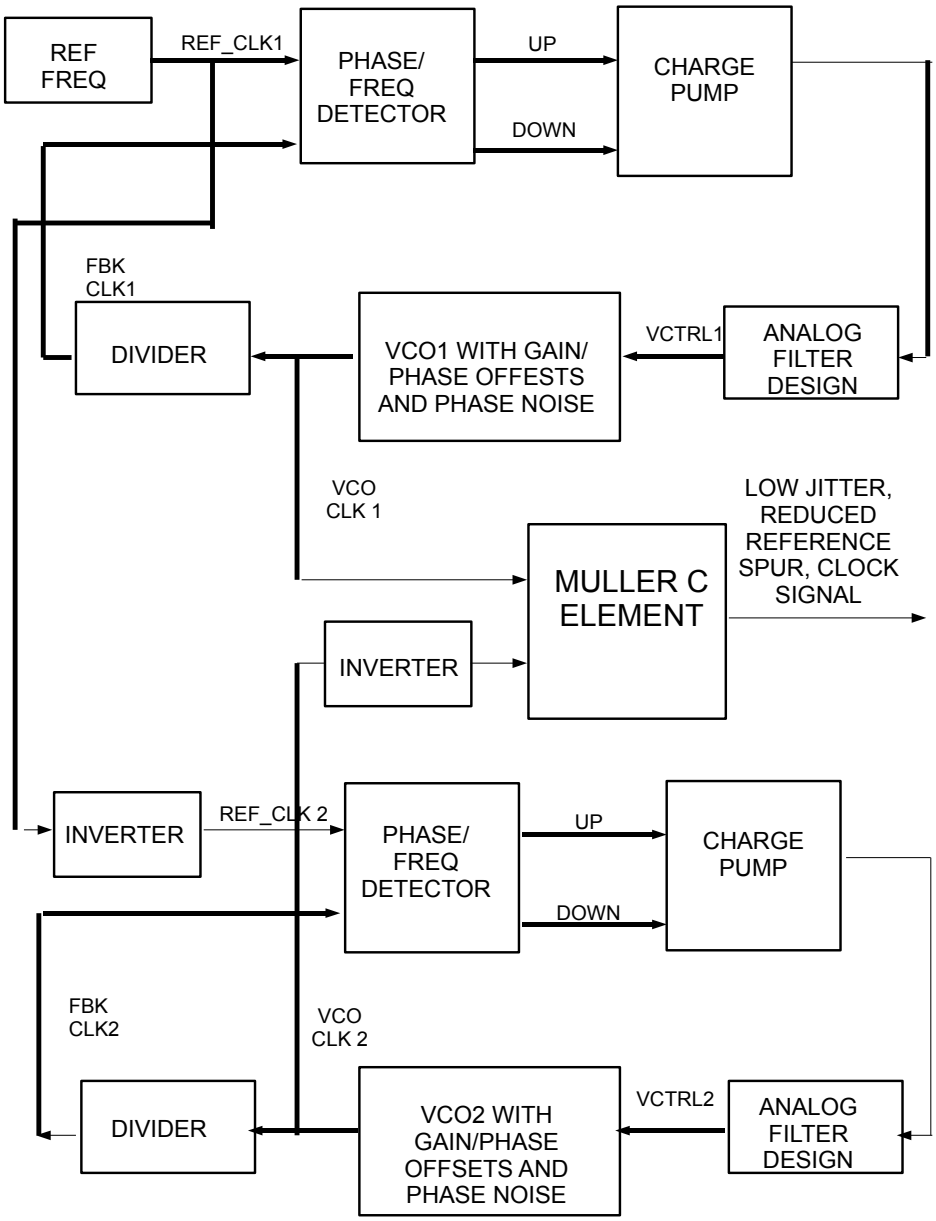


Fig. 4.7: Proposed jitter and reference spur reduction scheme.

4.4 Results

The output spectrum from the PLL in the absence of phase noise and when the integrated phase noise is set to 0.5 rms rad is shown in Figure 4.8. The addition of the phase noise corrupts the spectral purity of the VCO output and causes the reference sidebands (+/- 1MHz around the VCO frequency) to increase. The addition of phase noise also causes the jitter to increase. This is the typical behavior of charge pump based phase-frequency detector schemes. The PLL model as well as the modified PLL model with the C-element were simulated with 0.5 rms-rad integrated phase noise. Figure 4.9 shows the PSD of the VCO output for the traditional and proposed method. We see that the reference spurs are drastically reduced in the proposed PLL design. Figure 4.10 shows that the peak-to-peak jitter from the C element is reduced by about 70-75% of the jitter obtained from the traditional PLL, depending on the amount of phase noise added. The clock generated from the traditional PLL and from the Muller-C PLL were integrated into the system level PIP Matlab/Simulink model. As seen in Section 2.5, the non-idealities in the DAC have the highest influence on the fundamental output, which increases as its standard deviation increases. The gain amplifier stages have less of an impact on the fundamental component, but increases in the same manner as that of the DAC. The comparator offsets had no effect on the fundamental output. The offsets in the DAC can be reduced by using proper layout techniques [68]. Consequently, the simulations were performed by adding non-idealities to the gain amplifier stage.

In Figure 4.11, we can see that the jittered clock generated by the C-element closely follows the impedance curve generated by the ideal clock. Figure 4.12 depicts the error in the impedance measurement between the ideal clock and the jittered clock generated by the traditional PLL as well as the Muller C PLL.

One of the main objectives of the proposed PIP design is to provide accurate impedance measurements while still optimizing the area and power consumption. From Figure 4.11, we observed that the impedance curve generated the proposed PLL with phase noise (0.5 rms rad) closely follows the impedance curve generated by an ideal clock with no phase

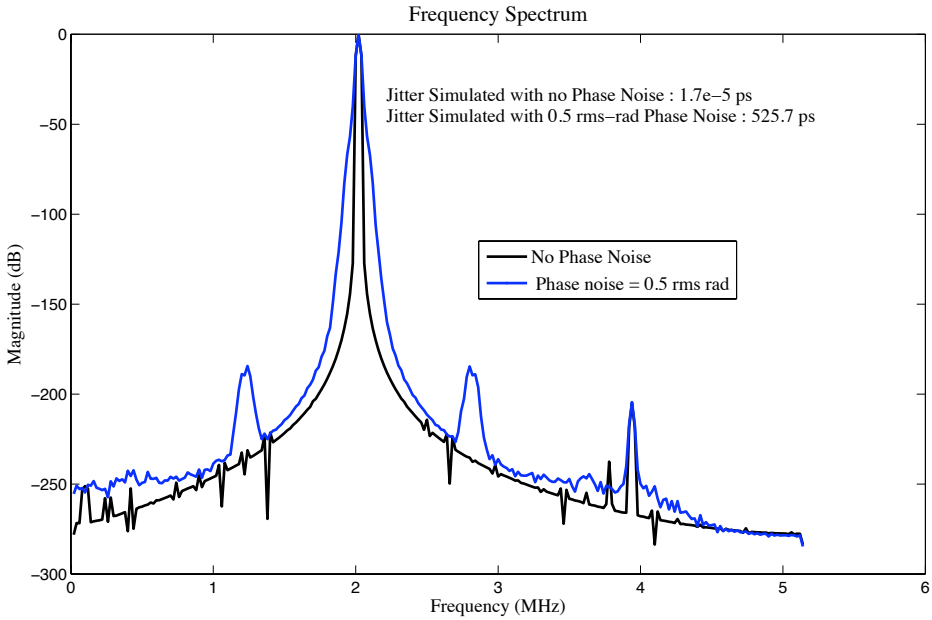


Fig. 4.8: PSD of the PLL in the presence and absence of phase noise.

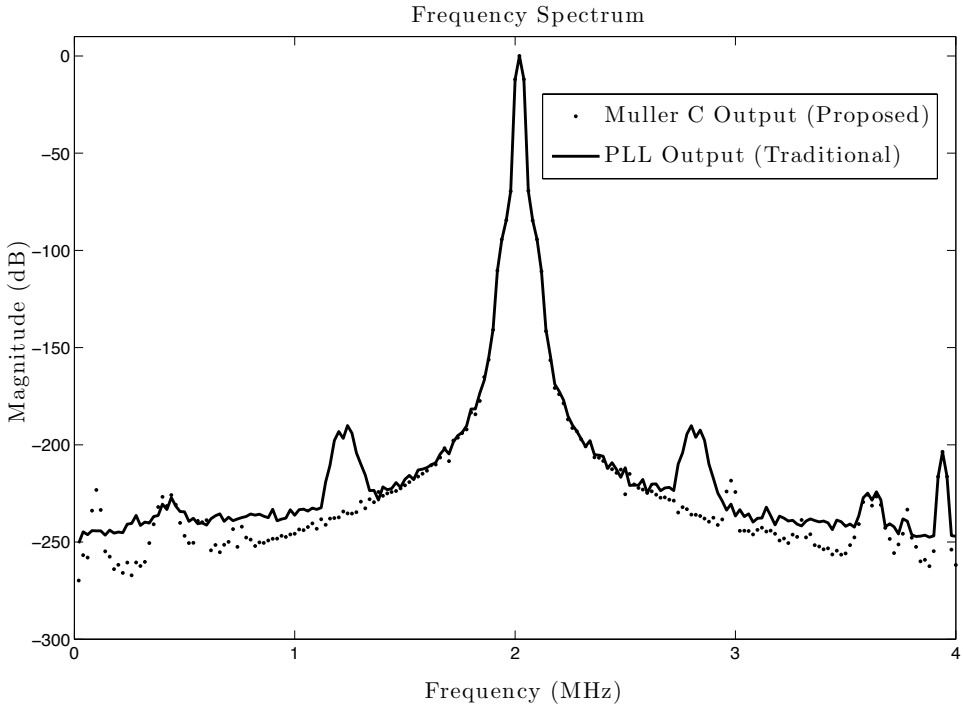


Fig. 4.9: PSD of the VCO output for the traditional and proposed method.

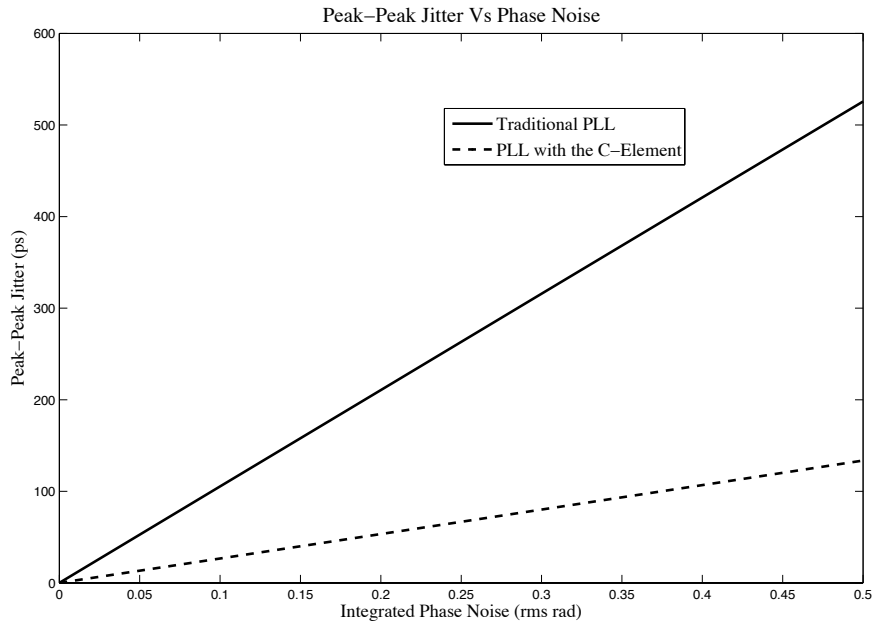


Fig. 4.10: Comparison of peak-to-peak jitter vs integrated phase noise for the traditional and proposed method.

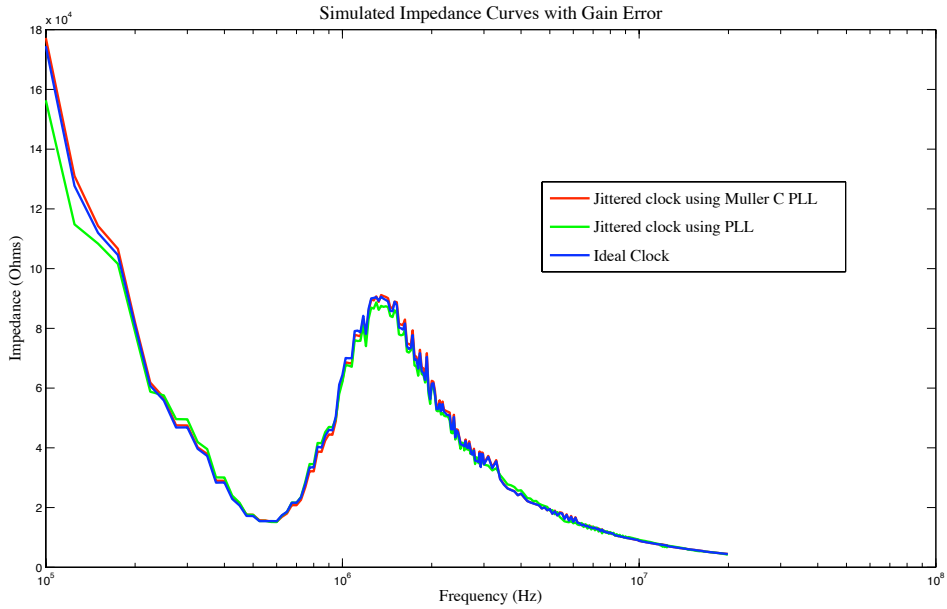


Fig. 4.11: PIP impedance curves generated with ideal and jittered clocks.

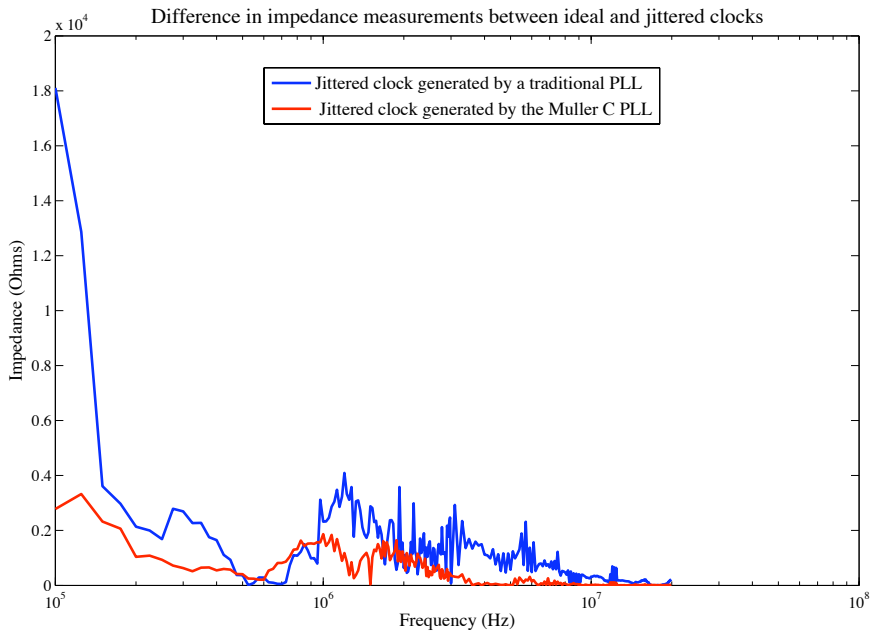


Fig. 4.12: Difference in impedance measurements between ideal and jittered clocks.

noise (and hence no jitter).

4.5 Performance Comparison

Our PLL design needs to be optimized for low jitter in order to provide a highly accurate clock for the high speed data converters. Further, the PLL design has to be optimized for power and area (low power and low area), so that it can be used for CubeSat applications. Based on our optimization parameters, a Figure of Merit is defined for the PLL.

$$FOM_{PLL} = 10 \log \left[\left(\frac{Jitter}{1ps} \right) \left(\frac{Power}{1mW} \right) \right] l \tag{4.2}$$

The unit of FOM_{PLL} is decibels. A smaller FOM_{PLL} corresponds to a better PLL design.

Tables 4.2 and 4.3 shows the performance of some PLL designs using 0.18 μm CMOS technology. We see that the Muller C-oscillator has the smallest FOM, and hence a better PLL design. With the defined PLL FOM, different PLL designs can be easily compared by using a single number.

Table 4.2: Performance comparison of Ring, LC, and Muller-C oscillators at a operating frequency of 1.6 GHz.

Parameter	Ring Oscillator [117]	LC Oscillator [117]	Muller C Oscillator
Power	10.4 mW	22.1 mW	20.8 mW
Area	0.07 mm^2	0.26 mm^2	0.14 mm^2
Jitter	91 ps	29 ps	22.75 ps
FOM	29.76 dB	28.06 dB	26.75 dB

Table 4.3: Performance comparison of Ring, LC, and Muller-C oscillators at a operating frequency of 1.2 GHz.

Parameter	Ring Oscillator [118]	LC Oscillator [119]	Muller C Oscillator
Power	10 mW	72.8mW	20 mW
Area	0.02 mm^2	2.71 mm^2	0.04 mm^2
Jitter	60 ps	9.9 ps	15 ps
FOM	27.78 dB	28.57 dB	24.77 dB

Chapter 5

Conclusions and Outlook

The theme of this thesis and its conclusion is that it is feasible to build a fully integrated plasma impedance probe for nano-satellite applications while maintaining the same scientific performance as past instruments.

The need for miniaturizing space environment instrumentation is emerging as a key function for nano-satellite research. The PIP instrument has undergone numerous iterations, and a variety of techniques on measuring the characteristics of the lower-altitude ionospheric plasma have been reported in literature [55–59]. However, precise impedance measurements were not necessarily the primary goal of previous PIP instrument designs, which were typically interested in locating resonance frequencies and could tolerate uncertainty in the absolute impedance magnitude. Our PIP design is intended to support a new generation of plasma instrumentation and research in which precise impedance measurements will be essential for studying an expanded set of plasma characteristics.

Most of the PIP and IS instruments currently available attach on-chip probes to bench-top instruments (either a PC with a DAQ or some sort of network analyzer) to do the actual impedance measurement. While this could prove useful for initial research, it presents some serious limitations as well. Bench-top equipments are expensive and severely limits the large scale production and deployment of these systems. Further, the few existing on-chip impedance spectrometers are unsuitable for the frequency range under consideration while the existing PIP instruments are unsuitable for CubeSat applications due to the power, bandwidth, and volume requirements of the CubeSat platform.

The proposed PIP chip integrates all of the major analog and mixed-signal components needed to perform swept-frequency impedance measurements. To the authors knowledge, no other fully integrated PIP has been explicitly reported in literature. By integrating

these components onto a single chip, the weight and volume of the PIP instrument are drastically reduced. This resulting instrument will be capable of long-term, low-cost, multi-point deployments in nanosatellite applications.

Unlike previous PIP designs, the integrated PIP performs direct voltage/current sampling on the probes terminal. A Fast Fourier Transform (FFT) is performed by an off-chip FPGA to compute the impedance of the probe and plasma. By performing analog-to-digital conversion as early as possible in the signal flow chain, the design is made less sensitive to variability in analog components. By using an FFT operation, the PIP instrument is less sensitive to transient spikes that proved disruptive in previous PIP designs.

A new design methodology strongly focused on analog errors and variations was introduced. By evaluating each error and variation, design effort was focused on reducing the most significant error sources. The top-down strategy also allowed us to simulate errors and variations in groups, so that we could quantify the accuracy and precision of the PIP under the influence of all errors and variations. This assessment revealed the value and limitations of the PIP as a scientific instrument. The top-down design strategy was also used for system modeling and for transistor-level component design. As a result, the entire design hierarchy could be tested together as a cohesive instrument. By maintaining a top-down environment throughout the design process, the precision of the PIPs impedance measurements across its entire spectral range was fully quantified.

A custom ADC was uniquely built for the PIP chip and its non-idealities and its effect on the instruments accuracy were studied. The system clock was optimized in order to have a high performance ADC. Several different techniques have been reported for the design and implementation of low jitter clock circuits and to suppress the reference spurs as seen in Chapter 3. Most efforts to minimize timing jitter in the VCO focus on reducing power supply noise and ripple. In this dissertation, an alternative method using C-elements was proposed to reduce the timing jitter and reference spurs, and can be used concurrently with these standard methods.

One of the main objectives of the proposed PIP design is to provide accurate impedance

measurements while still optimizing the area and power consumption. Based on our optimization parameters, an unique Figure of Merit was defined for the PLL. With the defined PLL FOM, different PLL designs were easily compared by using a single number. The Muller C PLL performance was compared with some existing PLL designs [117–119] using 0.18 μm CMOS technology. The Muller C-oscillator had the smallest FOM, and hence was found to be the better PLL design for our application.

In conclusion, the new integrated PIP instrument architecture developed for CubeSats, would help in realizing an accurate ionospheric plasma density model with spatially distributed measurements. The design methodology followed provides a "push-button" platform for verifying the performance of future designs. Though this instrument was mainly developed for measuring the plasma impedance, the system architecture could be extended to develop a fully on-chip IS system that could be used for a wide variety of biological and medical applications as seen in Section 1.3. The novel clock generation circuit though ideal for the integrated PIP instrument can be optimally used in any general purpose high-speed data converter to provide an optimized (low jitter, reduced reference spur) system clock.

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Vita

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