博　士　論　文 (要旨)

Emerging embedded nonvolatile memory solution for ultra low power microcontroller systems

超低消費電力マイクロコントローラシステムを実現する次世代不揮発性メモリ応用の研究

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Abstract

This thesis reports emerging embedded nonvolatile memory solution for ultra low power microcontroller systems.

Many semiconductor devices are used nowadays. In case of microcontrollers, that with embedded flash memory have become the mainstream and that volume is 70% of all market of microcontroller and the average growth rate of the market is about 16%, compared to the growth rate of all microcontroller market. Thus, the non-volatile memory devices typified by Flash memory are core technologies of all industries. Currently, Flash-MCU has become the mainstream of the microcontrollers. In the future, in which the semiconductor miniaturization, and the greening of society advance, the conventional embedded memory (SRAM, Flash memory) has the technology limitation such as the leakage current problem with the miniaturization of process technology, the next-generation nonvolatile memory (NVRAM) is expected. This study is intended to overcome the challenge of embedded the nonvolatile memory and investigate that solution for ultra-low power microcontroller systems.

For microcontroller systems, critical issues related to embedded nonvolatile memory are pointed out in Chapter 2. The main issues of an embedded nonvolatile memory design are summarized as five limitations: low voltage operation, high endurance characteristic, high speed access, high density, and low leakage current design of system for low power dissipation. An explanation for each limitation is provided to enhance understanding of the study objective.

For the next three parts of this paper, practical nonvolatile memory design techniques against each limitation are demonstrated. In Chapter 3, Capacitor-coupled EEPROM design with capacitor-coupled EEPROM cell and dual-mode sensing scheme for low voltage, high endurance, and high speed access is discussed.

In Chapter 4, practical high density 1T-4MTJ MRAM (Magnetic Random Access Memory) design with 1T-4MTJ cell and voltage-offset self-reference sensing scheme for high endurance, high density, and high speed access is discussed.

In Chapter 5, the zero standby microcontroller system technology with normally-off system architecture and its power management scheme for low voltage operation and low leakage current in point view of hardware and software technologies is discussed.

The overall conclusion of this contribution is presented as a summary in Chapter 6.

1. Background of research area

Many semiconductor devices are used nowadays. In case of microcontrollers, that with embedded flash memory have become the mainstream and that volume is 70% of all market of microcontrollers. The market overview of microcontrollers is shown in Figure 1. The average growth rate of the market is about 16%, compared to the growth rate of all microcontroller market, it has remained at a high rate. Thus, the non-volatile memory devices typified by Flash memory are core technologies of all industries. Microcontroller applications and market volume is shown in Figure 2. Thus, nonvolatile memory is embedded to almost of microcontroller devices.

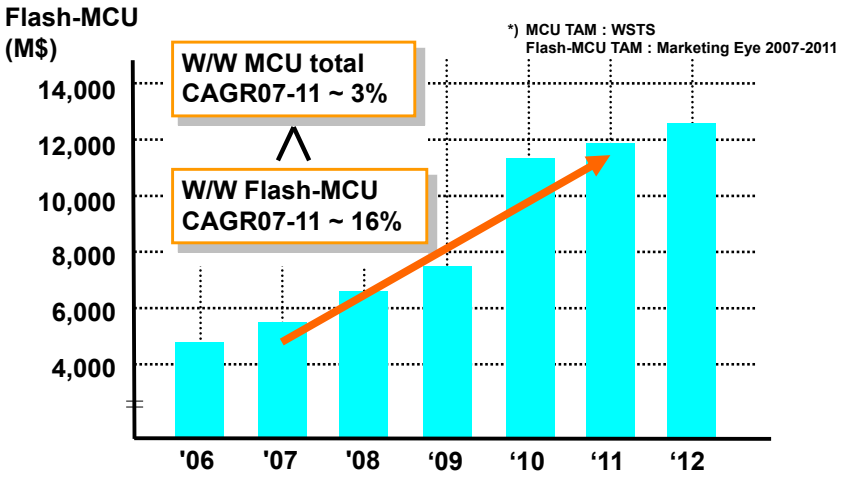

Figure 1: Market overview of microcontrollers

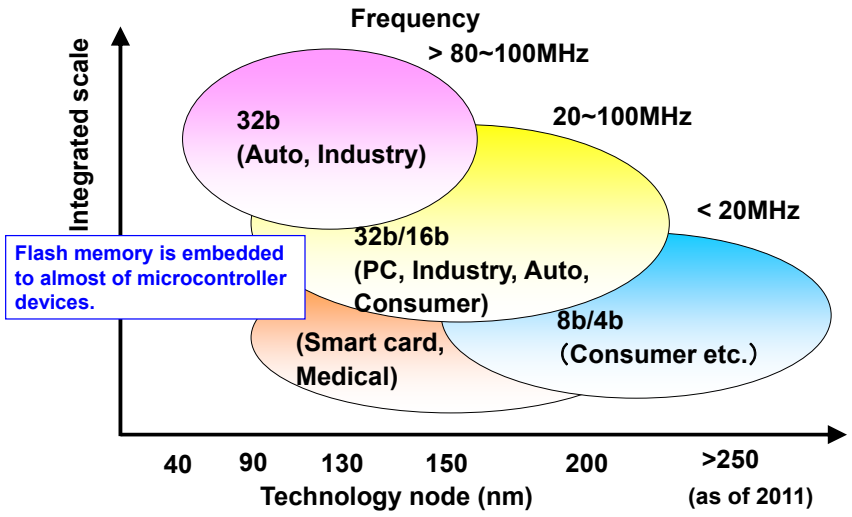

Figure 2: MCU applications and market volume

2. Objective of this study

As mentioned in previous chapter, nonvolatile memory is a key device for recent microcontroller systems. The trend of microcontroller with embedded nonvolatile memory is shown in Figure 3.

Through ’80 years from the end of the ’70s, it appeared single-chip microcontroller with embedded mask ROM, and it becomes possible to make the generalization with instruction sets architecture and real time control. Thereby, it has made a big evolution in terms of performance and ease of use. In the late of ’80s, it appeared the microcontroller with EPROM (Erasable Programmable Read Only Memory) or OTP (One Time Programmable read only memory), and it becomes possible to write the program data at production stage by user. Thereby, the development and production cost has been greatly improved. After then, in the half of ’90s, it appeared the microcontroller with embedded Flash memory (Flash-MCU), and it becomes possible to rewrite the program data after production. Thereby, a mass production setup has become possible at program development completion and the development period has become enabled to be shorten. In addition, a big change has been happened on production and distribution cost side because of commonization of microcontrollers. Currently, Flash-MCU has become the mainstream of the microcontrollers. In the future, in which the semiconductor miniaturization, and the greening of society advance, the conventional embedded memory (SRAM, Flash memory) has the technology limitation such as the leakage current problem with the miniaturization of process technology, the next-generation nonvolatile memory (NVRAM) is expected. This study is intended to overcome the challenge of embedded the nonvolatile memory and investigate that solution for ultra-low power microcontroller systems.

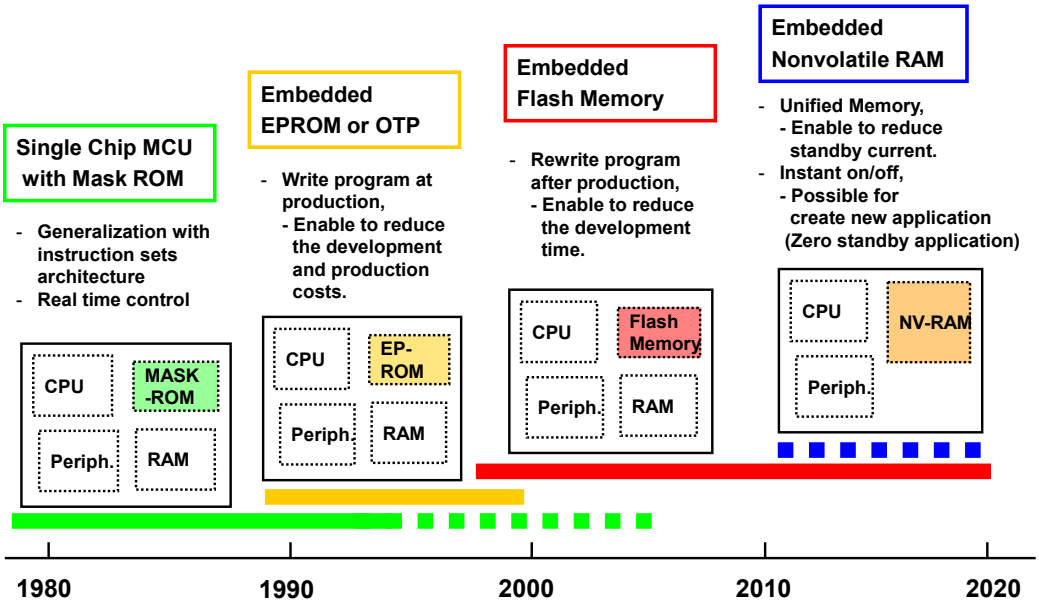

Figure 3: Trend of microcontroller with embedded nonvolatile memory

3. Overview of this thesis

Figure 4 presents the outline of this thesis, as visualized very simply. First, the background and objective of this study are described. For microcontroller systems, critical issues related to embedded nonvolatile memory are pointed out in Chapter 2. The main issues of an embedded nonvolatile memory design are summarized as five limitations: low voltage operation, high endurance characteristic, high speed access, high density, and low power consumption energy design of system for low power dissipation. An explanation for each limitation is provided to enhance understanding of the study objective.

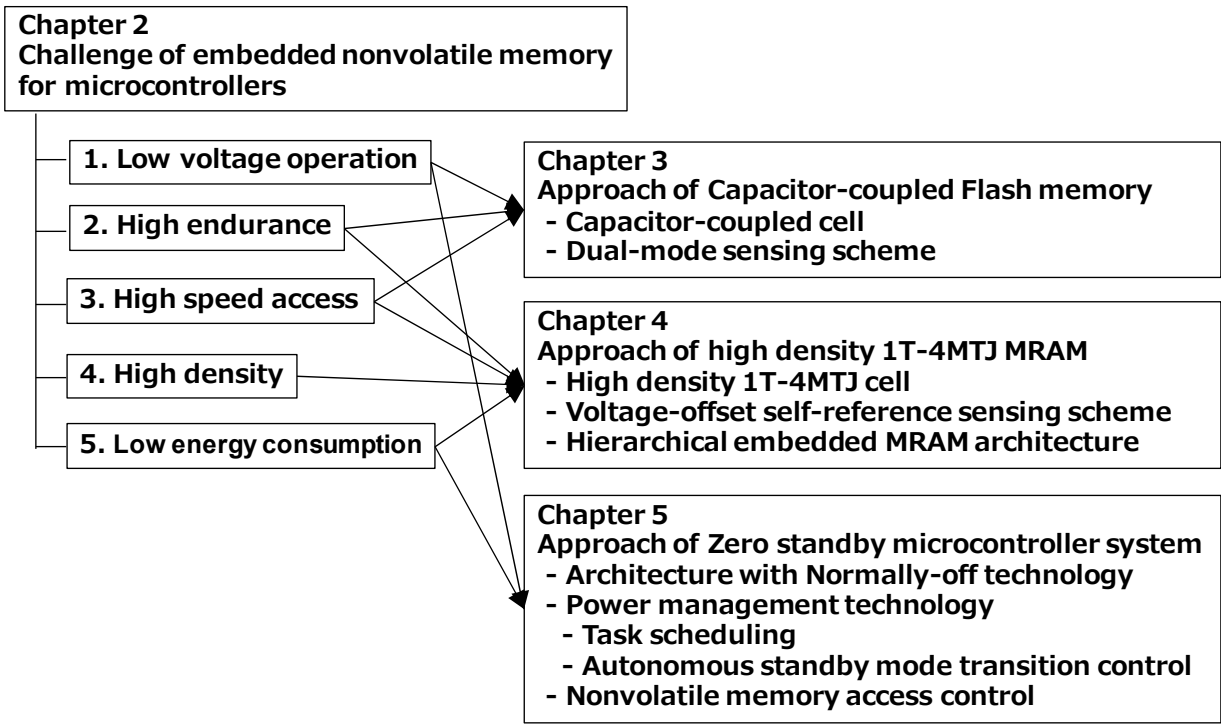

Figure 4: Outline of this thesis

For the next three parts of this paper, practical nonvolatile memory design techniques against each limitation are demonstrated. In Chapter 3, Capacitor-coupled EEPROM design with capacitor-coupled EEPROM cell and dual-mode sensing scheme for low voltage, high endurance, and high speed access is discussed.

In Chapter 4, practical high density 1T-4MTJ MRAM (Magnetic Random Access Memory) design with 1T-4MTJ cell and voltage-offset self-reference sensing scheme for high endurance,

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In Chapter 5, the zero standby microcontroller system technology with normally-off system architecture and its power management scheme for low voltage operation and low leakage current in point view of hardware and software technologies is discussed.

The overall conclusion of this contribution is presented as a summary in Chapter 6.

4. Essentials of this thesis

In Chapter 3, a dual-mode sensing (DMS) schenie of a capacitor-coupled EEPROM cell has been discussed. A new memory cell structure shown in Figure 5 and a new sensing scheme are proposed and estimated. The new memory cell combines an EEPROM cell with a DRAM cell. The DMS scheme utilizes the charge-mode sensing of the DRAM cell in addition to the current-mode sensing of the EEPROM cell. Using this DMS technique, the sensing speed can be enhanced by 36% at a cell current of 15 FA by virtue of the additional charge-mode sensing. Furthermore, the stress applied to the tunnel oxide of the memory transistor can be relieved by decreasing the programming voltage and shortening the programming time. Therefore, with this memory cell structure and sensing scheme, it is possible to realize high-speed sensing in low-voltage operation and high endurance.

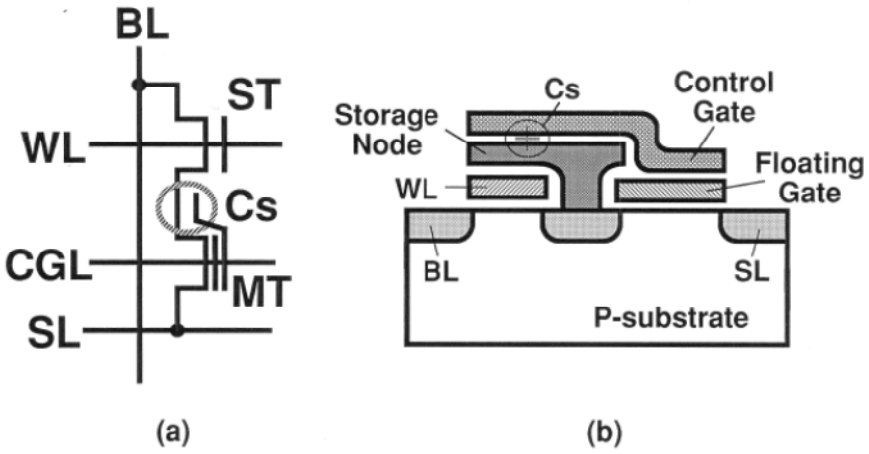

Figure 5: A newly proposed capacitor-coupled EEPROM cell.
(a) A memory cell circuit. (b) A cross sectional view.

In Chapter 4, a high-density memory cell named 1-Transistor 4-Magnetic Tunnel Junction (1T-4MTJ) has been proposed for Magnetic Random Access Memory (MRAM) shown in Figure 6. The new 1T-4MTJ cell has been successfully demonstrated by a 1-Mb MRAM test chip using 130-nm CMOS process. A 1-Mb 1T-4MTJ MRAM with 50MHz@4cycle operation

(tAC=56nsec) is demonstrated. Furthermore, the effective array size of 1T-4MTJ cell is estimated to be reduced of -35.7%. By using 1T-1MTJ and 1T-4MTJ cells, on-chip hierarchical memory scheme composed of fast 1T-1MTJ cell for cache memory and small 1T-4MTJ cell for large-capacity memory is feasible. Thus, microcontroller design indicates chip size reduction with keeping a microcontroller performance.

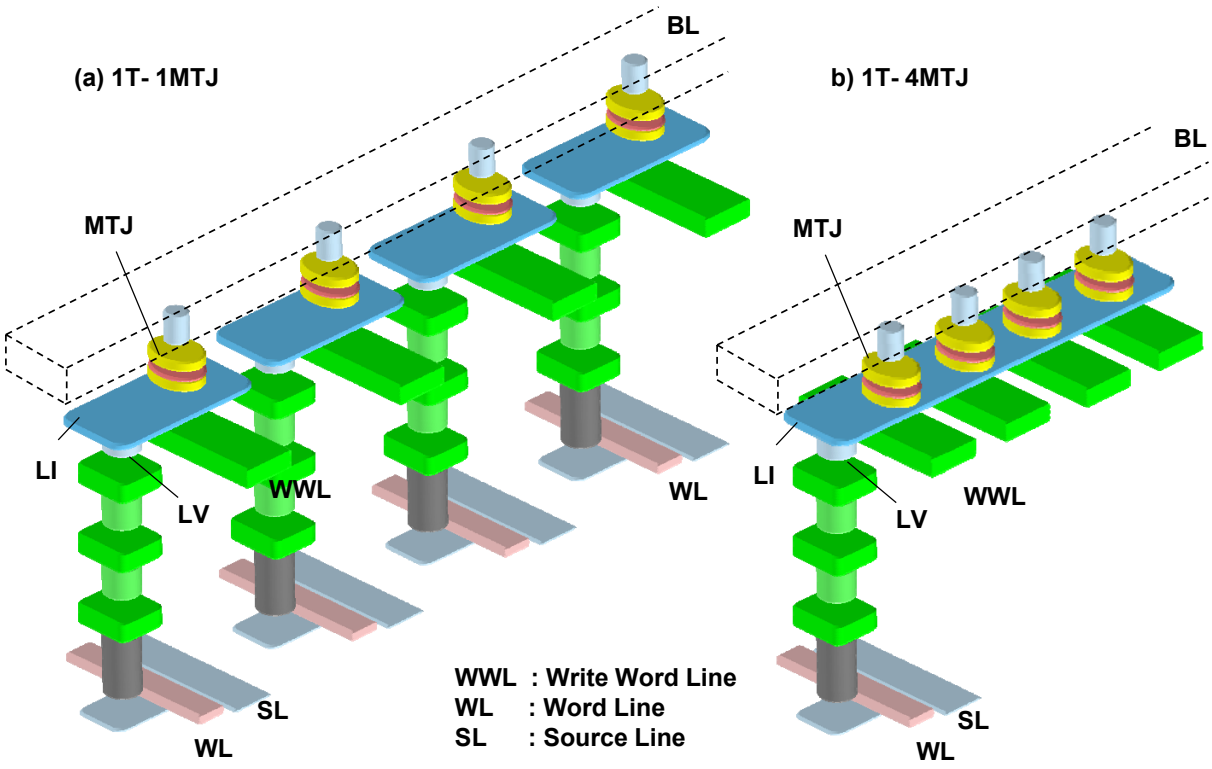

Figure 6: 1T-4MTJ MRAM cell structures

In Chapter 5, the low-power multi-sensor system with power management and nonvolatile memory access control for IoT applications, which achieves almost zero standby power at the no-operation modes has been proposed. System diagram of proposed normally-off multi-sensor node is shown in Figure 7. In here, power management scheme with activity localization can reduce the number of transitions between power-on and power-off modes with rescheduling and bundling task procedures. In addition, autonomously standby mode transition control selects the optimum standby mode of microcontrollers, reducing total power consumption. We demonstrate with evaluation board as a use case of IoT applications, observing 91 percent power reductions by adopting task scheduling and autonomously standby mode transition control combination. Furthermore, we propose a new nonvolatile memory access control technology, and estimate the possibility for future low-power effect.

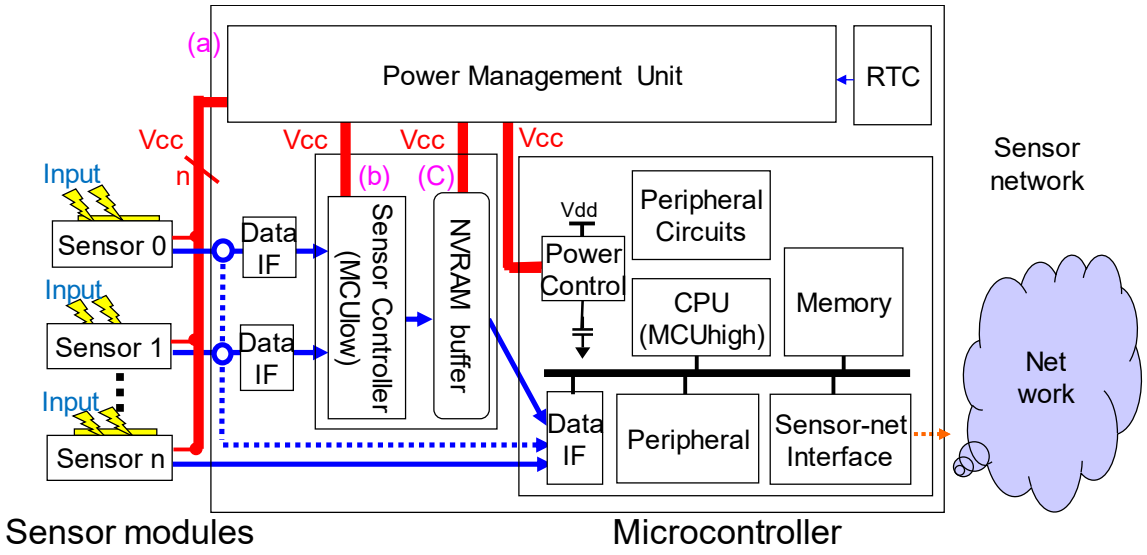

Figure 7: System diagram of proposed normally-off multi-sensor node

This study is presented as measures to address the following three main points:

1. A dual-mode sensing scheme of capacitor-coupled EEPROM cell (Chapter 3)
2. A high-density and high-speed 1T-4MTJ MRAM with voltage offset self-reference sensing scheme (Chapter 4)
3. Low-power multi-sensor system with power management and nonvolatile memory access control for IoT applications (Chapter 5)

These technologies are the most promising candidates for future embedded nonvolatile memory solution for ultra low power microcontroller systems.

平成３０年　７月３１日

学位論文審査報告書（甲）

１．学位論文題目（外国語の場合は和訳を付けること。）

Emerging embedded nonvolatile memory solution for ultra low power microcontroller systems

（超低消費電力マイクロコントローラシステムを実現する次世代不揮発性メモリ応用の研究）

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(2) 氏（ふり）　名（がな）　林越（はやしこし）　正紀（まさのり）

３．審査結果の要旨（600～650字）

平成30年7月31日に第1回学位論文審査委員会を開催した。同日に口頭発表を実施し、その後に第2回学位論文審査委員会を開催した。慎重審議の結果、以下の通り判定した。なお、口頭発表における質疑を最終試験に替えるものとした。

IoTの普及とともに使用される半導体デバイスの数量が爆発的に増加してきており、社会的な要請として消費電力を最小化する必要がある。本論文はこの課題を克服する技術である不揮発性メモリおよびその応用に関する研究成果をまとめたものである。まず新構造のEEPROMおよびdual-mode sensing方式を考案し、低電力性・高速性を両立しながらデータ保持特性に優れたEEPROMを提案した。次に次世代不揮発RAMの本命であるMRAMにおいて1T-4MTJという新メモリ構造を考案し、さらにこれに適したセンス方式を開発することで、高集積度・高速・高保持特性を満たす不揮発RAMを提案した。最後に、動作時以外は電源を切るノーマリーオフアーキテクチャへこれらの不揮発メモリ技術を適用し、ソフトウェアおよびハードウェアの協調設計と合わせて超低電力マイクロコントローラシステムを実現した。

以上のように、本研究は不揮発メモリ技術とそれを用いた超低消費マイクロコントローラシステムを実現する上で重要な知見を与えるものであり実用的価値は非常に高い。従って、本論文は博士（工学）に値すると判定する。

４．審査結果　(1) 判定（いずれかに○印）○合　格　・　不合格

(2) 授与学位　博　士（工　学）