# Wideband digital frequency detector with subtraction-based phase comparator for frequency modulation atomic force microscopy



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# Wideband digital frequency detector with subtraction-based phase comparator for frequency modulation atomic force microscopy

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We have developed a wideband digital frequency detector for high-speed frequency modulation atomic force microscopy (FM-AFM). We used a subtraction-based phase comparator (PC) in a phase-locked loop circuit instead of a commonly used multiplication-based PC, which has enhanced the detection bandwidth to 100 kHz. The quantitative analysis of the noise performance revealed that the internal noise from the developed detector is small enough to provide the theoretically limited noise performance in FM-AFM experiments in liquid. FM-AFM imaging of mica in liquid was performed with the developed detector, showing its stability and applicability to true atomic-resolution imaging in liquid. © *2009 American Institute of Physics.*
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## I. INTRODUCTION

Frequency modulation atomic force microscopy (FM-AFM) (Ref. 1) has traditionally been used in vacuum for subnanometer-resolution imaging of various materials. Recent advancement in AFM instrumentation[2] has enabled to operate FM-AFM in liquid with true atomic resolution,[3] which has opened up the possibilities of its biological applications.[4–6] While the previous studies demonstrated advantages of using FM-AFM in biological research, they also highlighted issues to be overcome.

Among the most serious issues is insufficient operating speed of FM-AFM. Biological systems have higher mobility, complexity, and height variations than the materials that have been investigated by FM-AFM in vacuum. For example, biological membranes contain inhomogeneous nanoscale domains known as "lipid rafts" while imaging of their constituent molecular complexes requires subnanometer lateral resolution.[5] Biological macromolecular assemblies such as amyloid fibrils often have a height of tens of nanometers while imaging of their constituent molecules requires subangstrom vertical resolution.[6] It has been a great challenge to perform such imaging with a realistic experimental timescale due to the insufficient operating speed of FM-AFM.

Development of high-speed FM-AFM requires enhancement of a bandwidth or a resonance frequency of all the components involved in the tip-sample distance regulation. In particular, a frequency detector has been one of the major speed limiting factors. To date, several designs of a frequency detector have been proposed, including analog[7,8] and digital[9] phase-locked loop (PLL) detectors, and an analog quadrature detector.[10] Among them, a digital PLL detector is now most widely used owing to the flexibility of a digital system and the ease of integration into a digital AFM controller. However, the bandwidth of a digital PLL detector has been limited to less than 10 kHz, which has hindered high-speed operation of FM-AFM.

In this study, we have developed a wideband digital PLL detector using a subtraction-based phase comparator (PC) instead of a multiplication-based one that has commonly been used so far. The bandwidth and the noise performance of the developed PLL detector are quantitatively characterized. The applicability of the developed PLL detector to true atomic-resolution FM-AFM imaging in liquid is also demonstrated.

## II. PRINCIPLE AND DESIGN

Figure 1(a) shows a block diagram of a digital PLL detector using a multiplication-based PC (M-PLL). In a M-PLL detector, the input signal $A_v \cos(\omega t+\phi)$ and the reference signal $\cos(\omega t)$ are fed into a PC, where $A_v$ and $\omega$ denote amplitude and frequency of the input signal, respectively. In the PC, the input signal is multiplied by in-phase $[\cos(\omega t)]$ and quadratic $[\sin(\omega t)]$ components of the reference signal, producing dc and $2\omega$ components. While the $2\omega$ components are suppressed by low pass filters (LPFs), the dc components $[(A_v/2)\cos\phi$ and $(A_v/2)\sin\phi]$ are fed into a $\tan^{-1}$ circuit, which outputs the phase difference $(\phi)$ between the input and reference signals.

The difference between $\phi$ and a phase offset $(\phi_0)$ is filtered by a loop filter (LF), producing a frequency shift signal $\Delta\omega(=2\pi\Delta f)$. This signal is routed to a voltage controlled oscillator (VCO) as well as output through a LPF. The VCO generates a sine wave with a frequency $\omega_0+\Delta\omega$, where $\omega_0(=2\pi f_0)$ is the free-running frequency of the VCO. In a steady state, the frequency of the reference signal agrees with that of the input signal, namely, $\omega=\omega_0+\Delta\omega$. Therefore, the output signal $\Delta\omega$ changes in proportion to the frequency shift of the input signal.

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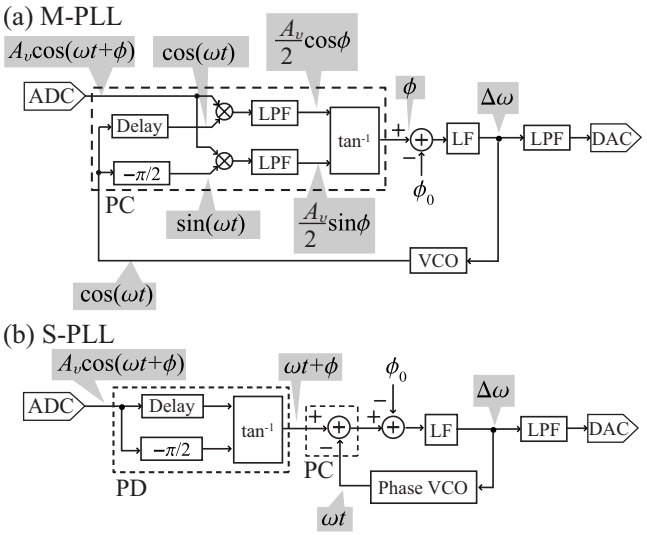


FIG. 1. Block diagrams of (a) M-PLL and (b) S-PLL detectors.

In this design, nonlinear multiplication is used in the PC, so that the generation of $2\omega$ components and other higher harmonics is inevitable. Unless the higher harmonics are sufficiently suppressed by the LPFs, the PLL oscillates at their frequencies. To avoid such instabilities, sufficiently strong LPFs must be used, which however results in a large phase delay in the PLL. Consequently, the LF must be designed to have a narrow bandwidth, leading to a slow time response.

We have solved this issue using a PLL with a subtraction-based PC (S-PLL) as shown in Fig. 1(b). In this design, the input signal is fed into a phase detector, which extracts the phase $(\omega t+\phi)$ of the input signal. The VCO outputs a phase signal $(\omega t)$ instead of a sine wave. Therefore, the phase difference between the VCO output and the input signal is obtained by subtraction. Owing to the linear subtraction, no harmonics are generated and hence no LPF is required. Thus, the LF can be designed to have a wider bandwidth than that in M-PLL, leading to a faster time response.

We implemented this digital signal processing circuit in a field programmable gate array (FPGA) chip (Vertex-4 SX: Xilinx) driven with a clock frequency of 20 MHz. The 14-bits analog-to-digital and digital-to-analog converters (ADC: AD6645 and DAC: AD9772) were used and driven with the same clock signal at 20 MHz as that for the FPGA. The cutoff frequency ($f_{\mathrm{LPF}}$) of the output LPF was set at 100 kHz.

## III. PERFORMANCE

### A. Detection bandwidth

Figure 2 shows the frequency response of the developed S-PLL. The frequency modulated signal was generated with a direct digital synthesizer (DDS) in the FPGA, output from an ADC on the same board, and routed to the S-PLL through a coaxial cable. The amplitude of the demodulated signal output from the S-PLL was measured with a digital multimeter (VOAC7523: IWATSU).

The frequency response shows that $-3$ dB bandwidth of the developed S-PLL is 100 kHz, which is much faster than that for conventional M-PLLs ($<10$ kHz). At present, the bandwidth is limited by the LPF ($f_{\mathrm{LPF}}=100$ kHz). We also

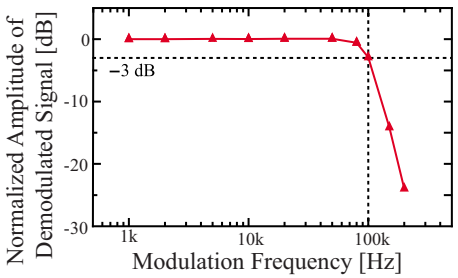


FIG. 2. (Color online) Frequency response of the developed S-PLL. Input signal: 5 MHz $\pm$ 2 kHz, 300 $\mathrm{mV}_{p-p}$. The amplitude was normalized with respect to the value at $f_m=1$ kHz.

confirmed that the bandwidth can be extended to 1 MHz if we set $f_{\mathrm{LPF}}$ at 1 MHz. However, we observed distortions in the demodulated signal at the modulation frequencies $(f_m)$ close to 1 MHz. This is due to the small difference between the input and the modulation frequencies (5 and 1 MHz, respectively), and the distortion of the input signal itself. These technical limitations come from the relatively low clock frequency (20 MHz). Therefore, a further enhancement of the bandwidth should be possible by increasing the clock frequency.

### B. Noise performance

Noise performance of the developed S-PLL was quantitatively analyzed. A clean sine wave at 500 kHz was generated with a DDS in the FPGA and output from an ADC on the same board. A white noise generated with a custom-built noise generator was added to the sine wave and the signal was routed to the developed S-PLL circuit. The frequency noise density $(n_f)$ of the PLL output was measured with a fast Fourier transform analyzer integrated in the AFM controller (MFP-3D: Asylum Research) as shown in Fig. 3.

The solid lines show experimentally measured values, which agree with the theoretically calculated values (dotted lines) using the following equation:[2]

$$n_f=\sqrt{2}\frac{n_v}{A_v}f_m, \tag{1}$$

where $n_v$ is the power spectral density of the added white noise. The deviation observed at frequencies near 100 kHz is due to the roll-off of the output LPF.

The good agreement between the experiment and the theory shows that the influence from the internal noise generated by the developed S-PLL is negligible compared to that from the external white noise under these experimental conditions. From Eq. (1), the influence from the external noise increases in proportion to the slope $\alpha$ $(\equiv\sqrt{2}n_v/A_v)$. Thus, the experimental result obtained with $n_v=88$ nV/$\sqrt{\mathrm{Hz}}$ and $A_v=200$ mV ensures that the internal noise is negligible if $\alpha>6.2\times10^{-7}$ $\mathrm{Hz}^{-1/2}$.

In FM-AFM experiments in liquid, the cantilever oscillation amplitude $A_z$ is typically in the range of 0.1–1 nm. Assuming that deflection noise density around the resonance frequency $n_z$ is predominantly determined by the cantilever thermal vibration, $n_z$ is described by[1]

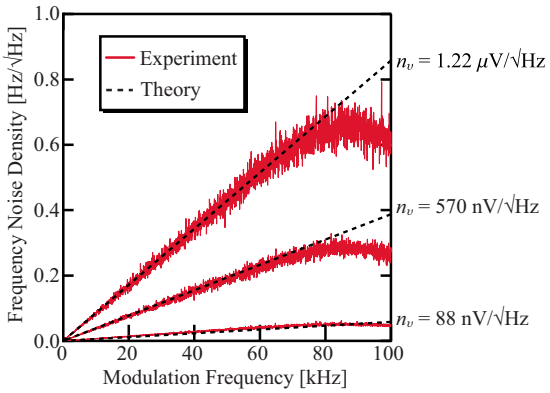


FIG. 3. (Color online) Frequency noise density distribution of the output signal from the developed S-PLL. The input signal is a sum of a clean sine signal and a white noise ($f_0$=500 kHz, $A_v$=200 mV, $f_{LPF}$=100 kHz).

$$n_z = \sqrt{\frac{2k_BTQ}{\pi f_{CL}k}}, \tag{2}$$

where $k_B$ is Boltzmann's constant and $T$ is absolute temperature. $Q$, $f_{CL}$, and $k$ are $Q$ factor, resonance frequency, and spring constant of a cantilever, respectively.

Although the thermal noise decreases as the offset frequency from the cantilever resonance increases, this effect is not significant in liquid owing to the low $Q$ factor of the cantilever resonance. For a typical cantilever used in FM-AFM experiments in liquid (NCH: Nanoworld, $k$=30 N/m, $f_{CL}$=130 kHz, $Q$=8), $\alpha > 1.0\times10^{-4}$ Hz$^{-1/2}$. For a cantilever with a relatively high resonance frequency (Arrow-UHF: Nanoworld, $k$=30 N/m, $f_{CL}$=650 kHz, $Q$=6), $\alpha > 4.0\times10^{-5}$ Hz$^{-1/2}$. These values are much larger than the criterion calculated above ($6.2\times10^{-7}$ Hz$^{-1/2}$). Therefore, the results demonstrate that the internal noise from the developed S-PLL detector is small enough to provide the theoretically limited noise performance in FM-AFM experiments in liquid.

### C. FM-AFM imaging in liquid

We applied the developed S-PLL detector to FM-AFM imaging of a cleaved mica surface in phosphate buffered saline (PBS) solution as shown in Fig. 4. A custom-built FM-AFM with a low noise cantilever deflection sensor[2,11,12] and a commercially available AFM controller (MFP-3D: Asylum Research) were used. A cantilever (Arrow-UHF: Nanoworld) was oscillated with a custom-built self-excitation circuit.

The FM-AFM image in Fig. 4 shows a honeycomblike pattern, which is characteristic of a cleaved mica surface. The atomic-scale protrusions on the honeycomb lattice, which were tentatively attributed to $Al^{3+}$ ions in the previous report,[3] are also resolved in the image. Such irregular atomic-scale contrasts in the image demonstrates that the developed FM-AFM is stable and sensitive enough to provide true atomic resolution in the actual FM-AFM experiments.

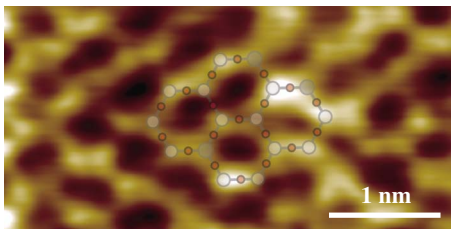


FIG. 4. (Color online) FM-AFM image of a cleaved mica surface in PBS solution (Scan size: 4×2 nm$^2$, Scan speed: 61 nm/s, $\Delta f$=−390 Hz, $A_z$=0.22 nm, $f_{LPF}$=100 kHz). A Si cantilever (arrow-UHF: Nanoworld) was used ($f_{CL}$=634 kHz, $Q$=5.8, $k$=27.7 N/m in liquid). An atomic-scale model of a mica surface is partially overlaid on the image.

While the imaging speed of our previous setup using a M-PLL (bandwidth: 1 kHz) was limited to 1 frame/min, that of our present FM-AFM is not limited by the developed S-PLL but by the data acquisition (10 s/frame) and feedback control circuits (<1 kHz bandwidth) in the commercial AFM controller. The design presented here has enabled to integrate a high-speed frequency detector into the same FPGA as the other digital circuits such as a feedback controller is implemented in. Therefore, by transferring the volume data directly from the FPGA to a PC via a high-speed interface, imaging speed should be further enhanced up to the limit determined by the developed S-PLL, which is approximately estimated to be 10 frame/sec. This is a clear advantage over the previously reported analog frequency detectors[7,8,10] and should facilitate the development of high-speed FM-AFM.

## ACKNOWLEDGMENTS

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