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学位授与の要件	論文博士(学位規則第4条第2項)
学位授与の題目	SYNTHESIS AND IMPLEMENTATION OF MAGNETIC CURRENT LIMITER(磁気式限流器の開発と実装法に関する研究)
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学 位 論 文 要 旨

Abstract. This work describes different topological configurations for a passive magnetic current limiter consisting of a permanent magnet and saturable core. The fabricated model for a series / parallel biasing mode, and single / three phase supply system is described. The transient simulation has been carried out with the help of the tableau approach and experiments have been performed to validate the simulation results. The feasibility of applying the current limiter for the protection of power semiconductor devices in moderately low voltage applications is investigated.

Keywords : Magnetic current limiter, permanent magnet, saturable core, fault current, topological study.

1. Introduction

A large fault current flows in power systems in the event of a short-circuit. The severity of this fault increases as the short circuit ratio for the system at the point of common coupling increases. System or devices connected in series with the fault current path are exposed to the fault current and thus the design of components must take into account the maximum anticipated fault current. Device selection is based solely on the devices' surge rating at high surge current to nominal current ratios. Thus current limiting becomes a necessity in order to reduce the rating of the component and thereby lower the capital cost and improve protection coordination.

Over the last few years, the author have been engaged in research and development of a passive type magnetic current limiter consisting of a NdFeB permanent magnet with axial magnetization, a flux directing core, a saturable core and a current winding[1]. The saturable core can be constructed of a ferrite, amorphous or steel material or any other material having a low saturated flux density and a low saturated permeability. The combination of two such assemblies connected electrically in series but in magnetic counter opposition to each other results in a bipolar fault current limiter. This limiter is placed in series with the source and load.

2. Topological Studies of Magnetic Current Limiter

The physical construction of the current limiter can be designed according to the following three criteria: type of biasing mode, saturable core implementation, number of phases in the supply system. Each of these is discussed in turn.

i) Type of Biasing Mode

The magnet can be configured either in a series or parallel biasing configuration. The magnet in a series biasing configuration is exposed to the magnet's dc flux and the ac flux generated by the winding current. The disadvantage to this approach is the generation of eddy current losses in the magnet and a potentially higher risk of demagnetization over time.

Detailed experiments were performed on a device consisting of a saturable yoke due to material limitations and cost constraints. The device in Fig.1 consists of two sets ferrite C cores placed pole to pole but separated by magnets. Hence the saturable core section and yoke for this setup represents one continuous piece rather than separate sections. The drawback to such an approach is the soft transition between the low inductance and high inductance state. Fig. 2 shows the construction of a device with a steel yoke.

Unfortunately due to material incompatabilities we were not able to design the steel yoke device to meet our specifications and thus the knee point current was too low. This can be overcome by a suitable choice of materials and geometry.

In contrast, the magnet in a parallel biasing configuration is exposed only to the magnet's own dc flux and thus the issue of demagnetization or eddy current losses does not play a significant role. On the other hand, the ratio of the unsaturated inductance to saturated inductance is lower and thus the let through peak current for this type of design will be higher. A picture of the experimental system is shown in Fig. 3 .

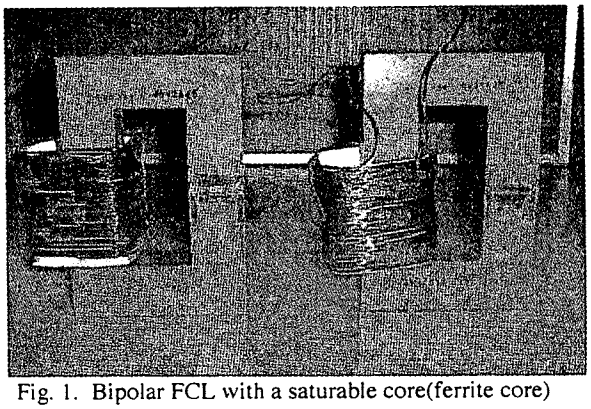

Fig. 1. Bipolar FCL with a saturable core(ferrite core)

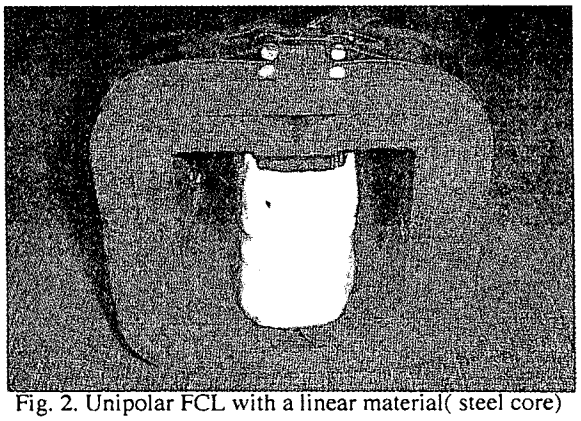

Fig. 2. Unipolar FCL with a linear material(steel core)

iii) *Number of phases in the supply system*

In multi phase systems, one has the choice of implementing a current limiter for each phase or to arrange all the closed cores in a symmetrical fashion around a circle and have each core share a common ring type magnet. For instance in a three phase system, the cores would be displaced 120° with respect to each other around the ring. An experimental prototype bipolar current limiter is shown in Fig. 4 . The core is constructed of a ferrite material.

3. Experimental Results

The experiments for single phase studies have been conducted on the fabricated models using the circuit as shown in Fig. 5. Fig. 6 shows the transient waveforms for the FCL voltage, line current and load voltage for a typical fault. A parallel biased scheme is used in this example. The fault is simulated by short-circuiting the load resistance with switch "SW". It is seen from the Fig. 6 that

the response of the limiter at fault initiation is almost instantaneous and no sensing device is required for its operation.

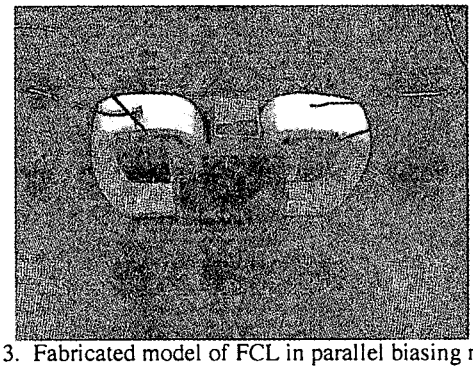

Fig. 3. Fabricated model of FCL in parallel biasing mode

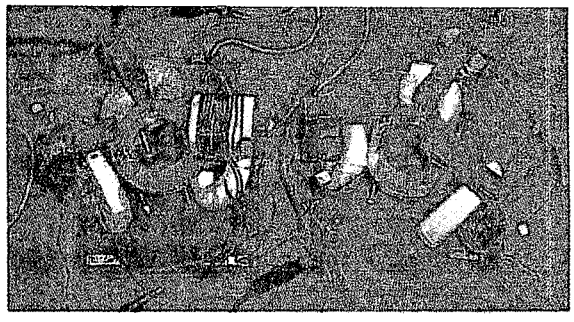

Fig. 4. Fabricated model for three-phase applications

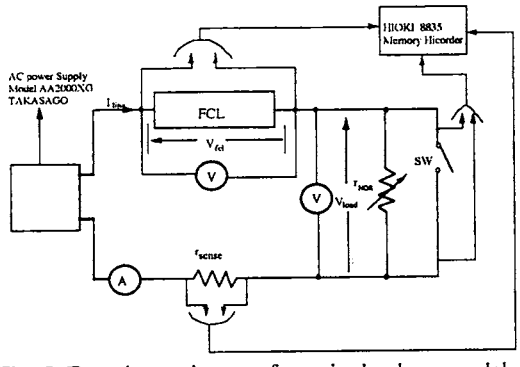

Fig. 5. Experimental set-up for a single phase model

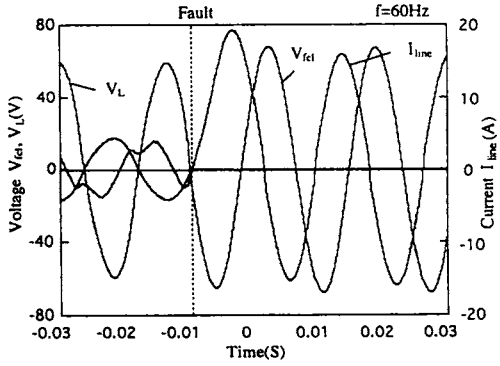

Fig. 6. Transient waveforms for a typical fault condition

Experiments for the three phase model have been carried out using the circuit shown in Fig.7. Fig.8 shows the experimental waveforms corresponding to the source voltage, current through the limiter, voltage across the limiter and load voltage of the u-phase under normal operating conditions. Fig.9 shows the three phase current waveforms and the voltage across the u-phase under a three-phase fault condition. The fault was initiated by closing the switches SW1 to SW3. The current increases considerably compared to the normal operating current but is smaller in comparison to the observed peak current in the absence of the limiter. The differences in the peak fault current values in the three phases may be due to the switching angle of the fault and the nonlinear coupled behavior of the limiter.

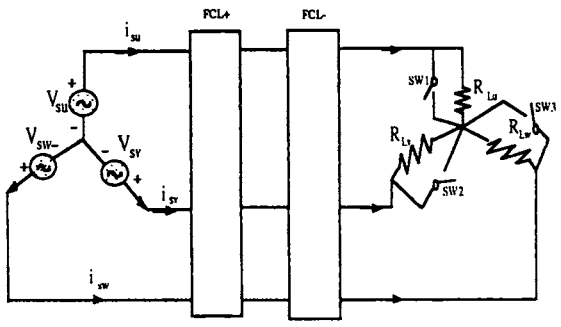

Fig. 7. Experimental set-up for three phase model

The application of a series type of fault current limiter for the protection of power semiconductor devices in moderately low voltage power electronics system has been investigated. Fig. 10 shows a scheme in which a FCL can be used to limit the peak current in the diode bridge in the event of a short circuited diode or a short circuit downstream of the diode bridge. The latter condition will occur when the dc link capacitor is initially charged from a discharged state or if the capacitor is shorted.

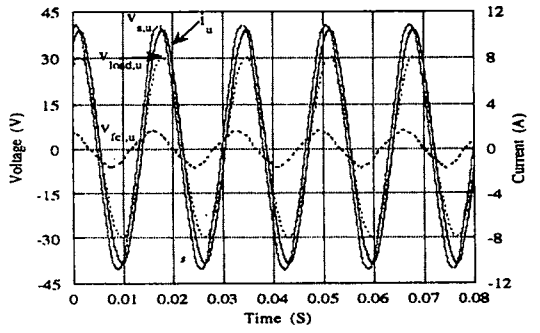

Fig. 8. Transient waveforms under normal operation

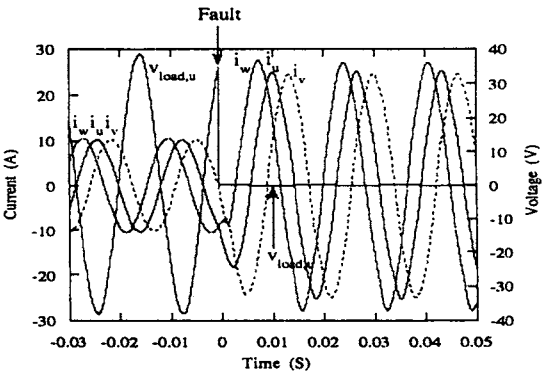

Fig. 9. Transient waveforms under three phase fault condition

Due to the limitation of our set-up a low voltage scheme has been considered. The specification of the system is: Single phase 60Vr.m.s. ; 60Hz, 30A(maximum nominal current); a maximum per-unit reactnace of 10% under nominal conditions; Typically this number should be very low unless we are dealing with an inverter. The peak value of the fault current should not exceed 200% of the nominal peak current. The following components were used: Diodes, Toshiba 12CD12; Capacitor, 5000μF, Load resistance 187.5Ohm.

The charging the capacitor from an initially dischaged state. The line current and voltage across the capacitor were recorded with and without the FCL in the circuit. The corresponding waveforms are shown in Fig.10. It is seen that in the absence of the FCL the peak starting current reaches nearly 95A. In contrast, the peak current with the FCL in place is 55A. This is less than 200% of the nominal peak current.

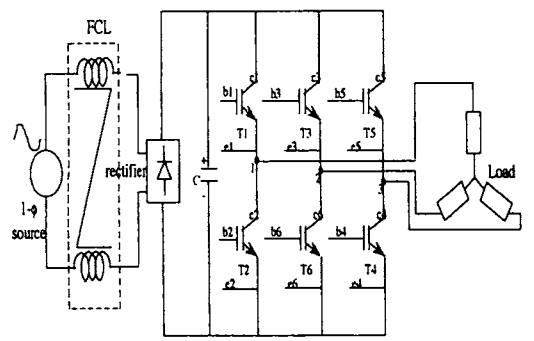

Fig. 10. Use of a FCL in a power electronics system

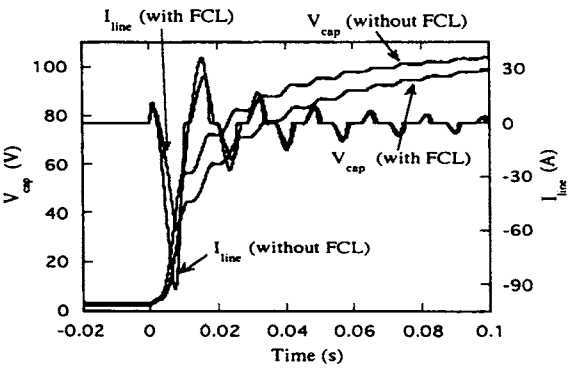

Fig. 11. Starting current waveforms with and without a FCL

4. Conclusions

This work has described the different ways of configuring a passive magnetic current limiter. Experimental results for small-scale laboratory based fabricated models have been reported. This type of fault current limiter can be designed for the protection of power electronics devices in moderately low voltage power systems. An input rectifier followed by a dc link capacitor and equivalent load has been considered for design purposes. With the future development of better magnetic material(rectangular B-H characteristiocs with a very low saturated flux-density magnetic core) improved performance should be attainable.

References :

[1] S.C.Mukhopadhyay, F.P.Dawson, M.Iwahara and S.Yamada, "Analysis, Design and Experimental Results for a Passive Current Limiting Device", *IEE Proceeding on Electric Power Applications*, vol. 146, no. 3, pp 309-316, May 1999.

学位論文審査結果の要旨

平成12年1月26日第1回論文審査委員会を開催、2月2日口頭発表を行った後、同日中に第2回審査委員会を開催し、審議した結果、以下の通り判定した。

本論文は、完全受動形の磁気式限流素子を提案し、素子の構成法・性能について理論解析を行い、試作器による特性を確認するとともに小電力配電系統での利用を想定し、単相用、三相用素子としての実用化などについて幅広く検討したものである。

その成果は、以下のように要約できる。

1）提案された素子は、配線系統内に挿入して使用され、系統内の負荷の故障等で系統に過大な電流が流れようとするとそれを瞬時に抑制し、また系統電流が正常値に戻ると自動的に復旧する特性を有し、駆動電源や素子冷却用の付帯設備等を一切必要としないでものであり、そのモデル素子を製作し、動作メカニズムの解明、基礎特性を明らかにした。

2）主磁心の偏磁方法の違いによる2種類の磁気式限流素子を考案し、素子性能に大きく影響を及ぼす主磁心の特性および永久磁石の特性と素子特性について非線形連成系の数値解析に有効な非線形電気・磁気等価回路手法により定常時および過渡時について解析を行い、望ましい磁心形状について明らかにしている。

3）有限要素法による磁界解析を行い、回路解析結果を補った上で素子の実用化に不可欠な設計パラメータの導出を行い、小電力配電系統へ適用する実用化モデルについて種々の数値解析を行い、得られる特性について検討するとともに実験を行ってその有効性を示した。

以上の研究は、近年における永久磁石の飛躍的な進歩と非線形磁気特性を巧みに活用したものであり、工学的に有用な機能を考案するとともに実用性の高い素子を実現しており博士論文に値するものと判定した。