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Pulse-number control of electrical resistance for multi-level storage based on phase change

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Abstract. Phase change nonvolatile memory devices composed of the SeSbTe chalcogenide semiconductor thin film were fabricated. The resistivity of the SeSbTe system was investigated to apply to multi-level data storage. The chalcogenide semiconductor acts as a programmable resistor that has a large dynamic range. The resistance of the chalcogenide semiconductor can be set in intermediate resistances between the amorphous and crystalline states using electric-pulses of a specified power, and it can be controlled by repetition of the electric pulses. The size of the memory cell used in the present work is 200 nm thick with a contact area of 1 μmϕ. The resistance of the chalcogenide semiconductor gradually varies from 41 kΩ to 840 Ω with in octal steps. The resistance of the chalcogenide semiconductor decreases with an increase in the number of applied pulses. The step-down characteristic of the resistance can be explained as the crystalline region of the active phase change region is increased with an increase in the number of applied pulses. The extent of crystallization was also estimated by the overall resistivity of the active region of the memory cell.

1. Introduction

Phase change (transition) random access memory (PRAM) [1, 2, 3, 4] could potentially substitute all forms of currently available memory devices such as dynamic random access memory (DRAM), static random access memory (SRAM), flash memory and others. PRAM utilizes a thin film chalcogenide semiconductor to store information which has excellent solid state memory properties. Chalcogenide semiconductor (glass) is also used to store information on optical phase change disks such as CD-RW, DVD-RAM and DVD±RW. In an optical disk application, a laser beam having variable intensity is used to heat a small value in order to switch the material between the amorphous and crystalline states. PRAM stores data in a similar manner, however, the electrical pulses are used for the reading and writing processes. The digital data of '1' and '0' can be stored as amorphous or crystalline structures because the reflectivity (refraction index) and resistivity of these states are different.

In this paper, an easy way for resistance control of a multi-level cell of PRAM is described. Multi-level cell (MLC) technology enables the realization of nonvolatile memory with greater density and lower cost. The multi-level cell PRAMs (MLC-PRAMs) respond to the performance improvements in products such as cell phones, digital cameras, hand held personal computers, portable audio and visual systems, and car-navigation systems, which have brought significant increases in program size and data size requirements.

The programming method and circuitry of MLC-PRAM devices (2bits/cell) based on phase change were reported in Ref. [5]. In this paper, the characteristics of the resistance change of SeSbTe chalcogenide semiconductor thin film are discussed.

2. Multi-level cell PRAM (MLC-PRAM) architecture

2.1. Single level cell PRAM

PRAM stores information using structural phase change (from the amorphous to crystalline state and vice versa) in thin film alloys that typically incorporate one or more elements from Column VI of the periodic table, such as Se and/or Te. These alloys are stable in both the crystalline state and amorphous state at room temperature. These two structural states have different electrical conductivity and regions of the alloy material can be switched back and forth between the two states by applying different electrical pulses. The crystallization process and the electric pulse for this operation are called set operation and set pulse, respectively. In the set operation, the sample must be heated up to crystallization temperature (T_c), and a certain amount of time (t_{in}) is required for crystallization at T_c for amorphous materials [6]. This time is called the induction time [6]. Conversely, the amorphization process and the electric pulse for this operation are called reset operation and reset pulse, respectively. The reset pulse is an electric pulse with a high current and narrow width. In the reset operation, the sample must be heated above melting temperature (T_m) and then rapidly cooled to

room temperature.

The memory cell acts between high and low resistance in a dynamic range of typically more than 10^2 times. The digital data of '1' and '0' is stored as the amorphous (low conductivity) or crystalline (high conductivity) states. Information ('1' or '0') stored in the cell is read out by measurement of the cell's resistance.

The details of the write and erase processes are described in Ref.[7]

2.2. Multiple bit per cell of PRAM

The memory cell of PRAM acts between high and low resistance of a very large dynamic range (>100). The resistance of a memory cell can be set in intermediate resistances between the resistance of the amorphous state and the resistance of the crystalline state using certain power pulses. The resistance of the memory cell can be controlled (varied) by the number of set pulses. The ability to attain an intermediate state (resistance) can be explained by the fact that the chalcogenide semiconductor materials can exist in configurations that range from completely amorphous to completely crystalline, including a continuum of structures having partial amorphous and partial crystalline states [12].

The electric pulses which induce partial crystallization are called MLset (Multi-level set) pulses in this paper. The MLset pulse has a lower power than that of the normal set pulse for single level cells (SLC). The applied voltages of V_{MLset} for MLC and V_{set} for SLC in this work were 2.7 V and 2.9 V, respectively. The resistance of the memory cell decreases gradually with an increase in the number of MLset pulses. By using this method, the memory cell can be set in small resistance steps. This is not over-writable for programming any logic value. However, this method has an advantage pertaining to the controllability of the resistance of cells, because there is no need to change the voltage of the applied pulses for each state.

3. Sample preparation and experiments

In this work, the SeSbTe thin films are used as a phase change material. The SeSbTe alloy[7] was prepared from a highly pure mixture of melted of Se, Sb and Te (99.999 %). Proper quantities (total: 4-6 g) of these elements were sealed in an evacuated quartz ampoule and heated in a rocking furnace of 1173 K for at least 24 h[2, 3, 7].

The electrical conductivity of the amorphous and crystalline states of the SeSbTe thin film were measured for evaporated films with a coplanar electrode configuration[8].

The memory device structure was a simple sandwich structure (metal/chalcogenide semiconductor/metal) as shown in figure 1. The thickness of the SeSbTe films and diameter of the active region were fixed at approximately 200 nm and 1 μm, respectively. The composition of the evaporated films is indicated by the composition of the evaporation source, although there might be a slight difference in the composition between the evaporated films and the starting bulk materials. The lower and upper

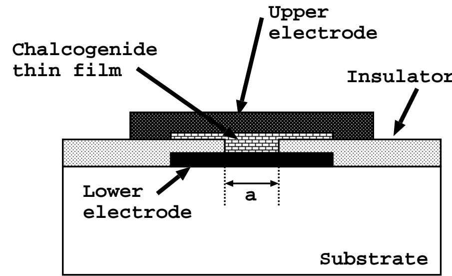

Figure 1. Schematic cross section of a memory cell.The diameter (a) and thickness of the chalcogenide region were fixed at 1 μm and 200 nm, respectively.

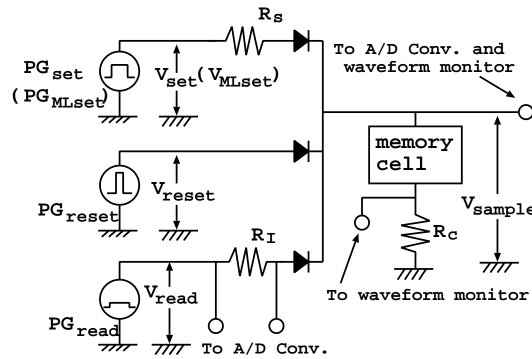

Figure 2. Electrical circuit used to control the phase change. V_{set} and V_{reset} are driving voltages for the set and reset operations. V_{read} is the voltage for reading of the sample resistance and is smaller than V_{th}. R_s is the current-limiting resistance for the set operation. R_c is much smaller than the resistance of the sample. V_{MLset} is the driving voltage for the MLset operation and is set lower than that of general set operation (V_{set}).

electrodes act as a heat-sink during the reset operation.

The sample preparation, composition of phase change alloy and structure of memory cells are the same as those of conventional PRAM [7].

Figure 2 shows the basic electrical circuit used to control the phase change between the amorphous and crystalline states. The driving voltages and pulse widths for each operation are controlled by this electric circuit. The resistance of the memory cell is also measured using this electric circuit. The waveforms of the voltage across the sample and the current flowing through the sample were monitored by a digital oscilloscope (HP, HP54540C). In the case of MLset operation, V_{MLset} is set lower than that of general set operation ($V_{MLset} < V_{set}$).

4. Results

The electrical conductivities of the $Se_xSb_{30-x}Te_{70}$ thin films at 300K are shown in figure 3. The dynamic ranges of the conductivities of amorphous and crystalline states

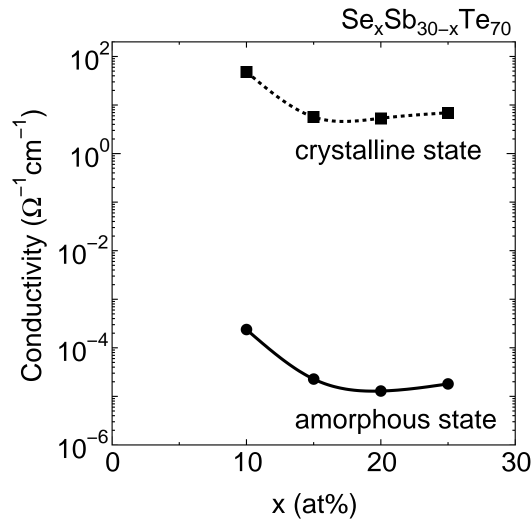

Figure 3. The electrical conductivity of the $Se_xSb_{30-x}Te_{70}$ thin film.

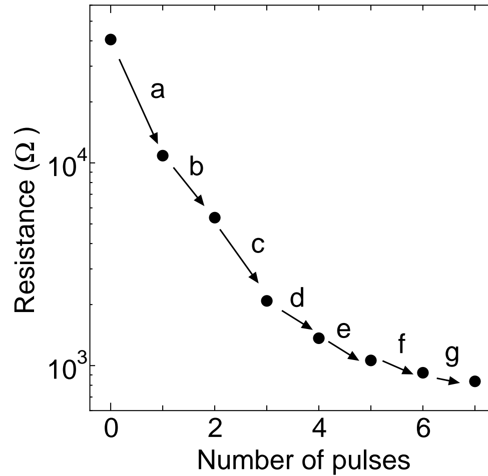

Figure 4. The pulse number dependency of the sample resistance. The resistance varies from 41kΩ to 840Ω with increasing the number of pulses from 0 to 7.

of the $Se_{15}Sb_{15}Te_{70}$ thin films are about 2.5×10^5. The conductivity is decreased with increasing Se contents (at the expense of Sb), however, the conductivity ratio between the crystalline state and amorphous state is kept up within the composition X (10 $\sim$ 30 at%). The large dynamic range shown in figure 3 is one of the great advantages of SeSbTe. Figure 4 shows the pulse number dependencies of the resistance of memory cell using the $Se_{15}Sb_{15}Te_{70}$ thin film. The height of voltage pulse V_{MLset} and pulse width W_{MLset} for every step and the current limiting resistor R_s were fixed at 2.7 V, 500 ns and 500 Ω, respectively. The pulse cycles of each of the MLset pulses were long enough for cooling the sample. The resistance varied from 41kΩ to 840Ω by increasing the number of pulses from 0 to 7, Figure 5 shows the voltage and current waveforms of each step. The '(a)' in figure 5 shows the waveforms of the step 'a' in figure 4. Electric pulses

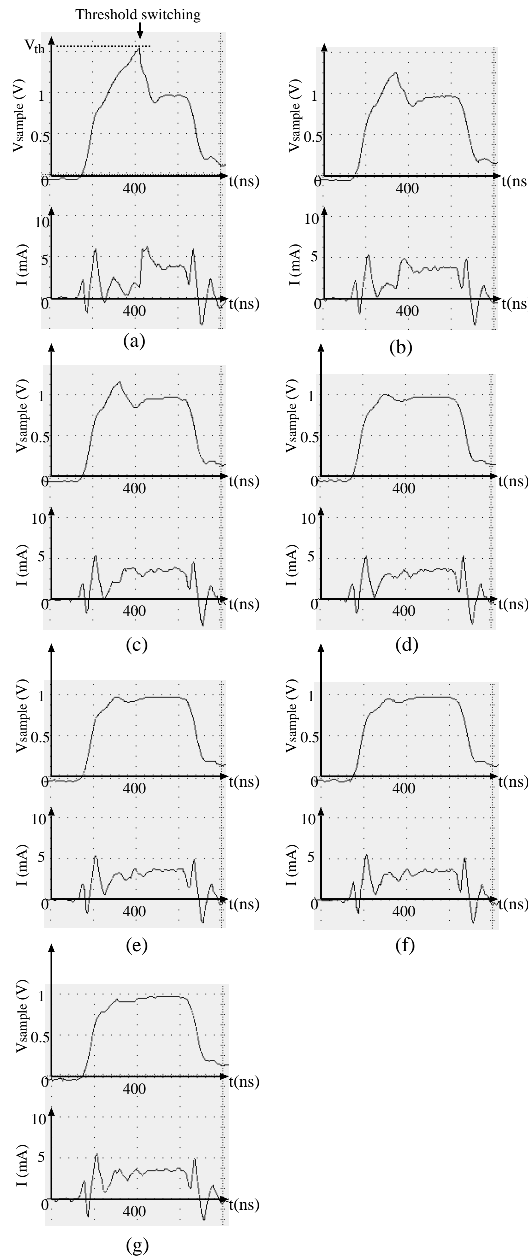

Figure 5. The voltage and current waveforms of each step. The V_{MLset} and W_{MLset} of every step pulse and R_s are fixed at 2.7 V, 500 ns and 500 Ω, respectively.

were applied to the memory cell, as was shown in figure 5 (a), causing a decrease in the resistance of the memory cell from 41kΩ to 11kΩ. The waveforms of (b), (c), (d), (e), (f) and (g) in figure 5 are also shown the voltage and current waveforms of steps 'b', 'c', 'd', 'd', 'e', 'f' and 'g' in figure 4. The threshold voltage V_{th} was decreased by increasing the number of pulses. The threshold switching phenomena was not clarified, when the number of applied pulses is more than 3 in the case of figure 5.

5. Discussion

It is known that the resistance of thin film chalcogenide semiconductors can be controlled by the current intensity of applied electric pulse [10, 11, 12, 13] and devices can be produced for both binary and multi-level storage [10, 11]. The 4 bits per cell (16 values) are demonstrated in Refs. [10, 12]. However, the extra circuits are required to vary the currents of the applied pulses for each of the bit lines. In comparison with a previous approaches, the method proposed in the present work is feasible, because the pulse power and width are fixed. It is an easy way to control the resistance of the thin film chalcogenide semiconductors by the number of the current pulses [5].

GeSbTe system is generally used as a phase change material of nonvolatile memory and digital versatile disk (DVD) and there are many previous works on the material properties. The SeSbTe system needs longer set operation (< 300 ns) than that of the GeSbTe system (10-100 ns). Although, the T_m of the SeSbTe system is lower than that of the GeSbTe system [7]. For example, the T_m of the $Se_{15}Sb_{15}Te_{70}$ and $Ge_2Sb_2Te_5$ are 672 K and 889 K[14], respectively. It indicates that the current and the power consumption for reset operation can be reduced. It is an important feature for the battery drive in mobile devices.

The decrease of the sample resistance MLset operation implies that the crystalline region is increased with an increase in the number of applied pulses. The sample resistance is determined by the volume fraction in each structure. The application of electrical conductivity of the characterization of phase transformation in a two-phase system has been examined by several investigators [16]. In this paper, the extent of crystallization (α) was estimated using the following relation:

$$\alpha = \frac{\ln \sigma_m - \ln \sigma_a}{\ln \sigma_c - \ln \sigma_a}, \tag{1}$$

where σ_m is the overall electrical conductivity of the programming region of the memory cell and σ_a and σ_c are the electrical conductivity of the amorphous and crystalline state of the chalcogenide semiconductors. Mehta *et al* [15] and Kotkata *et al* [16] have used equation 1 to calculate the extent of crystallization in some Se based chalcogenide glasses. Figure 6 shows the pulses number dependence of the extent of crystallization calculated by using equation 1 and figure 4. in the beginning state, over half of the phase change (programming) region was in the crystalline state (the number of pulses: 0). The α was increased from 0.64 to 0.95 with increasing the number of pulses. The resistance change (ΔR) and the extent of crystallization change ($\Delta\alpha$) were decreased with increasing the number of pulses. It seems that the first ΔR of 'a' in figure 4 is sufficient. However, the ΔR between the two lowest lying resistance levels seem to be insufficient in terms of size from a practical standpoint, because the MLset pulse was not optimized for MLC in this work. For example, it could be possible that the resistance decreases gently by decreasing V_{MLset}. The extent of actual phase change carried out occurs in less than half of the portion of the chalcogenide semiconductor region (circled in figure 6). If the region where phase change is actually carried out is expanded, ΔR

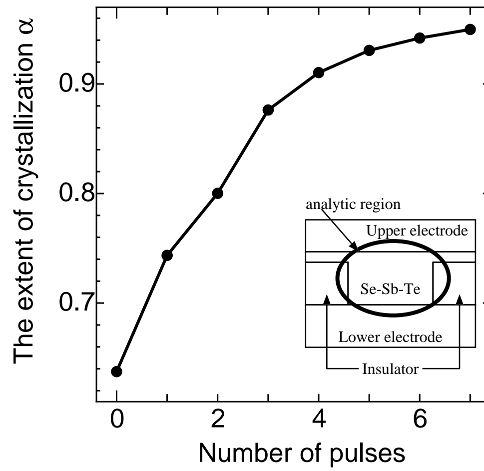

Figure 6. The extent of crystallization.

and the value of multi level could be increased.

The stability of the amorphous state of the sample is important for nonvolatile memory, because the data retention time depends on the stability of the amorphous state. This stability depends on the volume of the amorphous state of the sample [18, 19]. Therefore, in the low resistance state, it seems that the retention time becomes short.

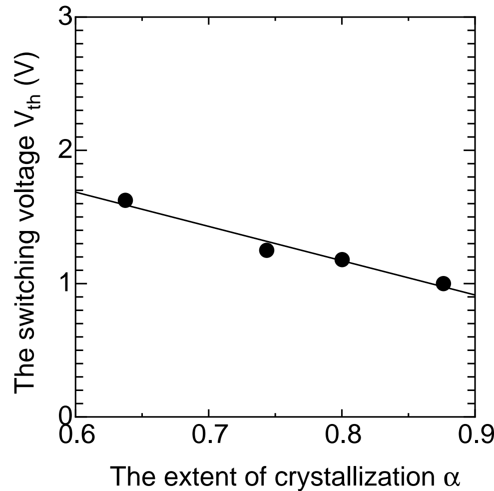

Figure 7. The extent of crystallization dependency of the threshold voltage V_{th}.

Figure 7 shows the α dependency of the threshold voltage V_{th}. The V_{th} was decreased with increasing the α proportionally. It has been demonstrated that the threshold switching transition occurs at a critical value of the electric field ϵ_c independent of sample thickness [20]. In other words, the threshold switching voltage V_{th} is proportional to the thickness of the amorphous region. It seems that the α expresses the thickness of the amorphous region roughly. Similar results for $Ge_2Sb_2Te_5$ thin films were reported [21]. It could be deduced from these notions that the V_{th} of the sample of the

completely amorphous state of the sample (200nm thickness) was 3.2 V. To rephrase, the ϵ_c of the $Se_{15}Sb_{15}Te_{70}$ thin film was 1.6×10^1 V/μm.

The powers for MLset processes were estimated by using figure 5. When the MLset pulse is applied to the sample, the V_{sample} rises to the threshold voltage. The time required (t_{th}) for the V_{sample} to rise to V_{th} depends on the CR time constant of the sample as the current does not flow through the sample for the t_{th}. The t_{th} of our sample was about 200 ns. The t_{th} is a rate limiting factor in the MLset operation. The parasitic capacitance of the memory cell must be reduced for high speed MLset operation. The effective electric power and energy for step 'a' in figure 5 were about 3.8 mW (= 1 V × 3.8 mA) and 0.95 nJ (= 3.8 mW × 250 ns), respectively. These values for electric power and energy for MLset process were 76% and 63%, respectively, of those of the set process for conventional (binary-mode) PRAM. In the SLC, it is important to enlarge the resistance drop by the set pulse. Conversely, it is important to minimize the resistance drop to gain tight control of the resistance in the MLC. Therefore, the power of the set process for SLC is larger than that for MLC.

6. Conclusions

The phase change nonvolatile memory devices composed of the SeSbTe system were fabricated. The memory cell used in the present work is 200 nm thick with a contact area of 0.8 μm^2 (diameter : 1 μm). The resistance of the memory cell can be controlled by certain voltage pulses. The pulse high V_{MLset} and pulse width W_{MLset} for MLset process and R_s were fixed at 2.7 V, 500 ns and 500 Ω, respectively. The resistance of the sample varies from 41kΩ to 840Ω with increasing applied electric pulses,

Acknowledgments

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