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| 著者 | Mohammed Napiah Zul Atfyi Fauzan, Hishiki Takuya, Iiyama Koichi |
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# Wavelength Dependence of Silicon Avalanche Photodiode Fabricated by CMOS Process

Zul Atfyi Fauzan Mohammed Napiah, Takuya Hishiki, and Koichi Iiyama

*Abstract*—**Avalanche photodiodes fabricated by CMOS process (CMOS-APDs) have features of high avalanche gain below 10 V, wide bandwidth over 5 GHz, and easy integration with electronic circuits. In CMOS-APDs, guard ring structure is introduced for high-speed operation by canceling photo-generated carriers in the substrate at the sacrifice of the responsivity. We describe here wavelength dependence of the responsivity and the bandwidth of the CMOS-APDs with opened and shorted guard ring structure.**

*Index Terms*—**Avalanche Photodiodes, CMOS Process, Guard Ring, Wavelength Dependence**

## 1. Introduction

Optical communication has been realized mainly in long-haul communication, and recently board-to-board and chip-to-chip optical interconnection have been actively studied. In order to realize the optical interconnection, it is necessary to integrate optical devices such as light sources, optical waveguides, photodetectors with electronic circuits. A number of researches on Ge photodetectors on Si substrate have been studied for a long wavelength band, while a number of researches on photodetectors fabricated by CMOS process are also studied for short wavelength band [1]–[5], and optical receivers have been demonstrated [6]–[12]. By using CMOS process, it is possible to easily integrate photodetectors and electronic circuits on same Si substrate with low-cost because CMOS process is mature process. Photodetectors fabricated by CMOS process have high avalanche amplification below 10 V bias.

We have already designed and prototyped avalanche photodetectors by using CMOS process (CMOS-APD) in [13], [14]. Our CMOS-APDs have the highest bandwidth of 10 GHz at a wavelength of 830 nm band [15], [16]. In addition, as an application of the optical disk, we also reported characteristics of the CMOS-APD at a wavelength of 405 nm band [17]. Here, in addition to the above wavelengths (405 nm and 830 nm), we characterize the CMOS-APD at 520 nm and 635 nm wavelengths, and summarize the wavelength dependence of the responsivity and the frequency response for the CMOS-APD with opened and shorted guard ring structure.

Zul Atfyi Fauzan Mohammed Napiah, is with the School of Electrical and Computer Engineering, Kanazawa University, Kanazawa 920-1192 Japan, on leave from the Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), 76100 Melaka, Malaysia (email: zulatfyi@utem.edu.my).

Takuya Hishiki and Koichi Iiyama, are with the School of Electrical and Computer Engineering, Kanazawa University, Kanazawa 920-1192 Japan.

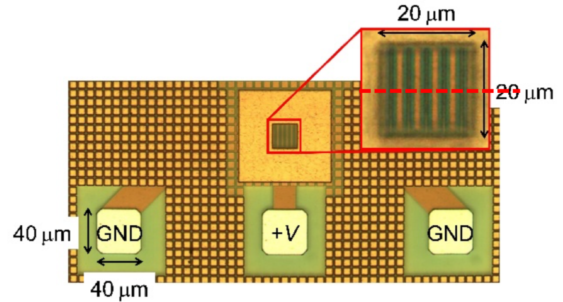



Fig. 1. Photograph of the CMOS-APD. Dash line represent the cross-section of the CMOS-APD.

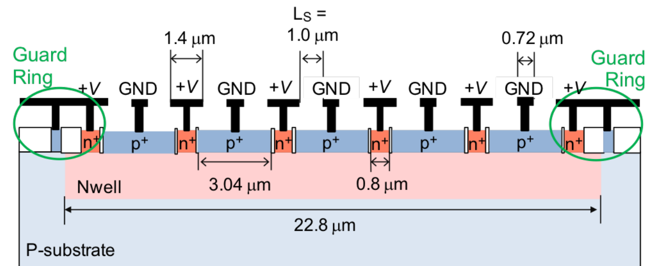



Fig. 2. Cross-sectional structure of a pMOS-type CMOS-APDs. The white areas are shallow trench isolation oxides.

## 2. Device Structure

Figure 1 shows a photograph of a CMOS-APD fabricated by 0.18 µm CMOS process. The anode and cathode electrodes are interdigitally formed on the photo-detection area with 20 x 20 µm$^2$ area. It also has electrode pads for the DC biasing and probing high frequency signal. The electrode spacing $L_S$ is $L_S$ = 1 µm. Figure 2 shows a cross-sectional structure of a pMOS-type CMOS-APD also known as hole-injection-type APD as we described in [14]. The P-substrate, Nwell and shallow trench isolation oxide are used to form p-n diodes in this CMOS-APD design. The shallow trench isolation oxides are used as isolation regions between n$^+$-layer and p$^+$-layer. The n$^+$-layer and p$^+$-layer are arranged alternately and then the electrodes are interdigital structure with the electrode spacing, $L_S$. The depth and the doping concentration of the p$^+$-layer, n$^+$-layer and Nwell are not disclosed from the manufacturer, and the doping concentration of the P-substrate is also not disclosed from the manufacturer. The width of the p$^+$-layer, n$^+$-layer, Nwell and electrodes are shown in Fig. 2. The length of the p$^+$-layer, n$^+$-layer and Nwell are 20 µm to from 20 x 20 µm$^2$ detection area. The n$^+$-layers are narrow and are covered

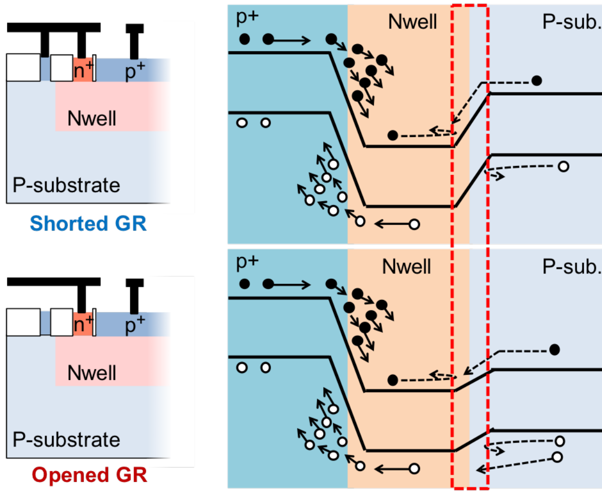



Fig. 3. Band diagram of the pMOS-type CMOS-APD opened and shorted guard ring.

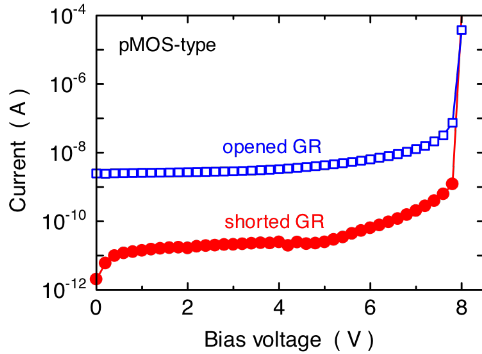



Fig. 4. Measured dark current characteristics.

by electrodes, and the light is illuminated from the top of the CMOS-APD through the $p^+$-layer. Since the electrodes are formed on the upper surface of the substrate, the photo-generated carriers in the p-type substrate (P-substrate) take a long time to move towards the electrodes because the carriers are slow diffusion carriers due to weak electric field, which limits high-speed response. To overcome the problem, the electrodes of the P-substrate are connected to the $n^+$-layer to form guard ring (described as shorted GR), while if the electrodes of the P-substrate are opened, the device is described as opened GR in this paper. The influence of the guard ring structure can be explained by using the band diagram shown in Fig. 3. For shorted GR structure, the guard ring blocks slow diffusion carriers photo-generated in the P-substrate from moving to the electrodes in the Nwell by the potential barrier between the Nwell and the P-substrate. As a result, high-speed response is obtained at the sacrifice of the responsivity. On the other hand, in opened GR structure, the potential barrier between the Nwell and the P-substrate is unidentified and may be low, and a part of the photo-generated carriers in the P-substrate move toward the electrodes in the Nwell. As a result, slow diffusion carriers reach to the electrodes and the response speed is degraded.

When the bias voltage is increased, high electric field is applied between the $p^+$-layer and the Nwell, and then the photocurrent is amplified and the responsivity is improved due to avalanche amplification.

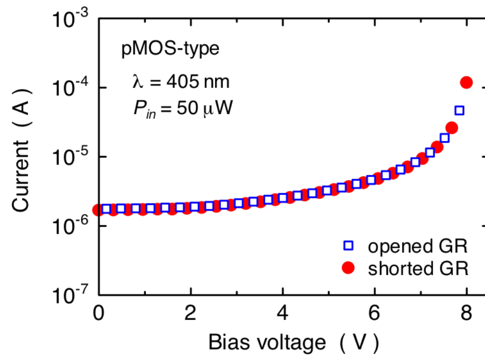
## 3. Results and Discussion

### *3.1 I-V Characteristics*

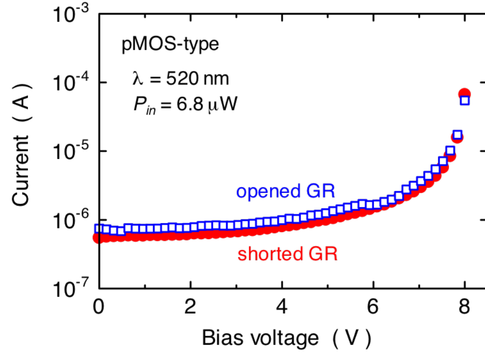
Figure 4 shows the dark current of the pMOS-type CMOS-APD with opened GR and shorted GR. The dark current at low bias is very small about 10 pA for the shorted GR structure. However, for the opened GR structure, the dark current at low bias is more than 1 nA. The dark current of 10 pA for the shorted GR structure is the same with other CMOS-APDs reported in [3], [4], [11]. In the CMOS-APD with shorted GR, the potential barrier between the P-substrate and the Nwell is fixed and stable because the P-substrate and the $n^+$-layer are shorted. The diffusion holes from the P-substrate move toward the P-substrate electrodes due to potential barrier between the Nwell and the P-substrate, and the diffusion electrons from the P-substrate move toward the $n^+$-layer, and the holes and the electrons are recombined and then canceled because the P-substrate and the $n^+$-layer are shorted. On the other hand, in the CMOS-APD with opened GR, the potential barrier between the Nwell and the P-substrate is unidentified and may be low as is shown in Fig. 3. Then carries in the P-substrate move toward the electrode without blocking at the potential barrier between the Nwell and the P-substrate, and the CMOS-APD with opened GR has higher dark current. In the CMOS-APD with opened GR, the dark current is different by samples, and is unstable due to measurement conditions (such as temperature) even though the same sample. This may be because the potential barrier between the Nwell and the P-substrate is unidentified and is unstable. In addition, the breakdown voltages for both guard ring structures are same and are about 8 V.

Figure 5 shows the measured I-V characteristics for the opened GR and the shorted GR structures at wavelengths of 405 nm, 520 nm, 635 nm and 850 nm. At 405 nm wavelength, the I-V characteristics for both the opened GR and the shorted GR structures are almost the same. This is due to strong optical absorption of Si at 405 nm wavelength, and therefore all the incident light is absorbed in the $p^+$-layer and the Nwell and does not reach the P-substrate. It can be seen that the photocurrent is increased gradually with the bias voltage, and is then significantly increased above 7 V by avalanche amplification. The avalanche gain at 8 V is about 100. At 520 nm wavelength, although the photocurrent of the CMOS-APD with shorted GR is slightly smaller than of the CMOS-APD with opened GR, the difference is insignificant. This is because most of the incident light is absorbed in the $p^+$-layer and the Nwell and only a few reaches the P-substrate region at 520 nm wavelength. The avalanche gain at 8 V is also about 100.

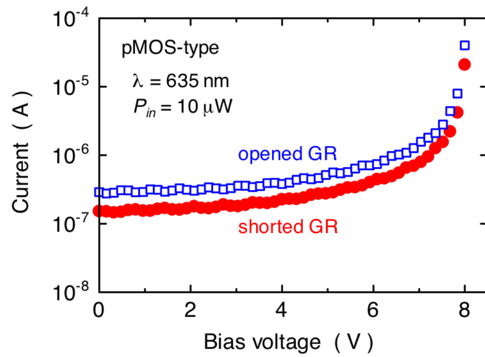
On the other hand, the difference of the I-V characteristics under illumination at 635 nm wavelength was clearly observed for the opened GR and the shorted GR structures, and the photocurrent of the CMOS-APD with shorted GR is about half



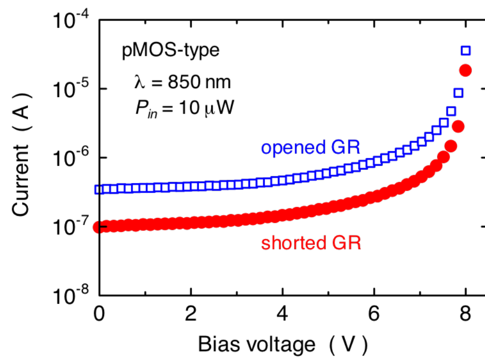
(a) λ = 405 nm



(b) λ = 520 nm



(c) λ = 635 nm



(d) λ = 850 nm

Fig. 5. Measured I-V characteristics for different wavelengths.

as compared to the CMOS-APD with opened GR. This is because the optical absorption of Si at 635 nm wavelength is decreased and a small portion of the incident light reaches the P-substrate region. The electrons and holes photo-generated in the P-substrate move toward the $n^+$-layer and the $p^+$-layer, respectively. For the CMOS-APD with shorted GR, the photo-generated holes are blocked from moving to the Nwell direction by the potential barrier between the Nwell and the P-substrate as shown in Fig. 3. As the $p^+$-layer on P-substrate is connected to the $n^+$-layer on the Nwell, the photo-generated electrons and holes are recombined and do not contribute to the photocurrent. Only electrons and holes photo-generated in the $p^+$ layer and the Nwell contribute to the photocurrent, and accordingly the photocurrent is decreased. In contrast, large photocurrent is obtained for the CMOS-APD with opened GR because the photo-generated electrons and holes in the P-substrate flow to the electrodes through the low potential barrier between the Nwell and the P-substrate as shown in Fig. 3. The avalanche gain at 8 V is about 100.

At 850 nm wavelength, the optical absorption of Si is further decreasing, therefore, more carriers are photo-generated in the P-substrate, and then the magnitude of the photocurrent is hugely affected by the mechanisms of the guard ring described above. For this reason, the difference of photocurrent has spread to around 3.3 times between the opened GR and the shorted GR structures. The avalanche gain at 8 V is also about 100.

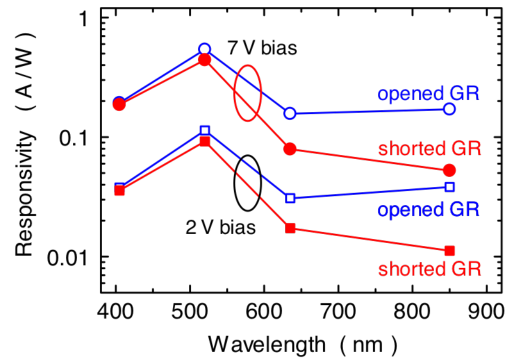


Fig. 6. Wavelength dependence of the responsivity.

### 3.2 *Responsivity*

Figure 6 shows the wavelength dependence of the responsivity at the bias voltage of 2 V and 7 V, obtained from Fig. 5. There is no difference in responsivity for both structures at 405 nm wavelength, and the difference increases with increasing the wavelength. At 405 nm wavelength, all the incident light is absorbed in the $p^+$-layer and the Nwell due to strong optical absorption of Si, and consequently does not reach the P-substrate. As a result, the responsivity is almost same regardless of the guard ring structure. In contrast, due to weak optical absorption of Si at 850 nm wavelength, the incident light can reach the P-substrate region and the shorted GR blocks the photo-generated carriers in the P-substrate, which are slow diffusion carriers, from moving toward the electrodes. Therefore, the reduction of responsivity is more severe with the guard ring. The increased responsivity at 7 V is due to avalanche amplification.

The responsivity at 2 V bias (no avalanche gain) for shorted GR structure at 850 nm wavelength is almost the same with that reported in [3], [4], [11], and the avalanche gain is also almost the same. However no experimental results of the responsivity for different wavelength have been reported except for our report [17].

The responsivity $R$ without avalanche gain is given as

$$R = \eta_{ext}\eta_{int}\frac{q}{h\nu} = \eta_{ext}\eta_{int}\frac{q\lambda}{hc} \quad (\mathrm{A/W}) \qquad (1)$$

where $\eta_{ext}$ and $\eta_{int}$ are the external and the internal quantum efficiencies, respectively, $q$ is the electron charge, $h$ is the Planck's constant, ν is the frequency of light, $c$ is the speed of light in vacuum, and λ is the wavelength of light. The external quantum efficiency $\eta_{ext}$ is composed of the ratio of effective illumination area excluding the electrodes and the surface reflection of the device. As is shown in Fig. 2, total electrode width is 9.2 μm, and then the ratio of effective illumination area is 54% because the detection area is 20 x 20 $\mu m^2$. From optical property of intrinsic Si [18], the surface reflectivity $R_{Si}$ depends on wavelength because the refractive index of Si depends on wavelength, and is tabulated in Table 1 along with the absorption length of Si, the external quantum efficiency $\eta_{ext}$, and estimated internal quantum efficiency $\eta_{int}$ from eq. (1) and the responsivity at 2 V shown in Fig. 6. The highest internal quantum efficiency is achieved at 520 nm wavelength. The internal quantum efficiency is slightly decreased with the shorted GR structure at 520 nm wavelength, and then the total thickness of the $p^+$-layer and the Nwell can be deduced to be slightly shallower than the absorption length of Si at 520 nm wavelength. For 405 nm wavelength, the internal quantum efficiency is decreased as compared with 520 nm wavelength. This is because the illuminated light is absorbed almost in the $p^+$-layer, and a portion of the photo-generated electrons is recombined with holes in the $p^+$-layer while traveling toward the $n^+$-layer. The difference of the internal quantum efficiency due to the guard ring structure is mainly due to measurement error in the photocurrent caused by misalignment of light illumination.

For wavelength longer than 520 nm, the absorption length of Si is increased and then the illuminated light is also absorbed in the P-substrate. A part of the photo-generated carriers is recombined in the P-substrate, and then the internal quantum efficiency is decreased even though opened GR structure. The internal quantum efficiency is also decreased by the shorted GR structure.

Table 1. Estimated quantum efficiency of the CMOS-APD.

| λ (nm) | $R_{Si}$ (%) | $\eta_{ext}$ (%) | $\eta_{int}$ (%) | | Absorption length (μm) |
|---|---|---|---|---|---|
| | | | Shorted GR | Opened GR | |
| 405 | 47.6 | 28.3 | 38.8 | 41.0 | 0.127 |
| 520 | 37.8 | 33.6 | 65.4 | 81.0 | 1.14 |
| 635 | 34.7 | 35.3 | 9.59 | 17.1 | 3.17 |
| 850 | 32.5 | 36.5 | 4.48 | 15.3 | 18.7 |

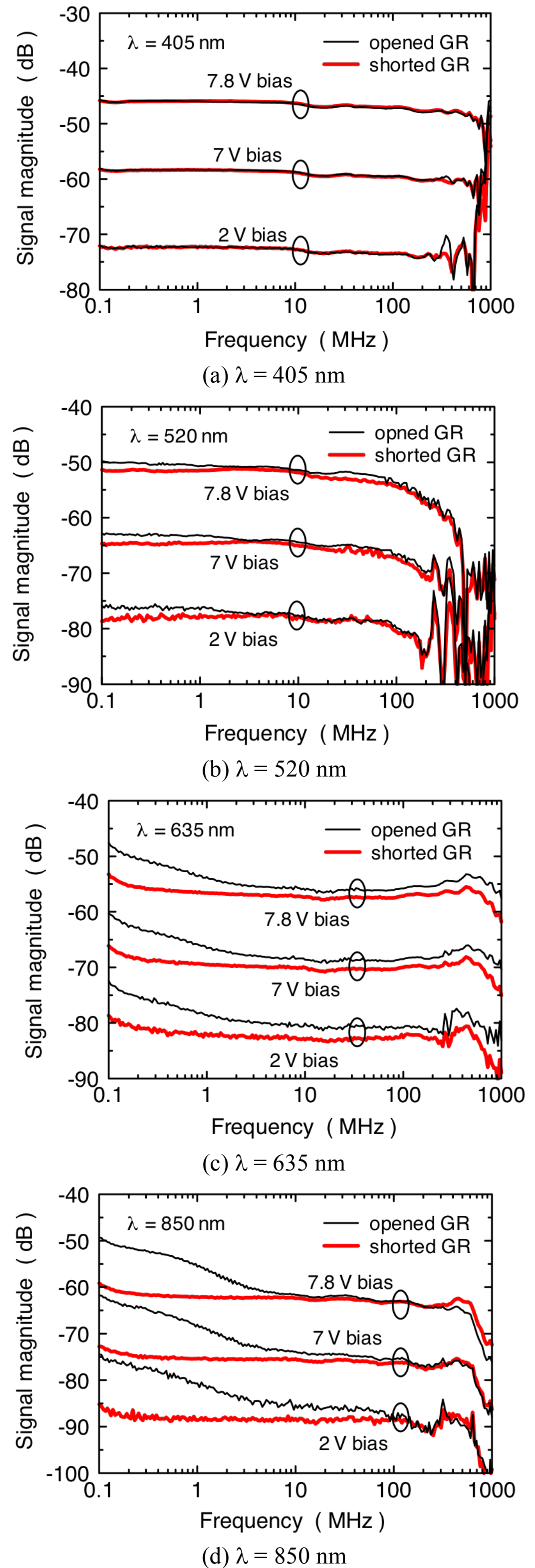



Fig. 7. Frequency responses for different wavelengths.

### *3.3 Frequency Response*

Figure 7 shows the measured frequency response for various wavelengths. In this experiments, we focused on the difference of the frequency response due to shorted or opened GR structure in low frequency region. Since the frequency response

of the intensity modulated laser light source is not compensated, it is impossible to evaluate the bandwidth of the CMOS-APDs in high frequency region. The decrease in the signal magnitude in high frequency region (more than 100 MHz) is due to decreased modulation efficiency of light sources.

At 405 nm wavelength, there is no difference in the frequency response regardless of the guard ring structure, which is a similar trend to the responsivity characteristics because all the incident light is absorbed in the $p^+$-layer and the Nwell. At 520 nm wavelength, the signal magnitude of the CMOS-APD with opened GR is slightly higher than the CMOS-APD with shorted GR in low frequency region, and no difference in the signal magnitude is observed for frequency range over 10 MHz. The difference in signal magnitude in low frequency region is related to the slight difference in responsivity at 520 nm wavelength. This is because a small portion of incident light is absorbed in the P-substrate region for 520 nm wavelength as mentioned before, and the carriers photo-generated in the P-substrate are diminished with the shorted GR. Thus, the signal magnitude is reduced as compared to the CMOS-APD with opened GR.

On the other hand, at 635 nm wavelength, the signal magnitude of the CMOS-APD with opened GR in low frequency region is obviously higher than the CMOS-APD with shorted GR. The difference is approximately 6 dB at 100 kHz and is also corresponding to the difference of responsivity at a wavelength of 635 nm in Fig. 6 which is about 2 times. This is because the carriers photo-generated in the P-substrate reaches the electrodes and contribute to the photocurrent. As the carriers photo-generated in the P-substrate is slow diffusion carriers due to weak electric field, the signal magnitude is reduced in the frequency of several MHz. At 850 nm wavelength, the difference in signal magnitude in low frequency region becomes more apparent, which is about 10 dB at 100 kHz. This difference also corresponds to the difference of responsivity in Fig. 6, approximately 3 times. There is no difference in the frequency response over 10 MHz regardless of the guard ring structure at 635 nm and 850 nm wavelength. The bandwidth of the CMOS-APD with opened GR is about 1 MHz or less, while the bandwidth of the CMOS-APD with shorted GR is found to be more than 100 MHz, which is limited by the modulation bandwidth of laser sources. The bandwidth of more than 1 GHz is expected for the CMOS-APD with shorted GR because the bandwidth of more than 1 GHz was already achieved for the same CMOS-APD at 830 nm wavelength [14]. The bandwidth is significantly improved by the guard ring because slow diffusion carriers photo-generated in the P-substrate are canceled by the shorted GR.

From above results, we conclude the CMOS-APD with shorted GR is very beneficial for practical application. The guard ring enhances bandwidth although the responsivity is decreased for wavelength longer than 520 nm. For wavelength shorter than 520 nm, although the bandwidth is same regardless of the guard ring structure, the guard ring is very effective for realizing low dark current shown in Fig. 4.

## 4. Conclusion

The wavelength dependence of the responsivity and bandwidth of the CMOS-APDs with opened GR and shorted GR has been successfully characterized. At a wavelength of 520 nm or less, there is no difference in the responsivity and the frequency response because all the illuminated light is absorbed in the $p^+$-layer and the Nwell due to strong light absorption of Si. On the other hand, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are canceled by the shorted GR for the wavelength longer than 520 nm, and then bandwidth was remarkably enhanced at the sacrifice of the responsivity. In terms of low dark current and wide bandwidth performance, the introduction of the shorted GR structure in CMOS-APDs is found to be effective.

## Acknowledgment

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