# 10 GHz bandwidth of Si avalanche photodiode fabricated by standard 0.18 μm CMOS process

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| 著者 | Iiyama Koichi, Shimotori Toshiyuki, Gyobu Ryoichi, Hishiki Takuya, Maruyama Takeo |
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# 10 GHz bandwidth of Si avalanche photodiode fabricated by standard 0.18 μm CMOS process

Koichi Iiyama[1], Toshiyuki Shimotori[1], Ryoichi Gyobu[1], Takuya Hishiki[1], and Takeo Maruyama[1]
[1]Kanazawa University, Kanazawa, Japan

***Paper Summary***
*Silicon avalanche photodiode was fabricated by 0.18μm CMOS process and was characterized. The bandwidth of 10GHz with the sensitivity of 0.1A/W was achieved with the electrode spacing of 0.84μm and the detection area of 10x10μm$^2$.*

**Introduction**
Short-distance optical data transmission has been widely studied for realizing board-to-board and chip-to-chip high-speed data transmissions. In these applications, short wavelength vertical cavity surface emitting lasers (VCSELs) and Si photodiodes (PDs) are used for low-cost system configuration. Si PDs fabricated by complementary metal oxide semiconductor (CMOS) process are promising optical devices for easy integration with electronic circuits without any process modification, and avalanche photodiode fabricated by CMOS process (CMOS-APD) has been developed for optical interconnection applications [1-5]. The CMOS-APDs with the bandwidth over 1 GHz and the avalanche gain of more than 100 have been proposed and realized.

Here we report a CMOS-APD with 10 GHz bandwidth with 0.05 A/W responsivity and the gain-bandwidth product of 350 GHz.

**Structure**
Figure 1 shows the structure of the CMOS-APD fabricated by a standard 0.18 μm CMOS process. The device is triple-well structure and is the same with nMOS structure on a p-substrate. The $n^+$- and $p^+$-layers are alternatively arranged and then the electrodes are interdigital structure. The light is illuminated from the top of the device. Since the P-substrate and the deep Nwell are electrically shorted, the photogenerated holes generated there move to the $p^+$-layers on the P-substrate, and the photo-generated electrons generated there move to the $n^+$-layers on the Nwell, which are recombined and don't contribute to the photocurrent. This structure is very useful for high-speed operation because the transit speed of the carriers photogenerated in the deep Nwell and the substrate is very slow due to weak electric field. As a result, the photogenerated carriers generated in the Pwell and the $n^+$-layers on the Pwell contribute to the photocurrent.

We have fabricated CMOS-APDs for the purpose of high-speed operation, and we reported 7 GHz bandwidth of the CMOS-APD with the detection area $S_{PD}$ = 20 x 20 μm$^2$ and the PAD size for RF probing $S_{PAD}$ = 80 x 70 μm$^2$ [6]. The bandwidth is enhanced with decreasing the electrode spacing $L_S$ due to decreased carrier transit time, and is also enhanced with decreasing the detection area and the PAD size for RF probing due to decreased depletion capacitance and the PAD capacitance, respectively. In this study, we fabricated the CMOS-APD with the electrode spacing $L_S$ = 0.84 μm and 1.00 μm, the detection area $S_{PD}$ = 10 x 10 μm$^2$ and the PAD size for RF probing $S_{PAD}$ = 30 x 30 μm$^2$, which is the minimum size for RF probing, to further enhance the bandwidth. The photograph of the fabricated CMOS-APD is shown in Fig. 2.

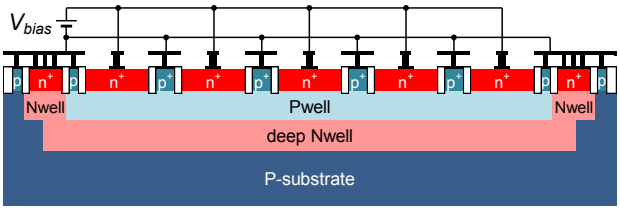


Fig.1: Typical structure of a CMOS-APD.

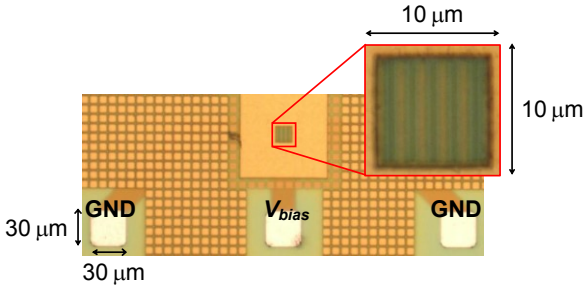


Fig.2: Photograph of fabricated CMOS-APD.

**Characterization**
Figure 3 shows the I-V characteristics (left axis) of the CMOS-APD. The dark current at a low bias is about 10 pA, and the breakdown voltage is 9.1 V. Under light illumination (λ = 830 nm, 20 μW), the current is almost constant for the bias voltage below 6 V, and is gradually increased; especially when the bias voltage is above 8 V, the current is significantly increased due to avalanche amplification, which occurs around the interface between the Pwell and the $n^+$-layers. The photocurrent of the CMOS-APD with the electrode spacing $L_S$ = 0.84 μm is lower than that with $L_S$ = 1.00 μm because the increased number of electrodes block the light incident into the device.

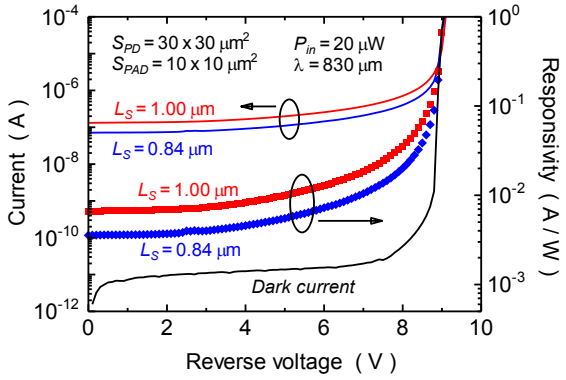


Fig. 3: Measured I-V charactristics and responsivity of the CMOS-APD.

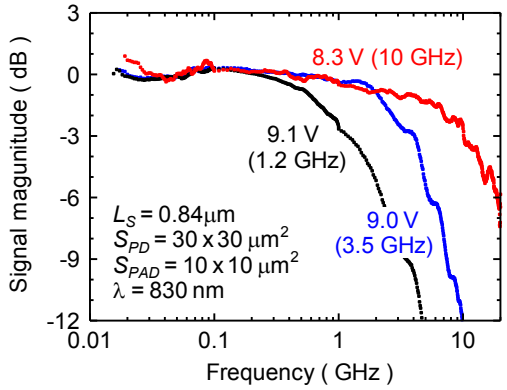


Fig. 4: Frequency response of the CMOS-APD.

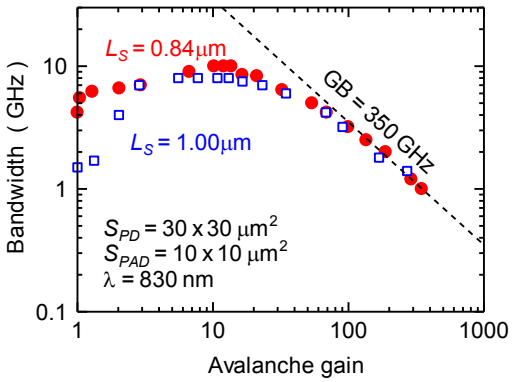


Fig. 5: Bandwidth against avalanche gain.

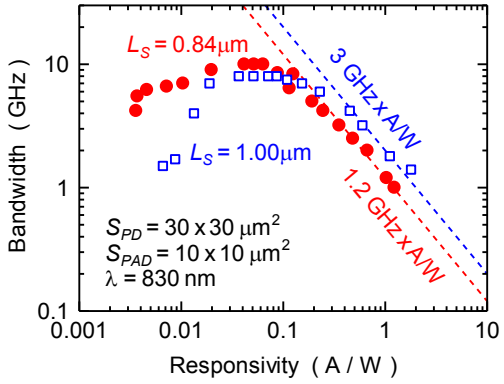


Fig. 6: Bandwidth against responsivity.

The responsivity is also shown in Fig. 3 (right axis). The responsivity at 0 V bias is 3.6 mA/W and 6.6 mA/W for $L_S$ = 0.84 μm and $L_S$ = 1.00 μm, respectively, and is increased due to the avalanche amplification, and the responsivity of about 1.0 A/W was achieved about 9 V bias voltage.

Figure 4 shows the frequency response of the CMOS-APD with the electrode spacing $L_S$ = 0.84 μm. In the measurement, a laser light with the wavelength of 830 nm is intensity modulated by an electro-optic modulator with the bandwidth of more than 25 GHz, and the frequency response of the modulator and RF cables are compensated by using a commercial GaAs PIN photodiode with the nominal bandwidth of 30 GHz. The largest bandwidth of 10 GHz is achieved at 8.3 V.

Figure 5 is the relationship between the bandwidth and the avalanche gain. The bandwidth is maximized when the avalanche gain is about 10, and the maximum bandwidth of 10 GHz is achieved for the electrode spacing $L_S$ = 0.84 μm. The gain-bandwidth product is 350 GHz for the two CMOS-APDs. Since the responsivity of the CMOS-APD at 0 V bias is quite low as is shown in Fig. 3, the responsivity under avalanche amplification is also low regardless of large avalanche gain. We also plot the bandwidth against the responsivity in Fig. 6. The maximum bandwidth of 10 GHz is obtained with the sensitivity of around 0.05A/W. The bandwidth-responsivity product is 3.0 GHz x A/W and 1.2 GHz x A/W for the CMOS-APD with the electrode spacing $L_S$ = 1.00 μm and $L_S$ = 0.84 μm, respectively.

## Conclusions

The CMOS-APD with 10 GHz bandwidth and 0.05 A/W responsivity is realized by narrowing the electrode spacing and decreasing the detection area and the PAD size for RF probing.


## Acknowledgement

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