Increasing static noise margin of single-bit-line SRAM by lowering bit-line voltage during reading

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Increasing Static Noise Margin of Single-bit-line SRAM by Lowering Bit-line Voltage during Reading

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***Abstract*— A 64-kb SRAM circuit with a single bit line (BL) for reading and with two BLs for writing was designed. Single-BL reading is achieved by using a left access transistor and a left shared reading port. We designed the cell layout and confirmed that there is no area penalty for producing two word lines in a memory cell. An analysis of butterfly plots clearly confirms that the single-BL SRAM has the larger static noise margin than the two-BL one. It is confirmed that the static noise margin in the single-BL SRAM is further increased when the BL is precharged to not VDD but to the lower value in the range of VDD/2 to 3VDD/4. In addition, a new sense amplifier circuit without reference voltage is proposed for single-BL reading. We also propose a divided word line architecture for writing to maintain the static noise margin for unwritten blocks.**

I. INTRODUCTION

With the recent rapid increase in data traffic, the power consumption of routers in network systems has become a serious issue. Of the total power consumption of routers, that of SRAM accounts for almost 50 %. Therefore, nanoscale SRAM is necessary for low-energy operation [1-3]. However, in nanoscale SRAM, a large variation of threshold voltage V_T occurs.

To solve the V_T variation problem in SRAM, we have proposed adiabatic SRAM that changes the memory-cell power line or memory-cell ground line (MCGL) gradually during writing [4, 5]. However, there has been no detailed discussion of static noise margin (SNM) during reading between two bit lines (BLs) and a single BL as a function of the precharged BL voltage. Therefore, in this work, we studied the SNM of SRAM with two BLs and a single BL. We found that the single-BL SRAM has a larger SNM than the two-BL SRAM and that the BL precharge voltage should not be VDD but the lower value in the range of VDD/2 to 3VDD/4. This single-lowered-BL SRAM is discussed in detail.

We also propose a sense amplifier (SA) that does not need medium reference voltage between the low BL level and the high one. Regarding the architecture during writing in the lowering BL state, a word divided architecture is proposed to maintain the SNM for unwritten blocks.

II. SRAM CIRCUIT STRUCTURE

The SRAM circuit in one block is shown in Fig. 1(a), which is based on the previous circuit [5]. The 16 cells are connected to the BL. The BL is connected to the global bit line (GBL) via the writing port and the reading port. The writing port is composed of an nMOS transistor. The reading port is composed of two pMOS transistors. The writing and reading ports are activated by the writing port switch signal (WPSW) and the reading port switch signal (/RPSW), respectively. The MCGL is shared in 16 words (row0-row15). The difference from the circuit in [5] is that only the read word line (RWL) goes high during reading, while the RWL and the write word line (WWL) go high during writing. The GBL and BL are set to the precharged voltage (VPC) using a precharged circuit. The SRAM circuit layout using the 0.18-μm process rule is shown in Fig. 1(b). The cell circuit is shown in Fig. 1(c) in detail. The cell size is 1.72 μm×4.62 μm. There is no area penalty compared with the previous circuit [5].

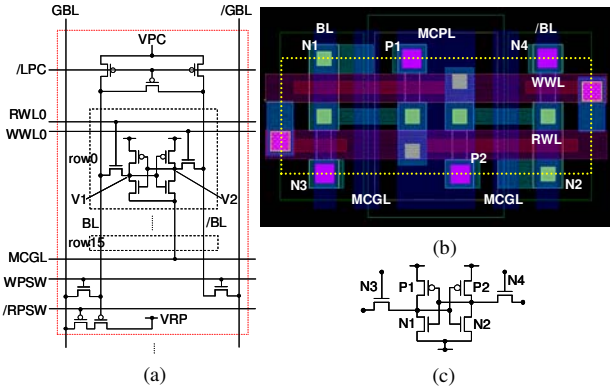

Fig. 1. SRAM circuit using single BL during reading. (a) Block circuit , (b) cell layout, and (c) FF circuit.

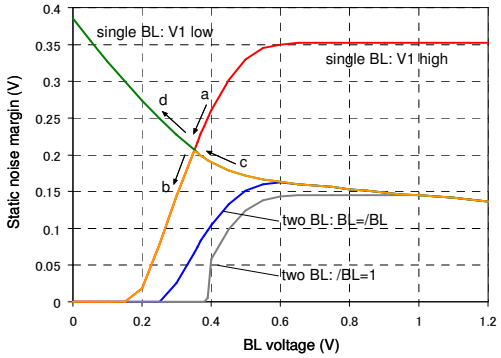

Fig. 2. Comparisons of SNM as a function of precharged BL voltage.

At reading, /RPSW is set to be low. When the flip-flop (FF) node voltage V1 is low, the GBL increases from precharged voltage to reading port power supply voltage (VRP); when V1 is high, GBL is maintained at precharged voltage. With this reading port, we can divide the BL from

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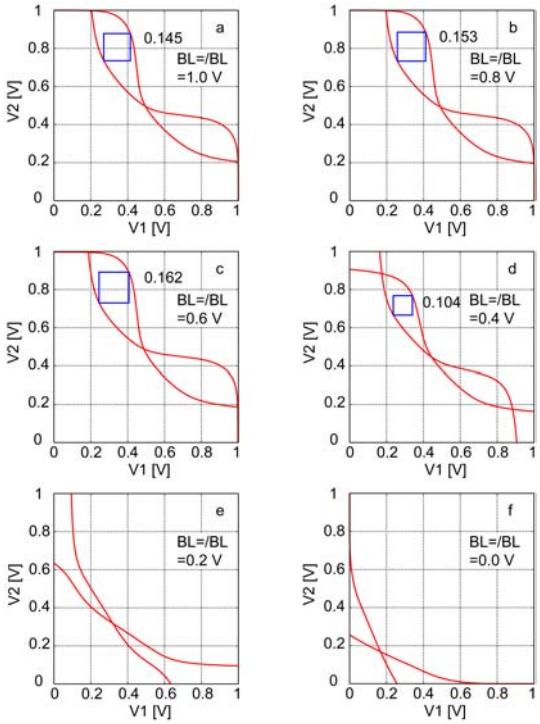

Fig. 3. Butterfly plots of two-BL SRAM when BL and /BL are decreased in the same way.

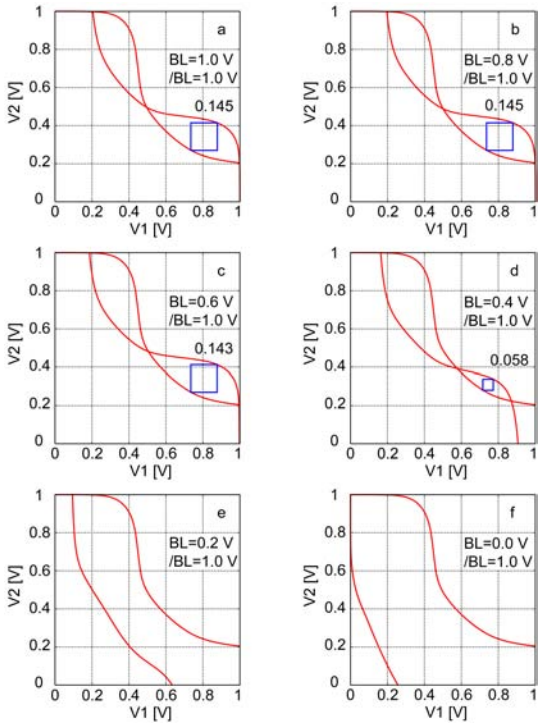

Fig. 4. Butterfly plots of two-BL SRAM by decreasing BL while maintaining /BL=1 V .

the GBL and can decrease the BL capacitance. Therefore, we can decrease the current flow into the cell so that electromigration can be reduced.

III. SNM SIMULATION RESULTS

In the single-BL SRAM, we confirm that the SNM is larger than that of the two-BL SRAM. We discuss this point in detail. The SNM of SRAM was simulated using SPICE. We used the 45-nm design rule. VDD was 1 V. V_T's were 0.43 and −0.33 V in nMOS and pMOS, respectively. The body biases of nMOS and pMOS are GND and VDD, respectively.

The simulation result is shown in Fig. 2. The blue line shows the SNM of the two-BL SRAM when BL and /BL are decreased in the same way. When the BL and /BL voltages are 0.6 V, the SNM becomes 0.16 V, the largest value. When the BL is lower than 0.6 V, the SNM decreases rapidly. The gray line shows the SNM of the two-BL SRAM when the BL is decreased with the /BL voltage maintained at 1 V. When the BL is in the range of 0.7 to 1.0 V, the SNM stays at the largest value, 0.145 V. When the BL is lower than 0.6 V, the SNM decreases rapidly.

For the single-BL SRAM, we explain the SNM according to the FF state. When V1 is high (case I), the SNM is the largest value when the BL is 1 V (red line, curve a). Until the BL decreases to 0.7 V, the SNM is maintained at 0.35 V. When the BL decreases from 0.6 to 0.4 V, the SNM decreases rapidly. Then, with a further decrease of the BL, the SNM decreases to zero, from on the red line (curve a) to the orange line (curve b).

When V1 is low (case II), the SNM is the lowest value, 0.145 V, when the BL is 1 V (orange line, curve c). When the BL decreases to 0 V, the SNM increases to the largest value, 0.385 V, (green line, curve d). The SNM of the single-BL SRAM takes the minimum value of cases I and II. Therefore, the SNM of the single-BL SRAM is shown in the orange line (curve c + curve d) in Fig. 2.

The simulated butterfly plots during reading are shown in Figs. 3-6 in detail. Here, V1 and V2 are the flip-flop node voltages as in Fig. 1. Graphs a-f in Figs. 3-6 correspond to the simulation when the BL voltages are 1.0, 0.8, 0.6, 0.4, 0.2, and 0.0 V, respectively.

First, we discuss the butterfly plots of the two-BL SRAM when the BL and /BL are decreased in the same way, which are shown in Fig. 3. The SNM increases first as 0.145, 0.153, and 0.162 V until the BL voltage reaches 0.6 V. After that, it decreases to 0.104 V when the BL is 0.4 V. When the BL is lower than 0.2 V, the stable points of the flip-flop disappear so that the SNM becomes zero.

Second, the two-BL SRAM in which the BL decreases while the /BL is maintained at 1 V is discussed. The butterfly plot is shown in Fig. 4. In this case, butterfly plot is not symmetric to the y=x line because the voltages of the BL and /BL are different. The SNM is defined as the voltage width of the smaller square in the butterfly plot. In the situation where the /BL is maintained at 1 V, the state such that V1 is high and V2 is low is more unstable. Therefore, the square width of this state in the butterfly plot determines the SNM. As shown in Fig. 4, the SNM holds the initial value of 0.145 V until the BL is 0.8 V. It begins to decrease to 0.143 and 0.058 when the BL voltages are 0.6 and 0.4 V, respectively. When the BL voltage is lower than 0.2 V, similarly, the stable points of the FF disappear so that the SNM becomes zero.

Next, we discuss the single-BL SRAM in Fig. 5. First, we consider the high-V1 condition. In this situation, when the BL voltage is 1 V, the stable point is V1=1 V and V2=0 V

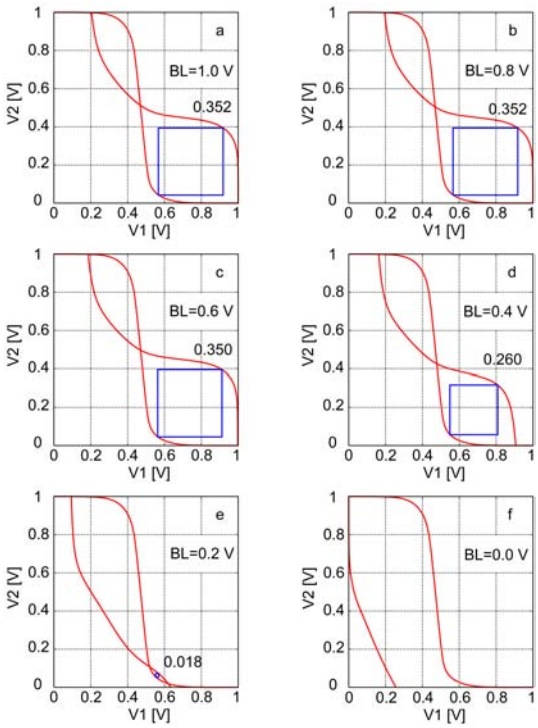

Fig. 5. Butterfly plots of single-BL SRAM by decreasing BL. Squares show the SNM of the state such that V1 is high and V2 is low.

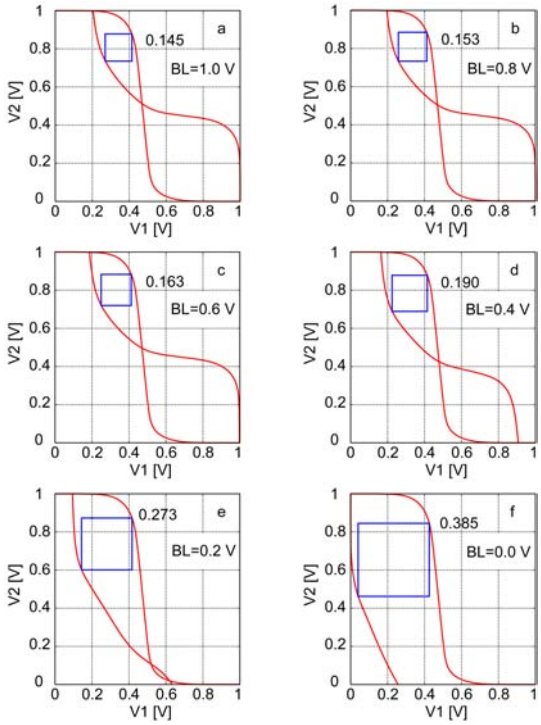

Fig. 6. Butterfly plots of single-BL SRAM by decreasing BL. Squares show the SNM of the state such that V1 is low and V2 is high.

as in Fig. 5(a). In Fig. 5(a), the SNM with V1 high is the largest value, 0.352 V. When the BL decreases, the SNM decreases to 0.350, 0.260, and 0.018 V. When the BL is 0 V, a state such that V1 is high does not exist. This means the FF

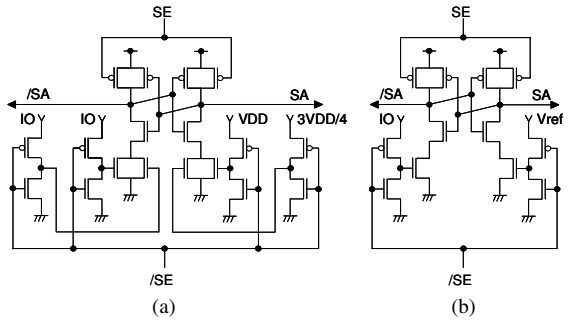

Fig. 7. (a) The proposed SA circuit and (b) the conventional one with Vref.

is inverted due to the decreased BL voltage.

Next, we consider the low-V1 condition. In this situation, when the BL voltage is 1 V, the stable point is V1=0.2 V and V2= 1 V as in Fig. 6(a). In Fig. 6(a), the SNM with V1 low is the smallest value, 0.145 V. When the BL decreases, the SNM increases to 0.153, 0.163, 0.190, 0.273, and 0.385 V. When the BL is 0 V, the SNM takes the largest value.

The SNM of the single-BL SRAM takes the minimum value in Figs. 5 and 6 so that it has a sharp peak as explained in Fig. 2.

It is clear from Fig. 2 that the SNM of the single-BL SRAM is larger when the precharged BL voltage is not 1 V but 0.6 V. We assume that the voltage noise variation of the BL is −0.1 V to +0.1 V. In this case, when the BL voltage is set to 1 V, SNM changes from 0.14 to 0.15 V. When the BL is set to 0.6 V, the SNM changes from 0.16 to 0.17 V. From this discussion, the BL voltage should be set lower than 1 V, or in other words, lower than VDD .

In the following discussion, we assume that the precharged voltage is 3VDD/4. This is because 3VDD/4 can be comparatively easily generated using a tank capacitor circuit without energy dissipation [5]. In this case, VRP in Fig. 1(a) is set to be VDD.

IV. SENSE AMPLIFIER

As only the single BL changes in the proposed SRAM in reading operation, a conventional differential sense amplifier (SA) is not applicable. For the single BL, reference voltage Vref is usually used, and it is input as one bit line in the differential SA. We propose a new SA without Vref, as shown in Fig. 7 (a). The SA is based on three cascaded transistors [6] for a future implementation on advanced process technology with a low power supply voltage. The proposed SA has two driver transistors (two inverters) each side. Both of the left driver transistors received the IO signal as their power sources. The IO is a signal of the GBL via a Y gate. The power sources of the two right driver transistors are 3VDD/4 and VDD. This 3VDD/4 corresponds to the precharged voltage.

Now, we explain the circuit operation in detail. First, the IO is precharged to 3VDD/4, the same voltage of GBL. When the IO is unchanged as 3VDD/4, the current caused by the 3VDD/4 is canceled on both sides. The SA amplifies the voltage difference caused by the current difference between the 3VDD/4 on one of the left-side driver transistors and the VDD on one of the right-side ones. On the other hand, when IO changes from 3VDD/4 to VDD, driver transistor currents due to the VDD cancel each other. The SA amplifies the current difference due to the VDD on one of the left driver

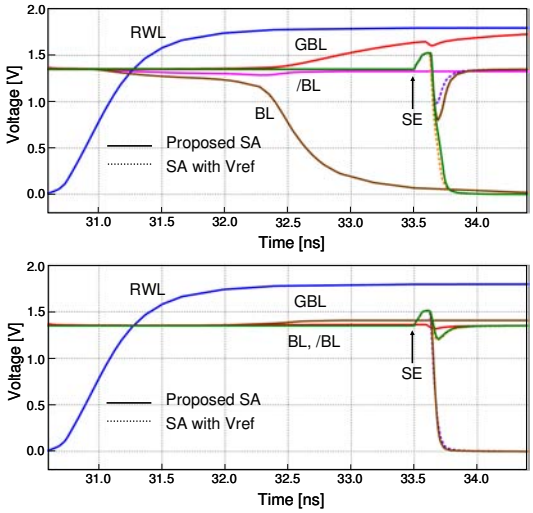

Fig. 8. Simulated waveforms for the proposed and the conventional SA in "V1=0" read (upper figure) and "V1=1" read (lower figure).

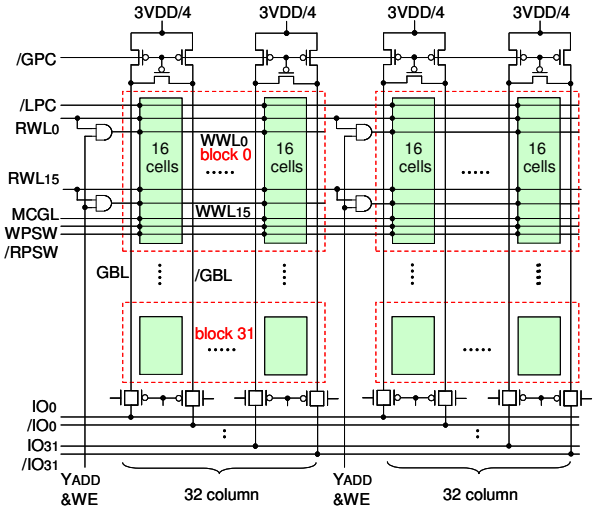

Fig. 9. The 32-kbit memory cell array structure of the designed SRAM.

transistors and the 3VDD/4 on one of the right ones. This SA does not need any Vref generator circuits using the medium voltage between 3VDD/4 and VDD.

SPICE simulation results are shown in Fig. 8. As a reference, waveforms of the conventional circuit with Vref, as shown in Fig. 7(b), are also shown. Here, we set VDD=1.8 V and *Vref*=1.6 V ≅ *(3VDD/4+VDD)/2*. The proposed new SA operates well and has the same effect compared to the conventional SA with Vref.

V. SRAM ARRAY STRUCTURE

One memory cell (MC) array is shown in Fig. 9. The 16 cells are connected to the BL. This unit is connected to the GBL via the reading port and writing port. A GBL pair has 32 units. In reading, only the RWL is activated for two MC arrays. In writing, the RWL is activated for the two MC arrays and the WWL is activated for only a written block in order to avoid the SNM degradation on an unwritten block. If both the RWL and WWL are activated, the SRAM becomes the normal two-BL SRAM so that the WWL should not be activated for an unwritten block. The WWL is controlled by the write

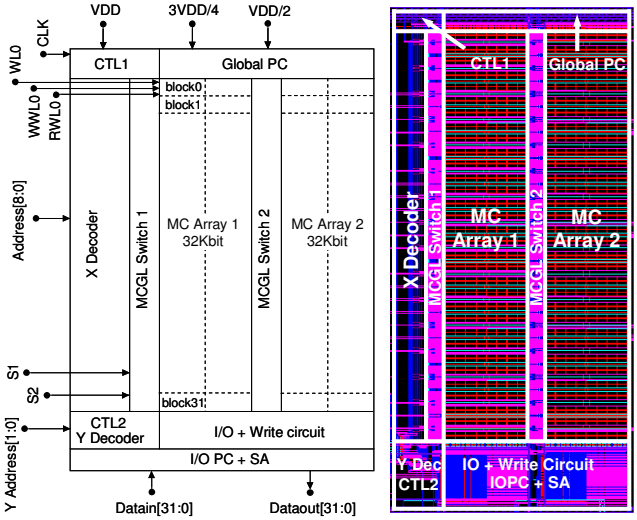

Fig. 10. (a) The 64-kbit memory cell array structure of the designed SRAM. (b) The whole layout of the designed SRAM.

enable signal (WE) and the Y addresses (YADD).

The 32-kbit MC array in Fig. 9 has 64 blocks (1024 words) and one word has 32 bits. Fig. 10 shows the designed SRAM block structure, which has two 32-kbit MC arrays. Addresses are 11 bits: X addresses are nine bits and Y addresses are two bits. To control the MCGL voltage, the MCGL switch block is set for each MC array.

The SRAM is designed in 0.18-µm process technology. The whole layout including the peripheral circuits is shown in Fig. 10(b). The core size is 1741 µm × 827 µm.

VI. CONCLUSION

In summary, we designed a new 64-kb SRAM with shared writing and reading ports. Single-BL reading is achieved by using a left access transistor and a left shared reading port. The single-BL SRAM has a larger static noise margin than the two-BL one, and the margin can be increased further when the BL is precharged to not VDD but to a value in the range of VDD/2 to 3VDD/4. In addition, a new sense amplifier circuit with no reference voltage is proposed. Also proposed is a word divided writing architecture to maintain the SNM for unwritten blocks.

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