Hole-injection-type and electron-injection-type silicon avalanche photodiodes fabricated by standard 0.18-μm CMOS process

Hole-Injection-Type and Electron-Injection-Type Silicon Avalanche Photodiodes Fabricated by Standard 0.18-μm CMOS Process

Koichi Iiyama, *Member, IEEE*, Hideki Takamatsu, and Takeo Maruyama, *Member, IEEE*

Abstract—A hole-injection-type and an electron-injection-type Si avalanche photodiode (APD) were fabricated by a standard 0.18-μm complementary metal–oxide–semiconductor process. The avalanche amplifications are observed below 10 V of the bias voltage, and the maximum avalanche gains were 493 and 417 for the hole-injection-type and the electron-injection-type APDs, respectively. The maximum bandwidth is 3.4 GHz, and the gain-bandwidth products were 90 and 180 GHz for the hole-injection-type and the electron-injection-type APDs, respectively.

Index Terms—Avalanche photodiode (APD), complementary metal–oxide–semiconductor (CMOS), photodiode (PD), silicon.

I. INTRODUCTION

DATA transmission speed in electronic systems can be enhanced by utilizing an optical transmission technique, and the optical transmission has been studied in board-to-board and chip-to-chip data transmission. In these applications, short wavelength vertical-cavity surface-emitting lasers (VC-SELs) and Si photodiodes (PDs) are used for realizing low-cost systems. Si PDs fabricated by the complementary metal–oxide–semiconductor (CMOS) process are expected for monolithic integration with transimpedance amplifiers and following electronic circuits. Fast PDs fabricated by the CMOS process using bulk Si have the responsivity of about 0.04 A/W and the bandwidth of about 1 GHz at 850 nm [1], [2]. In these PDs, the photocurrent generated in the substrate is canceled by differential configuration consisting of an illuminated and a shaded PD. As a result, the bandwidth is increased at the sacrifice of the responsivity. The bandwidth can be increased to 10 GHz by using a silicon-on-insulator (SOI) substrate [3], [4], and the responsivity is, however, 0.008 A/W because of the thin Si layer. Recently, avalanche photodiodes (APDs) fabricated by the standard CMOS process were reported to increase the responsivity [5]–[7], and the avalanche gain is, however, less than 5.

Here we report a hole-injection-type and an electron-injection-type Si APD fabricated by standard 0.18-μm CMOS process [8], [9]. The APDs have the maximum avalanche
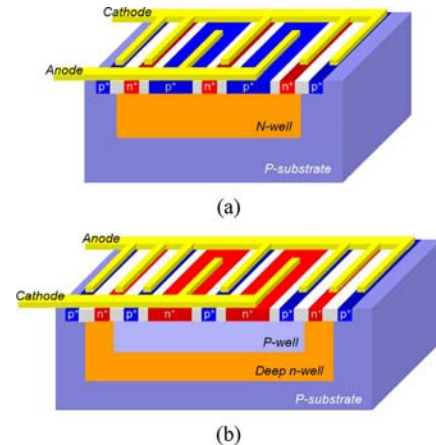
Fig. 1. Structure of APDs fabricated by standard CMOS process. (a) Hole-injection-type APD. (b) Electron-injection-type APD.

gain of 417 and 493 for the electron-injection-type and the hole-injection-type APD, respectively. The maximum bandwidth is 3.4 GHz, and the gain-bandwidth products were 90 and 180 GHz for the hole-injection-type and the electron-injection-type APDs, respectively.

II. STRUCTURE

Fig. 1 shows the schematic structures of the APDs by standard 0.18-μm CMOS process. In the structure Fig. 1(a), the interdigital anode and the cathode electrodes are formed on the p$^+$- and the n$^+$-layers in the n-well, respectively, and the p$^+$-layers in the p-substrate are electrically connected to the cathode electrodes. The light is illuminated from the top of the APD and is absorbed in the silicon through the silicide-free p$^+$-layer in the n-well. The photogenerated electrons and holes in the n-well are drifted toward the n$^+$-layer and the p$^+$-layer in the n-well, respectively. The photogenerated electrons in the p-substrate travel toward the n$^+$-layer, and the photogenerated holes in the p-substrate travel toward the p$^+$-layer in the p-substrate because of the built-in potential barrier between the p-substrate and the n-well, and are recombined and are not contributed to the photocurrent. In this structure, high electric field is applied around the interface between the p$^+$-layer and the n-well, and then the photogenerated holes are efficiently multiplied due to avalanche mechanism. Hence the APD is the hole-injection-type APD.

In the structure Fig. 1(b), the interdigital anode and the cathode electrodes are formed on the p$^+$- and the n$^+$-layers in the p-well in the deep n-well, respectively. Both the p$^+$-layer in the p-substrate and the n$^+$-layers in the deep n-well are

electrically connected to the anode electrodes. The light is illuminated from the top of the APD and is absorbed in the silicon through the silicide-free n$^+$-layer in the p-well. The photogenerated electrons and holes in the p-well are drifted toward the n$^+$-layer and the p$^+$-layer in the p-well, respectively. The photogenerated electrons in the p-substrate travel toward the n$^+$-layer, and the photogenerated holes in the p-substrate travel toward the p$^+$-layer in the p-substrate because of the built-in potential barrier between the p-substrate and the deep n-well, and are reconbined and are not contributed to the photocurrent. In this structure, a high electric field is applied around the interface between the n$^+$-layer and the p-well, and then the photogenerated electrons are efficiently multiplied due to avalanche mechanism. Hence the APD is the electron-injection-type APD.

The thickness and the doping concentration of the n-well, the p-well, the deep n-well, the n$^+$-layer, and the p$^+$-layer are not disclosed. The silicide widths below the electrodes for the n$^+$- and the p$^+$-layers are 0.44 and 0.72 μm, respectively, which are the minimum width determined by process. Between the n$^+$- and the p$^+$-layers, 0.48-μm-wide oxide regions are formed for electrical isolation. The widths of the silicide-free p$^+$- and n$^+$-layers are 1 μm. The detection area is $20 \times 20\ \mu$m^2. As a result, the number of the electrodes in the detection area are nine in both structures; four and five electrodes for the cathode and the anode, respectively, for the hole-injection-type APD, and four and five electrodes for the anode and the cathode, respectively, for the electron-injection-type APD. A passivation film with the thickness of about 8.6 μm is coated on the detection area.

III. CHARACTERIZATION

Fig. 2 shows the measured current–voltage (I–V) characteristics with and without the optical illumination for (a) the hole-injection-type APD and (b) the electron-injection-type APD. The wavelength of the illuminated light is 850 nm. The dark current is a few nanoamperes, and the breakdown voltages defined by the voltage at which the dark current exceeds 1 μA are about 8.05 and 9.25 V for the hole-injection-type and the electron-injection-type APDs, respectively. In Si pn diodes, when the breakdown voltage is larger than $6E_g/q = 6.7$ V, where E_g is the bandgap, the breakdown is caused by avalanche mechanism, and then the breakdown of our APDs is caused by avalanche mechanism. Under light illumination, the photocurrent is almost constant when the bias is below 4 V, and is gradually increased, especially when the bias is above 6 V, due to the avalanche amplification. Such a low breakdown voltage is due to relatively high doping concentration in the n-well and the p-well. The CMOS process we utilized is for 1.8- and 3.3-V operation, and then the n-well and the p-well are thin and the doping concentration are higher than the i-layer in the p-i-n PD. Since the breakdown voltage decreases with increasing the doping concentration, the breakdown voltage of our APDs are low. The breakdown voltage difference between the two-types of the APDs may be attributed to the difference in the doping concentration in the n-well and the p-well, which are not disclosed.

Fig. 3 shows the responsivity against the bias voltage at 850-nm wavelength obtained from Fig. 2 along with the avalanche gain $M(V)$. The open squares and the closed circles are the measured results for the hole-injection-type and the
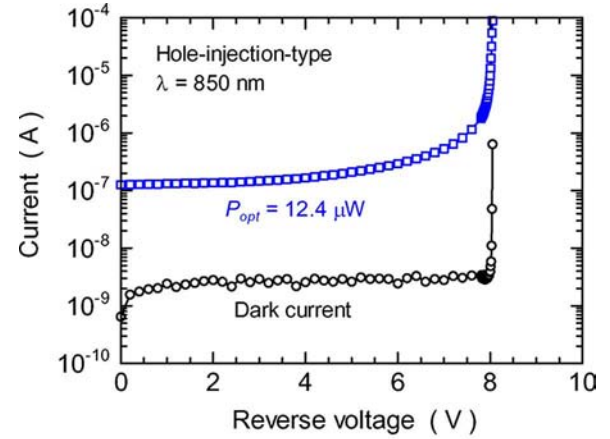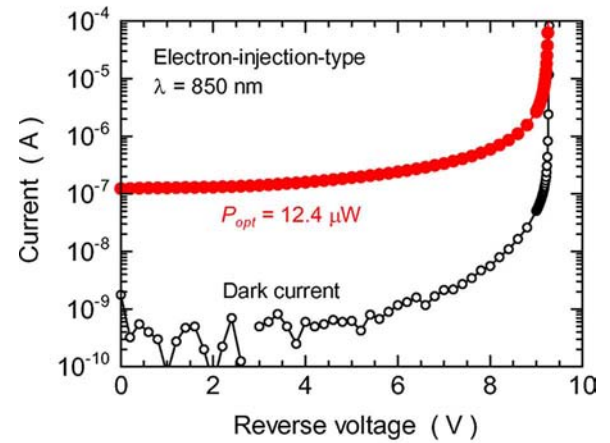
Fig. 2. I–V characteristics of the fabricated APDs. (a) Hole-injection-type APD. (b) Electron-injection-type APD.
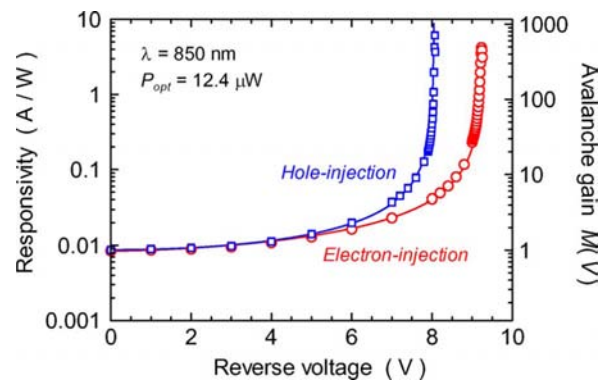

Fig. 3. Measured responsivity of the fabricated APDs at 850-nm wavelength.

electron-injection-type APDs, respectively. The avalanche gain $M(V)$ at the reverse voltage V is calculated from

$$M(V) = \frac{I(V) - I_d(V)}{I(0) - I_d(0)} \tag{1}$$

where $I(V)$ and $I_d(V)$ are the current under illumination and the dark current at the reverse voltage V, and $I(0)$ and $I_d(0)$ are the current under illumination and the dark current
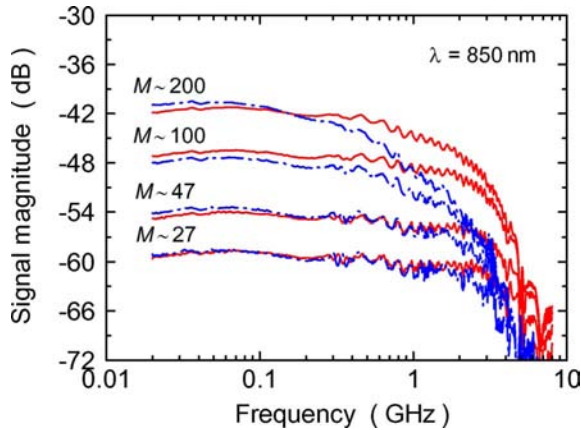
Fig. 4.   Measured frequency response of the fabricated APDs at 850-nm wavelength.

Fig. 5.   Gain-bandwidth characteristics of the fabricated APDs.

at zero reverse voltage. The responsivity in low bias region is 8.5 mA/W, which is lower than that of commercial Si PDs (typically 0.5 A/W at 850-nm wavelength). One reason is that about 30% of the Si surface is covered by the silicides and the electrodes, and the other is due to the cancellation of photogenerated carries generated in the p-substrate. The responsivities are increased with the reverse voltage, and are 4.30 A/W at 8.06 V and 3.52 A/W at 9.22 V for the hole-injection-type and the electron-injection-type APDs, respectively, showing the respective avalanche gain be 493 and 417.

In APDs, the avalanche gain M is well described by the following empirical formula:

$$M = \frac{1}{1 - \left(\frac{V}{V_B}\right)^n} \qquad (2)$$

where V is the reverse voltage, V_B is the breakdown voltage, and n is a constant. The solid lines in Fig. 3 are fitted curves for the measured results with $V_B = 8.05$ V and $n = 2.0$ for the hole-injection-type APD, and $V_B = 9.25$ V and $n = 1.6$ for the electron-injection-type APD.

Fig. 4 shows the measured frequency response of the hole-injection-type APD (the dashed–dotted–dashed lines) and the electron-injection-type APD (the solid lines). For almost the same avalanche gain M, the electron-injection-type APD is faster than the hole-injection-type APD due to faster avalanche buildup time of electrons. The maximum bandwidths are 3.0 and 3.4 GHz for the hole-injection-type and the electron-injection-type APDs, respectively. Fig. 5 is the relationship between the avalanche gain and the 3-dB bandwidth. The horizontal axis is an alternative current (ac) avalanche gain, which was obtained from the increase in the signal magnitude relative to the signal magnitude at 0-V bias around 50 MHz in Fig. 4. The ac avalanche gain is smaller than the avalanche gain M shown in Fig. 3 when the avalanche gain M is approximately $M > 300$ due to nonlinear current change against the illuminated optical power. The gain-bandwidth products are 90 and 180 GHz for the hole-injection-type and the electron-injection-type APDs, respectively.

IV. CONCLUSION

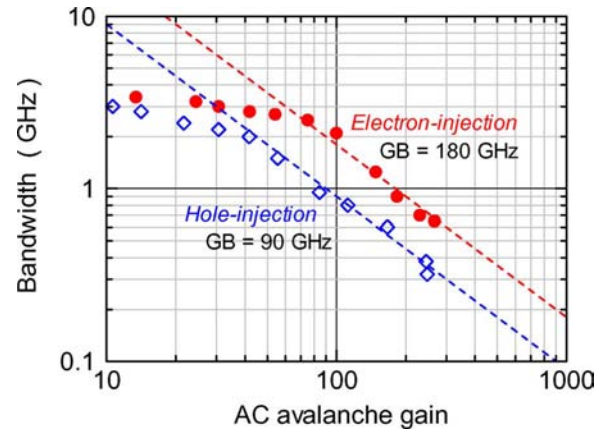A hole-injection-type and an electron-injection-type APDs are fabricated by standard 0.18-μm CMOS process and charac-terized. The avalanche amplification are observed below 10 V of the bias voltage, and the maximum avalanche gain were 493 and 417 for the hole-injection-type and the electron-injection-type APDs, respectively. The maximum bandwidth is 3.4 GHz, and the gain-bandwidth products are 90 and 180 GHz for the hole-injection-type and the electron-injection-type APDs, respectively.

REFERENCES

[1] T. W. Woodward and A. V. Krishnamoorthy, "1 GBit/s CMOS photoreceiver with integrated detector operating at 850 nm," *Electron. Lett.*, vol. 34, no. 12, pp. 1252–1253, Jun. 1998.
[2] M. Jutzi, M. Grözing, E. Gaugler, W. Mazioschek, and M. Berroth, "2-Gb/s CMOS optical integrated receiver with a spatially modu-lated photodetector," *IEEE Photon. Technol. Lett.*, vol. 17, no. 6, pp. 1268–1270, Jun. 2005.
[3] S. M. Csutak, J. D. Schaub, W. E. Wu, R. Shimer, and J. C. Camp-bell, "CMOS-compatible high-speed planer silicon photodiodes fabri-cated on SOI substrates," *IEEE J. Quantum Electron.*, vol. 38, no. 2, pp. 193–196, Feb. 2002.
[4] B. Yang, J. D. Schaub, S. M. Csutak, D. L. Rogers, and J. C. Campbell, "10-Gb/s all-silicon optical receiver," *IEEE Photon. Technol. Lett.*, vol. 15, no. 5, pp. 745–747, May 2003.
[5] W. K. Huang, Y. C. Liu, and Y. M. Hsin, "A high-speed and high-responsivity photodiode in standard CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 19, no. 4, pp. 197–199, Feb. 15, 2007.
[6] K. Iiyama, N. Sannou, and H. Takamatsu, "Silicon lateral avalanche photodiodes fabricated by standard 0.18 μm CMOS process," *IEICE Tran. Electron.*, vol. E91-C, no. 11, pp. 1820–1823, Nov. 2008.
[7] B. Ciftcioglu *et al.*, "3-GHz silicon photodiodes integrated in a 0.18-μm CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 20, no. 24, pp. 2069–2071, Dec. 15, 2008.
[8] K. Iiyama, H. Takamatsu, and T. Maruyama, "Silicon lateral avalanche photodiodes fabricated by standard 0.18 μm CMOS process," in *Proc. 35th Eur. Conf. Optical Communications (ECOC)*, Wien, Austria, Sep. 2009, Paper P2.06.
[9] K. Iiyama, H. Takamatsu, and T. Maruyama, "Silicon lateral avalanche photodiodes fabricated by standard 0.18 μm complementary metal-oxide-semiconductor process," in *Proc. 2009 Int. Conf. Solid State De-vices and Materials (SSDM)*, Sendai, Japan, Oct. 2009, Paper P-7-1.