# A 0.3-V operating, Vth-variation-tolerant SRAM under DVS environment for memory-rich SoC in 90-nm technology era and beyond



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# A 0.3-V Operating, Vth-Variation-Tolerant SRAM under DVS Environment for Memory-Rich SoC in 90-nm Technology Era and Beyond

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**Summary**
We propose a voltage control scheme for 6T SRAM cells that makes a minimum operation voltage down to 0.3 V under DVS environment. A supply voltage to the memory cells and wordline drivers, bitline voltage, and body bias voltage of load pMOSFETs are controlled according to read and write operations, which secures operation margins even at a low operation voltage. A self-aligned timing control with a dummy wordline and its feedback is also introduced to guarantee stable operation in a wide range of the supply voltage. A measurement result of a 64-kb SRAM in a 90-nm process technology shows that a power reduction of 30% can be achieved at 100MHz. In a 65-nm 64-Mb SRAM, a 74% power saving is expected at 1/6 of the maximum operating frequency. The performance penalty by the proposed scheme is less than 1%, and area overhead is 5.6%.

***Key words:*** *SRAM, DVS, Vth-variation-tolerant, low power*

## 1. Introduction

In order to save a power of an SoC, dynamic voltage scaling (DVS) that adaptively controls an operating frequency and supply voltage (Vdd) has been implemented in a mobile system [1]. However, a minimum operation voltage (Vmin) is becoming higher as a fabrication technology is scaled down, since operation margins of memory cells in an embedded SRAM are degraded under both read and write conditions due to threshold-voltage (Vth) variation of MOSFETs. Figure 1 illustrates so-called Pelgrom plots [2], which shows characteristics of standard deviation in 90-nm and 65-nm CMOS process technologies. A standard deviation of Vth ($\sigma_{Vth}$) has been formulated as follows [3].

$$\sigma_{Vth} \propto T_{OX} \cdot \frac{\sqrt[4]{NT \cdot \ln(N/n_i)}}{\sqrt{L_{eff} W_{eff}}}, \quad (1)$$

where $T_{OX}$ is a gate oxide thickness, $N$ is a channel dopant concentration, $T$ is a absolute temperature, $n_i$ is a intrinsic carrier concentration, and $L_{eff}$ and $W_{eff}$ are an effective channel length and width of MOSFETs, respectively. The 65-nm process technology has the smaller slopes in the Pelgrom plots thanks to thinner $T_{OX}$. However, the Vth variation in the 65-nm technology is larger than that in the 90-nm one because of its smaller $L_{eff}W_{eff}$. Since a chip area of 80% or more is supposed to be occupied with memories [4] and unfortunately a Vth deviation is getting larger, Vmin will be restricted by the Vth variation, which hinders wide-range power scaling of a future SoC with DVS capability.

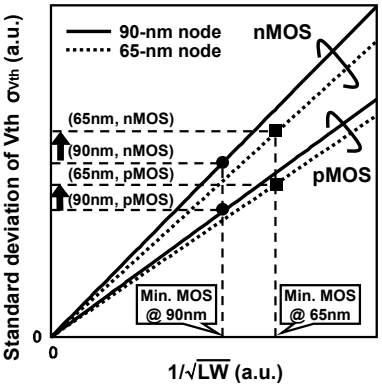


Fig. 1. Pelgrom plots in 90-nm and 65-nm process technologies.

Some techniques have been proposed to improve operation margins of memory cells. One is a power-line-floating in write operation for the conventional 6T memory cells [5], and another is a 7T cell which secures read margin by cutting a loop of a memory-cell flip-flop in read operation [6]. However, these techniques only improve either read or write margin, and thus Vmin is still limited by the other operation. Both read and write margins are

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important. The voltage switching using the dual-Vcc scheme is also proposed for improvement in both read and write margins [7], but it is not sufficient for DVS.

In this paper, we report an optimum voltage control scheme for 6T memory cells that lower Vmin under the DVS environment. This scheme selectively controls voltages in the memory cell to expand the read and write margins. A self-aligned timing control is also developed so as to secure a timing sequence of signals against process, voltage and temperature (PVT) variation.

The rest of this paper is organized as follows. Section 2 introduces the proposed optimum voltage control scheme, and shows the improvement of the operation margins in simulation. The circuit implementation of the proposed scheme and self-aligned timing control are also discussed in Section 2. In Section 3, experimental results of a 64-kb SRAM in a 90-nm CMOS technology are demonstrated, including a measured fail-bit count of memory cells and relationship between power and operating frequency. Simulation results in a case that a memory capacity increases and process technology is scaled down to 65 nm, are also shown in Section 3. Conclusions are given in Section 4.

## 2. Optimum Voltage Control Scheme

### 2.1 Concept

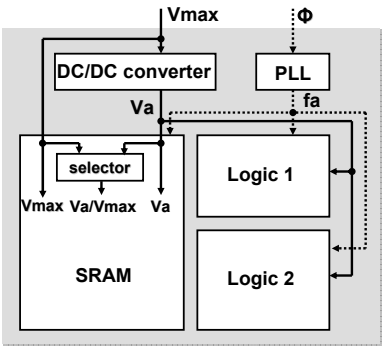


Fig. 2. Block diagram of SoC with DVS.

Under the proposed DVS environment, a high supply voltage (Vmax) is applied externally, and a variable supply voltage (Va) from a DC/DC converter is also provided to logic and SRAM modules in an SoC, as shown in Fig. 2. Va is adaptively controlled, which is between Vmin and Vmax. In this paper, Vmax is set to 1.0 V as a nominal voltage in a 90-nm process technology. In the optimum voltage control scheme proposed, both Va and Vmax are provided to the SRAM, and a supply voltage, wordline (WL) and bitline (BL) voltages of the memory cells are switched according to the read and write conditions in Table 1 and Fig. 3. Figure 3 is schematics of a 6T memory cell, where Vmc, Vwl, and Vbl are a supply voltage, a wordline voltage, and a bitline voltage of a cell under the read and write conditions, respectively, and V1 and V2 are voltages of data-stored nodes.

Table 1. Voltage controls in the conventional and proposed SRAM.

| State / Part | Conv. | Proposed | | |
|---|---|---|---|---|
| | | Read | Write | Non-access |
| Peripheral Vdd | Va | Va | Va | Va |
| BL pre-charge level | Va | Va | Va | Va |
| WL swing | Va | Va | Vmax | - |
| MC Vdd | Va | Vmax | Va | Va |
| MC Vbp | Va | Vmax | Vmax | Vmax |

Vmax: Maximum supply voltage
Va: Variable supply voltage under DVS environment
BL: Bitline
WL: Wordline
MC: Memory cell

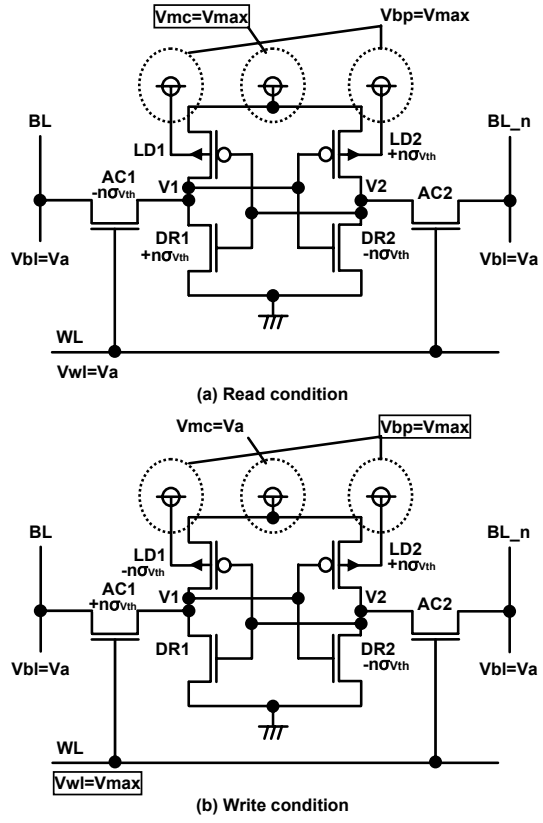


Fig. 3. Schematics of a 6T memory cell, the worst-case conditions of local Vth variations, and voltage controls in the proposed scheme. (a) Read condition, and (b) write condition.

The optimum voltage control scheme improves operation margins in both read and write operations. A supply voltage of memory cells is set to Vmax in the read operation to maximize the read margin. Alternatively in a write cycle, a WL voltage is set to Vmax to obtain the write margin. An n-well bias (Vbp) for load pMOSFETs in the memory cells is tied to Vmax, which increases the

pMOSFET Vth and write margin when Va is less than Vmax. Although the negative Vbp is utilized, a serious problem of a gate-induced drain leakage (GIDL) or negative bias temperature instability (NBTI) does not occur since Vbp does not exceed Vmax. Moreover, this scheme can be implemented with a twin-tub process technology, and soft-error immunity is higher than that in a triple-well technology. The improvement of the operation margins with the proposed voltage control scheme is given in the next subsection.

## 2.2 Improvement of Operation Margins

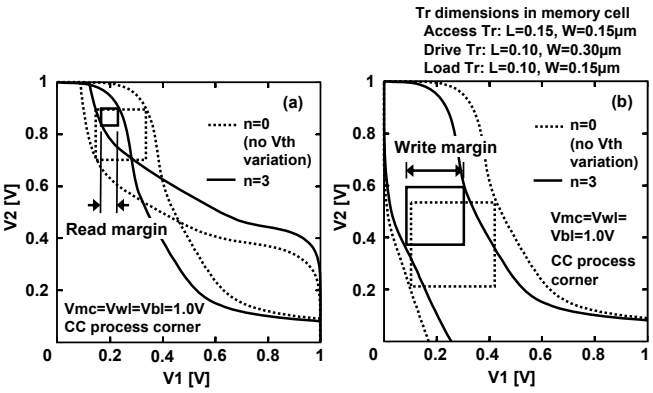


Fig. 4. (a) Read margins and (b) write margins at n=0 (no Vth variation) and n=3.

In order to estimate operation margins at each process corner, the worst case of local Vth variations (random variations) of MOSFETs in a memory cell are set as indicated in Fig. 3. $\sigma_{Vth}$ is a standard deviation of Vth in a MOSFET, but strictly the values are different among process corners, which will be discussed later. n is a coefficient. Four transistors in a memory cell (AC1, DR1, DR2 and LD2 for read; AC1, LD1, DR2 and LD2 for write in Fig. 3) affect operation margins [8][9], and n=3, for example, indicates that a local Vth variation of $6\sigma_{Vth}$ is considered in a memory cell. The read margin is determined by a logical Vth of an inverter in a memory-cell flip-flops (LD2 and DR2), and a voltage of a data-stored node, V1, when "L" is stored in V1 and a WL is activated. The worst case of the local Vth fluctuation for the read margin is that the logical Vth of the inverter is lowest, and that the ratio of the conductances between DR1 and AC1 are smallest. As for the write margin, the logical Vth of an inverter and the voltage of V1 are important, when V1 is already "H" and then "L" is being written. The write margin is getting worse at a lower logical Vth of the inverter and a larger ratio of the conductances between LD1 and AC1. Figure 4 (a) is called a butterfly plot and illustrates a read margin in a memory cell at n=0 (no Vth variations) and n=3. Figure 4 (b) shows a definition of a write margin [10]. The read and write margins worsen if Vth variation occurs, which raises Vmin.

Figure 5 is a so-called milky-way plot of a memory cell, and demonstrates the operation margins at three Vth points (A-C). A diamond illustrated at the center in Fig. 5 shows process corners (FF, FS, SF, SS, and CC). Global Vth variation (wafer-to-wafer / lot-to-lot variation) is reflected to the process corners. The local Vth variation of $6\sigma_{Vth}$ described above is also considered in this figure. Point (A) is out of the read limit, and there is no read margin as shown in the bottom left butterfly curves. Point (A) explains the situation that read margin cannot be obtained and V1 of "L" will not be kept in during a read operation, which is due to the lower logical Vth of the inverter. Similarly Point (B) is out of the write limit and write operation will fail, since the voltage of V1 is much higher than 0 V when "L" is written, which is caused by the larger conductance ratio between LD1 and AC1. Both read and write operations will pass at Point (C) where the logical Vth of the inverter is adequately high and the conductance ratio between LD1 and AC1 is much smaller. In the region between the read and write limit lines, a memory cell properly works.

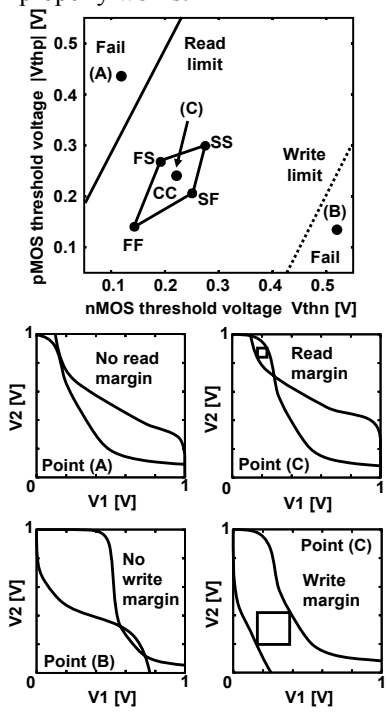


Fig. 5. Milky-way plot of a memory cell when Vdd=1.0 V. At Point (A), there is no read margin while there is at Point (C). Write margin exists at Point (C) while it does not at Point (B).

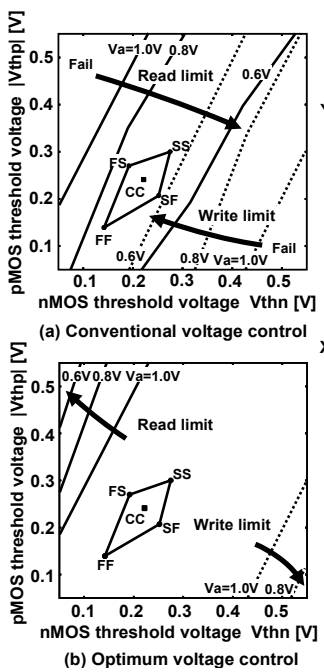


Fig. 6. Milky-way plots of (a) the conventional memory cell, and (b) the proposed one using optimum voltage control scheme.

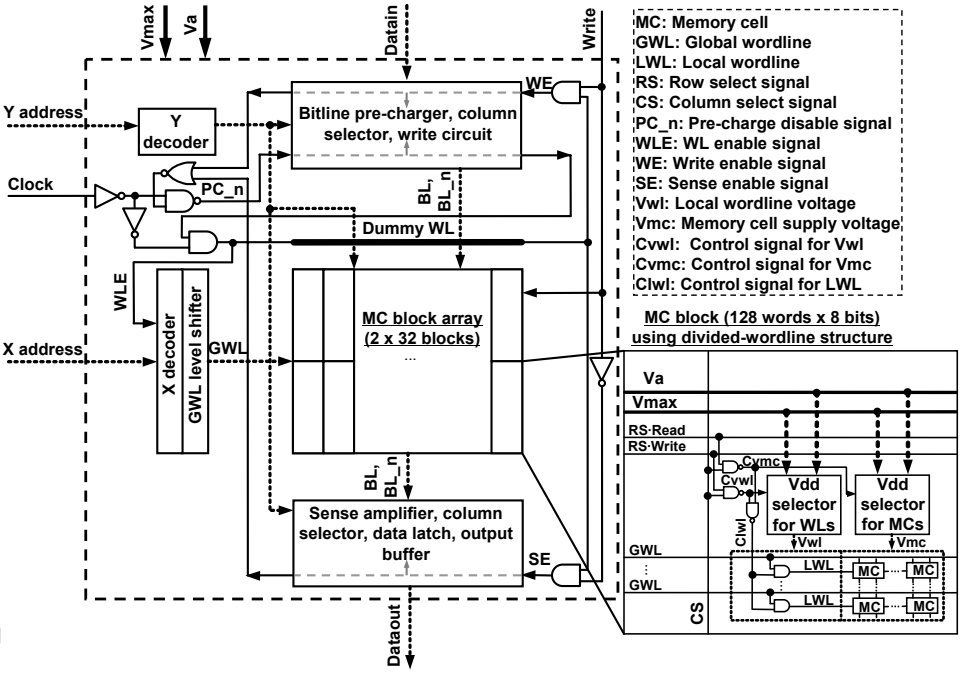


Fig. 7. Block diagram of the proposed 64-kb SRAM with the optimum voltage control scheme. The control signals, WE, SE, and PC_n are input to write circuit, sense amplifier, and bitline pre-charger, respectively. These signals are also utilized as control signals for other logic gates.

Figures 6 (a) and (b) show the detailed milky-way plots in the conventional and proposed optimum voltage control schemes. In the conventional SRAM, the margins become smaller as Va is decreased. In particular at a Va of 0.6 V, there is neither read nor write margin. To the contrary, the proposed scheme ensures sufficient read and write margins even if Va is low, and the margins rather becomes larger as Va is reduced. The expansion of read margin is due to a lower voltage of V1 when V1 is "L". The gate voltages of DR1 and AC1 are Vmax and Va, respectively, hence the conductance ratio between DR1 and AC1 is larger. Similarly in the write operation of "L", the voltage of V1 is sufficiently low since the conductance ratio between LD1 and AC1 is small, which is attributed to the gate voltage of AC1 (Vmax). This is why the write margin is widening when Va is low.

## 2.3 Circuit Design

Figure 7 illustrates a block diagram of the proposed SRAM to which the optimum voltage control scheme is applied. In the proposed SRAM, a memory cell array is divided into 64 blocks so that one block has 128 words by 8 bits, in which the voltage controls are done by a block-by-block basis since Vdd lines in the memory cells are along with bitlines (BLs) [11] unlike the row-by-row Vdd control [12]. Vdd selectors are implemented in order to change the voltages (Vmc and WL voltage). A Vdd selector consists of switches of p-channel MOSFETs, and the total channel width of the pMOSFET switches is set to 20-fold of the total channel width of MOSFETs in a memory cell. This value minimizes the Vdd switching time. If the switch width is small, the Vdd switching time becomes longer. On the other hand, even if the switch width is large, it still takes longer time to drive the gate of the switch.

Level shifters are introduced just after X decoders to amplify the WL voltages to Vmax in a write cycle. The output voltage of the Vdd selector for WLs (Vwl) is provided to an AND gate of GWL and Clwl, which controls local WL (LWL) voltages. Figure 8 demonstrates the read margins in a write cycle when Va is fixed to 0.4 V and a voltage on a WL is varied. The margin could not be obtained if the voltage of WL was Vmax (1.0 V). Again, this means that stored data would be destroyed under the write condition, since stored data in other blocks are destroyed if the conventional single WL scheme is used. Therefore, the divided-WL structure [13] that can hierarchically access to a local WL is applied in the proposed SRAM, in order to make a WL voltage in non-accessed memory cells grounded. Besides, a channel length of access MOSFETs (AC1 and AC2 in Fig. 3) is set

to 0.15 μm, which is longer than the minimum rule of 0.10 μm. This does not only improve the read margin but also reduces a BL leakage current within a marginal delay overhead. The delay overhead is discussed in Section 3.3.

### 2.4 Self-Aligned Timing Control

A proper sequence of the voltage controls is of importance to avoid unexpected flips in memory cells. As pointed out in the previous subsection, when a cycle is changing from a write (or non access) to read operation, a destructive read might occur because a WL voltage gets higher than Vmc. In order to clear this issue, a timing adjustment between the WL voltage and Vmc in Fig. 9 (a) is necessary. Moreover as shown in Fig. 9 (b), another sequence that a WE signal is negated after a WL voltage is grounded, is required as well when a write operation is concluded. Otherwise, the bitline voltages would be floating while the WL voltage is high, and wrong data would be written to memory cells.

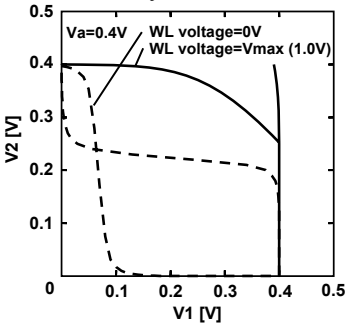


Fig. 8. Butterfly plots at voltage when Va=0.4 V and a WL voltage is varied.

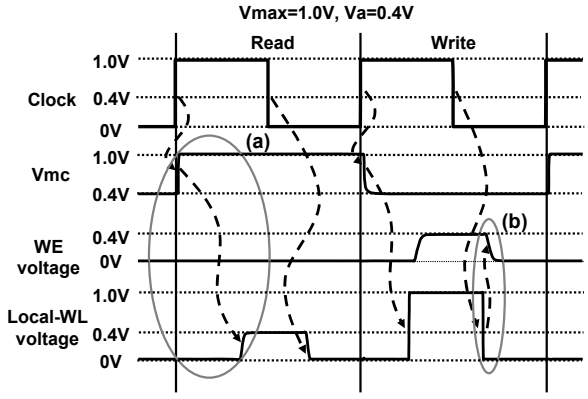


Fig. 9. Timing chart of voltage controls.

In order to secure these sequences, a self-aligned timing control is implemented with a dummy WL and its feedback (see Fig. 7). Cvmc in Fig. 7 is a control signal for memory cell power supply (Vmc), and Vdd selector for memory cells chooses Vmax if Cvmc is grounded. Cvwl means a control signal for a local WL voltage (Vwl), and Vwl is raised to Vmax when Cvwl is pulled down. At the beginning of a read cycle and when a row and a column are selected, a control signal of RS·Read and CS are pulled up and Cvmc is grounded, which results in selecting Vmax for Vmc. Then a local WL (LWL) is pulled up to Va after Cvmc and global WL (GWL) are activated, which secures the timing sequence in Fig. 9 (a). We confirmed that, in a simulation, the time required for the voltage switching is negligible compared to the cycle time because of a small capacitance in a memory-cell block power supply. In contrast, after data are written to cells, clock signal is pulled down and the dummy WL starts falling. A WE signal is deactivated after receiving the feedback signal of the dummy WL. The use of the dummy WL guarantees the timing sequences in Fig. 9 (b) against PVT fluctuation.

## 3. Simulation and Measurement Results

### 3.1 Chip Implementation

A 64-kb SRAM test chip was designed and fabricated in a 90-nm CMOS process technology to verify the feasibility of the proposed scheme. Figure 10 shows a micrograph of the test chip and a layout view of a memory-cell block. The area overhead of the proposed SRAM is 5.6%, which is basically caused by the Vdd selectors and level shifters.

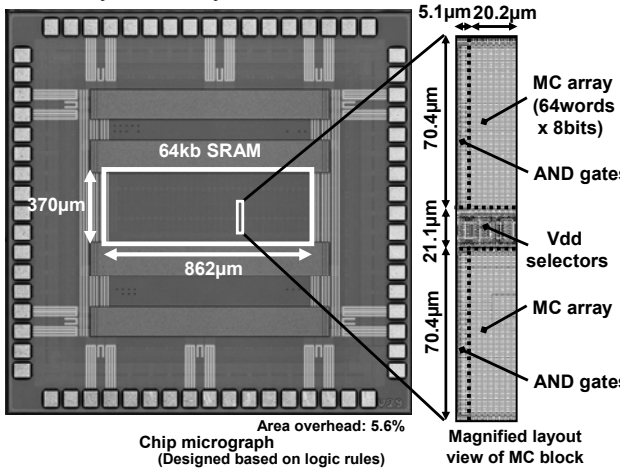


Fig. 10. Chip micrograph and layout view of a memory-cell block.

### 3.2 Fail-Bit Count

Figure 11 (a) demonstrates the proposed scheme improving the operation margins, by means of a measured fail-bit count (FBC) in a read operation. Vmin is limited by read operation in our design, since the process corners

are closer to the read limit curve in the milky-way plot as indicated in Fig. 6 (a). The clock-cycle time in this measurement is as slow as 1 μs in order to evaluate Vmin, which is 0.55 V in the conventional SRAM while that of the proposed one is as low as 0.3 V at the CC process corner. In the conventional scheme, the Vth variation of the memory cells governs Vmin. However in the proposed scheme, the value of 0.3 V means a lower limit of peripheral circuits since the memory cells have a larger margin as Va is decreased as already shown in Fig. 6 (b). In the proposed SRAM, the GWL level shifter does not work below 0.3V.

Note that in the conventional read/write operation, Vmin gets higher at the FS corner as shown in Fig. 11 (b) because the FS corner is closest to the read limit line in the milky-way plot. In addition, a bit error rate in data retention should be considered because the transistor Vth of cross-coupled inverters in a memory cell gets unbalanced as the Vth variation increases. Thus, the stored data cannot be kept even if memory cells are not accessed. The simulated curves in the conventional read/write operation and data retention are obtained as follows:

- Minimum operation voltages of memory cells are estimated with a bit error rate, which is defined as the inverse of the capacity. Coefficient n in Fig. 3 is set to 2.17 for 64-kb, 2.52 for 2-Mb, and 2.83 for 64-Mb SRAMs.

- At FS corner, the read margin is degraded further since $\sigma_{Vth}$ of load pMOSFETs, as expressed in (1), is larger due to a higher channel dopant concentration, *N*. This leads to get a BER-Va curve more gradual and raises Vmin.

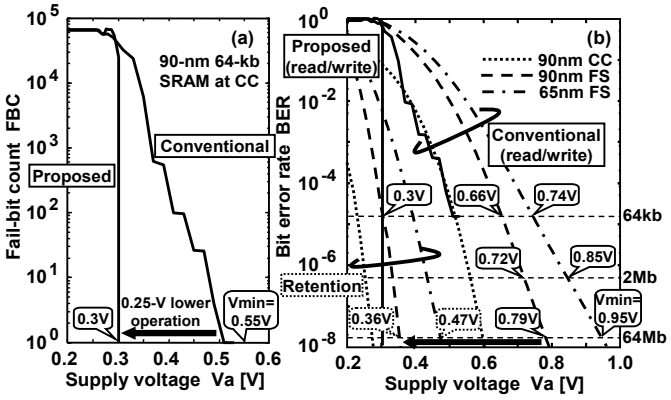


Fig. 11. (a) Measured FBC, and (b) simulated BER when a process corner and memory capacity are varied.

If a memory capacity is assumed to be 64 Mb, the conventional scheme does not work below 0.79 V in a 90-nm process technology, which hinders the DVS advantages. On the contrary, Vmin in the proposed scheme in a 64-Mb SRAM can be down to 0.36 V which is restricted by data-retention characteristics. BER in a 65-nm process technology is also shown in Fig. 11 (b). Since local Vth variation is larger as a process technology is scaled down as illustrated in Fig. 1, Vmin becomes as high as 0.95 V in the conventional 65-nm 64-Mb SRAM, which means that there is just a 0.05-V room to change the supply voltage, and thus DVS never function under that condition.

### 3.3 Power-versus-Frequency Characteristics

Figure 12 (a) shows power dependences on an operating frequency (P-f curves) in the designed 90-nm 64-kb SRAM. Va is implicitly adjusted according to the operating frequency. The performance penalty by applying the proposed scheme is less than 1% when Va is 1.0 V. Va must not be lowered than 0.66 V in the conventional scheme, which results in a higher power at a frequency of less than 300 MHz. The proposed scheme in the measurement allows the lower-voltage operation at the lower frequency, and we confirmed by the measurement that the 100-MHz 0.45-V operation has an advantage of 30% power reduction compared with the conventional scheme. As indicated in Fig. 12 (b), power savings are higher as a memory capacity increases and process technology is scaled down since Vmin in such situation becomes higher. A power saving of 57% in a 90-nm 64-Mb SRAM and 74% in a 65-nm 64-Mb SRAM can be achieved at 1/6 of the maximum operating frequency.

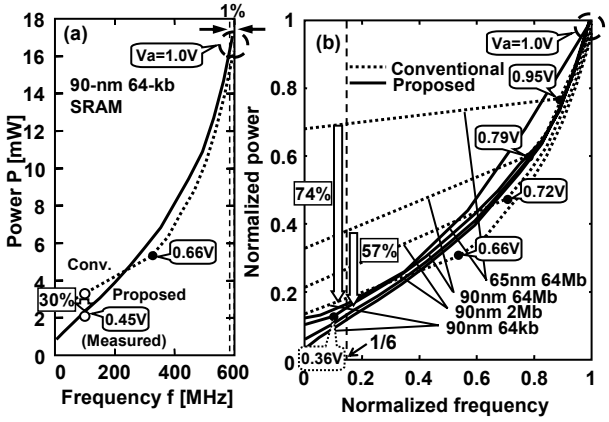


Fig. 12. P-f curves in (a) 90-nm 64-kb SRAM and (b) various capacities and process technologies.

## 4. Summary

This paper presented an optimum voltage control scheme in memory cells and self-aligned timing control method under DVS environment which expands read and write

operation margins and allows an operation at as low as 0.3 V in a 90-nm SRAM. The proposed scheme achieves a power saving of 30% at 100MHz in a 90-nm 64-kb SRAM, and power reduction of 74% at 1/6 of the maximum frequency in a 65-nm 64-Mb SRAM. Since the proposed scheme makes Vmin much lower as memory capacity increases and process technology is scaled down, DVS can be enjoyed even on a future memory-rich SoC.

## Acknowledgments

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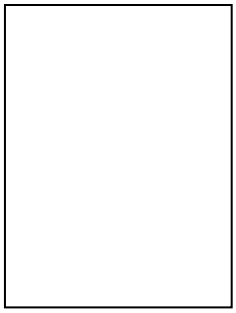
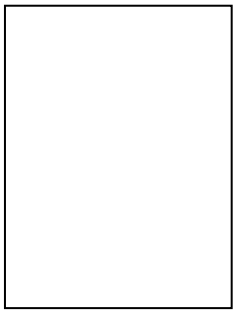


**Yasuhiro Morita** received the M.E. degree in electronics and computer science from Kanazawa University, Ishikawa, Japan, in 2005. He is currently working in the doctoral course at the same university. His current research interests include high-performance and low-power multimedia VLSI designs.
Mr. Morita is a student member of IEEE and the Institute of Electronics, Information and Communication Engineers of Japan.



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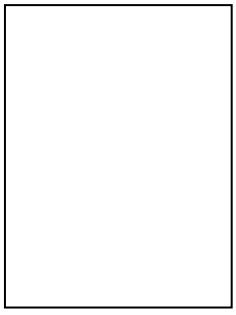
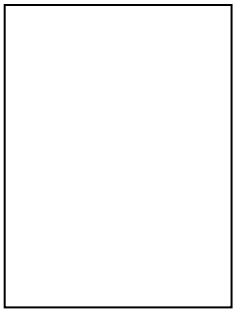
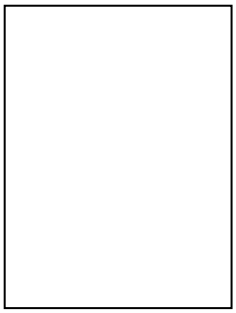


**Hiroki Noguchi** received the B.E. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2006. He is currently working in the M.E. course at the same university. His current research is high-performance and low-power SRAM designs.



**Kentaro Kawakami** received the B.E. degree in electrical and information engineering in 2002 and the M.E. degree in electronic and information system in 2004 from Kanazawa University, Ishikawa, Japan. He transferred his school from Kanazawa University to Kobe University in 2005. He is currently a Ph.D. candidate at Kobe University, Kobe, Japan. His research interests include low power circuits, motion video codec and LSI design methodology.



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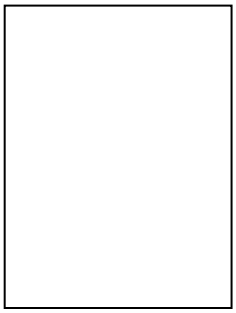

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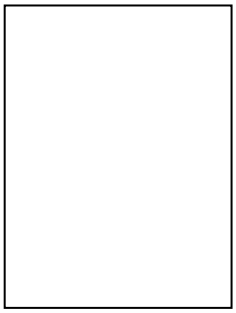

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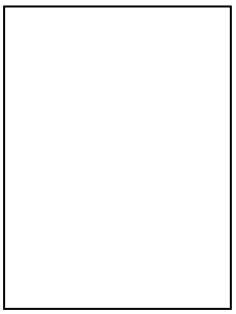

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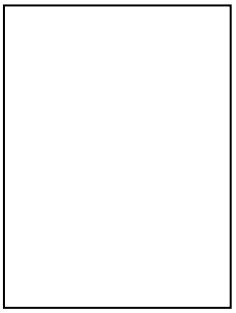
Dr. Kawaguchi is a member of the IEEE and ACM.



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