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Introduction

The effect of leakage current becomes dominant in the standby mode of memory area in Systems on chip (SoC) with rapid development of micro-fabrication technology [1]. The adoption of nonvolatile memories is effective to reduce the power consumption by the leakage current. Especially, PRAM excels other nonvolatile memories in compatibility with a CMOS process, and a simple structure of memory cell [2,3]. PRAM, however, has some demerits of program operation. There are a low speed, large power consumption and limited program cycle to compare SRAM electrical program. Therefore, we propose a novel architecture (Phase Change nonvolatile SRAM: PNSRAM) combining SRAM with PRAM. This architecture is possible solution to reduce the program cycle at the nonvolatile material to be divided a program sequence into volatile and nonvolatile. In this paper, we describe the PNSRAM architecture and a circuit simulation results of the volatile and nonvolatile operation.

Memory Cell Structure and Operation

Fig. 1 shows the proposed PNSRAM cell configuration. The architecture adds two chalcogenide semiconductors (2R) stacked on memory cell and one extra transistor (N_s) to a conventional six-transistor SRAM cell. These resistors are named "reference resistor (R_{ref})" and "memorize resistor (R_m)", respectively. This R_{ref} is set up, so that the resistance takes the intermediate value of a phase change resistance step beforehand. Fig.2 shows a state diagram of chalcogenide semiconductor. The value of '1' and '0' are assigned to the amorphous state and the crystalline state, respectively. These states are switched by applying current pulses. The PNSRAM cell has five operation modes as shown in Fig. 3. When power is restored, Recall operation is automatically carried out [Fig.4]. As the supplied voltage rises, the current flows from PWR line to the SRAM portion in this memory. This amount of the current depends on conductivity of chalcogenide semiconductors. If the R_m is low conductivity, the voltage at the storage node (S_0) rises faster than at the other (S_1). As a result, it recalls the value '1' to the SRAM portion. Fig. 5 shows Initialize operation. This operation must be carried out after Recall operation. Before Initialize operation, the memory cell recalled '1' has the low conductive R_m as a whole. In this memory circuit, transistor N_s is turned on and transistor P_1 is turned off. In this condition, the current path is formed from PWR to STR line by the STR line voltage driven from VDD to V_{init}, and then to VDD. As a result, the R_m is changed to high conductivity. On the other hand, this operation doesn't work to recalled '0' value into SRAM portion. Fig. 6 shows Read operation. Read/Write operation is similar to that in a standard SRAM cell. First, a pair of bitline is precharged. Then, a wordline is selectively driven to VDD, and one of the drive transistors in a memory cell pulls down one of the bitlines. Finally, the different voltage between the bitline pair is read out by the sense amplifier. During Read operation, the influence of additional circuits doesn't exist because the current path doesn't be formed though that node. The write operation is similar to Read operation. Fig. 7 shows Store operation. This operation must be carried out before Standby or power-off operation. During this operation, STR line is driven from VDD to V_{str}, and then to VDD. As a result, the R_m is changed to low conductivity.

Simulation Results and Discussion

The PNSRAM test circuit is designed 2kbit memory size. This cell size is 5.17μm×2.21μm. For the circuit simulation, the dc characteristic of R_m is modeled using Verilog-A and the other circuits are simulated with BSIM MOSFET model. This Verilog-A model parameter for GeSbTe was obtained in Ref. [4]. Also, this model is applicable to other chalcogenide semiconductors. Fig.8 shows the simulation result of Recall operation that is set to R_{ref} at 20kΩ in Fig. 8(a) and R_m at 0Ω (worst case) in Fig. 8(b). The supply voltage is set to 1V to avoid the switching phenomenon. Assuming that the supplied voltage rises from 0V to 1V, it has been confirmed that the stored logic value is properly recalled at the storage node (S_1) as shown in Fig. 8(a). Fig. 8(b) shows the current though R_m is less than the store current, so the Recall operation is undisturbed by the unexpected phase transition of R_m. The read operation is completed with 1.36nsec at supply voltage. And, we give an estimate of 2.56mW for the power consumption per memory cell. Fig. 9 shows the comparison of Standby energy between SRAM and PNSRAM. The Standby energy of PNSRAM has an advantage over that of SRAM at the Standby time of 0.50 second of the same process.

Conclusion

PNSRAM architecture adds nonvolatile to SRAM by incorporating 1T2R. It offers three advantages. The first two are high-speed operation from volatile programming and unlimited nonvolatile program cycle. These advantages stem from the characteristics of SRAM. The third advantage is the reduction of stand-by power consumption of SRAM. The whole operation of PNSRAM designed for CMOS 0.18μm process is confirmed by the circuit simulations with the Verilog-A model of the phase change device.

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[3] M. Takata et al., *IEICE Trans. Elec.. E87C,* 10, pp. 1679-1686, 2004.
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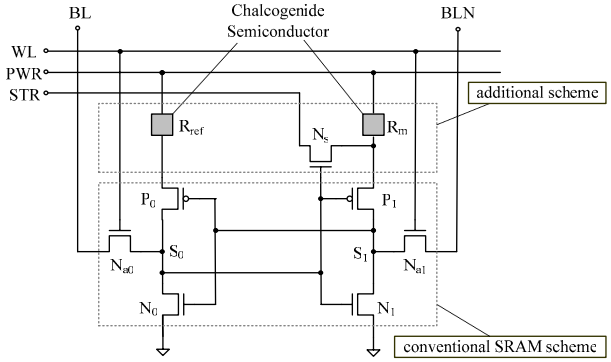

Figure 1. PNSRAM cell configuration.

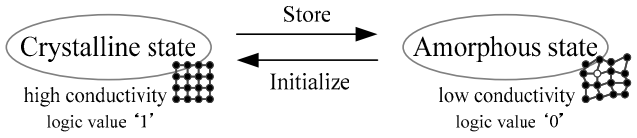

Figure 2. State transition diagram of chalcogenide semiconductor.

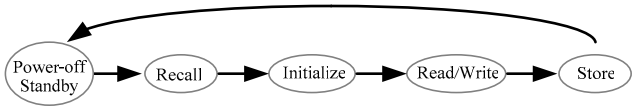

Figure 3. Sequence of the operations.

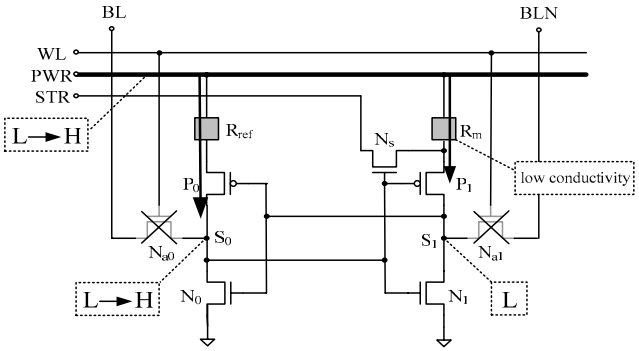

Figure 4. Recall operation.

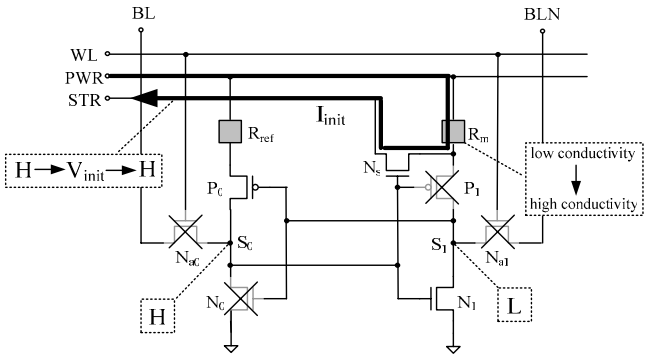

Figure 5. Initialize operation.

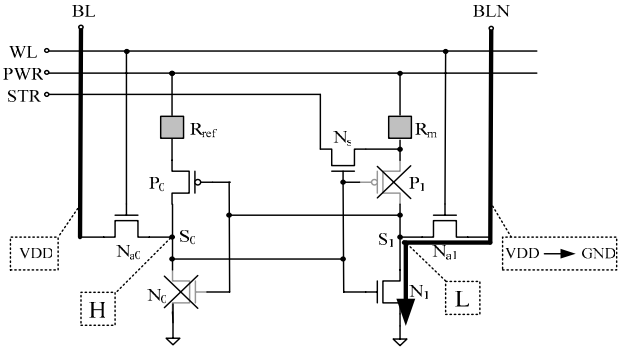

Figure 6. Read operation.

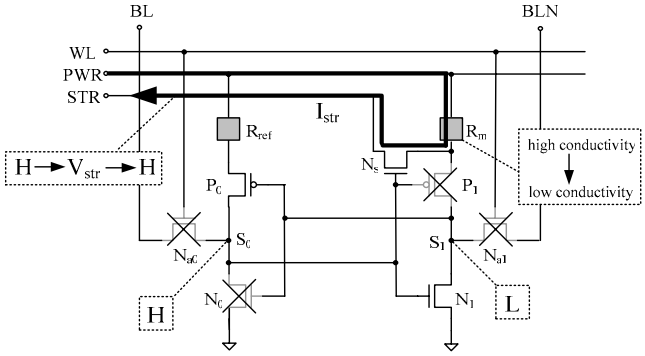

Figure 7. Store operation.

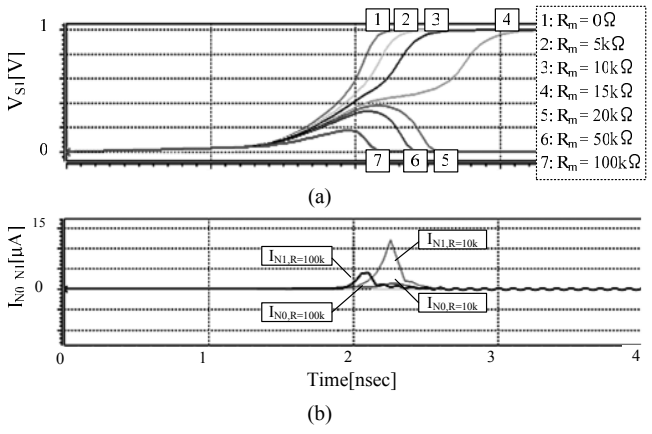

Figure 8. Transient analyses for Recall operation. (a) Voltage of Node S_1. (b) Currents flowing through N_0 and N_1 transistors.

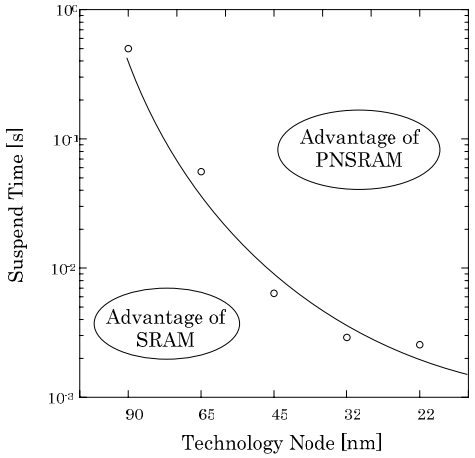

Figure 9. Standby energy comparisons between SRAM and PNSRAM.