特別寄稿

「Semiconductor Technology Roadmaps —Initial Study of An Industry Level MOT Tool—」

Irei Kyu
SanQ

Abstract

The number of transistors in an integrated circuit chip had grown exponentially for more than 40 years according to what is called Moore's Law. In the early 1990's after 25 years of Moore's Law, the Semiconductor Industry Association produced the first of many roadmaps for the semiconductor technology so that the trend could continue. These roadmaps may be viewed as a Management of Technology (MOT) tool that ensured the required technology solutions would be found and developed in time to maintain the trend. This paper reports results of an initial study, using the roadmaps' published documentation, into whether and how the roadmaps impacted the industry. It was found that the roadmaps identified technologies needed over a 15-year range and evaluated potential solutions regarding their readiness. However, the roadmaps were not like MOT tools used in companies because they did not consider market behaviors and did not specify R&D execution plans. They only served as guides for decision-making and objective evaluators of results like the advices from expert consultants.

1 Introduction

Moore's Law

In 1965, Gordon Moore, co-founder of Intel Corporation, who was then director of research and development at Fairchild Semiconductor, wrote in an article[1] in the Electronics magazine, that

> *The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least ten years.*

Complexity, in this case, meant the number of transistors integrated on one integrated circuit (IC) chip. In a paper[2] at the 1975 IEEE International Electron Devices Meeting (IEDM), Moore wrote that the 65,000-fold increase in complexity from the first single transistor planar circuit could be attributed to two main factors: 640-fold from larger chip area and higher density of finer micro-structures, and 100-fold from circuit and device advances that increased density. He thought that the latter contribution was approaching a limit "of another factor of four in component density," and hence increase in complexity would slow down to two-fold every two years. Despite being first to observe the exponential growth in circuit complexity, Moore did not offer a deeper analysis.

Dennard Scaling

Our present day understanding of how IC complexity and performance increase with finer minimum feature size was first explained by Dennard's paper[3] in Oct 1974. In his paper, he gave Table 1. He showed that the circuit density increased by the square of the scaling factor, k, a result that is now known as Dennard's Scaling. In other words, a two-fold increase may be achieved by $k=\sqrt{2}$. In most of the literature today, scaling is expressed as the factor multiplied to minimum feature size, that is, 1/k or approximately 0.7. Thus, Dennard showed quantitatively

how Moore's Law could be achieved, and which properties should be scaled.

Despite Dennard's contribution to our understanding of scaling for performance increase, Moore's Law became the name we associate with semiconductor technology progress. Carver Mead is credited with coining the term "Moore's Law" but the original article where the term was first mentioned had not been located.[4] What is now agreed upon is that Mead's efforts in the early 1970s to promote belief in the long-term growth of IC complexity using Moore's plots, was instrumental in popularizing Moore's Law.

Figure 1 plots the log of the number of transistors in high performance microprocessors against the years they were announced. The straight line shows the 2-fold per 2-year upward trend. In the 1960's the desk calculator market drove demand for one chip processors. The general purpose 4-bit processor Intel 4004 was developed with Japan's Busicom Corporation. In June 1978, Intel announced the 16-bit 8086 and when its variant 8088 was chosen for the first IBM PC, Intel won the war to dominate the microprocessor market. On Oct 17, 1985, Intel introduced the first 32-bit processor of the 80386 range. It had 275,000 transistors at 1.5-μm, and initially operated at 16-MHz clock to achieve 5-MIPS performance. The original Pentium was introduced on Mar 22, 1993, had 3.1-M transistors at 0.8-μm, and operated at 66-MHz to achieve 112-MIPS. A 4-times increase in clock rate was the main contributor to the 7-fold performance increase over the 80386. To satisfy demand for greater processing

Table 1 Dennard Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

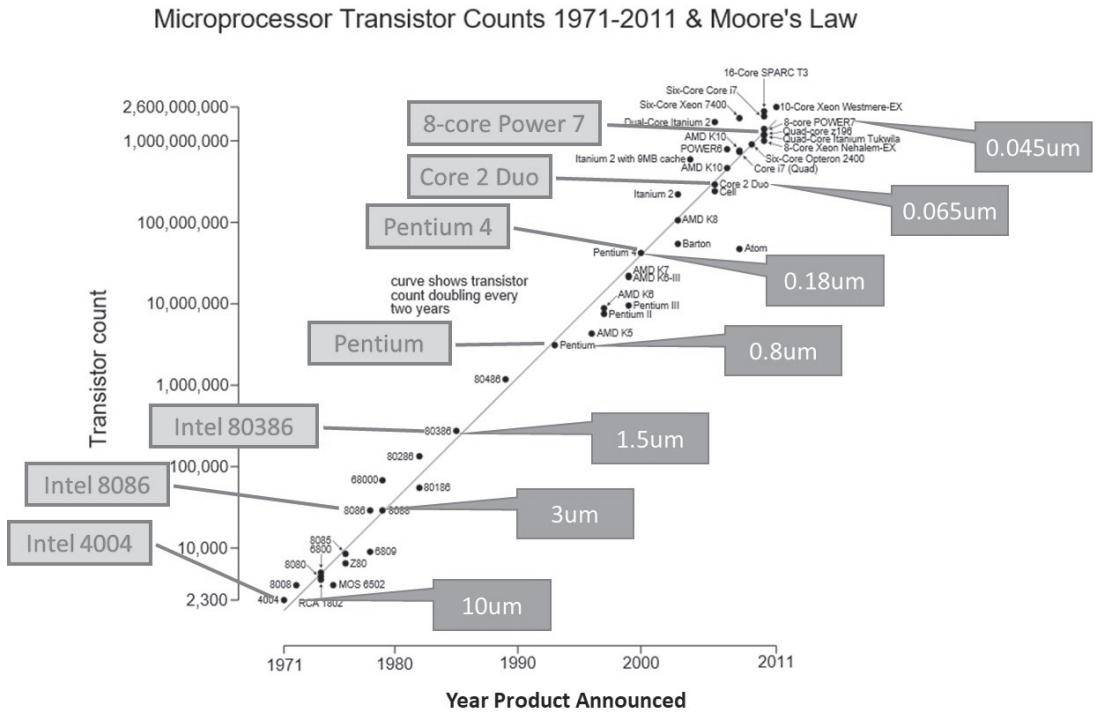


Fig.1 Moore's Law and trend of microprocessor transistor count

power, scaling of the process technology proceeded rapidly for the next few years; 0.35-μm in Mar 1995, 0.25-μm in Jan 1998, 0.18-μm in Oct 1999, 0.13-μm in Jul 2001, 90-nm (140-M transistors) in May 2004, 65-nm in Jan 2006, 45-nm in Nov 2008, 32-nm in Mar 2010, 22-nm in Apr 2012 and 14-nm in Q2 2015, which was equivalent to scaling of about 0.735x (almost doubled transistor count) every 2 years. Today's clock rates are often greater than 3-GHz. Aggressive scaling of process technology (from 10-μm to 14-nm) enabled higher clock rates (from less than 1-MHz to greater than 3-GHz), wider data/instruction buses (from 4-bit to 64-bit) and multi-core technology (from 1 core to more than 20 cores), which together pushed the performance horizon while keeping costs affordable.

Rock's Law

In the early 1970s, when minimum feature size was larger than 3-μm and complexity was below 100,000 transistors, fabrication facilities then were relatively inexpensive. As scaling progressed, control of defects become increasingly important. Expensive clean rooms had to be provided. High precision equipment were needed to control increasingly tight process tolerances. When wiring widths decreased and wiring levels increased, new fabrication methods had to be developed for passive structures. Active devices went through greater changes. The cost of semiconductor fabrication plants doubled every four years, reaching US$14b in 2015, and the phenomenon was given the name Rock's Law or Moore's Second Law. Although Rock's Law never became as well-known as Moore's Law, the exploding costs of fabrication facilities remains roughly true. The high capital expenditures that accompanied each time fabrication process was scaled had to be dealt with by an approach that also took into consideration factory integration.

NTRS, ITRS, and IRDS

How did the semiconductor industry continuously evolve at such a high pace? This paper hypothesizes that technology roadmaps born from cooperation among members of the semiconductor community played a significant role.

In the early 1990's, the semiconductor industry responded to the growing difficulty in sustaining Moore's Law via a concerted effort to keep R&D in all related technologies in pace with the trend. A National Technology Roadmap for Semiconductors (NTRS[5]) was produced in 1994 by the US semiconductor community, and was succeeded by an International Technology for Semiconductors (ITRS[6]) after 1998, and the ITRS was succeeded by the International Roadmap for Devices and Systems (IRDS[7]) after 2015. The NTRS/ITRS/IRDS were the master plans that coordinated technology R&D in critical technology sectors. For this paper, the common term "ST-Roadmaps" will be used to refer to them.

Whether the ST-Roadmaps had any impact on semiconductor technology and business had not been well studied. No one can deny that technology has advanced tremendously. The world semiconductor market in value has grown respectably but not as much as may be expected from the number of electronic devices nor the global impact on how people work, communicate and spend their free time. It is important to clarify for the sake of similar future efforts not only whether but how the ST-Roadmaps contributed to the semiconductor industry's growth.

This paper reports on an initial study of the ST-Roadmaps to understand their role as a Management of Technology (MOT) tool at the industry level. Existing literature that examined the ST-Roadmaps mostly discussed technical details. Schaller 2004[8], looked at the ST-Roadmaps as "organized innovation" and their impact on semiconductor technology from a theoretical perspective, but he did not examine the separation of roadmapping from innovation execution, and the total absence of market considerations in the ST-Roadmaps, that this author believes are central issues.

In this study, the author examined the history and features of the ST-Roadmaps from the published 2-yearly revision reports. Technical details are avoided as much as possible. The roles of the ST-Roadmaps as a MOT tool are analyzed against the background of the semiconductor business. A case study on the DRAM roadmap is used to provide a clearer picture of the dynamics in the roadmapping process. The ST-Roadmaps' effectiveness is also examined qualitatively, and observations are noted based on the author's experience in semiconductor research. Finally, the special nature of ST-Roadmaps as a

tool for MOT at the industry level is discussed.

Paper sections

Section 2 examines the objectives of the NTRS in the initial years, and features of the roadmap that were central to its effectiveness. Section 3 reviews in a case study the DRAM cell-size roadmap revisions as scaling approached physical limits. Various evolutionary changes of the ST-Roadmaps in response to market changes are also examined. Section 4 summarizes the main successes and pitfalls, and finally Section 5 discusses MOT tool features of the ST-Roadmaps and concludes.

2 NTRS, ITRS and IRDS

Historical background

In 1982, the US Semiconductor Industry Association (SIA) incorporated the Semiconductor Research Corporation (SRC) in a cooperative research effort to stop and reverse the loss of US technological leadership in semiconductors because company-level research duplication had become unsustainable. The main rival country then was Japan, which had surged forward through its successful 5-year research cooperation since 1975 under the R&D Consortium for VLSI, especially in larger wafers and manufacturing equipment for high quality control. SRC saw its mission as follows.

> *The SRC executes its mission by funding graduate-level research at North American universities. SEMATECH was formed in 1987 to address improvements in domestic manufacturing technology by funding the supplier industry to improve the quality and capabilities of their manufacturing equipment. In addition to the SRC and SEMATECH, the semiconductor industry, U.S. universities, government agencies, and federal and national laboratories all participate in finding solutions to semiconductor technology needs.*

In the mid-1980s Japan overtook the US in market share of semiconductors. To counter foreign rivalry, SIA believed research funding needed better focus. In 1992, the first semiconductor technology roadmap was prepared. In the words from the 1994 NTRS report's foreword:

> *The complexity of semiconductor technology is increasing at such a rapid pace that there is significant danger the U.S. industry will not be able to continue its historical rate of progress without a common vision and increased cooperation in precompetitive research and development. To meet this challenge, the first semiconductor technology roadmap was prepared under the sponsorship of the Semiconductor Industry Association (SIA) by the semiconductor community in 1992 and distributed in 1993 in two documents ... Broad acceptance of the Roadmap has rapidly materialized ... The success of these reports emphasized the need for continued renewal of a national roadmap for semiconductor technology.*

"..." is inserted in the above quote in place of omitted text.

From the experience of the first roadmap, SIA believed that

> *The roadmap creation process enables a common vision among industry, academia, and government. This vision must be nurtured to allow progression from academic research through manufacturing of commercial products. The Roadmap also provides a framework for guiding R&D; all relevant segments of the national R&D base can be efficiently enlisted to meet the increasingly complex technology needs of the semiconductor industry.*

The 1994 NTRS report was followed by the 1997 NTRS report. In April 1998, realizing that inputs from leading researchers around the world could provide better guidance for the industry, SIA extended an invitation to Europe, Korea, Japan and Taiwan to collaborate in producing an ITRS, and the NTRS was discontinued. The first output was the ITRS 1998 Update. Subsequently, a comprehensive revision was produced every other year from 1999 and a minor update of tables in between, till 2015 when the ITRS was discontinued. The International Roadmap for Devices and Systems (IRDS) was started as ITRS 2, with a revamped agenda, and the first report was completed in 2017 after 2 years of discussions.

Roadmap Purpose and Deliverables

By the beginning of the 1990s, semiconductor technology had stayed on the trend predicted by Moore's Law for 25 years. Intel was about to introduce the original Pentium that contained more than 3-M transistors in 0.8-μm process. Talk had begun about the looming fundamental limits to scaling and, though answers were not available yet, questions were articulated. The previous 25 years, in comparison, probably seemed like a road with few bumps. Faced with many uncertainties, the purpose of the roadmap was to determine what relevant questions must be asked and by when they must be answered to maintain complexity growth at the rate of Moore's Law.

According to the 1994 NTRS report, the roadmap provided a quality database of needs or requirements on technology and a framework by which the semiconductor community could systematically approach the enormous R&D tasks to meet these needs. The roadmap defined these needs by establishing a top-down hierarchy of technological requirements. The Overall Roadmap Technology Characteristics (ORTC) summarized the top level of needs. Lower level technology roadmaps prepared by Technology Work Groups (TWGs) broke down ORTC needs into greater detail specific to each technology area. For the 1994 roadmap, each TWG was responsible for also defining the needs of its area for crosscut technologies that overlapped many TWGs. These "needs" were the roadmap deliverables.

Roadmap Coordinating Group Organization Structure

For the 1994 NTRC, technology requirements were divided into eight groups. Each group was assigned a TWG comprising top experts in the respective technology area. A Roadmap Coordinating Group (RCG) headed the organization. The TWGs for fabrication processes, in the order semiconductors were fabricated, were 1) Materials and Bulk Processes, 2) Process Integration, Devices, and Structures (PIDS), and 3) Interconnect. 4) Lithography concerned technologies for patterning. Non-fabrication technologies included 5) Design and Test (from circuits to systems), 6) Assembly and Packaging, 7) Factory Integration, and 8) Environment, Safety, and Health (ESH).

When the NTRS effort was extended to four other regions, Japan, Korea, Taiwan and Europe, and became ITRS, in addition to TWGs, International Technology Work Groups (ITWGs) were formed, which consisted of eight Focus ITWGs and four Crosscut ITWGs. Members of ITWGs were representatives from regional TWGs. Each ITWG received inputs from TWGs for the Roadmap revision. In addition, each TWG organized "sub-TWG meetings" and public "Roadmap Workshops" in an attempt to build the widest possible consensus among the global semiconductor community.

Approach

Each roadmap revision covered a range of 15 years from the year of publication, equivalent to 5 generations of 3-yearly technology evolutions, and in terms of technology maturity extended from mass production level in the near term to exploratory research level in the far term. Each generation is referred to by its technology node, or minimum feature size expressed in micrometers (μm) or nanometers (nm), and is roughly equivalent to a major change of fabrication process, machinery and factory facilities.

Figure 2 is a conceptual illustration of the division of labor and funding over five generations of evolution. It is observed that the time range of 15 years was probably chosen not randomly but long enough so that the technologies required near the far end would have no known solutions at the start. For this approach to be possible, two conditions must be satisfied. Firstly, requirement projections must be fairly accurate, and secondly, the limit of existing solutions must be predictable. Dennard's Scaling allowed satisfaction of both conditions. For the first condition, if the same pace of scaling was kept, a simple formula predicted minimum dimensions and in turn other physical properties. The second condition was satisfied by state-of-art knowledge in science and engineering since the effects of scaling, the only variable, were relatively well understood. For this strategy of scaling to be successful, it can be observed from hindsight that the demand for better performance must remain strong, and that disruptive innovations do catch up. More on these observations will be left to the discussion section.

In the 1994 NTRS, it was written that "The Roadmap

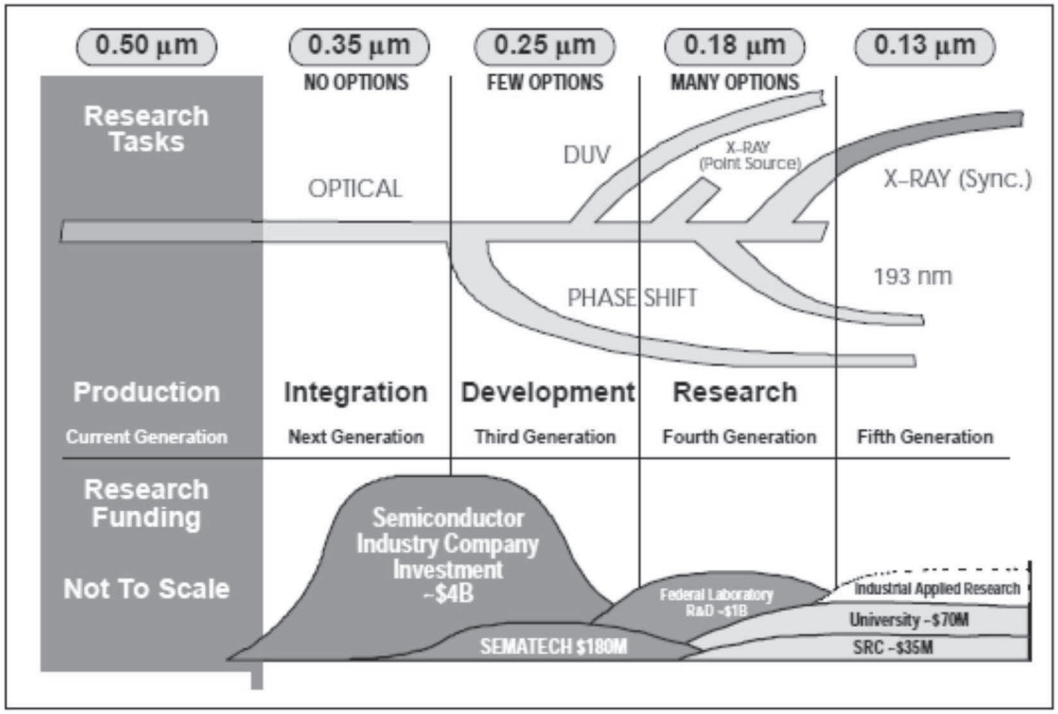


Fig.2 Conceptual Illustration of R&D Investment vs Technology Evolution, for the case of Lithography[5]

is analogous to paved roads of proven technology, unimproved roads of alternative technologies, footpaths towards new technologies, and innovative trails yet to be blazed." The first two of the five generations over the 15-year time range were the "paved roads" that had mostly well understood needs. The focus was on qualification, a technical jargon that means statistically testing fabrication machineries, processes, design tools, test protocols, and all other components of the mass manufacturing system so as to remove potential problems and to ensure production control for high yield. For these two generations, the ST-Roadmaps provided definitive information on what the industry needed to achieve, and it was expected that companies would undertake and fund their separate R&D programs.

The subsequent two generations, third and fourth, were the "unimproved roads or footpaths", for which alternative technologies had been discovered but required feasibility studies to show proof of concept on critical yet unproven elements before large investments were made in any one alternative. The primary activity expected was directed research for the third generation and conceptual research for the fourth. All sectors of the semiconductor R&D community would participate in and provide funding for research into these technologies.

The fifth generation and beyond would have many technology requirements that had no known solutions and awaited "trails to be blazed" where no paved roads and only few footpaths existed. A number of significant barriers to extension of current technology existed. R&D was expected to be dominated by activities to find new knowledge and generate new concepts including paradigm shifts. Funding and research leadership would be mainly from the non-industrial community such as universities, government laboratories and industry consortia.

Another equally important aim of this approach was to maintain good balance between resources allocated to the different needs of succeeding generations of technology, so that a continuous stream of new innovations could be born and nurtured in time to address the challenging requirements of the future.

Roadmap features

During the initial years of NTRS, extending the bit count of Dynamic Random Access Memory (DRAM) by a factor of four every 3 years was set as the target rate of technology advance, slower than the rate of Moore's 1965 paper but faster than the rate of Moore's 1975 paper. The choice of DRAM as pace-setter was probably decided by two considerations, 1) less system changes were expected so comparison between generations was straightforward, and 2) DRAM was expected to lead the need for scaling. It would be fairly accurate to take the

Table 2 System Drivers subset of ORTC

Year of First DRAM Shipment / *Minimum Feature Size (μm)*	*1995* / *0.35*	*1998* / *0.25*	*2001* / *0.18*	*2004* / *0.13*	*2007* / *0.10*	*2010* / *0.07*	*Driver*
Memory							D
Bits/Chip (DRAM/Flash)	64M	256M	1G	4G	16G	64G	
Cost/Bit @volume (millicents)	0.017	0.007	0.003	0.001	0.0005	0.0002	
Logic (High-Volume: Microprocessor)							L (μP)
Logic Transistors/cm^2 (packed)	4M	7M	13M	25M	50M	90M	
Bits/cm^2 (cache SRAM)	2M	6M	20M	50M	100M	300M	
Cost/Transistor @volume (millicents)	1	0.5	0.2	0.1	0.05	0.02	
Logic (Low-Volume: ASIC)							L (A)
Transistors/cm^2 (auto layout)	2M	4M	7M	12M	25M	40M	
Non-recurring engineering cost/transistor (millicents)	0.3	0.1	0.05	0.03	0.02	0.01	

view that the roadmaps of main technology requirements were aligned to the DRAM roadmap. The Overall Roadmap Technology Characteristics (ORTC) is a table of quantitative milestones that summarized the main technology requirement targets over 15 years into the future. *Table 2* is a subset giving only the bit-count or transistor density targets for the three main product classes: memory, microprocessor and ASIC (Application Specific Integrated Circuit). Most of the other main technology requirements are features that affected performance such as number of chip I/Os, chip frequency, maximum number of wiring levels, maximum power, and power supply voltage, features that affected yield such as electrical defect density and features that affected costs such as minimum mask count, maximum wafer diameter, chip size, and design and test.

Each main technology requirement had one or more associated quantitative properties that could be used to gauge technological difficulty. For example, higher chip frequency is more difficult to achieve than lower frequency. Power supply voltage poses increasing difficulty if it is lowered. New solutions in circuit design had greatly increased the former, whereas the latter required fundamental changes to transistor design that reduced leakage current. In these examples, the difficulties can be assessed quantitatively, for example, using simulation in the case of circuit design, and using statistical data in the case of transistor properties.

It is interesting that CMOS was chosen as the only process to be considered, because in the early 1990's it was still common wisdom to use other processes for higher speed, better noise performance, radio frequency circuits and other applications. The rationale given was "The primary focus of this Roadmap is on technology required for silicon CMOS integrated circuits. These products constitute over 75% of the world semiconductor market and therefore determine mainstream technology. This mainstream provides the primary advancements for other semiconductor products, such as compound semiconductor, microwave, and linear devices. Therefore, the Roadmap serves as a technology guide for all semiconductor products." The wisdom of choosing CMOS was proven in later years when integration of complex digital circuits with analog/RF circuits on one CMOS chip resulted in smaller footprints, and CMOS eventually overtook in performance because other processes could not follow the same pace of scaling. It was a lucky choice that CMOS had a long scaling life.

〈Redbrick Wall〉

The target technology requirements at technology node years or each year were tabulated, and their readiness grouped under 3 categories indicated by colors, white if manufacturable solutions existed and were being optimized, yellow if manufacturable solutions were known, and red if manufacturable solutions were still unknown. The red boxes in a table were trend-stopping obstacles and came to be called the redbrick wall. The wall of yellow boxes was not similarly called perhaps because solutions were known and needed only proof at high volume production. Table 3 shows an example from the DRAM technology requirements of the PIDS section

Table 3 DRAM Technology Requirements in the 2001 ITRS

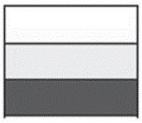
DRAM Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM 1/2 Pitch (nm)[1]	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
DRAM cell size (μm^2) [2]	0.135	0.106	0.060	0.049	0.038	0.029	0.025
DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	2.04	1.80	1.20	1.00	0.45	0.32	0.22
DRAM retention time (ms) [4]	64	64	64	64	64	64	64
DRAM soft error rate (fits) [5]	1000	1000	1000	1000	1000	1000	1000

DRAM Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (nm) [1]	45	32	22
MPU / ASIC ½ PITCH (nm)	50	35	25
MPU PRINTED GATE LENGTH (nm)	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	18	13	9
DRAM cell size (μm^2) [2]	0.0122	0.0041	0.0019
DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	0.084	0.028	0.010
DRAM retention time (ms) [4]	64	64	64
DRAM soft error rate (fits) [5]	1000	1000	1000

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known



of the 2001 ITRS. Looking at the roadmap for DRAM cell size requirement, the redbrick wall where no solution existed then was still 12 years in the future. It is no coincidence that the readiness grouping corresponds to the "paved roads", "footpaths" and "trails to be blazed" classification in the description of approach.

〈Gaps in R&D Effort〉

The Technology Work Groups (TWGs) for the 1992 Roadmap (pre-NTRS) brought up the question of technologies common to several TWGs or needing coordination between different TWGs. These so-called cross-cut technologies were Contamination-free Manufacturing, Sensors, Software, Materials, Metrology, Modeling, Standards, and Quality and Reliability. Each of these had no corresponding department-in-charge in industry then, so the initial Roadmap organization had no TWG assigned to them. As a result, it was noted in the 1994 NTRS, these technologies had no management direction nor budget, or the person-in-charge had no coordination responsibility. For the 1994 NTRS, the TWGs were charged to identify cross-cut technology needs related to their respective fields. Among the original cross-cut technologies identified in 1992, Sensors became part of Metrology, and Software became part of Modeling. Standards was added as the 6th field. From the 2001 ITRS, they were further reorganized into 3 fields: Yield Enhancement, Metrology, and Modeling and Simulation. Environment, Safety and Health became the 4th field. Each of these cross-cut technology fields was assigned a TWG at the regional level and an ITWG at the international level.

The difference in importance that researchers and management initially attached to cross-cut technologies highlights the dynamics of the roadmap creation process. Bottom-up concerns for these non-traditional fields were raised and heeded by the NTRS management, resulting in the formation of additional TWGs and ITWGs. In a factory, provision of these technologies tended to be assigned to support-service personnel or a secondary responsibility of researchers and designers. By 1992, they had become as important as focus technology fields

as a result of advances in software tools, metrology, greater demand for quality control, and higher awareness for protecting the environment and workers. The lesson to be learned is the importance for MOT managers to be sensitive and flexible also to trends of supporting technologies.

〈Market Drivers〉

Markets needs were reflected in the identified market drivers and their impact on system drivers. In the 1994 NTRS, only system drivers were differentiated: memory, microprocessor and ASIC. Under the topic of Assembly and Packaging, because packaging requirements differed, 5 market application segments were differentiated: commodity, hand-held, cost/performance, high-performance, and automotive. From the 2001 ITRS, market drivers were differentiated for all technology requirements, according to application markets (portable and wireless, broadband, internet switching, mass storage, consumer, computer, and automotive). In the 2005 ITRS, they were regrouped into 6 application markets (portable/consumer, medical, networking and communications, defense, office, and automotive) to align with the International Electronics Manufacturing Initiative (iNEMI) roadmap. The stated motivation was "introduction of new technology solutions is increasingly application-driven with products for different markets making use of different combinations of technologies at different times." It should be noted that the push for product differentiation came from market demand for products in new applications, reflecting the industry's evolution as market volume grew, not the result of innovation inspired by ITRS.

Another result of market evolution was the replacement of the system driver category ASIC by ASIC/SoC in the 2001 ITRS and by SoC that included ASIC as one sub-category again in the 2003 ITRS. "SoC" is the abbreviation for System on Chip. It was noted in the 2001 ITRS that logic densities of ASIC had caught up with MPU, custom high-performance ASIC were increasingly using tunable standard-cell methodologies that exceled in implementation productivity at competitive manufacturing cost, and integration of non-CMOS components was growing in demand. Whereas ASIC is a logic circuit that is custom-built for better performance than the programmable MPU, SoC is a hybrid integration of processor, custom logic, analog and other components, and hence, SoC requires a much more complex fabrication process.

〈Funding〉

Optimization of funding is a key motivation of the ST-Roadmaps. Two contributions to fund saving were highlighted: reduction of duplicate work and reduction of false leads.

The Roadmap provides a framework that can enhance collaboration, increase shared knowledge, and minimize duplication of efforts. The TWGs can assist in these collaborations and can help deduce common elements of programs that can be shared. For example, researchers could develop a common stage for lithography exposure tools for use with several light (or energy) sources. In this way, the Roadmap provides an opportunity to conserve research funds.

Early focus on critical elements of innovative approaches provides additional opportunities to conserve funds. By identifying and focusing early R&D on unproven elements of a given approach, the semiconductor community can often avoid the significant expense of attempting to commercialize approaches that cannot work. The TWGs are chartered to consult with researchers at their request to identify key concepts that need to be proven before considering a proposed solution for commercialization.

It was also a concern that "certain technology developments, even though critical to maintaining productivity, cannot be adequately funded solely through the commercial sales of products embodying that technology." Examples included lithography equipment, and tools for computer-aided design, inspection, metrology, etc.

In the ST-Roadmaps documentation, however, specific funding programs were either not documented or left out of the roadmap formulating process. One of the reasons may be the stated policy not to specify preferred technology solutions so as not to bias the search for solutions. Probably for the same reason, research programs were left to industry, academia and government labora-

tories. The ST-Roadmaps' impact was not reduced by leaving out information about funding. Studies on the question of impact on research funding on the semiconductor industry will have to look for evidence elsewhere.

3 DRAM cell size roadmap case study and Roadmap evolution history

〈Case Study: Tuning the roadmap〉

The pace set by Moore's Law is undoubtedly extremely fast. Technology became outdated rapidly. Even experts found it challenging to predict with accuracy how quickly advances could be made and the ST-Roadmaps' milestones had to be revised.

Using DRAM cell size as an example, in 2001 the redbrick wall was a comfortable 12-year distance away. The closest yellow box was two years away. In 2003, the closest yellow box and redbrick wall had not retreated and milestones were reset to a slower pace. In 2005, mile-

Table 4 Milestones for DRAM cell size from 2001 to 2017

Year	ITRS'01	ITRS'03	ITRS'05	ITRS'07	ITRS'09	ITRS'11	ITRS'13	IRDS'17
2001	0.135							
2002	0.106							
2003	0.060	0.082						
2004	0.049	0.065						
2005	0.038	0.048	0.0514					
2006	0.029	0.036	0.0408					
2007	0.025	0.028	0.0324	0.0277				
2008		0.019	0.0193	0.0202				
2009		0.015	0.0153	0.015	0.01500			
2010	0.0122	0.0122	0.0122	0.0122	0.01162			
2011			0.0096	0.0096	0.00640	0.00778		
2012		0.0077	0.0077	0.0078	0.00518	0.00577		
2013	0.0041	0.0061	0.0061	0.0061	0.00384	0.00314	0.00470	
2014			0.0048	0.0054	0.00310	0.00250	0.00406	
2015		0.0038	0.0038	0.0038	0.00230	0.00194	0.00346	
2016	0.0019		0.0030	0.0029	0.00176	0.00160	0.00194	
2017		0.0025	0.0024	0.0024	0.00130	0.00130	0.00160	0.00265
2018			0.0019	0.0019	0.00102	0.00102	0.00130	
2019		0.0016	0.0015	0.00154	0.00078	0.00078	0.00116	0.00194
2020			0.0012	0.00118	0.00068	0.00068	0.00090	
2021				0.00101	0.00058	0.00058	0.00078	0.00116
2022				0.00086	0.00040	0.00048	0.00068	
2023					0.00032	0.00040	0.00058	
2024					0.00026	0.00032	0.00048	0.00078
2025						0.00020	0.00040	
2026						0.00014	0.00034	
2027							0.00028	0.00048
2028							0.00024	
2029								
2030								0.00028
2031								
2032								
2033								0.00024

Yellow box

Redbrick Wall

stones were slowed down further. In 2007, a major breakthrough pushed the closest yellow box six years away and the redbrick wall was estimated to be 11 years away. In 2007 and 2009 consecutively, milestones were again revised to increase pace. Contrary to expectation, the milestones were again overly ambitious and pace had to slow down since 2011. Nevertheless, it is worthwhile to note that the redbrick wall in the 2001 roadmap had a known solution by 2007 and was cleared by 2013, after 12 years, leaving only the issue of optimizing mass production solutions. In contrast, the redbrick wall in the 2017 IRDS was only four years in the future at the same pace. The trend of Moore's Law finally had to slow down.

In the above example of a breakthrough, it took 12 years to find a solution and develop the technology for mass production. The breakthrough was achieved by a radical change of the transistor structure. Because it was known in 2001 that scaling alone would not provide a solution 12 years later, research started early to find alternative solutions. In this case, researchers succeeded barely in time. The roadmap served not only as a pacemaker, but also to identify the limits of existing approaches to advance technology.

〈More-than-Moore〉

The looming end of Moore's Law was mentioned in the 2003 ITRS and a framework for discussion in depth was proposed in the 2005 ITRS. The framework, shown in the following figure, envisaged progress along two different axes. The "More Moore" axis was defined in the 2007 ITRS Roadmap Technology Characteristics Terminology, as having two components, which were, Geometric Scaling that continuously shrank horizontal and vertical feature sizes for greater density and performance, and Equivalent Scaling that included 3-dimensional device structure improvements, non-geometric process techniques and new materials that improved performance. The difference compared to the original system drivers, DRAM, MPU and ASIC, was inclusion of the essential functions of data storage and digital signal processing on a system-on-chip (SoC), that is, functions that belonged to DRAM and ASIC, respectively, were integrated onto one chip with the MPU function. The second axis "More Than Moore," defined as the incorporation into devices of functionalities that do not necessarily scale according to Moore's Law but provided additional value to the customer in different ways, envisaged integration within a single package "functional requirements, such as power consumption, wireless com-

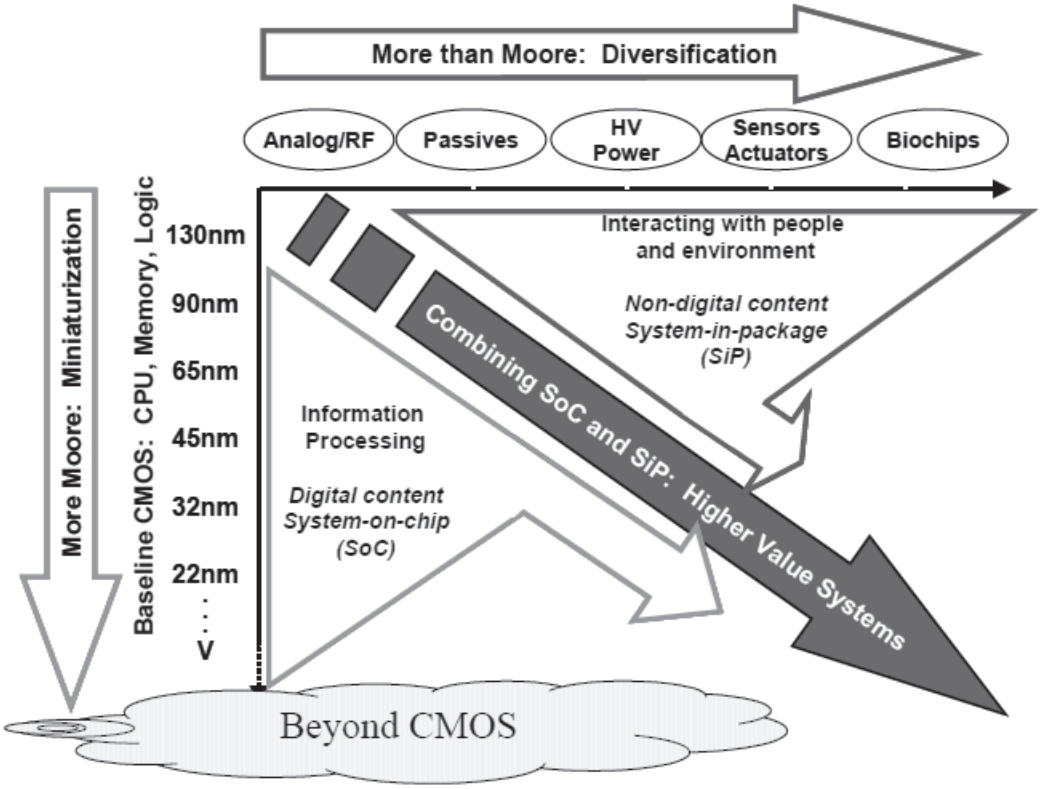


Fig.3 Discussion Framework for Future ST-Roadmaps

munication (RF), passive components, sensing and actuating, and biological functions" that may not scale with Moore's Law and/or may employ non-CMOS solutions, that is, system-in-package (SiP) products to become increasingly important. The keyword to both axes was integration because most market segments were demanding more functions on very small platforms, and the most obvious and direct solution was to eliminate bulky packaging.

The formulation of the "More Moore"-"More Than Moore" discussion framework is illustrative of the dynamics that vitalized the ITRS efforts. Discussions on Radio Frequency (RF) and Analog/Mixed-Signal Technologies (AMS) and non-CMOS device technologies had their roots in the Process Integration, Devices and Structures (PIDS) technology working group. RF and AMS was driven by the rapidly growing wireless communication market where industry led the introduction of IC chips for analog processing of RF signals using non-CMOS processes and intermediate frequency (IF) signals using CMOS-compatible processes. Non-CMOS was driven by the urgency to find solutions to scaling beyond the 45-nm technology node, which in 2005, was a complete redbrick wall extending over all PIDS technology requirements. The discussions culminated in extended sections on Wireless and Emerging Research Devices (ERD) added to the 2003 ITRS, and gave birth to above Fig. 3 in the 2005 ITRS. This bottom-up dynamics is clearly an important driving force that kept the ITRS relevant.

4 Evaluating the Impact: Successes and Failures

The impact of the ST-Roadmaps is well expressed by these words from the Introduction to the 2005 ITRS, which said the ITRS "has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and developments needs out to a 15-year horizon. As such it provides a guide to the efforts of companies, research organizations, and governments. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs."

〈Pace-setter〉

As the industry's pace-setter it maintained the complexity trend predicted by Moore's Law for almost 25 years, which in turn kept the improvement trends going for cost, speed, power, compactness and functionality. Is Moore's Law a self-fulfilling prophecy as some critics claimed? Some insights into the difficulties faced by industry may be found in the 1994 NTRS.

1. Industrial research laboratories faced diminishing funds for long term advanced research needed to maintain momentum, because of requirements to show clear return on investment, resulting in major gaps in the US infrastructure.
2. Escalating costs of research facilities were making it difficult for universities to invest in state-of-the-art wafer fabrication or advanced lithography programs.
3. Software engineering and cross-discipline technology optimization required cultural change to correct deficiency to produce high-quality software.

The problem was not one of technical capability but one about competitiveness. Spending enormous amounts of capital on R&D may maintain Moore's Law but also leaves an enormous problem in recovering the investment and weakens the company. The ST-Roadmaps helped to maintain or enhance competitiveness by encouraging information sharing that in turn saved costs. At the same time, accurate information from consensus among top experts helped management make better judgements for R&D investments.

〈Technology Breakthroughs〉

Another success that deserves mention is finding solutions that broke through redbrick walls. The ST-Roadmaps identified where redbrick walls existed and helped

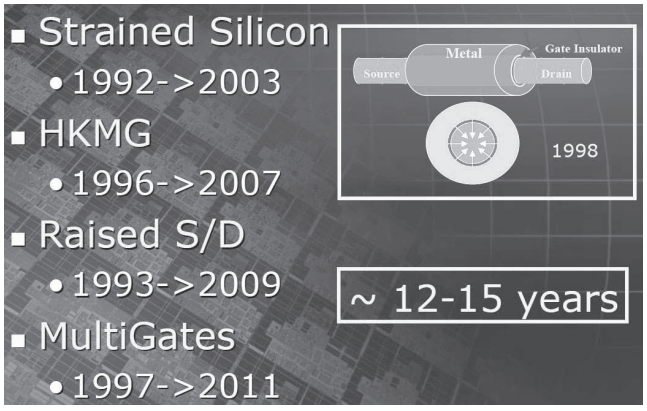


Fig.4 Incubation times needed for breakthroughs[9]

channel resources to tackle them in a timely manner. As the example of DRAM cell size shows, the accuracy may be poor at first so sufficient lead-time is important. For the ST-Roadmaps, 12-15 years was typical for breakthroughs to be found and solutions to be readied for mass production. Some examples are given in Fig. 4.

〈Pitfalls〉

The ST-Roadmaps also contained pitfalls. It should be remembered that milestones were meant only for the industry. Individual companies may find keeping the evolution pace set by the ST-Roadmaps a feat beyond their strength. Multi-billion capital investments every three years can be afforded only by the largest companies that had annual business volumes of several billions each. Even at slower evolution pace, huge investments were accompanied by huge risks. The growing demand for CMOS IC chips at first allowed many companies to risk building expensive fabrication facilities (fabs). In the late 1980's rising costs led to the birth of pure-play fabs that do not design circuits and design houses that do not manufacture chips.

Taiwan Semiconductor Manufacturing Company (TSMC), starting business in 1987, was the first pure-play fab. Its greatest difference from historical semiconductor producers, which operate as Integrated Device Manufacturers (IDMs) that design, manufacture and sell semiconductor IC products, is in providing only manufacturing services. At first TSMC provided processes that were 2 generations older than the most advanced IDMs, but it caught up after 10 years. Fabless companies or design houses that outsource their manufacturing requirements can enjoy the benefits of using the most advanced process for best performance, or using older processes for inexpensive IC chips, without heavy capital investments in expensive fabricating facilities. TSMC, by catering to the needs of many customers making products for a wide variety of markets, ensures high usage rate of its lines even if some customers do not sell well, thereby reducing risks. IDMs in contrast bear both the risk of high-cost fabrication facilities and the risk of poor sales of its products.

The top 10 fabless companies in 2017[10] included 6 U.S. companies, 1 Singapore company (Broadcom originally had its headquarters in the U.S. but moved to Singapore), 1 Taiwanese company and 2 Chinese companies. Three among the top 5 were incorporated later than 1990. In general, fabless companies performed better than IDMs, except during years when memory chips had exceptionally strong demand.

The strong performances of pure-play fabs and fabless companies demonstrate a growing trend of the semiconductor industry as Rock's Law progresses with Moore's Law. Advanced fabrication facilities become concentrated among the top companies. Many IDMs cannot afford to upgrade their fabrication facilities even though they slowly become obsolete. To survive, companies cannot have a narrow objective of achieving Moore's Law at any cost.

5 Discussion and Conclusion

The ST-Roadmaps probably have no parallel in their scope and scale of industry level research cooperation. They provide an interesting subject or material for studies on MOT. Many other research and/or industry consortia have been formed to enhance technology and other common goals within an industry. However, most of them do not open their publications to the public or they do not have roadmaps or their scopes are limited to narrow topics. Published reports of the ST-Roadmaps are in-detail documents that have several hundred pages, most of which contain technical details but also lengthy portions that include explanations of the rationale, notes about why and how changes have been made, and suggestions/cautions about how the information should be used. The ST-Roadmaps and revisions had been published 10 times over a period of almost 25 years, therefore, offer a rare chance to study the effectiveness of using roadmaps in MOT.

The ST-Roadmaps function as a MOT tool for industry-level open cooperation. Some of the most significant features are listed below.

1. They provide a shared vision that motivates researchers and focuses their efforts towards common goals.
2. They provide accurate information, from consensus among many top experts, about the state-of-art, what technology levels are required and when in the future, the readiness of technologies required, where solutions have not been found, what alterna-

tive technologies are promising, and how fast technology can advance.

3. They act as a pace-setter that provides quantitative milestones for overall targets as well as lower level technologies and coordinates R&D among interrelated technologies.
4. They list requirements for all key technologies so as to identify gaps that need more attention or provide opportunities from novel ideas. Examples of gaps are cross-cut technologies that had not been given much attention before. The ST-Roadmaps' documentation claimed that such gap technologies would be provided better research funding although no detail was given.

The ST-Roadmaps are, in several important aspects, different from roadmaps that are typical of company R&D management.

1. They were formulated to achieve only Moore's Law, or at least that was the only objective initially. The pace of technological evolution was independent of market fluctuations. It is noted that when milestones turned out to be more difficult than initially projected, roadmap pace had been suitably delayed. It was not like true MOT that must consider market opportunities and threats, such as in a SWOT review, when companies plot long-term investment plans. In the ST-Roadmaps, maintaining Moore's Law was the ultimate aim. It may even be pointed out that the headlong rush to maintain Moore's Law momentum could have been a factor that aggravated spiraling high costs. It should be added that the only market information were descriptions of market drivers (broad market segments) within the topic of system drivers. In the almost 25-year history, categories in both system drivers and market drivers went through minor revisions a few times to align with new market segments or trends.
2. They identified technological needs but were not accompanied by execution plans. No person nor organization was tasked to achieve the milestones. R&D investments were left entirely to companies, academic institutions, national laboratories and other R&D funding programs. The "R&D cooperation" is limited to obtaining consensus about technological needs, state of readiness of solutions, and the pace of evolution. It may be argued that absence of execution planning helped to avoid "not my job" kind of mental blocks to the search for solutions, or "protectionistic" reactions to adverse critical assessments. The Roadmap played the role of a neutral technology consultant who evaluated objectively and without bias.
3. The published ST-Roadmaps were open to anyone who was interested. In-depth technical details were shared at workshops among contributors and other participants, many of who belonged to rival companies. The objective was to facilitate cooperation for future R&D execution plans, but specific cooperation agreements were outside the roadmapping scope. Open discussion, furthermore encouraged voicing of more ideas and reduced biased pre-conceptions.
4. ST-Roadmaps' projections of technology requirements were based purely on scientific and engineering knowledge, hence, milestones in the near term were not affected by uncertain factors such as market demand and competition. On the other hand, readiness information depended on the opinions of top experts who might be wrong, inaccurate or misleading. Consensus from a pool of many top experts, who brought to the discussion a variety of experience and knowledge, under conditions unbiased by non-technical considerations, should give more accurate assessments compared to the situation in a company setting.

A clear picture of what the ST-Roadmaps were and were not can be seen from the published documentation. The more important question, whether and how did they contribute to the semiconductor industry, can only be answered partially, based on circumstantial evidence from the electronics industry. The history of the electronics market offers some clues. Electronics products that use the products of the semiconductor industry often follow a product evolution pattern that starts with corporate customers who demand high performance, followed by a wider market who can pay less but are satisfied with lower performance such as small businesses and families, and finally spreads to individual customers who demand small portable products. An example is the digital computer which evolved from large computers for business information processing, to office computers

for office information processing, to personal computers for each employee and family, and finally to smartphones for each individual. Another example is the video recorder/player, which evolved from specialist equipment, to family consumer product, to individual consumer products first as DVD players, and today integrated into smartphones. The semiconductor market for these products grow in volume, and often towards smaller, less bulky, less heavy, and low power consumption versions. What started as many circuit boards in large cabinets, evolved to a few circuit boards in side-cabinet-size units and desktop units, to single boards in laptops, notebooks, tablets and smartphones. Semiconductors makers must always push the performance envelop for products that can do more, use less power and have smaller form factors. The market for semiconductors is strongly technology-driven and new products soon find use in a variety of new applications. The strategy followed in the Roadmap to maintain Moore's Law is exactly what the industry needs. It must be added though that the actual rate achieved was 2-fold every two years instead of the target 4-fold every three years.

In the previous section, it had been noted that the 2005 ITRS documentation claimed the ITRS "has been an especially successful worldwide cooperation." This reputation is attested to by the large number of top experts who contributed to revising the roadmaps. If the roadmapping exercise had been meaningless, few top experts would spend time away from their jobs. The importance industry placed on the ITRS roadmap is evident from the large fraction of contributors from industry (73% in 2005 ITRS), Fig. 5.

A cause-effect relationship between the ST-Roadmaps and progress of the semiconductor industry, however, remains difficult to demonstrate. Although they defined the milestones to achieve Moore performance growth rate, they did not participate in R&D. In the PDCA cycle view of managerial actions, "D" was conducted by researchers in many organizations, a large number compared to about 1000 contributors to the ST-Roadmaps. Revising the roadmap every two years gave a chance for R&D results to be fed back to the contributors who could then evaluate the viability and/or readiness of candidate solutions.

A related question is: did the ST-Roadmaps give positive impact on the businesses of individual companies? As explained above, R&D funding fell outside the purview of the ST-Roadmaps. Companies or business units, in the case of large corporations, had to seek funds on their own merits, and get ready required technologies. However, the ST-Roadmaps only provided information for companies to plan ahead but how the information impacted individual businesses differed greatly. Managerial decisions in semiconductor companies to invest in new technologies might have been made using information from the ST-Roadmaps, but the outcomes of those decisions were affected by many other factors, such as market demand, company strengths and weaknesses, and competition, which together determined in a complex manner the degree of success, so that causal effect from one factor is difficult to demonstrate.

What does the long term trend data of semiconductor

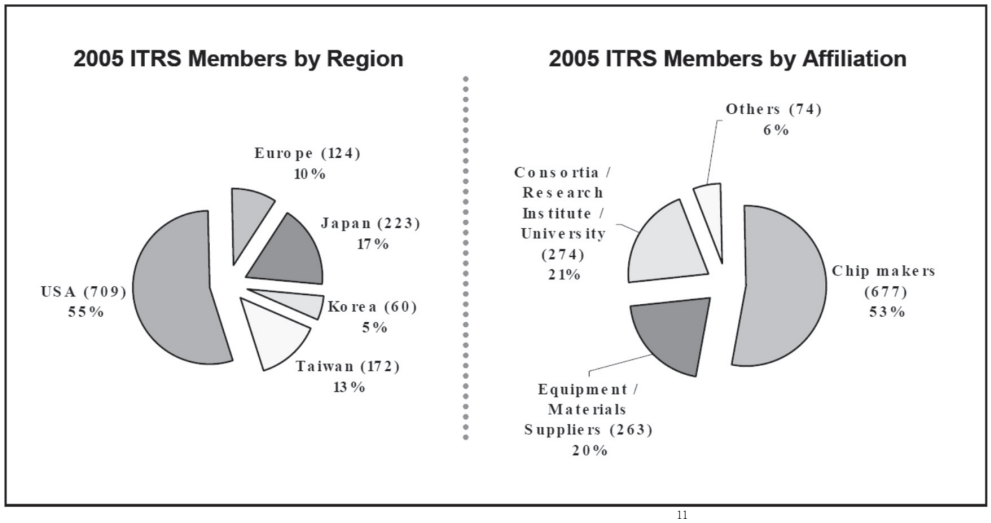


Fig.5 ITRS Membership Composition[11]

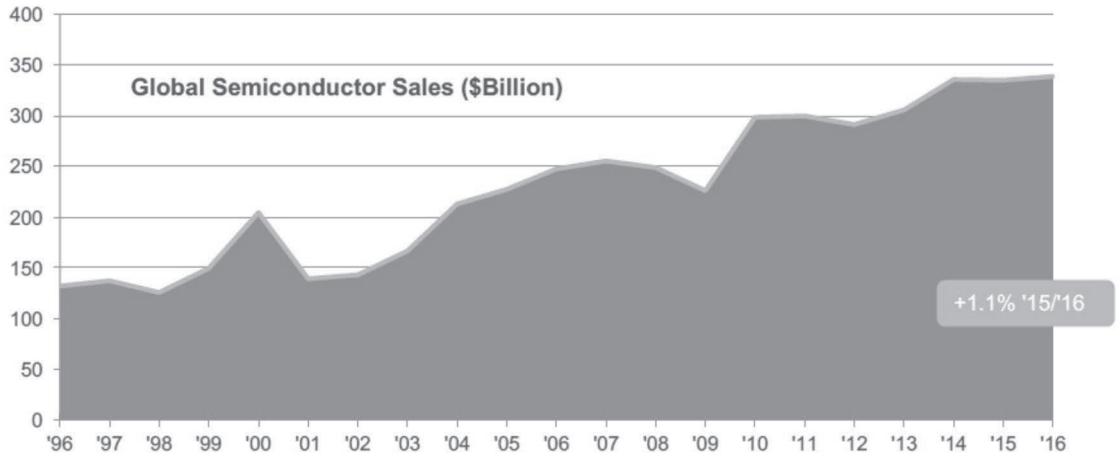


Fig.6 Annual Global Semiconductor Sales 1996−2016[12]

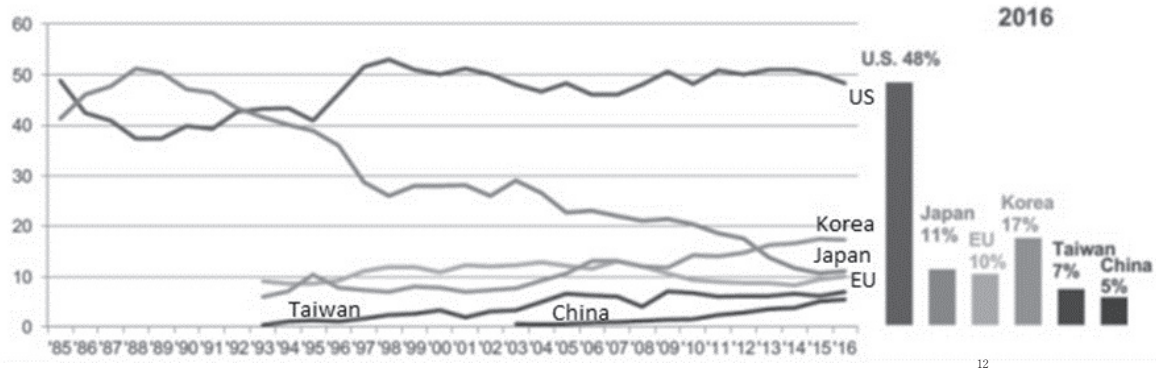


Fig.7 Market share trends of major semiconductor producing regions in 2016[12]

sales show?

The compound annual growth rate (CAGR) of the semiconductor industry between 1996 and 2016 was 4.8%/year according to the World Semiconductor Trade Statistics (WSTS) and SIA estimates, reaching US$346b in 2017, Fig. 6. This is below typical GDP growth rates of emerging economies and above those of developed economies. Although number of chips might have increased much more, falling prices suppressed the total sale value.

The market shares between top producing regions, however, showed trends different from the global sales trend, Fig. 7. The US market share, after being overtaken by Japan in the late 1980's, regained top position by the early 1990's and maintained roughly the same share since mid-1990's. On the other hand, Japan's market share declined almost continuously for 30 years, despite being a technology leader in semiconductors. The ST-Roadmaps provide information for "how" to make state-of-art semiconductors but not how to succeed in competing against others who have the same information.

Further research using company histories regarding investments in semiconductor technologies would be needed to clarify why business performances differed so greatly among companies and even among countries.

Conclusion

This paper looked into the impact of ST-Roadmaps on the semiconductor industry by examining their role as a MOT tool. The biannually revised reports provided primary source information. It was found that the ST-Roadmaps only considered technological needs for achieving Moore's Law but disregarded other factors such as market and competition. The ST-Roadmaps represented the consensus among top experts about key semiconductor technologies and were highly regarded by the semiconductor community. Although R&D execution was conducted by others, the ST-Roadmaps gave a common vision and challenging targets that guided and paced R&D to find timely solutions to satisfy market demands. The fact that ST-Roadmaps did not include non-technical considerations suggests that they may provide unique insights for research to clarify the separate contributions of technical and non-technical factors to MOT effectiveness.

References

1）E. Moore, “Cramming more components onto integrated circuits,” Electronics, Vol.38, No.8, Apr 19, 1965, pp.114 ff.

2）E. Moore, “Progress in Digital Integrated Circuits,” Tech. Dig. IEDM, IEEE, 1975, pp.11-13.

3）R.H. Dennard, et al., “Design of Ion-Implanted MOSFET’s with Very Small Physical Dimensions,” IEEE J. Solid-State Circuits, Vol.SC-9, No.5 Oct 1974, pp.256-268.

4）https://spectrum.ieee.org/tech-talk/semiconductors/devices/the-murky-origins-of-moores-law, last accessed Oct 20, 2018.

5）http://www.rennes.supelec.fr/ren/perso/gtourneu/enseignement/roadmap94.pdf, last accessed Oct 22, 2018.

6）http://www.itrs2.net/itrs-reports.html, last accessed Oct 22, 2018.

7）https://irds.ieee.org/, last accessed Oct 22, 2018.

8）R.R. Schaller, “Technological Innovation in the Semiconductor Industry: A Case-Study of the International Technology Roadmap for Semiconductors (ITRS),” Ph.D. Dissertation, Sch. Public Policy, George Mason Univ., Apr 15, 2004.

9）P. Gargini, “ITRS – Past, Present and Future,” ITRS-RC Workshop, Feb 26-27, 2015, http://www.itrs2.net/itrs-reports.html, last accessed Oct 22, 2018.

10）http://www.eenewsanalog.com/news/chinese-break-top-ten-fabless-ranking, last accessed Oct 22, 2018.

11）Executive Summary, 2005 ITRS report.

12）Semiconductor Industry Association 2017 Factbook, SIA