AN ISOLATED MOSFET GATE DRIVER

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Abstract

Traditional methods of isolated MOSFET/IGBT gate drive are presented, and their pros and cons assessed. The best options are chosen to meet our objective — a small, high speed, low cost, low power isolated gate drive module.
Two small ferrite bead transformers are used for isolation, one transmits power at 2.5MHz, the other sends narrow set reset pulses. On the secondary these pulses drive a transistor totem pole to ensure high current drive, and the value is held by CMOS buffers with positive feedback. An alternative design for driving logic level devices uses only an HC buffer on the secondary.
Double sided SMD construction (primary one side, secondary on the other) yields an upright module 40x18x5mm. Propagation delay was 20ns, and rise/fall time 15ns with a 1nF load. The design places no limits on frequency of operation or duty cycle. Power supply requirements were 5V @ 20mA for operation below 100kHz, dominated by magnetising current.

1 Introduction

As part of our research into multilevel converters, we needed 24 isolated MOSFET gate drivers. The number of drivers required dictated a small modular design suitable for prototyping, which was low in cost, and yet did not sacrifice performance. This prompted the following review of isolated gate drive techniques, and a subsequent design which borrowed a number of ideas from the reviewed techniques, and contributes some of its own.

2 Traditional Approaches

Isolated MOSFET gate drive circuits are varied, and range from the simple approaches used when the power MOSFET was new technology, to the complex chip-set solutions available today.

The gate (ie gate-source circuit) of a MOSFET (and similarly, IGBT) appears purely capacitive, so no gate drive current is needed in the steady state, unlike transistors. However, a high current low impedance drive circuit is needed to inject or remove current from the gate and slew V_{gs} in order to switch the device rapidly. The gate drain capacitance, although small, can also require significant charge as the drain voltage slews (the Miller effect). [1]

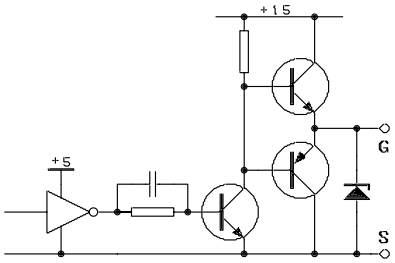

Figure 1: The circuit diagram of a discrete totem pole level shifter / gate driver

Usually a totem pole circuit powered from 12 or 15 Volts is used. A simple discrete circuit can serve admirably (fig 1) and is both effective and rugged. CMOS buffers or inverters can be parallelled, however the 4000 series has poor output drive, and the newer HC and AC devices have a maximum supply of 6V, suitable only for logic level devices. The National DS0026 MOS clock driver was used to fill the gap; now ICs specifically designed for the task have proliferated, both CMOS (Harris ICL7667, Telcom TC426) and bipolar (Unitrode UC3708,9) [2,3] . In addition to the basic functionality of these devices (TTL compatible inputs, high current outputs), other features found in these families include enable and shutdown inputs, internal flip-flops, and high speed comparators.

2.1 Isolation Using Pulse Transformers

The simplest method of isolating the MOSFET gate from the driving circuit is with a pulse transformer (fig. 2). This passive solution is simple, but transformer saturation limits on-time for a given transformer size, and magnetising current will reduce efficiency. A capacitor is usually placed in series with the primary, and since the transformer can only transmit the AC information, the duty cycle is generally limited to 0-50 %. This approach works well in Switch Mode Power Supply (SMPS) circuits, where the frequency is high, and the duty cycle change is small. One transformer can drive complementary MOSFETs in half (or full) bridge forward converters, by driving V_{gs} both positive and negative and using two (four) secondaries of opposite phase.

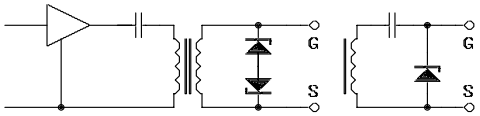

Figure 2: The circuit diagram of transformer isolated gate driver

The simple addition of a capacitor and zener on the secondary side can be used to restore the correct DC offset on the signal (fig. 2). This allows for a 1-99 % duty cycle. The zener voltage should be chosen slightly less than the secondary drive voltage, to ensure it conducts on both positive and negative peaks to maintain the correct capacitor voltage.

The Harris HV400 is a specific high current buffer for interfacing pulse transformers to large capacitive loads, BJTs and small GTOs. This chip stores additional energy from the pulse transformer in a capacitor an order of magnitude larger than the gate capacitance. A transistor emitter follower then routes additional current to the output from this capacitor on the leading edge of the gate drive pulse. The falling edge triggers a large thyristor to discharge the gate rapidly. A small minimum off-time of 1-2μs is required for the thyristor to turn off before the next pulse [2] .

Thinking laterally, only narrow pulses are necessary to inject or remove charge from the gate, so long as the gate can be isolated from the pulse transformer in the intervening interval. During this period, the gate capacitance (perhaps augmented by an external capacitor) maintains V_{gs}. The control signal is "differentiated" by driving the pulse transformer primary by the difference of the original and delayed control signals (fig. 3). The signal is reconstructed on the secondary side gate capacitance by the current steering and blocking of the zener or diode / MOSFET combination [1] .

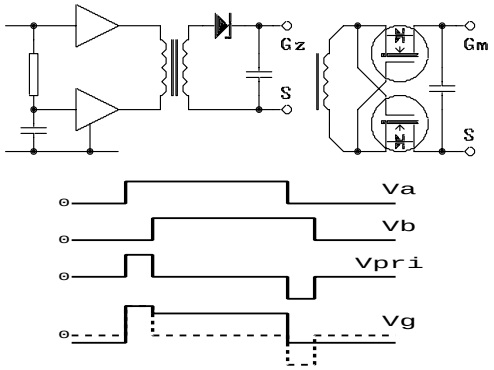

Figure 3: Only the edges are transmitted by the transformer in this arrangement. The zener / MOSFETs reconstruct the waveform, which is maintained between edges by the capacitor.

This approach offers unlimited duty cycle, but limited high-time as the circuit is dependent on the MOSFET input capacitance to hold the value of V_{gs}. This can improved by increasing the value of C_{gs} with an external capacitor (at the expense of speed), and minimising all sources of leakage. This approach is not particularly immune to noise, and so is again best suited to SMPS or similar applications. Peter Wolfs' circuit [4] is an improvement on this, regularly replenishing the charge on the gate.

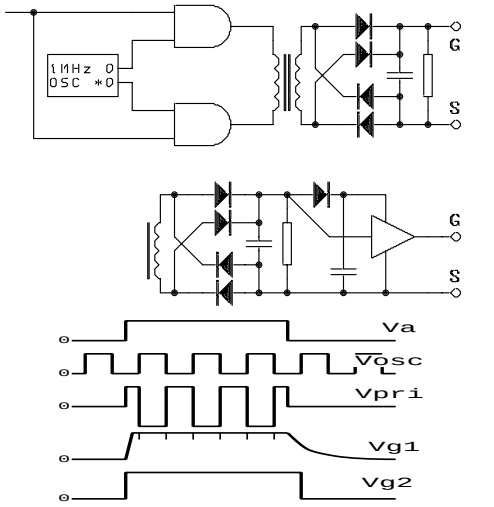

Figure 4: In this circuit, the input signal gates a high frequency carrier, which is rectified and filtered on the secondary side.

For larger capacitive loads where speed of operation is not critical (such as a solid state relay), the control signal can gate a high frequency carrier (fig. 4). A small transformer provides isolation, then, after being rectified, this signal is applied to the gate and a parallel re-

sistor. When the carrier is gated on, the gate capacitance can be charged very quickly, however, when removed, the parallel resistor is solely responsible for removing the gate charge. An improvement is to employ an active driver on the secondary side to detect the carrier and switch the MOSFET gate accordingly [1] .

2.2 Adding an isolated power supply

For higher power applications such as motor drives, an active gate drive circuit is employed directly at the MOSFET gate, and both control signal and power are transmitted across the isolation barrier.

The power is either provided by a small DC-DC converter, or more commonly by a flyback converter with multiple isolated outputs. The inter-winding capacitance of these transformers should be kept low to avoid the large common mode currents which would flow as the device common (source or emitter) terminal and attached gate driver slew.

Bootstrapping is another method of creating a quasi-isolated power supply. However it relies on the source of the floating MOSFET (and attached isolated driver) falling regularly to the ground potential of the control circuitry to replenish the charge on the driver's power supply capacitor. This imposes a 0-99 % duty cycle limit.

A separate power supply also allows the easy addition of features such as over-current and over-temperature protection. The status of these protection comparators can be passed back to the control electronics with additional optocouplers or signal transformers. Simple protection circuits can still be added without and auxiliary power supply however [5].

Opto-couplers are generally used for signal transmission and isolation, however suitable high speed opto-couplers with high dV/dt immunity are essential. A good alternative when the control electronics are physically separated from the power electronics is to use fibre optic links, which have by their nature excellent isolation and dV/dt immunity (but not always speed). These are generally expensive.

2.3 Purpose built ICs

IC manufacturers have continued to integrate more functionality into each chip, making purpose built solutions to problems such as isolated gate drivers. An example are integrated opto-coupler power drivers, such as the Telcom TC4803/4 [6] and Sharp PC922/3/4. These only require an isolated power supply to complete an isolated driver.

Another integrated solution are IC drivers with internal level shifters which drive an internal floating power driver. These could not be classed as truly isolated drivers, and are usually used with a bootstraped power supply to drive the two devices in a half bridge. They have voltage ratings limited by the semiconductor process used, for example, 500V for the International Rectifier IR2110 half bridge driver, and 80V for the Harris HIP4080/1 full bridge driver. The HIP4080 has an high speed input comparator and is easily configured as a hysteretic switching power amplifier [2] .

The Unitrode UC3724,5/6,7 are chip-set pairs, designed to be used with a small high frequency pulse transformer. The primary side transmitter encodes the switching information as duty cycle changes in the transformer drive outputs. The secondary side MOSFET driver rectifies the transformer signal for power, interprets the duty cycle and switches its output appropriately. The UC3726,7 has higher output current ability, a comparator for desaturation detection and other features aimed at IGBT drive [3] .

3 Two New Approaches

Our area of research is multilevel converters. These have a multiple of the usual six switches needed for a three phase converter. A five level converter would have 24 switches — each requiring individual isolated control. This suggested a small module suitable for prototyping. The focus of our current research is modulation techniques, with the aim of wide modulator bandwidth and spectral quality. For this reason, it was our desire to minimise delay and rise times so as to produce results close to ideal. Later, the effect of switching delays can be assessed and compensated. Finally, as our budget was small, minimising the cost also became one of the major design goals. Other desirable qualities were ruggedness, logic level inputs and a 5V supply.

It was decided to use a driver on the isolated secondary with separate transmission of signal and power. Preliminary tests with diode/zener and diode/MOSFET configurations showed they were unsuitable for low frequencies, and there was doubt about their noise immunity, especially in a prototyping environment.

A pulse transformer was chosen rather than an opto-coupler for signal transmission. A small pulse transformer optimised for this task contributes virtually no delay to the signal path, and exhibits excellent isolation and dV/dt rejection.

Another small high frequency transformer was used for the isolated power supply. Including the power supply as part of the module makes the module self contained; and easy to reuse in other projects. This also maintains the best isolation between drivers. The inclusion of the

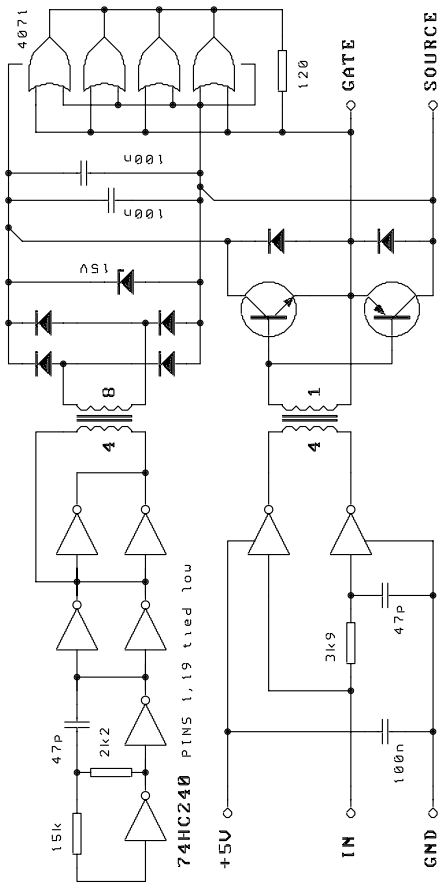

Figure 5: The circuit diagram of the SMD isolated gate driver

power supply makes little difference to the size or cost of the entire module.

The pulse transformers were made using ferrite beads. These are very inexpensive, however time consuming to wind. As each had only a small number of turns which could be reduced further by a larger core, a better alternative would be to etch the windings on the printed circuit board, and use a split ferrite core. [5]

The gate signal was sent as set-reset pulses. This permitted arbitrary duty cycle signals of any frequency, even DC levels. By using very narrow pulses, small transformers with minimal turns could be used. Little power is wasted in magnetising current.

The set reset pulse arrangement is also the ideal way to drive a capacitive load, which by its nature has "memory". The transistor stage isolates and amplifies the pulses, rather than the traditional diode/zener or diode/MOSFET approach. This simple approach works very well — the sharp exponential switching characteristic of the transistors allows large currents to flow with $V_{be} = 0.8$V, and yet very low leakage at $V_{be} = 0.2$V. In

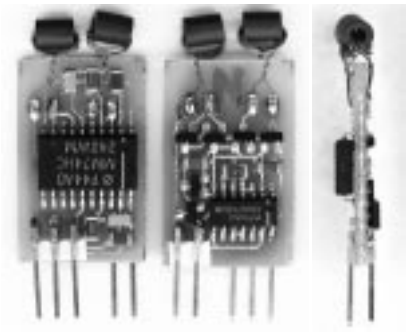

Figure 6: Front, rear and side view of SMD isolated gate driver, shown actual size.

practice, MOSFETs and (especially) zeners were found to be far less forgiving.

A pair of discrete transistors used in this way for the output stage have a number of other advantages —

- Discrete transistors are generally very rugged.
- Arbitrarily large peak currents can be designed for, with appropriate choice of transistor or darlington.
- This configuration sources or sinks constant current all the way to the supply rails.
- This configuration has essentially no delay.

To ensure the last dc value is held indefinitely at the output, a buffer with positive feedback is used to latch the value to one of the supply rails. This is one approach used for active termination of high speed logic signals.

A driver module using a set reset pulse transformer for signal transmission can easily be configured as either inverting or non-inverting simply by swapping the transformer's secondary connections. Performance should remain otherwise identical.

One disadvantage of the set reset approach is the ill defined startup state. For this evolution of driver, power supply sequencing will be used to avoid this problem — signal processing and driver circuitry will always be active before power is applied to the main converter. A future solution would be to generate a reset pulse at power up and power down, or use a gate pull down resistor in combination with the latching buffer to force a low state at start up.

The isolated power supply consists of another ferrite bead transformer, driven by parallelled HC CMOS outputs, and rectified by high speed signal diodes. HC CMOS is fast and pulls completely to the supply rails for low currents, so power transfer is efficient, even at 2.5MHz. Since only one MOSFET gate is driven by the power supply, its power rating is small.

Cost was minimised by the deliberate choice of common components. Greatest cost would have been the time consuming SMD construction and winding the small pulse transformers. The next version would seek to address these problems — professionally made PCBs with a soldermask and consistent pad levels would assist the SMD construction, and PCB based transformer windings would avoid the winding of transformers.

SMD construction reduced the size of the resulting module, and allowed the primary to be placed on one side and the secondary on the other. The SMD module (fig. 6) stands vertically, with input and output pins on the bottom edge, and the pulse transformers looping over the top edge. The complete module measures approximately 40x18x5mm.

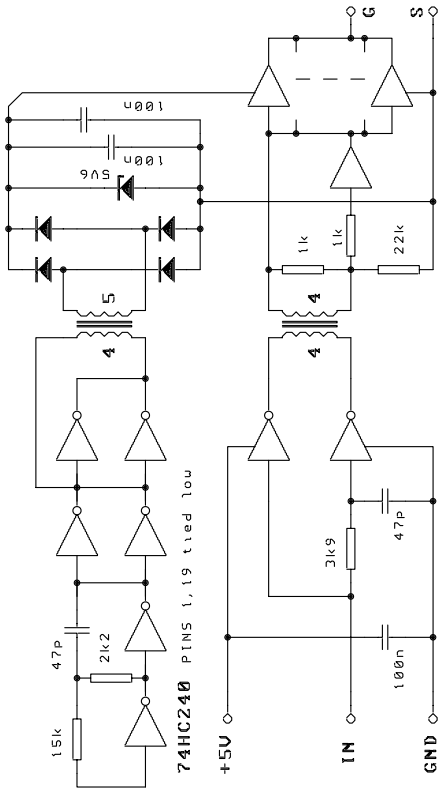

Figure 7: The circuit diagram of the alternative isolated logic level gate driver

An alternative approach to the final design (fig. 7) uses a second HC buffer on the secondary side rather than the transistor pair. It is limited to 6V output swing because of the HC CMOS, so is only suitable for Logic Level MOSFETs, or MOSFETs used at low currents. This circuit was bread-boarded and tested, with excellent results. It could be easily adapted to isolating ICs with synchronous serial interfaces such as a/d and d/a converters.

4 Performance

Performance of the driver met all expectations. Two modules were driven by one HC output, each with one standard 60V, 15A MOSFET (MTP3055) gate as a load. The measured propagation delay (input to gate) was approximately 20ns, and rise and fall times 15ns, for both the inverting and non-inverting versions of the driver (fig. 8). With different capacitive loads (1–5nF), the rise/fall time scaled linearly (15-65ns), while the propagation delay remained constant(20nS). The linear ramp of the gate voltage from rail to rail confirmed the transistor output stage behaves as a constant current source, here with a value of about 0.5A.

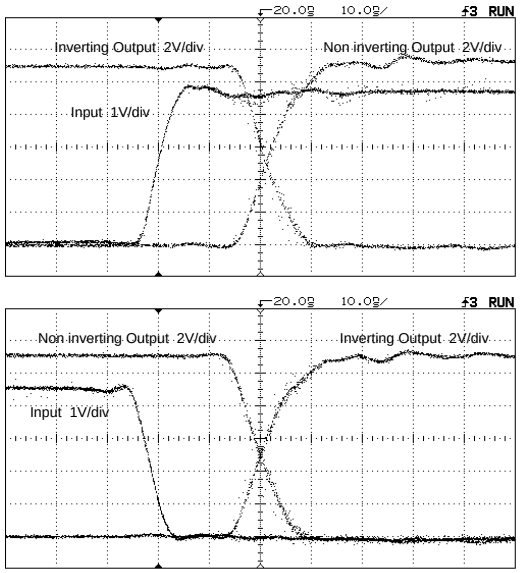

Figure 8: The response time of the isolated gate driver, input to output, inverting and non-inverting versions.

The drain of a MOSFET low-side switch (fig 9) and source of a MOSFET high-side switch (fig 10) driving resistive loads are also shown.

The output voltage regulation (fig 11) is poor because the power transformer rings when lightly loaded, producing a higher voltage than its turns ratio would suggest. When unloaded, the voltage is clamped by the zener on the secondary power supply. This zener is present to protect the secondary CMOS IC, rather than provide good regulation, and its value is chosen accordingly.

The power supply draws approximately 20mA even when the driver isn't switching; 15mA is due to the magnetising current of the small ferrite bead transformer, the remainder is due to the CMOS switching at 2.5MHz.

In its present form, this driver is quite suitable to oper-

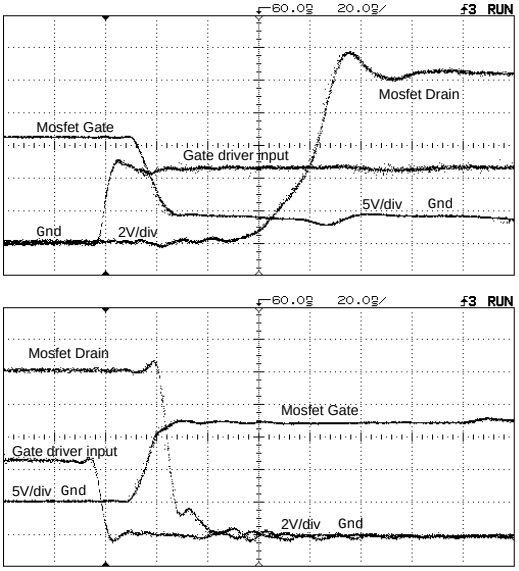

Figure 9: An inverting driver controls a low-side MOSFET switch (10V supply, 20Ω load, 1kHz 50% input). The HC input, FET gate and FET drain voltage waveforms are shown to demonstrate response time.

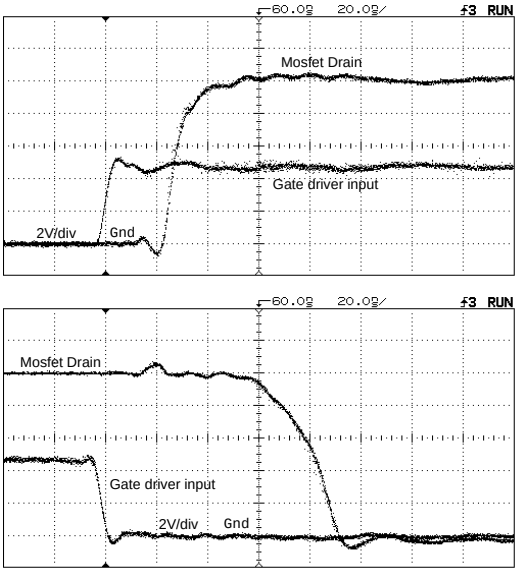

Figure 10: An non-inverting driver controls a high-side MOSFET switch (10V supply, 20Ω load, 1kHz 50% input). The HC input and FET source voltage waveforms are shown to demonstrate response time (FET gate not shown).

ation up to 100kHz, so long as 8-9V is sufficient gate drive. A future version needs more turns and/or a bigger core to reduce the quiescent current and improve the voltage regulation. If a 12V or 15V output voltage is necessary, the turns ratio can be chosen accordingly.

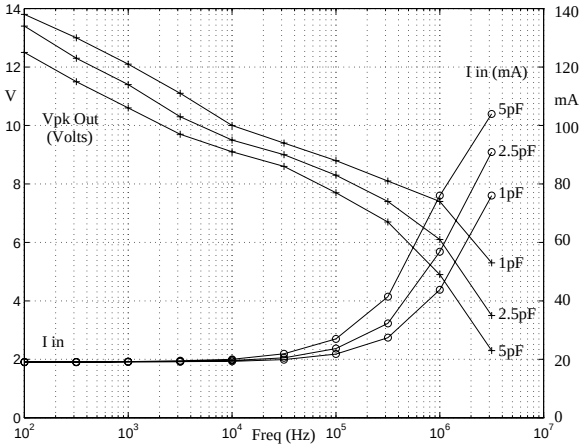

Figure 11: Peak driver output voltage and input supply current for different loads plotted against frequency.

5 Conclusion

Some traditional methods of isolated MOSFET/IGBT gate drive have been presented, and their pros and cons assessed. The best options were chosen to meet our objective — a small, high speed, low cost, low power isolated gate drive module.

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