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An Innovative Dual-Boost Nine-Level Inverter with Low-Voltage Rating Switches

Meysam Saeedian [1], **Edris Pouresmaeil [1],***, **Emad Samadaei [2]**,
Eduardo Manuel Godinho Rodrigues [3], **Radu Godina [4]** and **Mousa Marzband [5]**

[1] Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland; meysam.saeedian@aalto.fi

[2] Department of Electronics Design (EKS), Mid Sweden University, Holmgatan 10, 85170 Sundsvall, Sweden; emad.samadaei@miun.se

[3] Management and Production Technologies of Northern Aveiro—ESAN, Estrada do Cercal 449, Santiago de Riba-Ul, 3720-509 Oliveira de Azeméis, Portugal; emgrodrigues@ua.pt

[4] Research and Development Unit in Mechanical and Industrial Engineering (UNIDEMI), Department of Mechanical and Industrial Engineering, Faculty of Science and Technology (FCT), New University of Lisbon, 2829-516 Caparica, Portugal; rd@ubi.pt

[5] Department of Maths, Physics and Electrical Engineering, Faculty of Engineering and Environment, Northumbria University, Newcastle upon Tyne NE1 8ST, UK; mousa.marzband@northumbria.ac.uk

* Correspondence: edris.pouresmaeil@aalto.fi; Tel.: +358-505-984-479

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Abstract: This article presents an innovative switched-capacitor based nine-level inverter employing single DC input for renewable and sustainable energy applications. The proposed configuration generates a step-up bipolar output voltage without end-side H-bridge, and the employed capacitors are charged in a self-balancing form. Applying low-voltage rated switches is another merit of the proposed inverter, which leads to extensive reduction in total standing voltage. Thereby, switching losses as well as inverter cost are reduced proportionally. Furthermore, the comparative analysis against other state-of-the-art inverters depicts that the number of required power electronic devices and implementation cost is reduced in the proposed structure. The working principle of the proposed circuit along with its efficiency calculations and thermal modeling are elaborated in detail. In the end, simulations and experimental tests are conducted to validate the flawless performance of the proposed nine-level topology in power systems.

Keywords: power conversion; multilevel inverter; improved switched-capacitor module; multi carrier based modulation

1. Introduction

In recent years, extensive research has been carried out on multilevel inverters (MLIs) due to their potential in various industrial applications, particularly grid-connected renewable energy sources, machine drives, and high-voltage direct current transmission systems. Improved output waveforms quality, reduced device stress (dv/dt), and increased efficiency are some merits of the MLIs in comparison with the standard two-level inverter [1–4]. The most popular traditional/basic multilevel topologies are CHB, NPC, and FC, which have widely been put into commercial use in high/medium voltage systems (above 3 kV). Nonetheless, high control/modulation technique complexity and large power electronic device count (dc power supplies, semiconductors, and capacitors) are cited as demerits of the aforementioned topologies [5–7].

To overcome these drawbacks, researchers and industrialists all around the world are contributing to present innovative topologies with the ability to produce more voltage levels with reduced device

count and to further improve energy efficiency. Apart from that, it has tried to develop MLIs with lower voltage-rating switches and to cope with the voltage unbalancing problem in NPC and FC. These attempts lead not only to reducing filter requirement and simplicity, but also cost/volume reduction of the conversion system [8–10].

Despite a plethora of multilevel topologies that have been presented, intensive effort has been devoted to introduce promising topologies. For example, ref. [11,12] presented novel MLIs employing the technique of switched-capacitor. Although a substantial reduction in the device count is achieved in these topologies as compared to the conventional ones, they however require H-bridge circuits to generate bipolar voltages. This weakness leads to a sharp increase in total standing voltage (TSV) and thereupon switches cost. A single source nine-level (9 L) inverter has been proposed in [13], which applies semiconductors with the same Peak inverse voltage (PIV) equal to input voltage level. Nevertheless, this topology utilizes numerous insulated-gate bipolar transistors (IGBTs) and gate drivers, which enlarge the system. A hybrid cascaded MLI with improved symmetrical sub-module was introduced in [14]. It employs four dc sources and ten switches with high PIVs to produce a 9 L voltage waveform. Furthermore, [15] introduced a single source inverter which is comprised of an H-bridge inverter and two switched-capacitor modules. It employs sixteen IGBTs with low voltage ratings for generating a 7 L output voltage. Yet, these presented MLIs in the literature suffer from either a large number of circuit elements or relatively high PIVs.

In summary, the main contribution of this paper is the development of a modified 9 L inverter for single phase systems, which is superior to all the earlier topologies. The switches employed in the proposed configuration enjoy low PIVs. At the same time, a further reduction in device count and implementation cost is attained in the proposed circuit compared to the traditional/cutting-edge ones. Moreover, there is no difficulty in the capacitors' charging process since the inverter is inherently self-balanced. Due to the voltage boosting capability, this inverter is proposed for grid-connected renewable energy sources (such as solar and wind farms), uninterruptible power supplies, and electric vehicles in which low input DC voltages are required to be boosted to an acceptable range for these systems.

The rest of this article is structured into five sections. Following the introduction, Section 2 presents the operating principle and a detailed comparative study of the proposed topology in order to demonstrate the superiority of the proposed inverter against newest 9 L topologies. Section 3 describes PWM strategy applied to the proposed inverter. Efficiency calculations and thermal analysis are carried out in Section 4. The simulation and experimental results are brought in Section 5 in order to prove the feasibility and effectiveness of the presented topology. Eventually, conclusions are presented in Section 6.

2. Analysis of the Proposed Nine-Level Inverter

2.1. Circuit Description

Figure 1 depicts the proposed switched-capacitor based inverter with the potential of generating a 9 L staircase waveform ($\pm 2V_{IN}$, $\pm 3V_{IN}/2$, $\pm V_{IN}$, $\pm V_{IN}/2$ and 0). As demonstrated in Figure 1, it comprises twelve power switches, two capacitors (C_1, C_2), and only one input DC source with the advantage of regenerative capability. The output voltage can be boosted up to $2V_{IN}$ by connecting the input source with pre-charged capacitors in series. It should be underscored that the blocking voltage of all switches employed in the proposed inverter is equal to the input DC source (i.e., V_{IN}), with the exception of S_7, S_8, and S_{12} which block only half the V_{IN}. In other words, it generates a bipolar output voltage without using end-side H-bridge. This ability is considered a beneficial feature of the proposed circuit since the lower switch voltage rating, the cheaper switch.

The working principle of the proposed inverter is illustrated in Figure 2. As can be observed, C_1 and C_2 are charged up to $V_{IN}/2$ by turning S_3 and S_4 on during 0 and $\pm 1V_{IN}$ levels. Then, the capacitors are connected in parallel at $\pm V_{IN}/2$ and $\pm 3V_{IN}/2$ levels. Thereby, the voltage across them

is balanced. Finally, they are discharged across the load during $\pm V_{IN}/2$ and $\pm 2V_{IN}$ levels. Relying on this simple switching plan, the proposed inverter does not require any external balancer circuit.
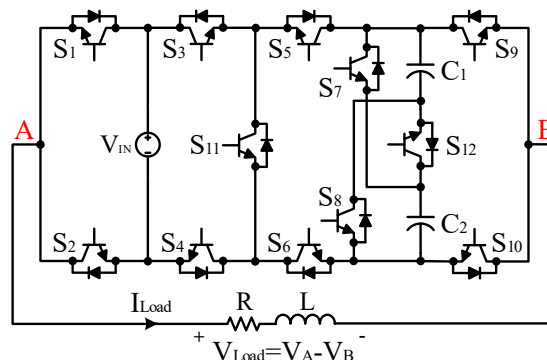
Figure 1. The proposed 9 L topology.
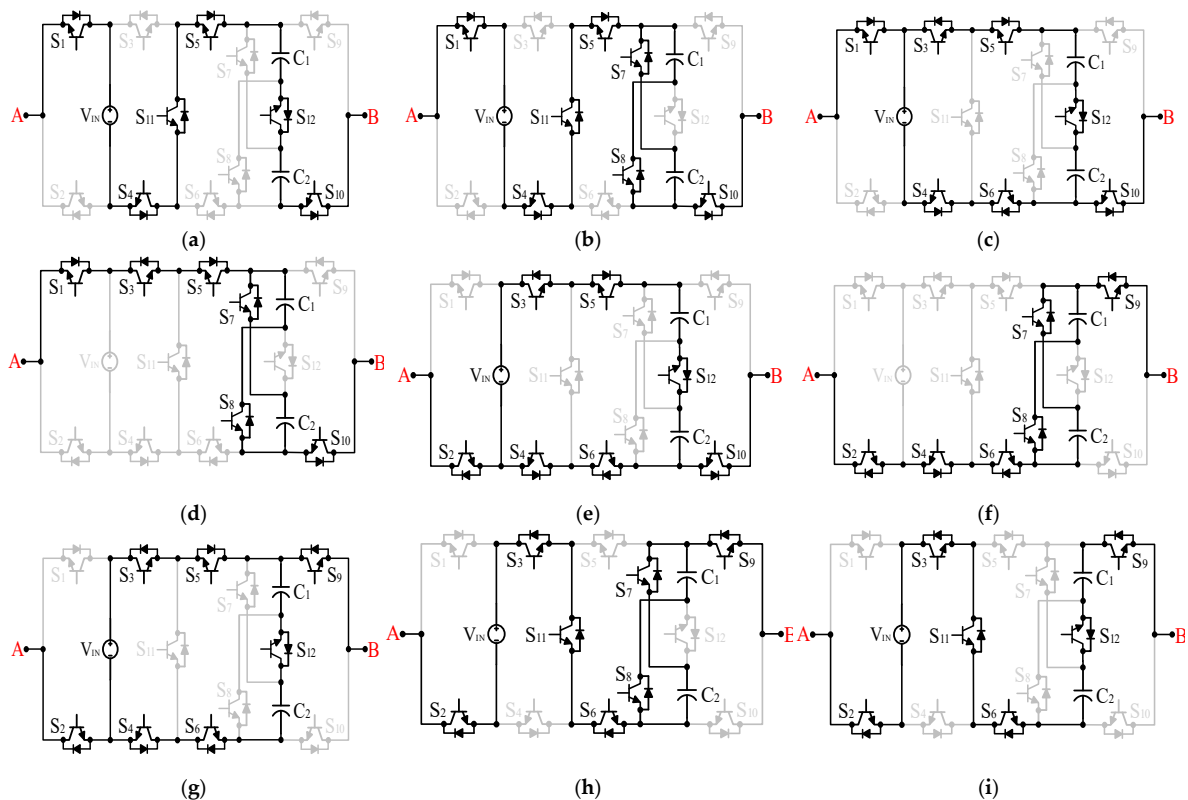
Figure 2. Switching states of the proposed inverter, (**a**) $+2V_{IN}$, (**b**) $+3V_{IN}/2$, (**c**) $+V_{IN}$, (**d**) $+V_{IN}/2$, (**e**) 0; (**f**) $-V_{IN}/2$, (**g**) $-V_{IN}$, (**h**) $-3V_{IN}/2$, (**i**) $-2V_{IN}$.

2.2. Comparative Assessment

Table 1 compares the presented circuit with other recently-introduced topologies in terms of the number of required semiconductors/DC sources and switches voltage rating. As observed from the table, ref. [14] the proposed circuit employs the least number of switches and capacitors compared to the other ones. These minimizations result in simpler control and a higher degree of compactness. Apart from this, the table depicts a fourfold increase in the number of required DC power supplies for [14] and conventional CHB, while the others and proposed inverter utilize only one DC source.

Applying switches with lower PIV is also a distinct advantage of the proposed inverter. In other words, it enjoys the lowest level of TSV. To prove this, the number of employed IGBTs with the same voltage rating for each structure is presented in the following table. For instance, the proposed 9 L

inverter needs nine and three switches with the PIV of $1V_{IN}$ and $V_{IN}/2$ respectively, while [13] requires nineteen IGBTs with the voltage ratings of V_{IN}. Thereby, the proposed inverter can be an acceptable alternative to the topologies listed in Table 1.

Table 1. Comparison of the proposed topology with other recently presented inverters.

Comparison Item	CHB (Con.)	[11] (2010)	[12] (2017)	[13] (2018)	[14] (2018)	[15] (2018)		Proposed
Level	9	9	9	9	9	7	9	8M * + 1
Switch	16	13	12	19	10	16	12	12M
Capacitor	-	3	4	3	-	2	2	2M
DC source	4	1	1	1	4	1	1	M
N * × PIV	$16 \times 1V_{IN}$	$4 \times 4V_{IN}$ $9 \times 1V_{IN}$	$4 \times 4V_{IN}$ $8 \times 1V_{IN}$	$19 \times 1V_{IN}$	$4 \times 4V_{IN}$ $2 \times 3V_{IN}$ $4 \times 1V_{IN}$	$16 \times 1V_{IN}$	$9 \times V_{IN}$ $3 \times V_{IN}/2$	$9M \times V_{IN}$ $3M \times V_{IN}/2$
TSV	$16V_{IN}$	$25V_{IN}$	$24V_{IN}$	$19V_{IN}$	$26V_{IN}$	$16V_{IN}$	$21V_{IN}/2$	$M \times (21V_{IN}/2)$

M *: Number of cascaded modules.

Furthermore, the single-source topologies are also compared in terms of total implementation cost (see Table 2). It should be noted that CHB and [14] are not considered in the cost-comparative analysis since they require four DC power supplies. For a fair comparison, power rating (i.e., volt/ampere rating) of all the MLIs are assumed to be equal to 5 kW/30.7 A. Moreover, a 50% voltage rating margin is considered for the selection of switches and capacitors. It is observed from Table 2 that the proposed inverter requires the least implementation cost compared to the other ones.

Table 2. Price Comparison of the Single-Source MLIs.

Part	Part Number	Voltage Rating (V)	Unit Price * (€)	[11]	[12]	[13]	[15]	Proposed
MOSFETs	STW40NF20	200	3.53	9	8	19	-	3
	SUP40N25-60-E3	250	4.43	-	-	-	16	9
	FQL40N50	450	7.73	-	-	-	-	-
	SIHG47N60AEFGE3	600	7.82	4	4	-	-	-
Capacitors	E32D151HPN472TEE3M	150	23.00	3	2	4	-	2
	B43713F2478M000	250	39.39	-	-	-	2	-
	ALS31A472NF350	350	48.83	-	2	-	-	-
Gate driver	IRS21271SPBF	-	1.34	13	12	19	14	12
Total cost (€)				149.47	219.26	184.53	168.42	112.54

* Source: www.mouser.com.

3. Multicarrier PWM Strategy

Therein, phase disposition PWM technique is applied to control each IGBT of the proposed topology. To do this, eight triangular carriers (V_{t1} to V_{t8}) arranged with shifts in amplitudes are required (see Figure 3a). It should be noted that they are the same in amplitude (A_t), frequency (f_t) and phase [16,17]. The carriers are compared to a reference waveform (V_{ref}) which results in generating appropriate fire pulses for all switches. For instance, S_{11} is turned on when $V_{ref} > V_{t1}$ or $V_{t2} < V_{ref} < V_{t1}$ or $V_{t8} < V_{ref} < V_{t7}$ or $V_{ref} < V_{t8}$. In other words, S_{11} must be turned on when S_1: ON, S_4: ON, S_3: OFF (or S_2: ON, S_3: ON, S_4: OFF), which can be observed in Figure 2. Similarly, S_{12} is turned on when $V_{ref} > V_{t1}$ or $V_{t3} < V_{ref} < V_{t2}$ or $V_{t5} < V_{ref} < V_{t4}$ or $V_{t7} < V_{ref} < V_{t6}$ or $V_{ref} < V_{t8}$. In other words, S_{12} must be turned on when S_7 and S_8 are OFF (see Figure 2). Further clarification concerning switching strategy is brought up in Figure 3b and Table 3.
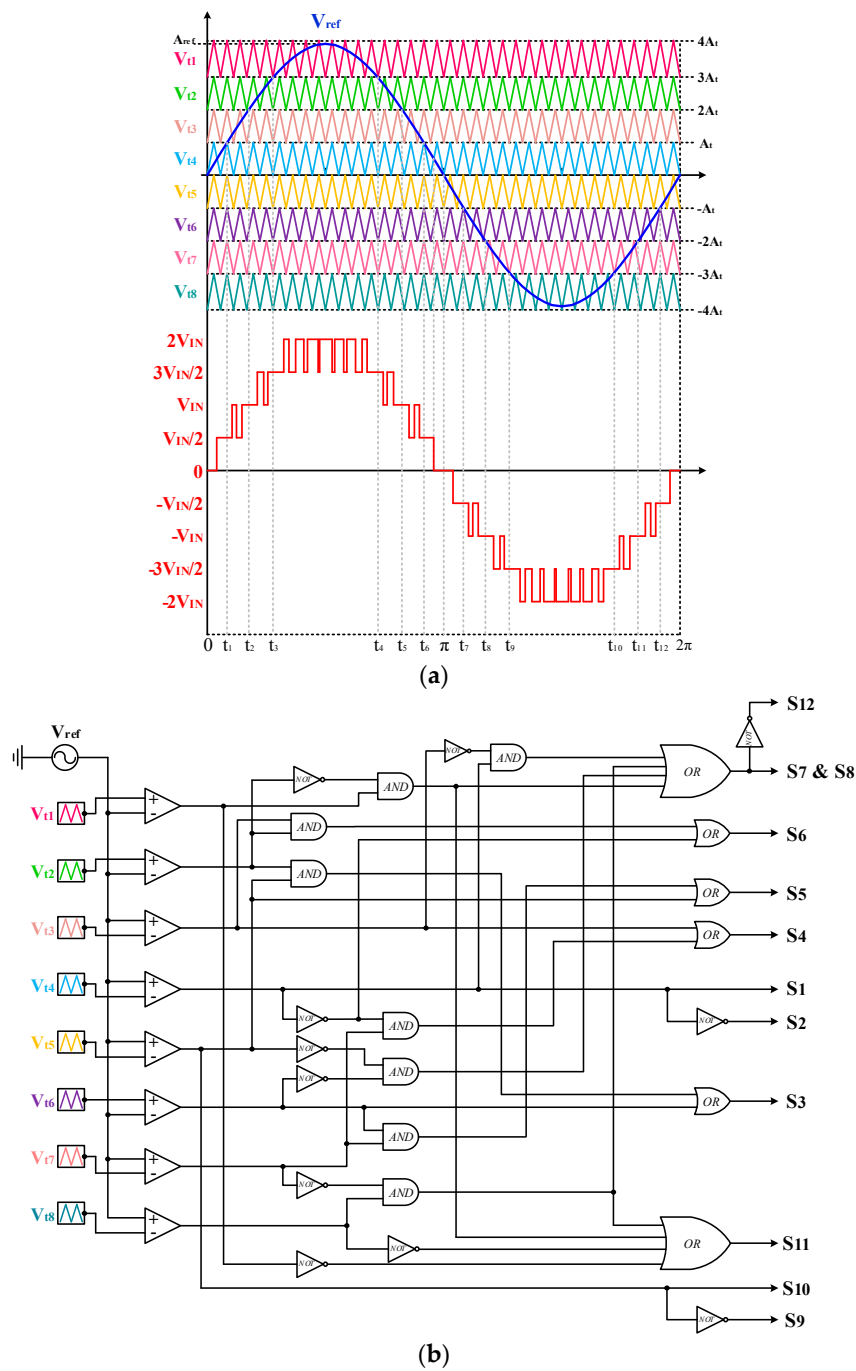
(**a**)

(**b**)

Figure 3. (**a**) PWM technique, (**b**) Logic schematic.

Table 3. On-State IGBTs for Each Level.

Relationship between the Carriers and V_{ref}	ON-State IGBTs	Levels
$V_{ref} > V_{t1}$	S_1-S_4-S_5-S_{10}-S_{11}-S_{12}	$+4V_{IN}$
$V_{t2} < V_{ref} < V_{t1}$	S_1-S_4-S_5-S_7-S_8-S_{10}-S_{11}	$+3V_{IN}$
$V_{t3} < V_{ref} < V_{t2}$	S_1-S_3-S_4-S_5-S_6-S_{10}-S_{12}	$+2V_{IN}$
$V_{t4} < V_{ref} < V_{t3}$	S_1-S_3-S_5-S_7-S_8-S_{10}	$+1V_{IN}$
$V_{t5} < V_{ref} < V_{t4}$	S_2-S_3-S_4-S_5-S_6-S_{10}-S_{12}	0
$V_{t6} < V_{ref} < V_{t5}$	S_2-S_4-S_6-S_7-S_8-S_9	$-1V_{IN}$
$V_{t7} < V_{ref} < V_{t6}$	S_2-S_3-S_4-S_5-S_6-S_9-S_{12}	$-2V_{IN}$
$V_{t8} < V_{ref} < V_{t7}$	S_2-S_3-S_6-S_7-S_8-S_9-S_{11}	$-3V_{IN}$
$V_{ref} < V_{t8}$	S_2-S_3-S_6-S_9-S_{11}-S_{12}	$-4V_{IN}$

4. Loss Distribution and Thermal Modeling

4.1. Power Loss Analysis

The power loss for a multilevel inverter is composed of three parts including P_C, P_S and P_R which are elaborated as follows:

4.1.1. Conduction Loss (P_C)

P_C is caused by parasitic resistance (i.e., ON-state resistance of the switch (R_S) and its parallel diode (R_D), capacitor internal resistance (R_C)) involved in the current paths [18]. Table 4 shows the equivalent value of the parasitic resistance (R_{eq}) existing in each voltage level. It should be noted that in the present work R_S, R_D, and R_C are considered equal to 0.27 Ω, 0.05 Ω, and 0.03 Ω, respectively.

Table 4. R_{eq} in Each Step.

Output Level	R_{eq} (Ω)
0	$2R_S + 2R_D = 0.64$
$\pm V_{IN}/2$	$3R_S + 2R_D + R_C = 0.94$
$\pm V_{IN}$	$3R_S + R_D = 0.86$
$\pm 3V_{IN}/2$	$5R_S + R_D + R_C = 1.43$
$\pm 2V_{IN}$	$6R_S + 2R_C = 1.68$

If $|V_{ref}| < A_t$, the output voltage switches between 0 and $+V_{IN}/2$ (see Figure 3a). Consequently, the output current passes through two switches and two diodes (three switches, two diodes, and one capacitor) during 0 ($+V_{IN}/2$) level, as depicted in Table 4. In this case, the energy dissipated within $0 < t < t_1$ ($t_6 < t < t_7$ or $t_{12} < t < 2\pi$) is attained by Equation (1) in which A_t, A_{ref}, and f_{ref} are considered equal to 0.25, 0.9, and 50 Hz, respectively [18]. Moreover, t_1 is calculated as follows:

$$E_{0\&V_{IN}/2} = \int_0^{t_1} \left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[(3R_S + 2R_D + R_C)\frac{A_{ref}\sin(2\pi f_{ref}t)}{A_t} + (2R_S + 2R_D)\left(1 - \frac{A_{ref}\sin(2\pi f_{ref}t)}{A_t}\right)\right]dt \tag{1}$$
$$= 2.04 \times 10^{-5} \times \left(P_{out}/V_{IN}\right)^2$$

$$t_1 = \frac{\sin^{-1}\left(A_t/A_{ref}\right)}{2\pi f_{ref}} = \frac{\sin^{-1}(0.25/0.9)}{100\pi} = 9 \times 10^{-4} sec. \tag{2}$$

Similarly, the energy losses that occurred in other time intervals are calculated by Equations (3)–(8).

$$E_{V_{IN}/2\&V_{IN}} = \int_{t_1}^{t_2} \left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[(3R_S + R_D)\frac{A_{ref}\sin(2\pi f_{ref}t)-A_t}{A_t} + (3R_S + 2R_D + R_C)\left(1 - \frac{A_{ref}\sin(2\pi f_{ref}t)-A_t}{A_t}\right)\right]dt \tag{3}$$
$$= 2.03 \times 10^{-4} \times \left(P_{out}/V_{IN}\right)^2$$

$$t_2 = \frac{\sin^{-1}\left(2A_t/A_{ref}\right)}{2\pi f_{ref}} = \frac{\sin^{-1}(0.5/0.9)}{100\pi} = 1.87 \times 10^{-3} sec. \tag{4}$$

$$E_{V_{IN}\&3V_{IN}/2} = \int_{t_2}^{t_3} \left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[(5R_S + R_D + R_C)\frac{A_{ref}\sin(2\pi f_{ref}t)-2A_t}{A_t} + (3R_S + R_D)\left(1 - \frac{A_{ref}\sin(2\pi f_{ref}t)-2A_t}{A_t}\right)\right]dt \tag{5}$$
$$= 7.2 \times 10^{-4} \times \left(P_{out}/V_{IN}\right)^2$$

$$t_3 = \frac{\sin^{-1}\left(3A_t/A_{ref}\right)}{2\pi f_{ref}} = \frac{\sin^{-1}(0.75/0.9)}{100\pi} = 3.1 \times 10^{-3} sec. \tag{6}$$

$$E_{3V_{IN}/2\&2V_{IN}} = \int_{t_3}^{t_4} \left[I_{Load}\sin\left(2\pi f_{ref}t\right)\right]^2 \times \left[(6R_S + 2R_C)\frac{A_{ref}\sin(2\pi f_{ref}t)-3A_t}{A_t} + (5R_S + R_D + R_C)\left(1 - \frac{A_{ref}\sin(2\pi f_{ref}t)-3A_t}{A_t}\right)\right]dt \tag{7}$$
$$= 0.0051 \times \left(P_{out}/V_{IN}\right)^2$$

$$t_4 = \frac{\pi - sin^{-1}(3A_t/A_{ref})}{2\pi f_{ref}} = \frac{\pi - sin^{-1}(0.75/0.9)}{100\pi} = 6.86 \times 10^{-3} sec. \tag{8}$$

Due to quarter-wave symmetry of the output voltage, the total conduction loss for the proposed 9 L topology is:

$$P_C = \left(4E_{0\,\&V_{IN}/2} + 4E_{V_{IN}/2\,\&V_{IN}} + 4E_{V_{IN}\,\&3V_{IN}/2} + 2E_{3V_{IN}/2\,\&2V_{IN}}\right) \times f_{ref} = 0.69 \times \left(P_{out}/V_{IN}\right)^2 \tag{9}$$

4.1.2. Switching Loss (P_S)

The overlap of switch voltage and current during rise and fall times (i.e., t_{on} and t_{off}) leads to P_S, which is highly proportional to the f_S. The turn-on and turn-off power loss of the switch S are attained by [19]:

$$P_{S,on} = f_S \int_0^{t_{on}} v_S(t)\, i_S(s)\, dt = f_S \int_0^{t_{on}} \left(\frac{V_S}{t_{on}}t\right)\left(-\frac{I_S^{on}}{t_{on}}(t - t_{on})\right) dt = \frac{1}{6}f_S V_S I_S^{on} t_{on} \tag{10}$$

$$P_{S,off} = f_S \int_0^{t_{off}} v_S(t)\, i_S(t)\, dt = f_S \int_0^{t_{off}} \left(\frac{V_S}{t_{off}}t\right)\left(-\frac{I_S^{off}}{t_{off}}(t - t_{off})\right) dt = \frac{1}{6}f_S V_S I_S^{off} t_{off} \tag{11}$$

In which I_S^{on} (I_S^{off}) is the switch current after (before) turning on (off). Considering $t_{on} = t_{off} = 58$ ns and $f_t = 4$ kHz, P_S for all the switches is obtained as follows:

$$P_{Sj,on} = P_{Sj,off} = \frac{1}{6} \times \frac{1}{2} \times 4 \times 10^3 \times V_{IN} \times \frac{I_{Load}}{\pi} \times 58 \times 10^{-9} = 6.15 \times 10^{-6} \times P_{out}, j = 1, 2, 9, 10, 11 \tag{12}$$

$$P_{Sj,on} = P_{Sj,off} = \frac{1}{6} \times 4 \times 10^3 \times V_{IN} \times \frac{I_{Load}}{\pi} \times 58 \times 10^{-9} = 12.3 \times 10^{-6} \times P_{out}, j = 3, 4, 5, 6 \tag{13}$$

$$P_{Sj,on} = P_{Sj,off} = \frac{1}{6} \times \frac{1}{2} \times 4 \times 10^3 \times \frac{V_{IN}}{2} \times \frac{I_{Load}}{\pi} \times 58 \times 10^{-9} = 3.07 \times 10^{-6} \times P_{out}, j = 7, 8 \tag{14}$$

$$P_{S12,on} = P_{S12,off} = \frac{1}{6} \times \frac{1}{2} \times 4 \times 10^3 \times \frac{V_{IN}}{2} \times \frac{I_{Load}}{\pi} \times 58 \times 10^{-9} = 3.07 \times 10^{-6} \times P_{out} \tag{15}$$

Consequently, the total switching loss for the presented 9 L inverter is calculated by:

$$P_S = \sum_{j=1}^{N_{switch}} \left(P_{Sj,ON} + P_{Sj,OFF}\right) = 178 \times 10^{-6} \times P_{out} \tag{16}$$

4.1.3. Power Loss Generated by Capacitor Voltage Ripple (P_R)

P_R is due to the voltage difference between the capacitor and input DC source during the charging periods. Generally, the maximum discharging value of each capacitor in a switched-capacitor circuit is attained by [13,18]:

$$\Delta Q_C = \int_{t_c}^{t_d} I_{Load} Sin(2\pi f_{ref} t) dt \tag{17}$$

where $[t_c, t_d]$ is the discharging interval of each capacitor. According to Figures 2a and 3a, the maximum discharging period of C_1 (or C_2) is equal to $[t_3, t_4]$. Thus, considering maximum acceptable voltage drop across C_1 (or C_2) equal to ΔV_{ripple}, the capacitance of each capacitor is calculated by [13,18]:

$$C \geq \frac{\Delta Q_C}{\Delta V_{ripple} \times 0.5V_{IN}} \tag{18}$$

For example, considering $P_{out} = 1.4$ kW ($I_{Load} = 7$ A, V_{IN}=200 V) and $\Delta V_{ripple} = 10\%$, the capacitances for the proposed inverter are obtained as follows:

$$C_1 = C_2 = \frac{\int\limits_{0.0031}^{0.00686} 7 \times Sin(100\pi t)dt}{0.1 \times 100} = \frac{0.024}{10} = 2400 \, \mu F \tag{19}$$

It also should be noted that nominal voltage of the capacitors is equal to $V_{IN}/2$ (see Figure 2). Consequently, P_R for the proposed topology is attained as follows:

$$P_R = \frac{f_{ref}}{2}\left(\sum_{i=1}^{2} C_i\left(\Delta V_{ripple} \times 0.5V_{IN}\right)^2\right) = 50 \times \left(\int\limits_{0.0031}^{0.00686} I_{Load}sin(100\pi t) \, dt \times \Delta V_{ripple} \times 0.5V_{IN}\right) = 0.088 \times \Delta V_{ripple} \times P_{out} \tag{20}$$

Therefore, considering Equations (9), (16), and (20), the efficiency is calculated by Equation (21).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_C + P_S + P_R} \tag{21}$$

Theoretical efficiency of the proposed inverter has been calculated at different output power and presented in Figure 4. It is observed that there is a marked rise in the efficiency by increasing the output power.
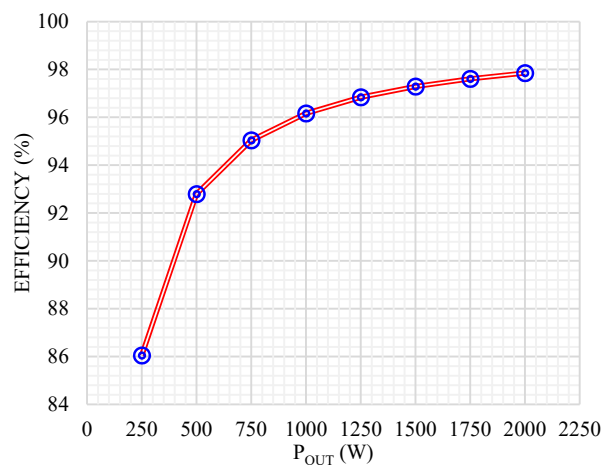

Figure 4. Inverter efficiency at different power output.

4.2. Thermal Model

Heat distribution through semiconductor components is caused by power loss, which leads to an increasing of T_j [20]. This temperature, for safety reasons, should be monitored and kept within a specified range during the inverter operation. Figure 5a illustrates the thermal model implemented for a single semiconductor, in which the thermal impedance between junction and case (Z_{th}) is considered a four-layer foster network (see Figure 5b) [21,22]. It should be noted that Z_c and Z_s are the thermal impedances from the case to the heat sink and from the heat sink to the ambient, respectively. These are found on the manufacturer datasheet.
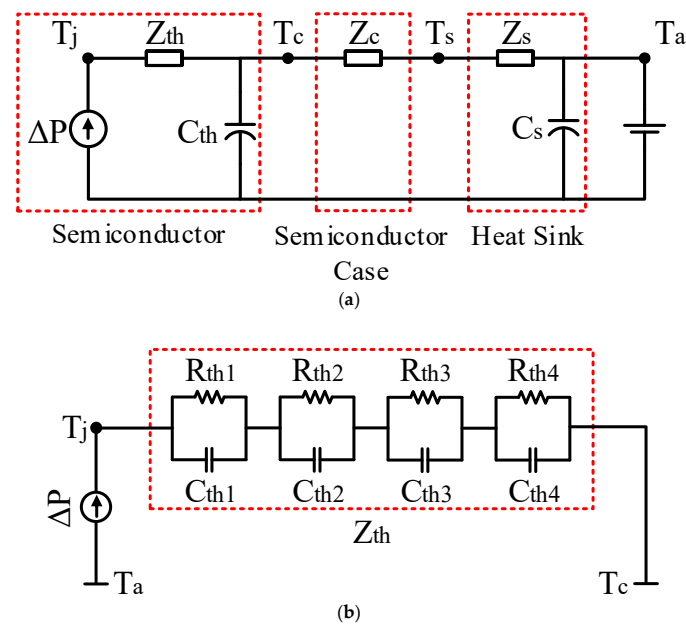
Figure 5. (**a**) Semiconductor thermal model; (**b**) foster network of Z_{th}.

Modelling loss dissipation of the proposed 9 L inverter in MATLAB/Simulink yields the junction temperature of the power electronic devices [23–25]. Herein, T_a is considered equal to 40 °C and the PM75CLA060 switch produced by Mitsubishi Electric is chosen in the thermal estimation.

The estimated T_j of some power switches employed in the proposed inverter at 20 kW output power is illustrated in Figure 6. It can be observed that S_{12} has the lowest T_j (approximately 43.9 °C), while this temperature approaches 46.7 °C for S_{11}.
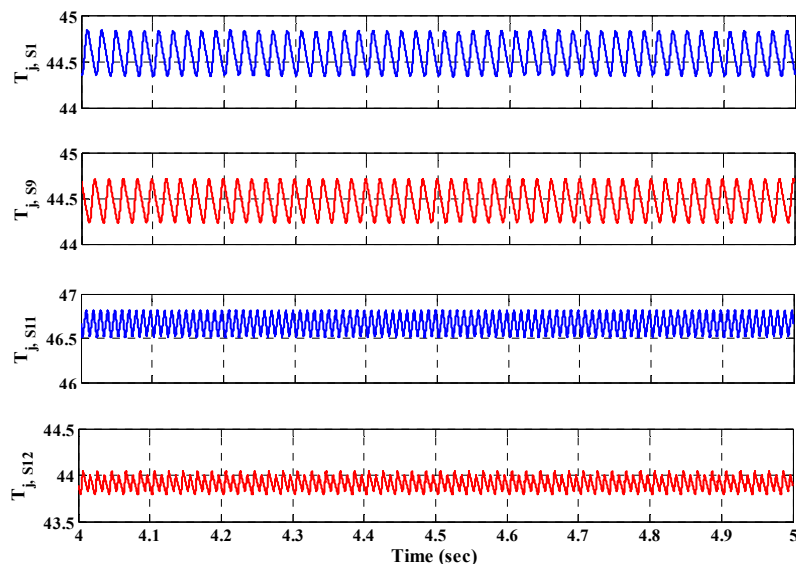

Figure 6. The estimated T_j at 20 kW output power.

5. Simulation and Experimental Results

Simulations have been conducted in MATLAB for steady-state and transient modes, as presented below. Figure 7 shows the inverter output voltage/current and capacitors voltage at resistive-inductive load (f_t = 4 kHz, $C_1 = C_2$ = 2300 µF, R = 100 Ω, L = 100 mH). These results confirm the flawless performance and self-balanced ability of the presented 9 L inverter. Moreover, the value of the input DC source is selected at 200 V. Thus, the capacitors and output voltages reach 100 V and 400 V,

respectively. The proposed topology has also been simulated under step change in the load, and the results are presented in Figure 8. As can be observed, the voltage ripple across the capacitors rises promptly from 3.5% to 7.2% by decreasing the load impedance. Once again, these figures verify the inherent capacitor voltage balancing ability during inverter operation.

Figure 9 shows the voltage waveforms across some power switches employed in the proposed topology. It is clear that S_3, S_5, and S_{11} (also S_1, S_2, S_4, S_6, S_9 and S_{10}) must withstand voltages equal to the input DC source (i.e., 200 V). Other switches (S_7, S_8 and S_{12}), however, block voltages equal to half the input DC source (i.e., 100 V). To sum up, unlike topologies with end side H-bridge, none of the switches required for the proposed inverter tolerate maximum output voltage (i.e., 400 V).

Furthermore, the effect of different modulation indexes and switching frequencies on the operation of the proposed inverter is shown in Figure 10. It is observed that the inverter output voltage has lower THD at higher modulation index (and higher switching frequency). Moreover, the fundamental component of output voltage is decreased at lower modulation index.
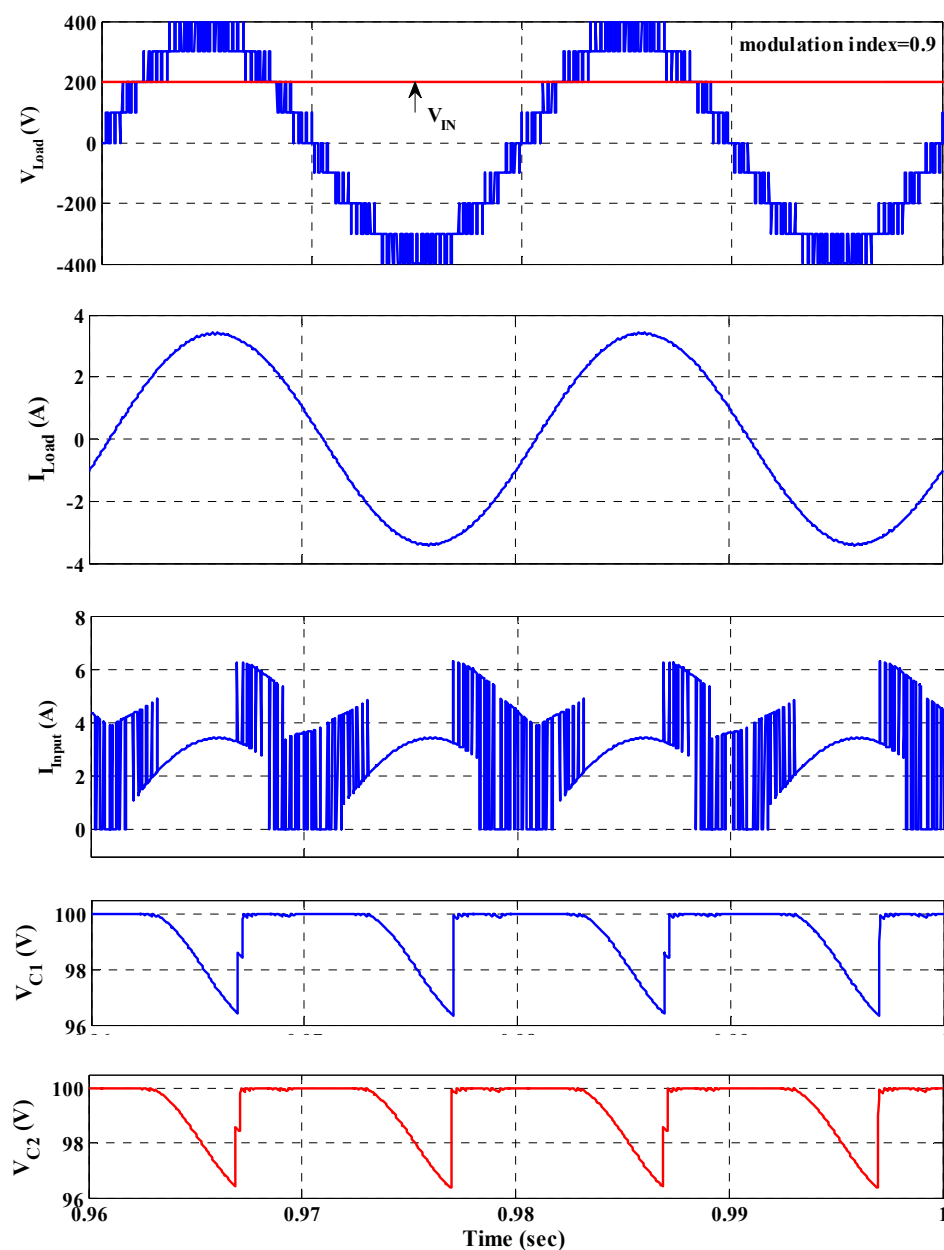

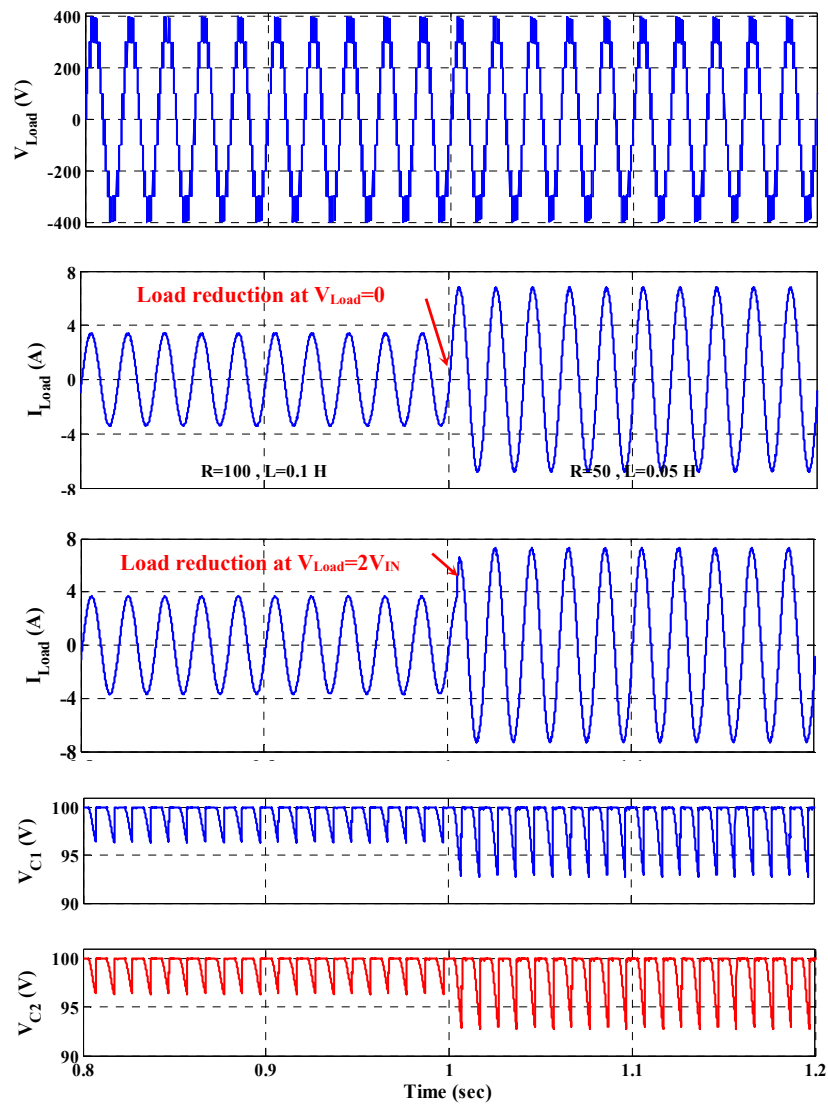**Figure 7.** Operation of the presented model under constant load.

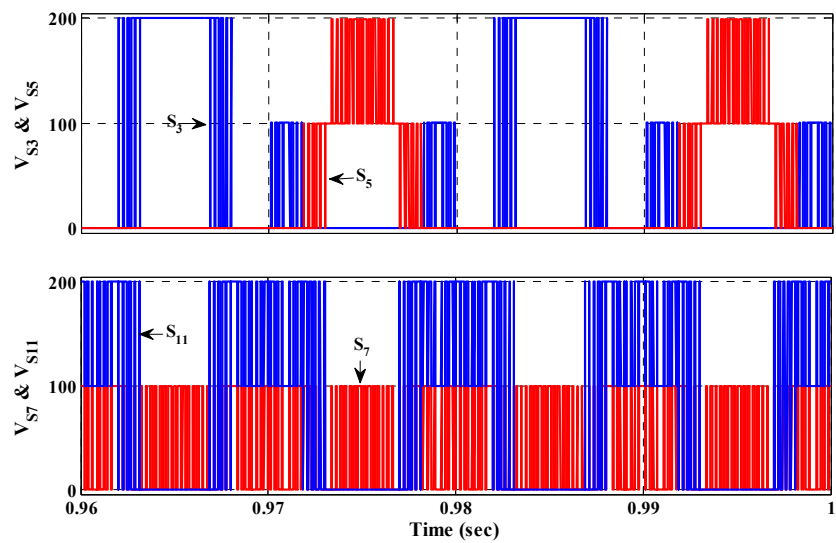**Figure 8.** Operation of the presented model under sudden load reduction.
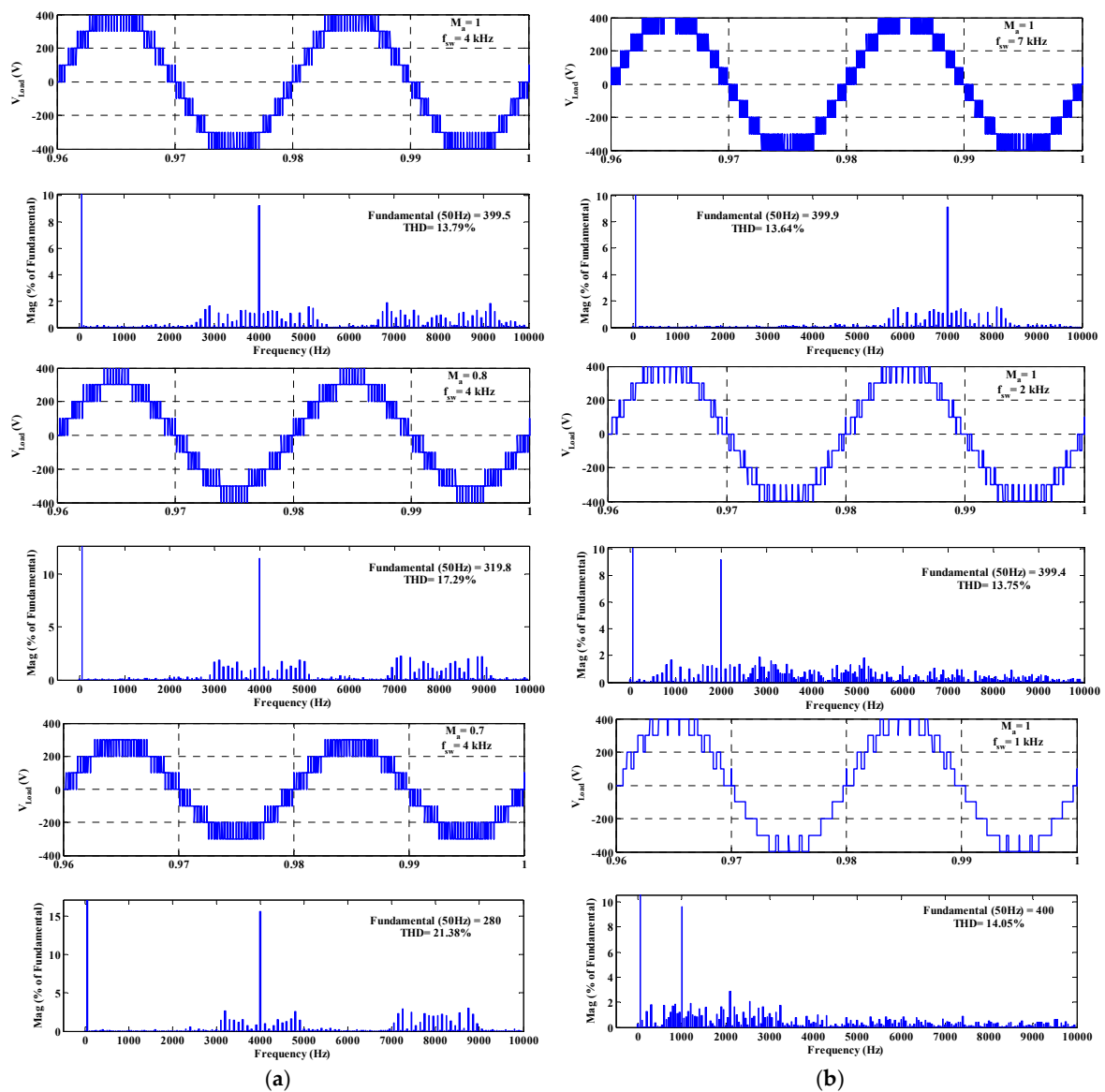

Figure 9. Voltages across the switches.

Figure 10. The effect of (**a**) modulation index on the V_{Load}, (**b**) switching frequency on the V_{Load}.

To validate the high performance of the proposed model, a low-power prototype of the proposed inverter has been implemented and tested. Accordingly, a Texas Instruments (TMS320F28335) fixed-point DSP control board generated gate pulses for employed switches (IRFP460 500 V/20 A). Moreover, the value of capacitances and input DC source are selected at 2300 µF and 140 V, respectively. Figure 11 illustrates the results obtained from the hardware implementation of the proposed inverter model under steady-state and transient operating conditions. These figures fully confirm the flawless performance of the proposed inverter.
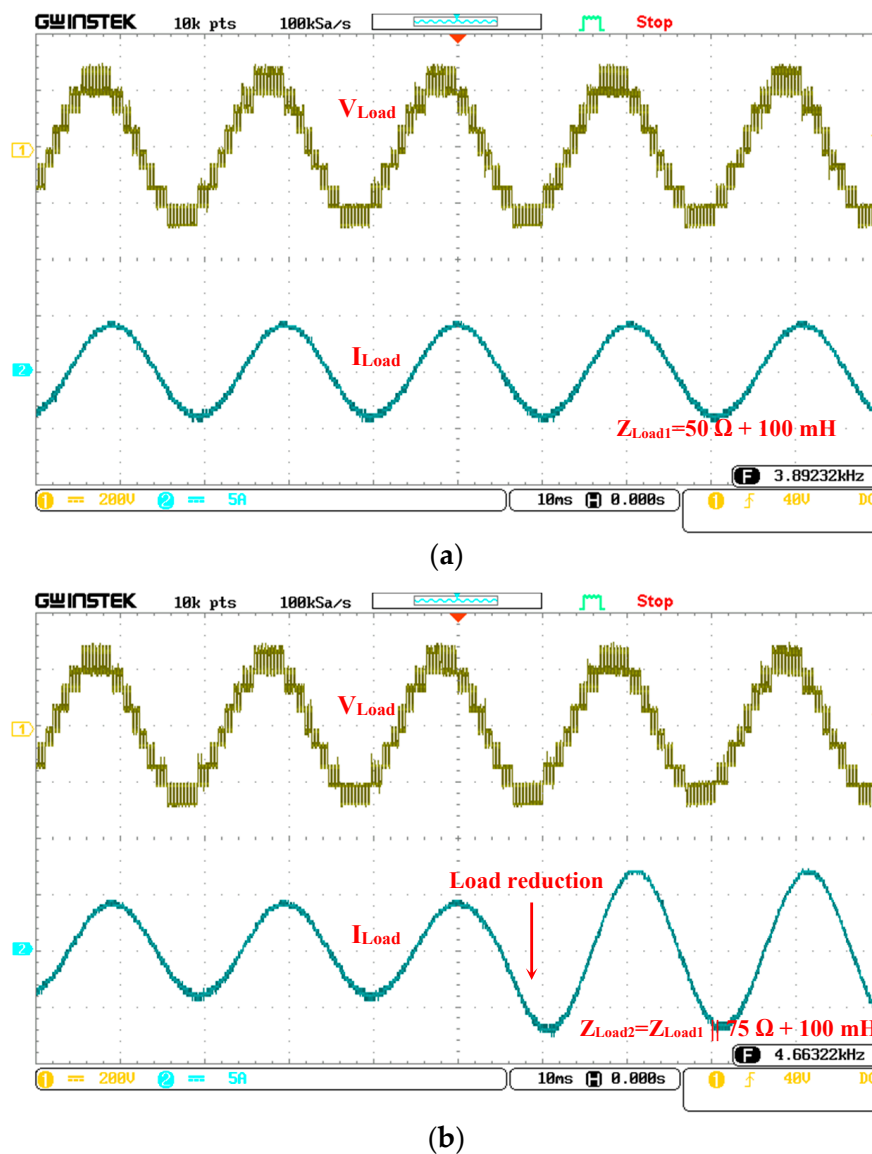
(**a**)

(**b**)

Figure 11. Output voltage/current under, (**a**) constant load; (**b**) step change in the load.

6. Conclusions

Herein, the operating principle of a new 9 L inverter has been discussed and confirmed experimentally. The comparative analysis depicted that the presented topology not only reduces the number of semiconductors/DC links required for generating a 9 L voltage waveform, but also employs IGBTs with lower PIV. These merits lead to a high compactness and cost reduction of the conversion system. Due to the intrinsic self-voltage balancing ability, there is no need for complex modulation methods. Thereupon, it enjoys simple control and implementation. Furthermore, the theoretical efficiency demonstrated that the presented configuration has higher efficiency by increasing output power (up to 2000 W). Eventually, the feasibility and effectiveness of the proposed model was verified by the simulation and experimental results.

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Nomenclature

MLIs	Multilevel inverters
CHB	Cascaded H-bridge
NPC	Neutral point clamped
FC	Flying capacitor
TSV	Total standing voltage (V)
PIV	Peak inverse voltage (V)
PWM	Pulse width modulation
DSP	Digital signal processor
V_{IN} and I_{IN}	Input voltage (V) and current (A) of the inverter
V_{Load} and I_{Load}	Maximum load voltage (V) and current (A)
V_t	Triangular carrier of the PWM modulation
V_{ref}	Reference waveform of the PWM modulation
V_S and I_S	Voltage (V) and current (A) of the switch S
ΔV_{ripple}	Voltage ripple across each capacitor (V)
ΔQ_C	Maximum discharging value of the capacitor C
N	Number of power switches with the same PIV
M	Number of cascaded modules
A_t and f_t	Amplitude and frequency of the triangular carriers (V_t)
A_{ref} and f_{ref}	Amplitude and frequency of the reference waveform (V_{ref})
P_C	Conduction loss (W)
P_S	Switching loss (W)
P_R	Power loss caused by capacitor voltage ripple (W)
$P_{S,\,on}$ and $P_{S,\,off}$	Turn-on and turn-off power loss of the switch S (W)
P_{out}	Inverter output power (W)
R_S and R_D	ON-state resistance of the switch S and its parallel diode (Ω)
R_C	Capacitor internal resistance (Ω)
R_{eq}	Equivalent value of the parasitic resistance in each voltage level (Ω)
R and L	Resistance (Ω) and inductance (H) of the load
t_{on} and t_{off}	Rise and fall times of the switch S (s)
f_S	Switching frequency (Hz)
T_j	Semiconductor junction temperature (°C)
T_c	Semiconductor case temperature (°C)
T_s	Heat sink temperature (°C)
T_a	Ambient temperature (°C)
Z_{th}	Thermal impedance between junction and case of the semiconductor
Z_c	Thermal impedance between semiconductor case and its heat sink
Z_s	Thermal impedance between heat sink and ambient

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