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Research of Low Inductance Loop Design in GaN HEMT Application

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Abstract—High electron mobility transistor (HEMT) is one popular research topic in the field of power electronic devices. Gallium Nitride (GaN) HEMT has the advantages of high slew rate and low operation loss. In high frequency application, parasitic impedance introduced from PCB layout can have huge impact on operation efficiency and reliability. Minimizing the loop inductance is important. In this paper, three different low inductance loop design methods are analyzed and compared in details. Numerical comparison based on finite elements analysis (FEA) is carried out. Double pulse test is carried to verify the idea. Simulation and experimental results of switching transient are given for comparison. Low inductance loop design is further corroborated by the switching loss and switching time characterization.

Keywords—GaN HEMT; low inductance loop design; parasitic extraction; switching characterization

I. INTRODUCTION

Along with the development of power transistor, efficiency and power density of converter has been improved dramatically through the last four decades. During this process, evolution of semiconductor material plays an important role [1]-[3]. First commercial transistor switch is introduced as silicon metal oxide semiconductor field effect transistor (Si MOSFET) in 1976 [4]. Structure and manufacturing process of Si MOSFET has been steadily optimized and improved ever since. Commercial Si MOSFET in recent year's market has already reached the theoretical boundary of Silicon semiconductor characteristic [5]. Novel semiconductor material is critical for the next generation transistor development.

Wide band gap semiconductor material, Gallium Nitride and Silicon Carbide (SiC), is widely recognized as the promising solution for high performance power transistor fabrication [6]-[8]. Benefit from wide semiconductor bandgap, HEMT has much lower parasitic capacitance and much lower on-state resistance than its Silicon counterpart [9]-[11]. Compared with SiC HEMT, GaN HEMT even shows more potential in high frequency application, which already dominates the commercial HEMT market of low to medium voltage range. Slew rate of GaN HEMT can be as high as 100V/ns [12]. During such high dv/dt switching condition, the parasitic inductance from PCB layout has a critical impact on the GaN HEMT switching performance [13], [14]. To fully

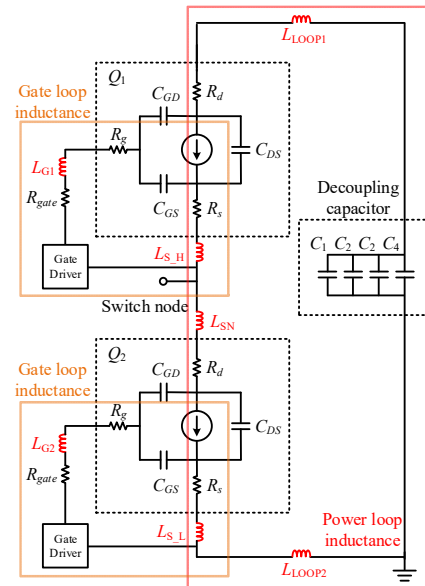


Fig. 1. Parasitic inductance in GaN HEMT switching module.

harness the potential of GaN HEMT in high frequency application, research of low inductance loop design is essential.

Parasitic impedance in the half-bridge GaN HEMT switching module is shown in Fig. 1. Q_1 and Q_2 are the equivalent circuit of high side and low side GaN HEMT respectively. Parasitic capacitors inside the GaN HEMT are the chief source of power loss during the switching operation, where input capacitor ($C_{iss}=C_{GS}+C_{GD}$) leads to gating loss and output capacitor ($C_{oss}=C_{GD}+C_{DS}$) leads to switching loss [15], [16]. For PCB layout, special attention should be paid to minimize inductance of the two highlighted loops shown in Fig.1: gate loop and power loop. Gate loop inductance shall detriment the gating safety and slow down the switching speed. Power loop inductance shall increase the voltage over shoot in the transistor drain-source voltage, which affects the operation reliability as well as leads to additional switching loss. The source inductance of transistor (L_{S_H} and L_{S_L}) is part of both gate loop inductance and power loop inductance [17]. Kelvin connection is adopted by some GaN HEMT manufacturer to decouple it from the power loop [18], [19]. Low inductance

PCB layout design has been widely researched in academia to improve the GaN HEMT switching performance [20]-[23]. In [24], several popular low inductance loop designs are introduced and compared. Theoretical analysis is given, while quantitative analysis is absent for comparison.

In this paper, different low loop inductance design methods are analyzed and compared in details. FEA based on ANSYS Q3D is given for quantitative comparison. According to the subtracted parasitic inductance, power loop is modelled in LTSpice. Based on double pulse test, simulation and experimental result are given to verify the analysis. Finally, switching loss and switching time characterization based on the low inductance loop design are given to validate the low inductance design. The paper is arranged as follows: In Section II, low inductance loop designs are introduced and compared based on FEA analysis and simulation. Experimental validation is given in Section III. Section IV concludes the paper.

II. LOW INDUCTANCE LOOP DESIGN ANALYSIS

A. Design methodology

For low inductance loop design, the chief idea is to minimize the total PCB track length of the power loop. Since gate loop and power loop shares the same design idea, this paper will explain the mechanism based on power loop. Three different low inductance loop designs of the half bridge GaN HEMT switching pair is shown in Fig. 1. Arrowed loop shows the current flow path during the switching pair operation.

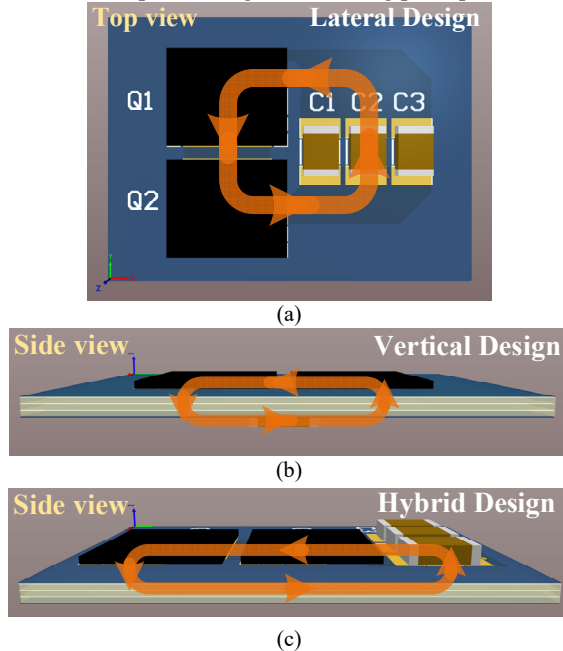


Fig. 2. Parasitic loop inductance in GaN HEMT switching pair: (a) Lateral design (top view) (b) Vertical design (side view) (c) Hybrid design (side view).

Lateral design places the GaN HEMT pair and decoupling capacitors on the same side. All the PCB tracks are located on the top layer of the board. This method is intuitive and doesn't

require for multi-layer PCB. However, the magnetic field generated by this loop is vertical to the PCB board, which may affect the operation of surrounding electric magnetic interference (EMI) sensitive components.

Vertical design solve the EMI problem by placing the GaN HEMT and decoupling capacitors on different side of the PCB board. Decoupling capacitors are placed right beneath the transistor pair and the length of power loop is minimized. Furthermore, current flow on each side of PCB board are in opposite direction. Magnetic field generated by the power loop is self-cancelled, which can help to reduce the parasitic inductance. Drawback of this method results from the PCB board thickness. In a multi PCB design, the total length of power loop is longer with extra middle layers, which shall increase the parasitic inductance. In addition, heat sink design is limited by the position of decoupling capacitors. Vertical design is not preferred for transistors that requires bottom side heat dissipation.

Hybrid design is a trade-off between the two methods mentioned above. GaN HEMT pair and decoupling capacitors are placed on the top layer, which forms the current charging loop. Current returned path is located at the adjacent layer beneath the top layer, where the two paths are connected by a group of vias to form a close loop. Compared with vertical design, parasitic inductance is decoupled from PCB board thickness. Power loop magnetic maintains self-cancelled. However, power loop length of hybrid design is longer than vertical design when applied in large package device routing.

B. Finite Element Analysis

Finite element analysis is a numeral method for solving engineering physic problems. To provide a numeral view and detailed comparison of the low inductance designs mentioned above, each design is applied respectively in PCB routing of the GaN HEMT switching pair, which is composed of two 650V GaN HEMT (GS66516B) and three decoupling capacitor (C1812 packaging). PCB model from Altium Designer is imported to ANSYS Q3D for FEA analysis. Excitation and sink points are added according to the current flow during switching pair operation. Parasitic inductance of each design is subtracted and shown in TABLE I.

TABLE I
POWER LOOP INDUCTANCE COMPARISON

	Lateral Design	Vertical Design	Hybrid Design
L_{SN}	0.06nH	0.06nH	0.06nH
L_{LOOP1}	3nH	0.46nH	0.02nH
L_{LOOP2}	0.63nH	0.59nH	1.21nH
Sum	3.69nH	1.11nH	1.29nH

L_{SN} is the parasitic inductance at the switching node, which is extracted from the connection cooper between the high-side transistor source pad and the low-side transistor drain pad. L_{SN} is the same for three designs for the identical transistor pair placement. L_{LOOP1} and L_{LOOP2} are the parasitic inductance between the switching pair and two terminals of the decoupling capacitors. Benefit from the magnetic field cancellation, vertical design and hybrid design can each reduces 70% parasitic inductance compared with the lateral

design. L_{LOOP1} and L_{LOOP2} is highly dependent on the package of transistor pair and decoupling capacitor. L_{LOOP1} and L_{LOOP2} are similar in vertical design for the symmetrical components placements. In the hybrid design, L_{LOOP2} is the dominant part of the loop inductance, which is resulted from the long ground returned loop in the middle layer.

C. Application Scenario Analysis

TABLE II
APPLICATION CHARACTERISTIC COMPARISON

	Lateral Design	Vertical Design	Hybrid Design
Lateral Space	494.25mm ²	247mm ²	316.8mm ²
Horizontal Distance	1 layer	Board thickness	2 layer
Device Placement	1 side	2 sides	1side
Magnetic Cancellation	No	Yes	Yes

Application characteristic of three designs is shown in TABLE II. Vertical design takes up least lateral space, while, on the other hand, requires for vias through the whole PCB board to form a close conduction loop. Loop inductance of vertical design is sensitive to the board thickness. Hybrid design and lateral design are not sensitive to the board thickness. They both place all the switching pair components on the same side. Hybrid design adopts the adjacent PCB layer for ground returning which helps to maintain the magnetic cancellation.

According to the analysis above, application scenario of each design method can be summarized as follows:

- Lateral design is favored in constraint layer application.
- Vertical design is favored in large package transistor application, when the lateral inductance dominates the power loop impedance.
- Hybrid design is favored in small package GaN HEMT application, as well as transistor that requires bottom side heat dissipation.

III. DOUBLE PULSE TEST VALIDATION

A. Double Pulse Test

Double pulse test is a general method for GaN HEMT characterization and switching transient analysis. Minimization of loop inductance is critical for accurate loss calculation. To validate the feasibility of the researched low loop inductance design, double pulse test is carried out.

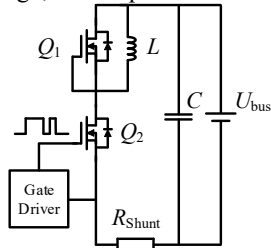


Fig. 3. Double pulse test circuit.

Double pulse test circuit can be shown as Fig. 3. Inductive load is clamped to the high side transistor. High side transistor gate is pulled down to act as the current circulating path during the low side transistor gated off. Double pulse signal is added to the gate of low side transistor. The first pulse is designed to charge the inductor to a desired load current. The second pulse provides an extra switching cycle for transient analysis and loss calculation. Test condition and test equipment are shown in TABLE III.

TABLE III
TEST CONDITION AND EQUIPMENT

Condition	Value	Equipment	Model
Voltage rate	400V	Voltage probe	LeCroy PP008
Current rate	5~30A	Current Probe	AP015
Inductive load	0.633mH	Digital oscilloscope	LeCroy 104MXs-B (10GB/s)
Gate resistor	10 Ω, 2 Ω	Controller	TI C2000

GaN HEMT GS66516B is chosen as device under test (DUT). According to analysis in the last section, hybrid design is adopted for low inductance design in both gate loop and power loop. GS66516B is driven at 400V, 5~30A switching condition. Voltage probe with ground clip is used to obtain the accurate drain-source voltage waveform. Low inductance current shunt method is used for current measurement and shunt gain factor is calibrated according to inductor current measured by current probe. The experiment setup of double pulse test is shown in Fig. 4.

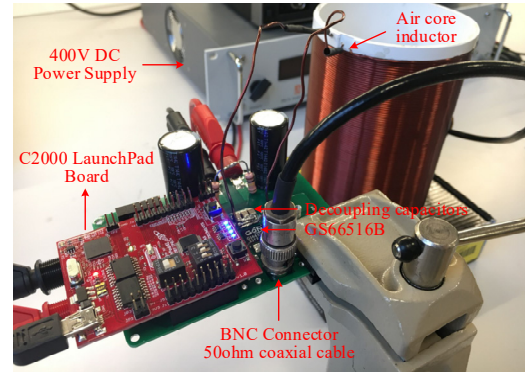


Fig. 4. Experiment setup of double pulse test.

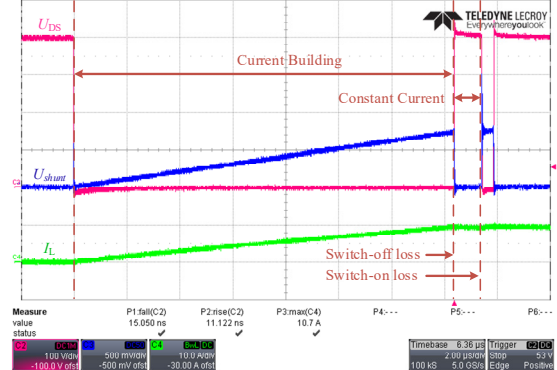


Fig. 5. Experimental result at 400V, 10A.

Experimental result is shown in Fig. 5. During the current forming stage, inductor is charged to 10A and DUT is switched off at the end. During the interval, inductor current keeps almost constant while circulating in the high side transistor. After 1 μ s, low side DUT switches on again. Accordingly, switch on and switch off transient at the same voltage/current rate is captured at the notated point in Fig. 5.

B. Switching Transient Analysis

Transistor in double pulse test is in hard switching condition. Voltage ringing is expected to exist in drain-source waveform when the transistor is switched off. This ringing is resulted from the oscillation between transistor output capacitor and loop parasitic inductance. To validate the analysis of low inductance loop design, simulation of double pulse test is carried out in LTSpice. Parasitic inductance extracted by ANSYS Q3D is added to the simulation circuit. Simulation model of GS66516B is obtained from the manufacturer.

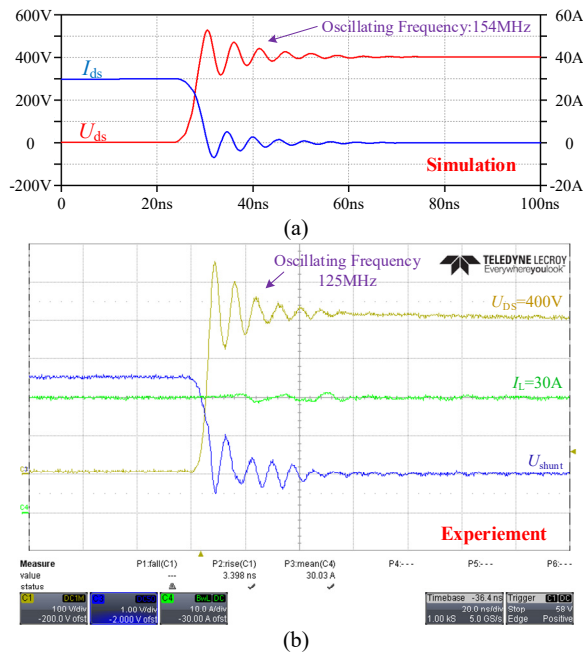


Fig. 6. Comparison of DUT switch-off transient: (a) Simulation waveform (b) Experimental waveform.

Comparison of DUT switch-off transient is shown in Fig. 6. DUT is switching at 400V, 30A. Experimental results and simulation results are similar in oscillation waveform, which validates the analysis above. Benefit from the low loop inductance design, waveform shows tolerable voltage and current ringing during the switch-off transient. Oscillating frequency is 154MHz in simulation result and 125MHz in experimental result. Drain-source voltage overshoot is 32% in simulation results and 37% in experimental results.

C. Switching Characterization

Based on the low inductance loop design, switching characterization of GS66516B is carried out. Data captured during the switching cycle is processed in MATLAB, which is

shown in Fig. 7. Switching loss is calculated according to the integral of instant loss power during the switching transient. Common mode noise coupled in the drain-source voltage and current waveform cannot be fully eliminated. However, positive and negative part of the noise signal is self-cancelled in loss calculation, which will not violate the measurement results.

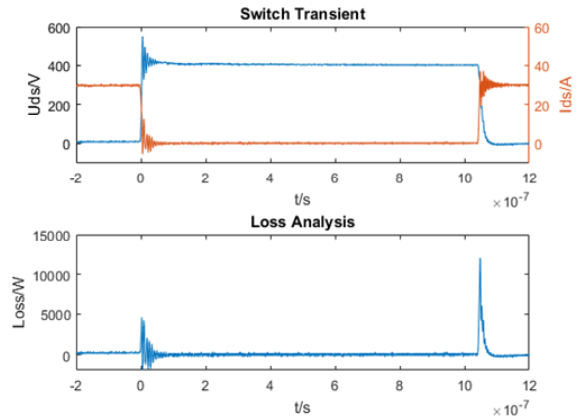


Fig. 7. Comparison of DUT switch-off transient: (a) Simulation

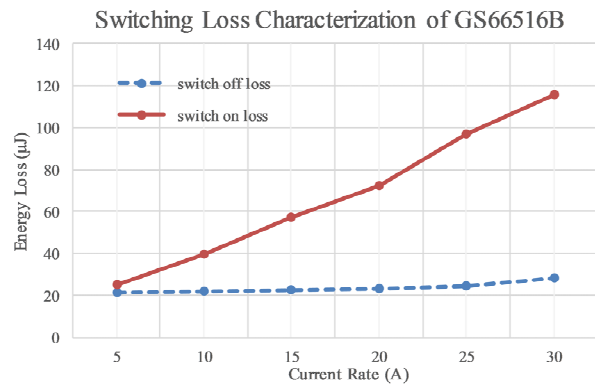


Fig. 8. Switching loss characterization.

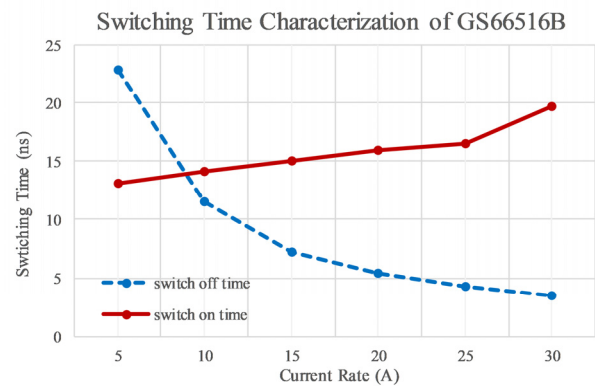


Fig. 9. Switching time characterization.

Switching loss characterization is shown in Fig. 8. GS66516B is switching under 400V, 5~30A condition. Switching loss rises in the higher load current range. Switch-on loss is the dominant part, which is resulted from the charging and discharging process of transistor output capacitor. Compared with the data from the application note of GS66516B evaluation board, total switching loss is reduced by 20%, which validates the low inductance loop design. Switching time characterization is given in Fig. 9. Switch on time increases and switch off time decreases in a higher switching current, which is resulted from the Miller plateau voltage shifting. In 30A switching condition, GS66516B can switch off in 3.47ns. Accordingly, slew rate of this point is 108V/ns, which is consistent with the manufacturer datasheet.

IV. CONCLUSION

In this paper, low inductance loop design for PCB layout is researched in details. Compared with lateral design, vertical design and hybrid design can reduce parasitic inductance by more than 70%. Vertical design has even lower parasitic inductance, but is restricted by board thickness and placement of heat sink. To validate the design, double pulse test of GaN HEMT is carried out. Experimental results of the switching transient is consistent with the simulation waveform. Switching loss characterization corroborates the design effectiveness. Switching time characterization validates the high slew rate capability of GaN HEMT based on low inductance loop design.

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