Design Considerations of Data Converters for Industrial Technology

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***Abstract*—This paper presents circuit design considerations of high resolution data converters applied for industrial technology, some important design issues related to filter in analog-to-digital converters (ADCs) are discussed. Whole design flow about filter is given in this work and the design considerations mentioned in this paper are useful for the industrial practice and applications of high resolution ADC, finally, a practical design is illustrated with discussion of $\Sigma\Delta$ modulator.**

***Index Terms*—Analog-to-Digital Converter, Nyquist-Rate ADC , Noise Transfer Function, $\Sigma\Delta$ Modulator, Over-sampling ADC.**

I. Introduction

In the real world, all signals in the nature are essentially analog signal. Before the middle of the 1970s, almost all of the signal processing is carried out in the analog domain. Over the past 30 years, very large scale integrated circuits have appeared and because noise suppression capacity of digital circuit is much better than that of the analog circuit, various signal processing functions can be performed with higher accuracy, higher reliability, and much lower price in the digital domain than analog domain.

In the data process of storage and transmission by using analog techniques, the noise and distortion will be accumulated, which disturbs the original signal, while in the digital domain, digital signals can be stored and transmitted without any loss. In industrial monitoring, telecommunications, voice, video, computer and many other fields, in order to make full use of these advantages of digital signal processing, analog signals are often converted into digital signals by data converters, therefore, the data converter circuit becomes very critical. Data converters include analog to digital converters (Analog-to-digital, converter, ADC), and digital to analog converters (Digital-to-analog, converter, DAC), which are essential components for analog and digital domains. At present, in typical digital signal processing (Digital, signal, processing, DSP) systems, as shown in Fig. 1, first, the analog signals are converted to digital signals through ADC, then the digital signal processor processes the digital signals, finally, the processed signals are converted into analog signals through DAC. Digital signals are discrete in amplitude and time, while analog signals are continuous in amplitude and time. ADC has two important performance specifications: speed and precision. The speed reflects how fast discretization is in time, and the precision reflects how accurate the discretization is in amplitude. Effective number of bits (ENOB) are often used to characterize the conversion accuracy characteristics.

Modern complicated data converter consists of many analog units such as operational amplifier, sample hold circuit, comparator, etc. The design of data converters combines analog and digital technologies. Data converters are the bottleneck of the digital signal processing system and their precision requirements are at least equal to the accuracy of digital processors. However, in the past more than 10 years, digital signal processing capability has developed very fast, while progress of ADC has been slow. Today, digital signal processors process data much faster than ADC can provide (in many digital systems, ADC becomes a bottleneck). Therefore, in analog to digital conversion, any improvement in analog circuits always excited the digital designers, and its improvement always improved the performance of the whole system.

ADC is mainly divided into Nyquist-Rate ADC and Over-sampling ADC. The disadvantage of Nyquist ADC lies into the fact that their accuracy can not be very high. This is due to the limited process matching of analog components. If no correction or trimming technology is applied, Nyquist ADC can actually only achieve an accuracy less than 14 bits. On the other hand, the basic principle of $\Sigma\Delta$ modulator is oversampling and noise shaping. Band quantization noise is eliminated by digital decimation filter, then its precision can reach 32 bits [1], therefore, over-sampling ADC is widely used in filed of industrial technology.

In the process of designing a $\Sigma\Delta$ ADC, $\Sigma\Delta$ modulator

Fig. 1. Typical digital signal processing (DSP) system

is the main functional part in it, in this paper, a third-order feedforward structure is uesd in the modulator, simulation results show that the signal bandwidth of modulator has reached 50KHZ, the signal to noise ratio (SNDR) and Spurious Free Dynamic Range (SFDR) are 66.94 dB and 75.87 dB respectively, and effective number of bit (ENOB) reaches 10.83 bits. The remainder of this paper is organized as follows. Section II concludes some important progress of ΣΔ ADC in recent years, and section III describes design considerations, circuit architecture and simulation results. The conclusions are finally drawn in section IV.

II. Overview of progress in ΣΔ Analog-to-Digital Converters

Multi-bit ΣΔ modulators with the modern deep-submicron CMOS process are widely used in analog-to-digital conversion [2], [3]. As the quantizer resolution of ΣΔ modulators increases, the SNR performance improves. However, the feedback DAC has to maintain high linearity. The general practice to achieve that is to use dynamic element matching (DEM).

In [4], a 4-bit Data Weighted Averaging (DWA) DEM circuit unit has been realized, and then is verified in a third-order four-bit continuous-time ΣΔ modulator with a 1% standard deviation added to the current sources. At first, the 15-bit thermometer codes of the quantizer will be rotated by a barrel shifter, and then be converted to feedback DAC switch control signal. Simulation results show that DEM improves the SFDR from 65.14 dB to 75.08 dB. In [5], an improved DWA technique is applied to improve the performance of SAR ADC.

Although DEM is an effective method to improve performance of ΣΔ modulator, the hardware consumption is not negligible, leads to an extra power consumption. The methodology proposed in [6] can greatly reduce the complexity or even avoid usage of DEM for multi-bit ΣΔ modulators. The proposed methodology (truncation error shaping and cancellation) can reduce the feedback DAC levels for multi-bit quantizers. This work has achieved targeted performance without DEM at low power consumption with small silicon area.

In recent years, to satisfy with the urgent demand of portable electronic products as well as need of saving energy in large electronic systems, low voltage and low power design have become the mainstream of ΣΔ ADC design. For example, a gain-boost class C inverter has been reported to replace traditional OTA to save power. Meanwhile, an on-chip body bias is used to compensate the performance degradation of the inverter [7]; Another low power ΣΔ ADC design has been reported in [8], in this work, an oversampling, noise-shaping SAR ADC architecture has been designed, which achieves 10-bit ENOB with an 8-bit SAR DAC array. A noise-shaping scheme shapes both comparator noise and quantization noise. This work utilizes highly efficient charge-redistribution SAR ADC to counteract the disadvantages of the conventional ΣΔ ADC, which is a typical hybrid architecture ADC design [9]. Nowadays, many noise shaping SAR ADC have appeared on the top journals and top conferences in the field of microelectronics, for instance, an ultra-low power 0.46 mW noise-shaping SAR ADC with 5MHz Bandwidth and 79.7 dB-SNDR incorporating a dynamic-amplifier-based FIR-IIR filter has been published in 2017 IEEE International Solid-State Circuits Conference (ISSCC) [10]; A low power 2.4-mW 300-MS/s passive noise shaping SAR ADC with 25-MHz Bandwidth [11] and a 4.2 mW 10MHz BW 74.4 dB SNDR fourth-order CT DSM with second-order digital noise coupling utilizing an 8b SAR ADC [12] have been published in 2017 Symposium on VLSI Circuits; Furthermore, an 84 dB dynamic range 62.5–625 kHz bandwidth clock-scalable noise-shaping SAR ADC with open-loop integrator using dynamic amplifier has been designed [13]. In a conclusion, noise shaping SAR ADCs have become research focus over the years [14].

III. Design and Realization of Filters in ΣΔ modulator

The architecture of modulator is usually classified into four kinds: a feedback type ΣΔ modulator, a feed-forward ΣΔ modulator, a feedback ΣΔ modulator with a resonator and a feed-forward ΣΔ modulator with a resonator. These four kinds are commonly used, and some are feed-forward and feedback hybrid or improved on these basic frameworks [15].

In this work, the feed-forward modulator structure is selected, as shown in Fig. 2.

The feedforward architecture of signal transfer function (STF) is generally close to 1 (b_1=1, $b_2 \sim b_4$=0), but at high frequencies there will be peaking, then the noise and interference will be amplified; The advantage of the feedforward structure lies into the fact that the feedforward structure has many forward paths. When the input signal suddenly becomes large and the modulator is overloaded, the latter integrators are saturated, but the first few integrators still operate properly; The higher order modulator degenerates into lower order modulator until it is reduced to the first order, then the modulator is absolutely stable at this point. Therefore, the overload will cause the SNR to decrease, but it will not oscillate; When the input signal returns to normal, the lower order modulator automatically reverts to a higher order regulator without the additional reset process. Then the transfer

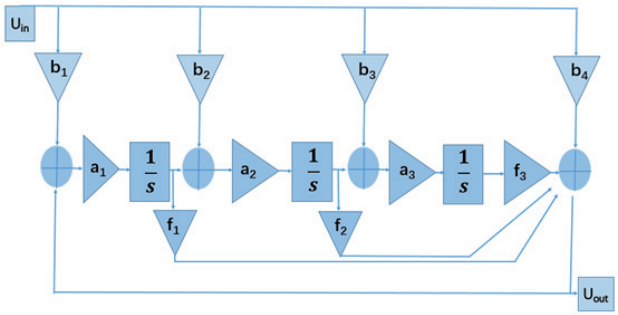

Fig. 2. Third order feedforward ΣΔ modulator

function derived from Fig. 2 is:

$$H_s = \frac{a_1 f_1 s^2 + a_1 a_2 f_2 s^1 + a_1 a_2 a_3 f_3}{s^3}, \quad (1)$$

After the structure is determined, the following parameters are needed to be confirmed: Order, oversampling rate (OSR), clock frequency (Fs). The common method is to use synthesize NTF function of matlab TOOLBOX to synthesize the transfer function, and then predict performance which the NTF can achieve by using the simulatesNR function. The oversampling rate is generally set to be 2, 4, 8, 16, 32 or 64, and here, we set it to be 64. Order corresponds to the order of filter we need, here, order is set to be 3. BW is the input signal bandwidth and also the passband frequency, which is set to be 50KHZ, so we can get a third order filter transfer function with a sampling frequency of 6.4 MHz, and ultimately, we need to realize the transfer function at the circuit level in cadence.

By using those above parameters of the filter, the amplitude response of noise transfer function (NTF) is shown as follows:

$$LFsRZ = \frac{1.224s^2 + 0.4663s + 0.8797}{s^3} \quad (2)$$

By comparison between formula (1) and formula (2), the following relationships can be obtained: $a_1 f_1 = 1.224$; $a_1 a_2 f_2 = 0.4663$; $a_1 a_2 a_3 f_3 = 0.8797$. Set $f_1 = 3$, $f_2 = 2$, and $f_3 = 2$, we get $a_1 = 0.408$, $a_2 = 0.571446$, and $a_3 = 0.188677$. Take them into the third order $\Sigma\Delta$ modulator for simulation, FFT result is shown in Fig. 4. Simulation results show that the signal-to-noise ratio (SNR) is 69.81 dB, and the ENOB is 11.11. These two specifications are the most important specifications to measure the performance of the filter. In addition, we need to record the output of each of the three integrators to ensure that each level of output does not exceed the supply voltage, so that the system is in stable.

In the third-order $\Sigma\Delta$ modulator, there are three integrators. The primary task of realizing a filter is to implement the integrator. A common structure in CT $\Sigma\Delta$ modulator is an active RC integrator. It has the advantage of better linearity

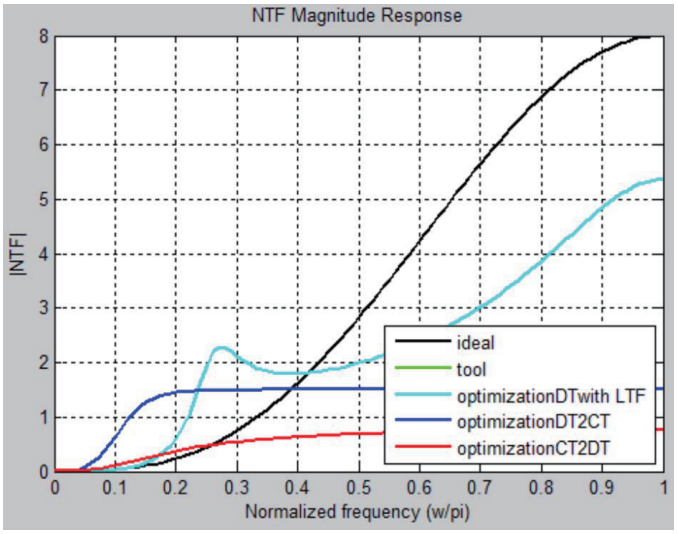

Fig. 3. Amplitude response of noise function

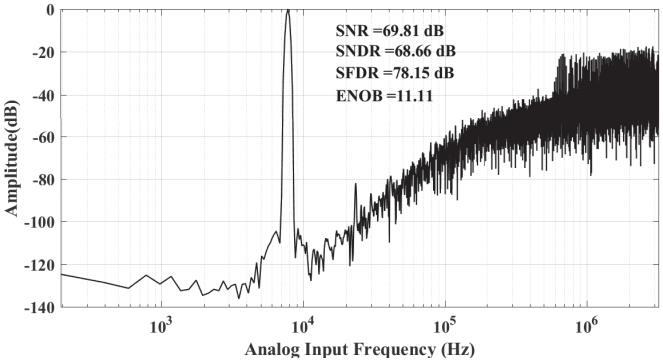

Fig. 4. Transfer Function of Filter

and larger signal swing. In contrast to other types, the Gm-C integrator can operate at higher frequencies or consume less power, but the architecture is more complicated. Moreover, MOSFTE-C integrator, which is similar to the Acitve-RC integrator, uses transistors which work in the linear region instead of integral resistors. It has the advantage of being able to continuously adjust the magnitude of the resistance, but with the disadvantage of being low linearity.

There are three integrators in a third-order filter, and there is a feedforward resistor at the output of each stage, let the unipolar output feedforward to the system, and in order to guarantee the output stability of the third level, especially a new feedforward resistance R0 has been added, as shown in Fig. 5.

The transfer function of active RC integrator is as follows,

$$H(S) = \frac{1}{SRC} \quad (3)$$

In this system, C1=10p, C2=5p, and C3=5p, which leads R'1=95.7KΩ, R'2=135.2KΩ, and R'3=340KΩ.

For feedforward resistors, the current equation is required at the output

$$\frac{V_I - V_{out}}{R1} + \frac{V_{II} - V_{out}}{R2} + \frac{V_{III} - V_{out}}{R3} = 0 \quad (4)$$

After simplification,

$$V_{out} = \frac{R2R3V_I + R1R3V_{II} + R1R2V_{III}}{R1R2 + R2R3 + R1R2} \quad (5)$$

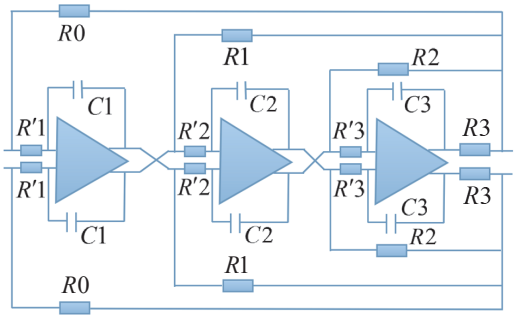

Fig. 5. The Third-Order Filter

The coefficient of the output voltage at each stage is related to the values of the resistors, then we can deduce that the coefficient of the resistance is R1:R2:R3=2:3:3, we set the value of R1, R2 and R3 are 1.66K, 2.5K and 2.5K respectively, and the value of R0 is 10K.

All the components in the circuit are finally set according to the above parameters, and at the output, a comparator and a simple logic unit are added to form a filter loop, differential operational amplifier is realized by Verilog-A. The simulation results are shown in Fig. 6, the red, green and purple waveform correspond to the output of the first stage filter, the output of the second stage filter and the output of the third stage filter respectively, during the simulation, output of every filter can not exceed the power supply, or else the system is not stable.

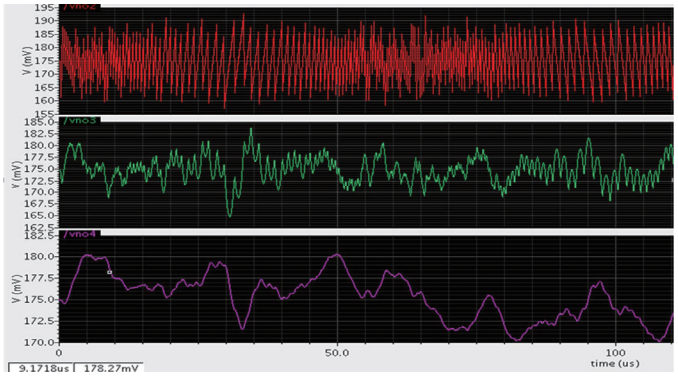

Fig. 6. Output of each stage of Third-Order Filter

Finally, Fig. 7 shows the FFT result, where SNR, SNDR and SFDR are 67.94 dB, 66.94 dB (10.83 ENOB) and 75.87 dB respectively, which approximate the FFT result in Matlab shown in Fig. 4, therefore, a reasonable third-order filter has been constructed.

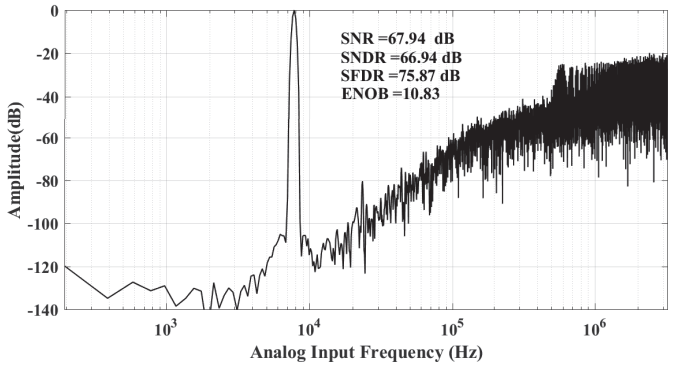

Fig. 7. Third-Order Filter

IV. Conclusion

Continuous-Time Sigma-Delta Modulator (Filter) is one of the most important directions of the Analog-to-Digital Converter, because it can achieve high bandwidth and low power at the same time. It would be widely applied in industrial and wireless areas. In this work, the modulator uses a third-order feedforward structure, through simulation, the signal bandwidth of the modulator reached 50KHZ, SNR, SNDR and SFDR are 67.94 dB, 66.94 dB (10.83 ENOB) and 75.87 dB respectively.

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