Stretchable Mould Interconnect Optimization: Peeling Automation and Carrierless Techniques

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***Abstract*—The primary bottleneck of the stretchable mold interconnect (SMI) technology is its reliance on carrier boards. These are necessary to handle the meandered circuit during production and to ensure dimensional stability of the flexible circuit board before encapsulation. However, for all the problems it solves, it also introduces a new major problem by requiring a peeling step – which is difficult to automate. This manuscript aims to present some of the work that went into eliminating this problem, discussing both unsuccessful and functioning methods to tackle this conundrum and some of the experimental work that went into verifying these techniques. First, alterations to the design to simplify peeling are considered, followed by adhesive-based peeling processes and mechanical pin-based systems. Next, masking and structuring of the carrier board adhesive are considered. Finally, two carrierless methods which circumvent the problems are discussed, a two-step process – which cuts temporary support structures after partial encapsulation – and a technique whereby the frame is designed to fail in a controlled manner during the first use of the circuit, creating a carrierless process feasible for high-volume production.**

***Index Terms*—SMI, stretchable, flexible, process development, automation, substrate peeling.**

I. Introduction

STARTING from the early days of imec's Stretchable Mold Interconnect (SMI) process, and similar technologies, process carriers are a common sight [1]–[4]. Using carrier boards makes sense from a process development perspective; meandered stretchable interconnects can rarely support themselves, causing them to get tangled up with each other or inside production equipment. The (reusable) carrier board prevents this potentially fatal production defect from occuring by holding onto the circuit using an adhesive layer, preventing the meanders from lifting off the carrier, and away from the rest of the circuit [5]. Once all pre-encapsulation steps are finalized the circuit is then transferred from the carrier into the final encapsulation material [6]–[9].

Sadly, introducing a carrier board also creates a bottleneck when attempting to implement the process on an industrial scale, it requires removing unwanted circuit elements – called *residuals*. In practice, a typical SMI process flow starts by applying a flexible circuit board (FCB) to a carrier board covered with a pressure sensitive adhesive or wax [10]. Next, the circuit outline – indicated in Fig. 2a – is patterned using punching or laser cutting the FCB without damaging the underlying adhesive layer [10]–[12]. Finally, the process operator removes the residual material not part of the circuit by manual peeling [7]. For some designs – and low volume production – manual peeling is an acceptable method; However, when looking towards industrialization, peeling is potentially problematic because no automated standard equipment to perform this step exists. Additionally, most of the yield loss occurs during peeling; as a result, a reliable automated residual peeling method is highly desirable.

Before diving into process details, the scale of the problem and materials commonly used should be defined. For a full process overview please consult recent publications by Plovie et al [10]. In all following sections, the typical FCB substrate used for the SMI process is 25 to $100\,\mu m$ thick with copper layers of $18\,\mu m$ to $35\,\mu m$, with a panel size of $9\,\mathrm{inch}$ by $12\,\mathrm{inch}$ or $12\,\mathrm{inch}$ by $18\,\mathrm{inch}$; larger sizes tend to require thicker substrates to maintain mechanical stability [11]. Polyimide flexible copper clad laminate (FCCL) from Dupont, UBE, and Shengyi were verified to be compatible with the developed processes, with a preference for SF305 (Shengyi Technology Co. Ltd., China) and Upisel-N SR1220 (UBE Industries Ltd., USA) due to availability and cost. The carrier boards are $1.6\,\mathrm{mm}$ or $2.4\,\mathrm{mm}$ thick FR-4 laminates (Hitachi Chemical, Japan) – chosen for its excellent mechanical stability. Thinner carrier boards tend to experience excessive bow and twist after thermal steps. As carrier adhesive, FH20LB Tacsil Tape (Taconic, Republic of Korea) was used and applied using the method presented in earlier publications [10]. First, the adhesive is roll laminated onto a clean FR-4 board at $180\,^{\circ}\mathrm{C}$ with a low feed speed, followed by 2 hours in a vacuum press at $200\,^{\circ}\mathrm{C}$ with $2\,\mathrm{MPa}$ of platen pressure applied. Finally, the carrier boards are pre-baked in a reflow oven using a representative profile of the solder alloy used in the final application. Next, the circuit is placed on the carrier using a hand roller, after which it is partitioned into a the circuit and residual material using laser cutting or punching. Finally, the residuals are removed – the focus of this paper.

Practically, the operator will peel the residuals by lifting the side of the residual using tweezers, scalpels or dental hooks and using the surrounding circuit as fulcrum to provide sufficient leverage if necessary, as illustrated in Fig. 1a, by

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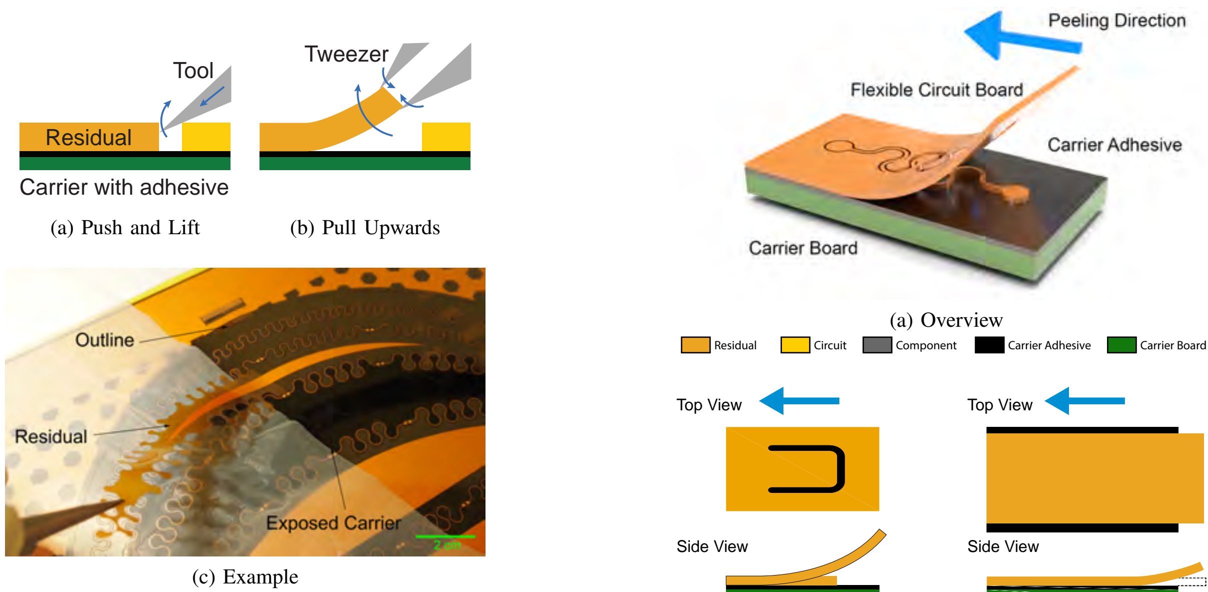


(a) Push and Lift (b) Pull Upwards

(c) Example

Fig. 1. To peel a residual, (a) the operator will use a tweezer or other tool to grab the edge of the residual and then (b) uses tweezers to remove the residual entirely. (c) An example of peeling of residuals in practice.

pushing against the side of the residual and attempting to lift it upwards. They will then use a tweezer to grab the residual and peel it away from the carrier, as illustrated in Fig. 1b and shown in Fig. 1c. To avoid problems with small residuals, it is best to peel them ahead of time. Furthermore, peeling from the centre outwards is desirable since it reduces the hazzle of partially peeled residuals sticking to the carrier board. Alternatively, a non-stick foil can prevent the peeled residual from sticking to the carrier, as illustrated in Fig. 1c.

The absolute minimum width of a polyimide trace of a horseshoe meander in the SMI technology is $\pm 250\,\mu m$, though high-yield processes tend to use $700\,\mu m$ or broader trace widths [10]. The minimum spacing to be maintained between outline definitions should exceed $1\,mm$ at the very least; higher values are desirable for the sake of process yield.

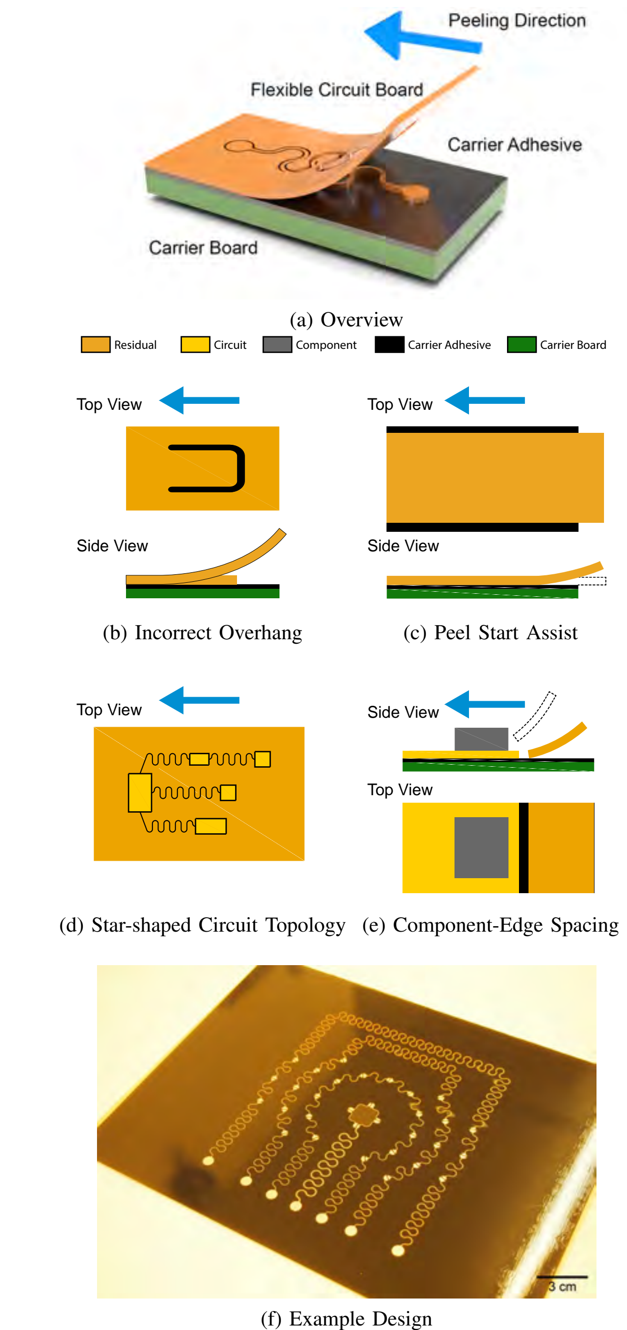
II. Peeling Automation

The first approach to tackling the bottleneck is automating the peeling process; the following sections list the approaches tested at a lab scale over the past few years, and discuss the feasibility of applying them for an actual manufacturing process. Wet etching of the polyimide using caustic solutions was not considered, as this would most likely cause damage to the carrier board [13].

A. Design Based

Panel-based processing is still prevalent in the circuit board industry due to the high volumes needed for roll-to-roll production. As a result, any process which fits within this panel-based production methdology without causing significant delays is still feasible if the residual material not part of the circuit can be removed with one swift pull (e.g. while preparing the press book).

The main factors to achieving a *peelable-design* are primarily related to the circuit layout and meander design choices.



(a) Overview

(b) Incorrect Overhang (c) Peel Start Assist

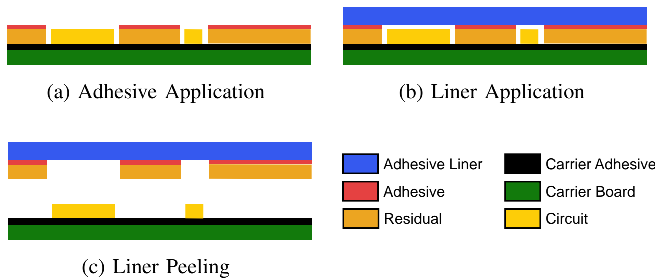
(d) Star-shaped Circuit Topology (e) Component-Edge Spacing

(f) Example Design

Fig. 2. Design strategies and features can ease peeling to the point where automation is no longer considered necessary: (a) Illustration of different parts of the structured FCB on a carrier. The blue arrow indicates the direction of peeling; (b) An overhang perpendicular to the direction of peeling might cause tearing of the flexible substrate near the overhang; (c) Making the FCB slightly longer than the carrier board makes peeling significantly easier by providing a starting position. (d) Star-shaped circuit topologies can be peeled in a single operation. (e) Components placed near the edge might cause the residual to hook behind the components, tearing the circuit away from the carrier. (f) An example of an easily peelable design after peeling.

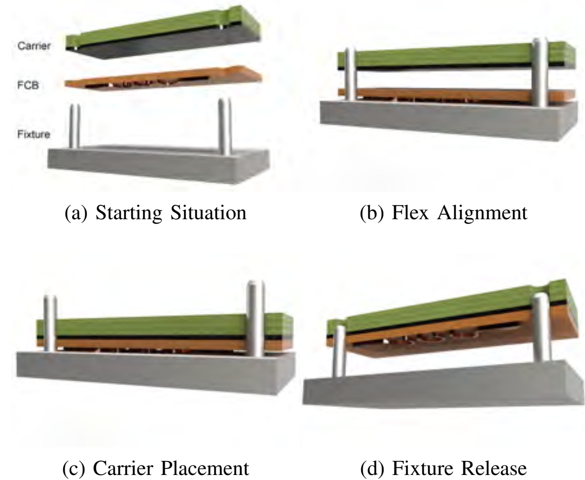
For a graphical overview, please consult Fig. 2, but the general guidelines can be described as follows:

- Ensure no overhangs exist from a peeling point of view as illustrated in Fig. 2b,
- Peel the circuit in-line with the meander axis (Fig. 2d),
- Use no meander designs which might lead to excessive



(a) Adhesive Application (b) Liner Application (c) Liner Peeling

Fig. 3. Local adhesive peeling applies an adhesive in a well-specified pattern to assist in removal of the residuals. (a) First, an adhesive is applied on top of the residuals; (b) A liner is placed on top of the entire circuit and the adhesive is cured, bonding the residuals to the liner; (c) The liner is peeled away, together with the residuals.



(a) Starting Situation (b) Flex Alignment (c) Carrier Placement (d) Fixture Release

Fig. 4. Alignment of a FCB on a carrier using a fixture: (a) Starting situation; (b) The FCB is placed on the pins with the top-side facing downwards; (c) The carrier board is placed on top with the adhesive side facing the FCB. (d) After applying firm pressure, both are removed from the fixture.

overhangs, such as spirals or horseshoe-shaped meanders with opening angles α greater than $10°$ [10],
- Ensure the carrier board is slightly shorter than the FCB to provide a convenient start point (Fig. 2c),
- Design circuits with a star-shaped topology so the residual material consists out of a single piece (Fig. 2d),
- Achieve maximum copper coverage on both the circuit and residuals to prevent tearing of the FCB material.
- Use large spacing between the circuit outline and copper features to avoid outline defects.
- Avoid placing components near the circuit outline to avoid peeling defects (Fig. 2e).

Respecting these guidelines, it is possible to peel the circuit with one swift movement, an example of a circuit which can be peeled in one swift move is visible in Fig. 2f. However, such designs are not always feasible due to electrical or mechanical constraints. Preferably the residual foil is peeled before assembly, strong air streams (e.g. nitrogen air knives) or excessive liquid (e.g. vapor phase reflow) can otherwise cause the circuit to release from the carrier prematurely.

B. Local Adhesive Peeling

Patterned adhesives form a simple and effective solution at first glance, an adhesive is applied to the residual FCB material, a sacrificial liner is placed on top and the adhesive is cured, after which the liner is pulled away together with the residuals, as illustrated in Fig. 3. None of the considered approaches (screen printed, UV (de)activated, pressure activated) following this principle proved feasible, additionally the overall economics of such a solution are questionable, the additional process steps and generated waste do not necessarily offset the cost of manual peeling.

C. Pin Board

The pinboard method and some of the other following methods require alignment of the FCB versus the carrier. At the same time, placement without the inclusion of air bubbles is paramount to the success of the outline definition process. To combine both requirements, we propose two methods: edge-based alignment and whole-flex alignment. Both methods require the use of alignment pins and accompanying holes in both the carrier board and FCB. Edge-based alignment uses two, or more, alignment pins in an area at the side of the substrate where no adhesive is present. The FCB is placed over these pins and is rolled onto the carrier board while applying tension to the FCB. Alternatively, the whole-flex method illustrated in Fig. 4, a frame can be made on which the FCB is tensioned over a set of alignment pins with the top-side facing down towards the frame (a); next, the carrier board is placed on top (b), with the adhesive facing downwards, and pressure is applied to attach the carrier to the FCB (c). The whole-flex method is preferable because there is less chance of wrinkling. When using a transparent tool, as shown in Fig. 5e, the FCB can be inspected before removal from the fixture (d).

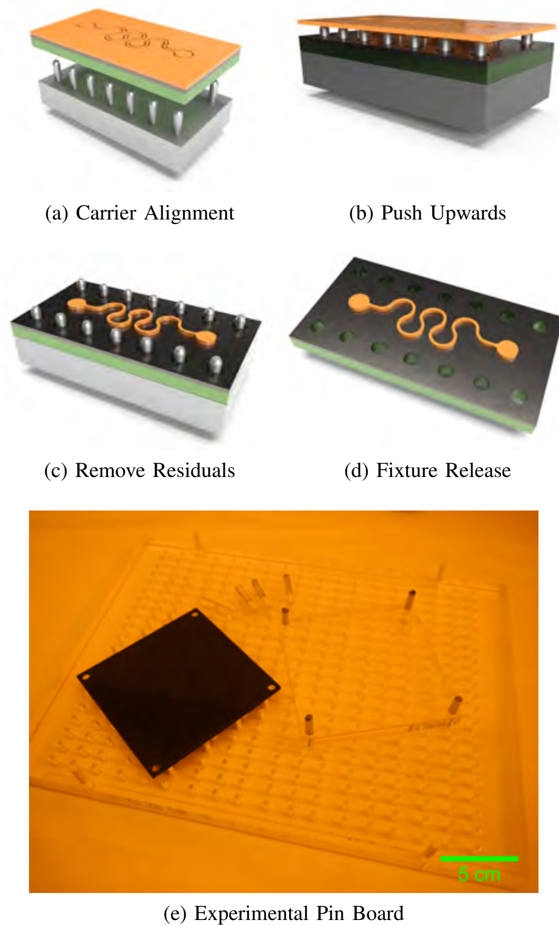
The pinboard approach, demonstrated in Fig. 5 makes use of a similar system to release residuals; Not only are perforations in the carrier board used for circuit alignment (a), but also for pusher pins capable of displacing the FCB material upwards and away from the carrier board (b). The residuals can then be blown away using a blast of compressed air (c). Lab-scale tests indicate this method works, but it comes with a few significant drawbacks:

- Producing small and clean perforations through a carrier board is difficult due to the presence of the adhesive layer.
- Removal by compressed air is far from perfect; small pieces still land on the board.
- Production tooling becomes design dependent.

Overall this approach has potential, and is feasible depending on the method used to make holes in the adhesive-covered carrier boards.

D. Adhesive Masking

Adhesive masking maintains the uniform adhesive layer on the carrier board and instead introduces a structured layer between the adhesive and the FCB. After outline definition the residuals should be easily removable from the carrier board, eliminating the need for a peeling step.

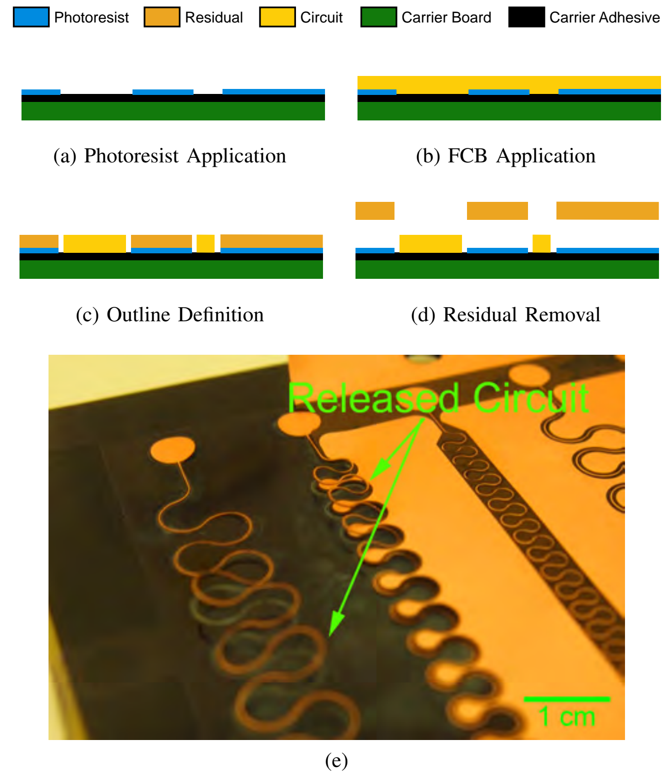


(a) Carrier Alignment (b) Push Upwards

(c) Remove Residuals (d) Fixture Release

(e) Experimental Pin Board

Fig. 5. Removal of the circuit residuals using a pin board: (a) Carrier board alignment over the pinboard; (b) Pressing the carrier down on the pins lifts the residuals away from the carrier board; (c) Residuals are removed by flipping the fixture upside-down or using a blast of compressed air. (d) Releasing the board from the fixture. (e) Alignment and pinboard tool for A4-sized circuit boards made out of clear plastic, with an alignment tool and carrier board for smaller 10 cm by 10 cm samples resting on top. Transparent plastic is used to provide to enable inspection of the result before releasing the board from the fixture.



(a) Photoresist Application (b) FCB Application

(c) Outline Definition (d) Residual Removal

(e)

Fig. 6. Adhesive masking techniques employ a non-stick layer (e.g. photoresist) to cover the carrier adhesive, defining zones where the residuals do not attach to the carrier. (a) First, photoresist is applied to the carrier; (b) After which the FCB is aligned and placed on the carrier; (c) Next, the outline of the circuit is defined through punching or laser cutting; (d) At which points the circuit residuals should fall off. Finally, the photoresist can potentially be stripped. (e) Board where dry-film photoresist acts as an adhesive mask. The meanders part of the circuit release from the carrier board the moment the residuals are removed, making further processing impossible.

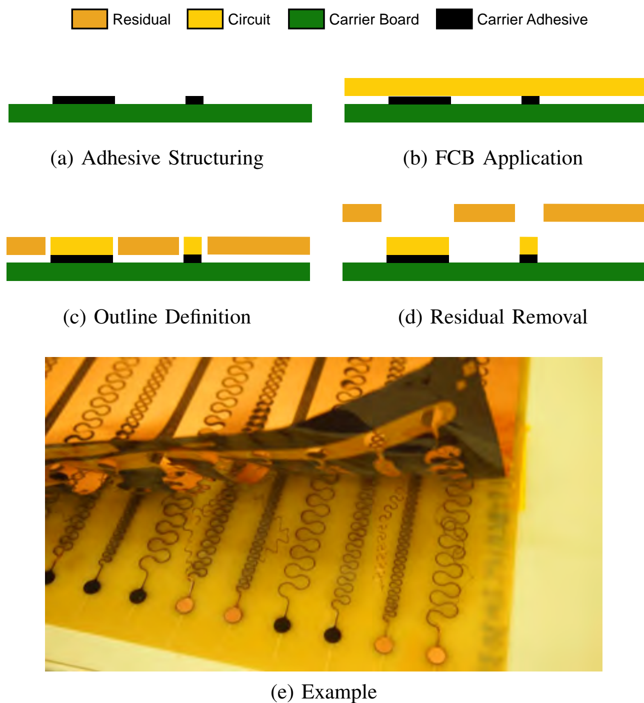
For this approach, illustrated in Fig. 6, a standard carrier board was first covered on both sides using 20 µm thick Riston FX920 (Dupont, USA) dry film photoresist, applied using hot roll lamination. First, the photoresist was patterned and developed using standard practices for circuit board production (a). As an additional step, the photoresist was baked at 120 °C for half an hour in a convection oven to eliminate the tackiness of the surface and to promote adhesion to the carrier [14]. The resist is patterned in such a way that it is present underneath the residual FCB material, preventing the residuals from adhering to the carrier board. Next, the FCB was aligned on the carrier board using the above method (b). Outline patterning proceeds as usual, for example, using a depanelling laser (c). Afterwards, the residuals should release from the carrier, leaving behind the circuit. However, two phenomena occurred virtually instantly depending on the design: either the complete FCB (circuit and residuals) instantly released from the carrier during laser outline definition, shown in Fig. 6e, or the residuals stuck to the photoresist when the photoresist was not baked beforehand.

As an alternative, 25 µm PTFE release foil (Holders Technology, United Kingdom) was applied to the carrier and laser structured. Similar issues appeared after applying the circuit and defining the outline, the desired circuit released from the carrier due to topological differences no matter how large the spacing between the outline edge and PTFE foil was.

E. Adhesive Structuring

An alternative to masking is directly structuring the carrier adhesive. Two viable methods exist to achieve this: Either the adhesive is selectively removed, by cutting an outline and peeling it away in the areas where the residuals should release, or locally destroying the adhesion, for example by superficial laser ablation.

For the first method, selective removal of the adhesive – illustrated in Fig. 7, the carrier adhesive tape was laser cut after application to the carrier board, and the areas where no adhesion was required were peeled away manually (a). Next, the flexible circuit board is placed on the carrier board and aligned to the patterned adhesive (b). Then the outline is defined using laser ablation or punching (c), after which the residuals should be easy to remove (d).



(a) Adhesive Structuring (b) FCB Application

(c) Outline Definition (d) Residual Removal

(e) Example

Fig. 7. Structuring the carrier adhesive removes the need for peeling by preventing the residuals from adhering to the carrier in the first place. (a) Structuring of the carrier adhesive; (b) Alignment and placement of the FCB; (c) Circuit outline definition using a depanelling laser; (d) Removal of the residuals by flipping the board upside-down or compressed air; (e) In practice, this method does not perform very well, while the residuals along the circuit release immediately, they drag the circuit along with them.

Practically, peeling the carrier adhesive proved to be difficult due to its tacky nature. The glass-fiber mesh contained within the adhesive tape also made laser cutting difficult, often requiring additional rework with a scalpel. After removal of all residuals, a series of additional issues arose, namely the remaining thin strips of adhesive easily shifted position on the carrier board. On top of that, they provided insufficient adhesion to the FCB to hold it in place during laser ablation, and the residuals entangled with the circuit after FCB outline definition – causing the circuit to release from the carrier as shown in Fig. 7e. Even if this issue could be solved (e.g. by stepping towards a stronger adhesive), an exposed carrier board would still lead to significant issues during the following process steps.

From this perspective destroying the adhesion with superficial laser ablation is far more attractive. To confirm this methodology the surface of the carrier adhesive was ablated using a picosecond pulse-length Nd:YAG UV laser (3D Micromac AG, Germany); a single low-intensity pass destroyed the adhesion entirely, but a significant amount of debris was left behind which affected the non-targetted areas as well. Quickly adhesion over the entire carrier board was lost, making this approach non-viable.

III. Carrierless Processes

Removal of the carrier would solve all of the above problems and simplify the encapsulation significantly. However, it would also remove the added stability provided by the carrier board, requiring the FCB has to support itself. Two possibilities come to mind, either an alternative carrier (e.g. disposable foil), or design modifications to enable the FCB to support itself. The former solution shifts the problem, while the latter solution appears risky. Nonetheless, removal of the carrier board is feasible if the minimum trace width increases to $1\,\mathrm{mm}$. At that point, a polyimide trace is unlikely to be damaged during manual handling if the circuit does not entangle, which is easily achieved using a support frame surrounding the circuit, as illustrated in Fig. 8. These FCBs might require some extra caution during handling, but behave much like any FCB.

The exact design requirements for such a frame are yet to be determined, and are most likely highly dependant on both substrate material and meander design. For example, it stands to reason that a higher trace width or shorter length meander would require less support. However, based on current experimental observation a few base rules were determined for designs using meanders with trace widths exceeding $1\,\mathrm{mm}$:

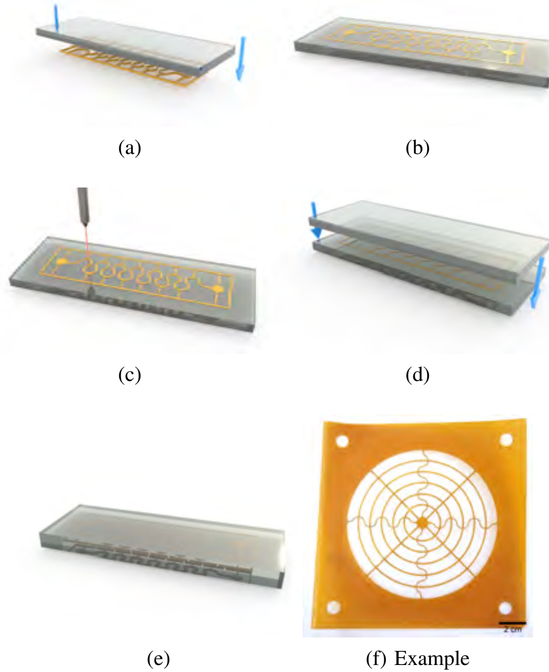
- For horseshoe-shaped meanders with values of $\alpha \leq 45°$, an unsupported meander can traverse a distance of at least $40\,\mathrm{mm}$ between two anchor points part of the frame.
- Two meanders placed within $30\,\mathrm{mm}$ of each other should be separated by a piece of the frame, with the individual meander segments attached to the frame.
- Islands for which repeatable positioning is desirable should be attached to the frame to prevent movement during encapsulation.
- Not each meander segment needs to be connected to the frame using a support structure.
- Large continuous copper surfaces should be avoided on the frame because these can lead to buckling due to a thermal expansion coefficients mismatch. Hexagonal, hatch or dot patterns are recommended for large copper surfaces.

Assuming the frame residuals can be left behind within the final device, an assumption which generally holds true, two approaches can be considered to remove the frame: two-step methods, which cut the frame after partial encapsulation, and controlled frame failure, where the frame is designed to fail under normal use conditions, releasing the circuit.

A. Two-Step Process

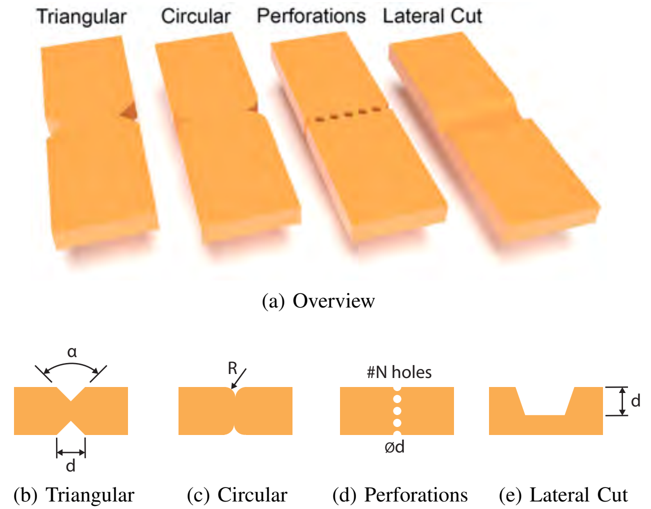
The process flow for the two-step approach requires a two-step encapsulation process, as illustrated in Fig. 8. First, the outline of the FCB is defined using punching or laser cutting, after which the circuit is partially encapsulated (a). The meanders are then released from the frame by flipping the device upside-down (b), and cutting the frame using a laser cutter or punch (c). This is then followed by final encapsulation of the device (d), resulting in a normal functioning stretchable circuit (e). The simplicity of this technique allows implementation of the SMI process in virtually any PCB manufacturing environment capable of handling flexible circuit boards.

This method was tested with multiple designs, one of which is shown in Fig. 8f, and achieved a $100\,\%$ yield over 14 samples. The only observed drawback is the fact that it leaves



(a) (b) (c) (d) (e) (f) Example

Fig. 8. Two-step processes remove the need for a carrier board by introducing a support frame which is cut during fabrication after partial encapsulation: (a) A structured FCB is partially encapsulated; (b) The partially encapsulated circuit is flipped upside down; (c) Laser cutting of the support frame, releasing the circuit; (d) Final encapsulation step; (e) Finalised circuit ready for use. (f) Circuit designed and fabricated using a two-step process. The majority of the frame was placed outside of the deformation area, meaning it does not affect the stretchability of the circuit.



(a) Overview

(b) Triangular (c) Circular (d) Perforations (e) Lateral Cut

Fig. 9. The controlled frame failure method depends on structures which fail when a given tensile load is applied. Four variants, easily manufactured using laser cutting, are proposed: (1) Top view of a triangular notch defined by angle α and distance d, (2) Top view of a circular notch defined by radius R, (3) Top view of perforations defined by the number of holes N and hole diameter $\varnothing d$, and (4) Side-view of a lateral cut with depth d. The results of tensile tests on these structures can be found in Table I.

random strips of FCB material attached to the meanders in some location, which might negatively affect mechanical reliability.

B. Controlled Frame Failure

Controlled frame failure takes the two-step process even further by eliminating the need to cut the frame during a separate production step, reducing the production process to a single encapsulation step after outline definition. The principle behind this method is simple: structural defects are introduced within the support frame, these defects then break when the circuit stretches, permitting free movement of the meanders and islands.

These intentional structural defects can take the shape of perforations, notches, shallow cuts, or any other method which will significantly reduce the strength at which the substrate tears at a specific location. Some of these proposed methods are listed in Fig. 9. A series of these structures was tested free-standing at room temperature to gauge their performance. To create a uniform laminate that accurately represents a FCB substrate, two foils of $35\,\mu\mathrm{m}$ thick SF305C coverlay (Shengyi Technology Co. Ltd., China) were bonded together using the manufacturer's recommended vacuum press profile, creating a $100\,\mu\mathrm{m}$ thick dummy substrate. This flexible laminate was then cut using a $3\,\mathrm{W}$ $354\,\mathrm{nm}$ Nd:YAG laser system (Optec, Belgium) with a $25\,\mu\mathrm{m}$ spot size, pulse rate of $1\,\mathrm{kHz}$ at $20\,\mathrm{mm\,s^{-1}}$, and with five repetitions to avoid a jagged edge. Holes were drilled using bursts of 250 laser pulses.

For testing, samples were clamped into a tensile tester (Instron, USA) with a $1\,\mathrm{kN}$ load cell and pulled apart at a rate of $50\,\mu\mathrm{m\,s^{-1}}$. The design parameters used are listed in Table I, together with the tensile test results for 7 samples per design. The depth of the lateral cuts is only an estimated value due to the need of the lasers stage to speed-up/slow down at the start/end of the cut, creating a parabolic profile which is difficult to measure exactly.

The reference, a $1\,\mathrm{mm}$ wide polyimide track with a length of $32\,\mathrm{mm}$, can extend on average $12.86\,\mathrm{mm}$ before breaking, requiring approximately $11.1\,\mathrm{N}$ of force, as listed in Table I.

Of the four test designs, with various parameters, all seem to affect both the required extension and force to break the polyimide track. However, it quickly becomes apparent that the perforations are the least effective of all. Moreover, an increase beyond 10 holes would take more time to ablate than either the notches or lateral cuts. Triangular notches with the parameters $\alpha = 45°$ and $d = 0.3\,\mathrm{mm}$ and lateral cuts with a depth of approximately $40\,\mu\mathrm{m}$ had a tendency to break during handling. Of the two remaining test cases, the 90° arc circular notches with a radius of $300\,\mu\mathrm{m}$ appear to result in the best performance. It combines a short required extension with a low force at breakage while being sufficiently strong for ease-of-handling – something the triangular notches and lateral cuts are significantly worse at.

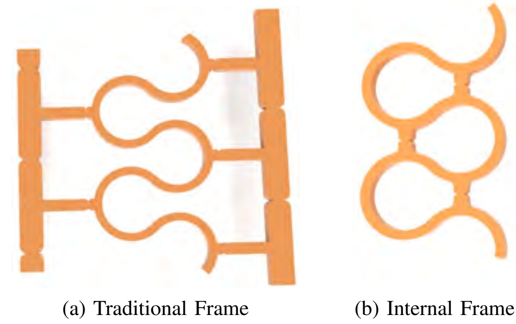
Based on the above measurement results, adding these structural defects to the frame design presented within Fig. 8f might seem like an attractive solution. However, such a traditional frame is critically flawed for this type of application, because the structural defects would experience a lateral shear force instead of a tensile load, resulting in unpredictable defect failures. For this reason, it is better to place the

TABLE I
MEASUREMENTS PERFORMED ON TEAR STRUCTURES.

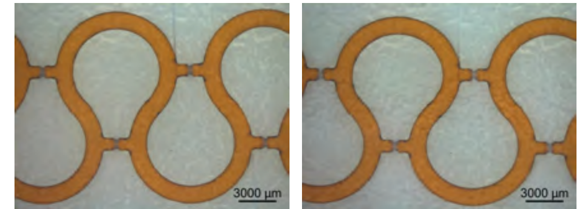
	Parameters		Force at Failure $\bar{F}$ [N]	$\sigma_{\bar{F}}$ [N]	Extension at Failure $\bar{d}$ [mm]	$\sigma_{\bar{d}}$ [mm]
Reference	1 mm polyimide		11.1	0.6	12.9	2.6
Triangular (α, d)	45°	200 µm	5.1	0.2	1.0	0.1
	45°	300 µm	2.7	0.6	0.4	0.1
	90°	724 µm	2.6	0.7	0.4	0.1
Circular (R)	0.150 mm		6.5	0.1	1.8	0.1
	0.300 mm		4.1	0.2	0.7	0.1
Perforations ($\#N$, $\varnothing d$)	4	25 µm	9.7	0.4	7.0	1.5
	7	25 µm	9.0	0.6	5.4	1.6
	10	25 µm	8.3	0.8	4.0	1.5
Lateral (d)	±20 µm		4.4	0.5	0.7	0.1
	±40 µm		2.5	0.5	0.4	0.1

structural defects between the meander segments themselves; this guarantees an axial load on the defect during elongation of the meander, resulting in a predictable failure. As shown in Fig. 10, this modified frame design comes with the added advantage of taking up significantly less space compared to the traditional frame and requires significantly less laser cutter time. However, the behaviour of this type of structural defect depends heavily on the encapsulation material exerting a sufficiently large force on each individual segment. Otherwise, a single structural defect will fail, after which that segment is extended entirely until the next defect fails.

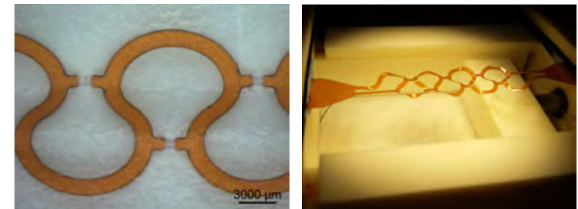
As a practical test, the above representative test laminate was cut into horseshoe-shaped meanders using the circular notch tear structures with a radius of 0.3 mm. Some of these were encapsulated between two layers of 100 µm *Covestro Platilon U4201 AU* thermoplastic polyurethane using a vacuum press (180 °C and 100 kPa pressure for 30 min). After mounting in a test fixture, shown in Fig. 10f, the samples were slowly extended using a micro-screw. The tear structures in the encapsulated samples tore between 2 mm to 3 mm extension on a length of 90 mm. Afterwards, the meander is free to extend without interference of the tear structures as shown in Fig. 10c through Fig. 10e – demonstrating the functionality of this method. In the case of the free-standing structures, as shown in Fig. 10f, the defect fails at 6.3 mm, after which the segment had to be fully extended before the next structure failed.



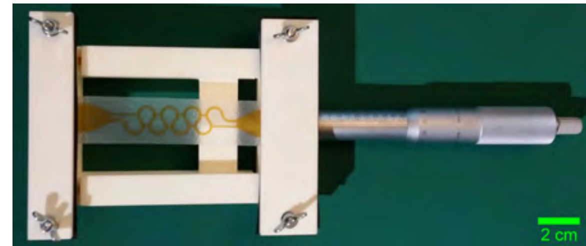
(a) Traditional Frame (b) Internal Frame



(c) 0 mm extension (d) 5 mm extension



(e) 15 mm extension (f) Non Encapsulated



(g) Test Fixture

Fig. 10. Testing of the controlled frame failure approach: (a and b) Traditional support frames use significantly more substrate surface area than the new internal frame approach; (c) Horseshoe-shaped meander with structural defects in resting condition suspended in a test fixture; (d) The same meander with an extension of 5 mm on a starting length of 90 mm applied to it; (e) The same meander stretched to 15 mm extension. (f) Non-encapsulated sample clamped into the test fixture under a microscope; (e) Test fixture with an encapsulated sample clamped into it, the microscrew directly controls the achieved extension.

IV. CONCLUSION

Several methods were proposed to remove the primary bottleneck, the peeling step, from the stretchable mold interconnect (SMI) production flow. These solutions fall into two categories, carrier-based and carrierless. Of the proposed methods only three were deemed feasible for implementation in an industrial production environment: the carrier-based design for peelability approach, and the two carrierless methods. In all three cases, basic design guidelines were provided, and proof-of-concept tests were performed.

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REFERENCES

[1] D. Brosteaux, F. Axisa, M. Gonzalez, and J. Vanfleteren, "Design and fabrication of elastic interconnections for stretchable electronic circuits," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 552–554, July 2007.

[2] T. Someya, Ed., *Stretchable Electronics*. Wiley-VCH, 12 2012.

[3] S. Wagner and S. Bauer, "Materials for stretchable electronics," *MRS Bulletin*, vol. 37, no. 3, p. 207213, 2012.

[4] C. Kallmayer, F. Schaller, T. Lher, J. Haberland, F. Kayatz, and A. Schult, "Optimized thermoforming process for conformable electronics," in *2018 13th International Congress Molded Interconnect Devices (MID)*, Sept 2018, pp. 1–6.

[5] F. Axisa, F. Bossuyt, T. Vervust, and J. Vanfleteren, "Laser based fast prototyping methodology of producing stretchable and conformable electronic systems," in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*. IEEE, 2008, pp. 1387–1390.

[6] J. Vanfleteren, M. Gonzalez, F. Bossuyt, Y.-Y. Hsu, T. Vervust, I. De Wolf, and M. Jablonski, "Printed circuit board technology inspired stretchable circuits," *MRS Bulletin*, vol. 37, no. 3, p. 254260, 2012.

[7] J. Vanfleteren, F. Bossuyt, and B. Plovie, "A new technology for rigid 3d free-form electronics based on the thermoplastic deformation of flat standard pcb type circuits," in *2016 12th International Congress Molded Interconnect Devices (MID)*, Sept 2016, pp. 1–4.

[8] J. Vanfleteren, T. Loeher, M. Gonzalez, F. Bossuyt, T. Vervust, I. D. Wolf, and M. Jablonski, "Scb and smi: two stretchable circuit technologies, based on standard printed circuit board processes," *Circuit World*, vol. 38, no. 4, pp. 232–242, 2012.

[9] Y. Yang, G. Chiesura, T. Vervust, F. Bossuyt, G. Luyckx, J. Degrieck, and J. Vanfleteren, "Design and fabrication of a flexible dielectric sensor system for in situ and real-time production monitoring of glass fibre reinforced composites," *Sensors and Actuators A: Physical*, vol. 243, pp. 103 – 110, 2016.

[10] B. Plovie, Y. Yang, J. Guillaume, S. Dunphy, K. Dhaenens, S. V. Put, B. Vandecasteele, T. Vervust, F. Bossuyt, and J. Vanfleteren, "Arbitrarily shaped 2.5d circuits using stretchable interconnects embedded in thermoplastic polymers," *Advanced Engineering Materials*, vol. 19, no. 8, p. 1700032, 2017.

[11] C. Coombs, *Printed Circuits Handbook*, ser. McGraw-Hill handbooks Printed circuits handbook. McGraw-Hill, 2001.

[12] C. Song, "Micromachined flow sensors for velocity and pressure measurement," Ph.D. dissertation, Georgia Institute of Technology, 2014.

[13] H. Ji-Song, T. Zhi-Yong, K. Sato, and M. Shikida, "Polyimide film micromachining by wet-etching technology," *IEEJ Transactions on Sensors and Micromachines*, vol. 125, no. 1, pp. 27–36, 2005.

[14] C. T. Conrad, "Photoresist processing for improved resolution having a bake step to remove the tackiness of the laminated photosensitive layer prior to contact imagewise exposure," Feb. 21 1995, uS Patent 5,391,458.

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