70 Gb/s Low-Power DC-Coupled NRZ Differential Electro-Absorption Modulator Driver in 55 nm SiGe BiCMOS

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(Highly-Scored Paper)

***Abstract*—We present a 70 Gb/s capable optical transmitter consisting of a 50 μm long GeSi electro-absorption modulator (integrated in silicon photonics) and a fully differential driver designed in a 55 nm SiGe BiCMOS technology. By properly unbalancing the output stage, the driver can be dc-coupled to the modulator thus avoiding the use of on-chip or external bias-Ts. At a wavelength of 1560 nm, open eye diagrams for 70 Gb/s after transmission over 2 km standard single-mode fiber were demonstrated. The total power consumption is 61 mW, corresponding to 0.87 pJ/b at 70 Gb/s. Bit-error rate measurements at 50 Gb/s and 56 Gb/s (performed both back to back and with up to 2 km standard single-mode fiber) demonstrate large (0.4 UI at a BER of 10^{-12}) horizontal eye margins. This optical transmitter is ideally suited for datacenter applications that require densely integrated transceivers with a low power consumption.**

***Index Terms*—DC-coupled, differential, driver, EAM, low power, modulator bias.**

I. Introduction

CLOUD based applications are putting the servers and links inside data centers under continued pressure. Industry is therefore considering transitioning to 400 Gb/s, 800 Gb/s and 1.6 Tb/s links [1], which will require optical transceivers built from densely integrated parallel channels that operate at high bitrates (>50 G/s) with extremely low power consumption. At these speeds, external modulation is then a good option to facilitate data transmission with sufficiently high quality (e.g. low error rates at given optical budget). In this work, we only consider electrically "small" modulators such as Silicon Photonic electro-absorption modulators (EAMs) or microrings [2] that do not use any traveling wave electrodes. This is possible if the physical dimensions of the modulator are sufficiently small compared to the electrical wavelength corresponding to the highest electrical modulation frequency. From the electrical point-of-view, such a modulator is equivalent to a (small, e.g. <100 fF) capacitor.

A driver circuit is required to convert the digital signal that needs to be transmitted to a signal with appropriate amplitude, DC-offset (bias voltage), shape (in case transmit-side equalization would be used) and impedance level according to the used modulator. At the targeted speeds in this work (>50 Gb/s) the interface between the driver and the modulator is extremely critical. This interface can be implemented using either matched transmission lines (i.e. terminated with load resistors matched to the characteristic impedance of these transmission lines, typically 50 Ω) or a sufficiently electrically short connection between the driver output pads and the modulator pads (referred to as lumped driving scheme hereafter). A driver designed for a transmission line interface [3]–[6] can be used to drive any modulator as long as the modulator input impedance resembles a 50 Ω impedance (i.e. has sufficiently low return loss). For the capacitive modulators considered here, this can be readily realized by placing a 50 Ω resistor in parallel to the modulator. In addition, the distance between driver and modulator is less critical and can be made electrically long if the RF losses along the transmission lines are not too high. The price to be paid for this flexibility is the power dissipated in the termination resistors.

If the distance between the modulator and driver can be made sufficiently small, a lumped driving scheme can be used. The driver can then be connected directly to the modulator, and needs to drive only its capacitance (possibly through bondwires). The termination resistors can now be eliminated and hence significant improvements in energy efficiency can be realized. For Silicon Photonic microring resonators, the modulator is a capacitor and due to its relatively low drive voltage requirements can be (almost) directly driven using drivers based on simple CMOS inverter circuits. Transmitters based on such microrings and CMOS inverter drivers have been demonstrated to achieve bitrates >50 Gb/s at very low powers (<50 mW) [7],

Manuscript received October 15, 2018; revised December 17, 2018 and January 31, 2019; accepted February 15, 2019. Date of publication February 19, 2019; date of current version March 27, 2019. This work was supported in part by the Research Foundation Flanders (FWO), EU-funded H2020 Projects ICT-STREAMS under Grant 688172 and in part by TERABOARD under Grant 688510. *(Corresponding author: Hannes Ramon.)*

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Digital Object Identifier 10.1109/JLT.2019.2900192

[8]. Since the resonance wavelength of a microring is highly sensitive to temperature and process variations, EAMs are an interesting alternative. GeSi modulators integrated in Silicon Photonic integrated circuits have been shown to achieve bitrates up to 100 Gb/s [9]. While inverter based drivers are ideally suited to drive microrings, they cannot handle the considerable photocurrent generated by the EAM while in its absorptive state. This photocurrent needs to be sunk by the driver, which in the case of a CMOS inverter driver results in significant distortion. Increasing the transistor sizes of the CMOS inverter driver helps however at the expense of bandwidth and increased power consumption. In addition, the photocurrent complicates the generation of the necessary DC bias voltage across the modulator. AC-coupling the driver's output to the modulator with a simple on-chip RC bias-T [10], [11] is typically not possible due to the large voltage drop (ranging from a few Volt as high as 20 V) caused by the photocurrent over the resistive DC-feeds. An LC bias-T [12], [13] solves this problem, however, cannot be integrated on-chip (due to the large inductance and/or capacitor values), and requires too much space to be integrated into typical modules form factor for data center applications [14].

This paper is an invited extension of [15], in which we presented a fully differential ultra-low power (61 mW) DC-coupled driver in a SiGe BiCMOS technology, delivering 2 V_{ppd}, with V_{ppd} the differential peak to peak voltage, to a lumped EAM. The driver is able to sink the photocurrent and properly reverse bias the EAM up to 1.5 V while operating at 70 Gb/s with sub-pJ/bit efficiency. First, a summary of the used EAM is given. Next single-ended and differential drivers with bias-T's are discussed in terms of topology and power consumption. A solution to the discussed problems will be provided. Section IV shows the ASIC implementation, where we cover the design process of the output stage in the presence of a bondwire. Finally electro-optical measurements are presented using a demonstrator where the electrical chip is wire bonded to a GeSi EAM.

II. Electro-Absorption Modulator

The transmitter should have sufficient launch power as specified in standards to overcome losses and meet the link budget [16]. The EAM modulates the light by changing the absorption coefficient with modulation voltage. This means that the EAM is also acting as a photodiode, producing a considerable amount of photocurrent due to the high laser power. For example, assuming a laser power of 5 dBm and an EAM responsivity of 0.6 A/W, the photocurrent is already 1.9 mA. When designing an EAM driver, it is important to take the driver's capabilities to sink this photocurrent into account. Some topologies will exhibit lower bandwidth or distortion in the presence of photocurrent.

In this work, we used a 50 μm long GeSi EAM from imec's 200 mm silicon photonics platform [2]. The operation of the GeSi EAM is based on the Franz-Keldysh effect where the bandgap shifts when an electrical field is applied, changing the absorption. This EAM has a junction capacitance around 20–25 fF and a series resistance around 40 Ω. The physical size of the device is sufficiently small to drive at $>$50 Gb/s without requiring 50 Ω traveling wave structures. The EAM has a small signal bandwidth above 50 GHz. At 1560 nm, the EAM has an insertion loss (IL) of around 4 dB and an extinction ratio (ER) of 5 dB for a 2 V_{ppd} voltage swing.

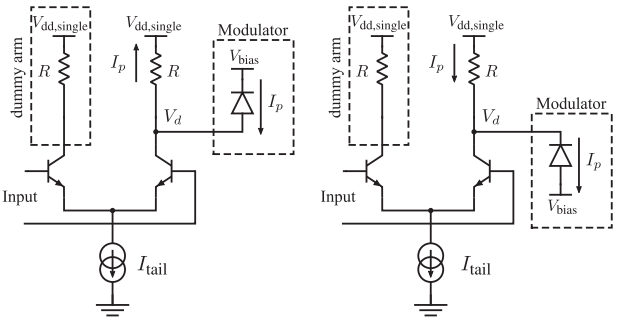

Fig. 1. Typical single-ended EAM biasing configurations when using a differential pair.

For capacitive modulators, the feasibility of implementing a lumped driving scheme is determined by the physical size of the device, capacitance, required bandwidth and the packaging parasitics. The effect of the package parasitics depends on the capacitance of the device, because the bondwire inductance creates a resonance with the input capacitance of the modulator as explained in Section IV. Further discussions in this manuscript will focus on non-terminated EAMs.

III. Differential Drivers

A. Conventional Single-Ended Driver

For capacitive modulators, one of the lowest power driver topologies is the inverter based driver. This topology theoretically consumes only dynamic power, which makes it the preferred driver for microring modulators. In the single-ended case, the modulator is typically biased by connecting one terminal to the driver and the other terminal to a DC voltage well chosen to generate a reverse bias [7], [10]. As described in Section I, this driver cannot be used for an EAM because it generates photocurrent, which disturbs the operation of the NMOS and/or PMOS transistors. The resistively loaded differential pair (Fig. 1) on the other hand, is less susceptible to photocurrent coming from the EAM, because the photocurrent flows through the resistors R, generating a voltage drop changing linearly with the current. This type of driver consumes, unlike e.g. the inverter driver, mainly static current due to the always on current I_{tail}. The EAM photocurrent lowers the reverse bias by RI_p, with I_p the photocurrent. Here, a large output impedance of the transistors was assumed, which means that the differential pair transistors always switch a current I_{tail} to their load, irrespective of the voltage at their output terminals. The photocurrent I_p cannot flow into the transistors thanks to their large output impedance and hence flows into the load resistors albeit with the opposite sign as the current I_{tail}. The total DC current in the load resistors is now $I_{\mathrm{tail}}/2 - I_p$. The EAM or more generally, the modulator is typically connected by directly connecting (no DC-blocking capacitor) the anode (Fig. 1a) or cathode (Fig. 1b). The other terminal of the modulator is placed on a constant DC voltage V_{bias} to generate a reverse bias over the modulator [17]–[19]. By doing this, the DC output voltage of the driver plays an important role in

the biasing of the driver. This single-ended topology is used for a broad range of modulators and even directly modulated lasers and vertical cavity surface emitting lasers (VCSEL) [20]–[23].

Using a differential pair as a single-ended driver is not power efficient because half of the power is dissipated in the dummy load (assuming a data stream consisting of 50% 1's and 50% 0's). A solution to lower the power dissipation in the dummy load is to place the dummy arm on a lower supply voltage, with a smaller dummy resistor [19]. In the limit, the dummy resistor can be replaced with a short to a reduced supply voltage. This reduction in supply voltage is limited by the need to maintain approximately the same voltage on both collectors of the switching transistors, thus maintaining balance in the differential pair which minimizes signal distortion. A good starting point for a design is to place the collector voltage of the transistor in the dummy path at approximately the time averaged collector voltage of the transistor in the output path, hence at $V_{\text{dd,single}} - RI_{\text{tail}}/2$, with $V_{\text{dd,single}}$ the supply voltage. The dummy arm consumes less power since the same current is drawn from a lower supply voltage. The power reduction of the differential pair with lower supply on the dummy arm ($S_{\text{single,lower dummy}}$) with respect to the conventional differential pair is maximally 25% (1), with $V_{\text{swing,pp}}$ the peak-to-peak voltage swing applied to the modulator, $P_{\text{single,lower dummy}}$ the power consumption of the single-ended driver with lower dummy arm and P_{single} the power consumption of the standard single-ended differential pair.

$$\begin{aligned} S_{\text{single,lower dummy}} &= 1 - \frac{P_{\text{single,lower dummy}}}{P_{\text{single}}} \\ &= \frac{1}{4}\frac{RI_{\text{tail}}}{V_{\text{dd,single}}} \\ &= \frac{1}{4}\frac{V_{\text{swing,pp}}}{V_{\text{dd,single}}} \end{aligned} \tag{1}$$

In (1) a zero valued dummy resistor was assumed, leading to the highest power consumption reduction with respect to the normal differential pair. The power consumption of the modulator was neglected. A dummy resistor different from 0 will decrease the power reduction specified in (1). For a realistic voltage swing (2 V_{pp}) and a supply voltage of 3.5 V, the power reduction $S_{\text{single,lower dummy}}$ is only 14%. 3.5 V supply voltage was chosen in this example so that the collector voltage of a differential pair with 40 mA tail current and a load resistor of 50 Ω is 1.5 V, enough margin for nominal operation.

B. Differential Driver With Bias-T

The obvious solution to lower the power consumption when using a differential pair as an output stage, is to drive the modulator using both arms (differential drive). The modulator is placed between both output terminals of the differential pair and instead of dissipating current in a dummy load, the current is switched to the other terminal of the modulator. The output swing of the differential driver is now $V_{\text{swing,pp}} = 2RI_{\text{tail}}$, two times higher than the single-ended driver for the same I_{tail}. Equivalently, for the same output swing as the single-ended variant, only half the current is required, leading to a 50% power reduction. On top of that, because the voltage swing in a single arm is now also halved, the supply voltage can also be lowered with respect to the single-ended driver supply.

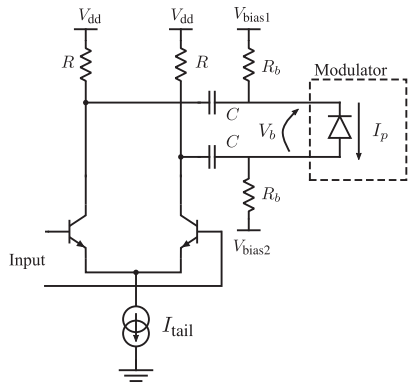

Fig. 2. Fully differential driver output stage with RC bias-T.

Unfortunately, driving a modulator differentially, poses problems related to the biasing of the modulator. Due to the differential nature of the topology, the modulator junction voltage is either forward or reverse according to the sign of the generated differential voltage. The time averaged bias voltage across the modulator is 0 V. For some modulators this is not necessarily a problem, however, most junction based modulators require a (preferably easily configurable) reverse bias. The simplest and most common solution to change the DC voltage of a circuit is to use an LC bias-T. The low frequency cut-off (f_{LF}) of the bias-T needs to be sufficiently low to limit DC-wanders and the corresponding power penalty [24]. For a 0.05 dB power penalty at 50 Gb/s and 31 identical consecutive number of bits, f_{LF} must be below 3 MHz. However, an LC bias-T with such a low f_{LF} is not suited for high speed integrated applications. For an on-chip implementation of the capacitor, the required area on the chip needs to be reasonably small. A typical value for the capacitance per unit area of an on-chip capacitor is no more than 5 fF/μm^2 [25], hence a 100 × 100 μm^2 area results in a 50 pF capacitor. For a cut-off frequency of 3 MHz, the inductor must be in the 100 μH range, too large for on-chip integration and even impractical off-chip.

Placing the entire bias-T off-chip permits the use of larger capacitors, e.g. 10 nF, leading to an inductor in the 100 nH range, however, bringing the capacitor off-chip increases the packaging size and complexity. Even though the inductor can be 1000 times smaller, it is still too large to include in a multi-channel package with sub-millimeter channel pitch [14].

On the other hand a resistive bias-T (Fig. 2) can be integrated on-chip because a resistor has a much smaller footprint. For the same low frequency cut-off of 3 MHz and a capacitor of 10 pF, a resistor around 5 kΩ is required, which can be made in a couple of square micrometers. The on-chip RC bias-T is often used in conjunction with modulators without photocurrent generation, e.g. the microring modulator. Typically in these drivers, the resistor is chosen as large as possible given the bandwidth and size constraints [10], [11].

A similar power reduction $S_{\text{bias-T},I_p=0}$ (2) is calculated for the differential driver with bias-T assuming $I_p = 0$ mA, with $P_{\text{bias-T},I_p=0}$ the power consumption of the bias-T differential

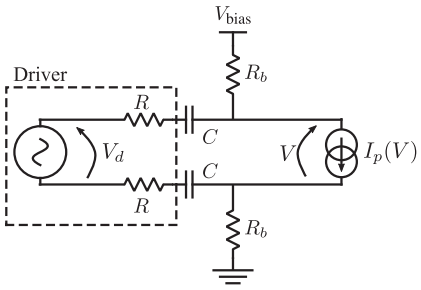

Fig. 3. Equivalent model of a differential driver with an RC bias-T connected to an EAM. Only the photocurrent of the EAM is modeled and it is assumed that the EAM and photocurrent generation is infinitely fast.

driver for $I_p = 0$. V_{dd} is defined as the supply voltage of the differential driver. This power reduction is always $\geq 50\%$ because $V_{dd,\text{single}} \geq V_{dd}$. For typical supply voltages ($V_{dd} = 2.5$ V and $V_{dd,\text{single}} = 3.5$ V), the power reduction is 64%. In this example, the supply voltages again give rise to a collector voltage of 1.5 V when using load resistors of 50 Ω and respectively 20 mA and 40 mA for the differential and single-ended driver.

$$S_{\text{bias-T},I_p=0} = 1 - \frac{P_{\text{bias-T},I_p=0}}{P_{\text{single}}} = 1 - \frac{1}{2}\frac{V_{dd}}{V_{dd,\text{single}}} \quad (2)$$

When the modulator produces a photocurrent I_p, the average photocurrent flows into the bias resistors and causes a voltage drop. The modulator bias voltage becomes I_p dependent, which also means laser power dependent. To evaluate the effect of the average photocurrent $\overline{I_p}$ on the modulator bias, we replace the modulator with a voltage dependent current source (Fig. 3). In Fig. 3, the junction capacitance, resistance and other parasitics of the EAM are not included to simplify the calculations, whereas the conclusion remains the same. To further simplify the analysis, we place one bias voltage on 0 V. It is easily deduced from Fig. 3 that the voltage source needed to generate the modulator bias V_b is $V_{\text{bias}} = V_b + 2\overline{I_p}R_b$. This voltage is not only highly I_p dependent, but also much higher than V_b assuming a large R_b for a sufficiently low frequency cut-off. For example, $\overline{I_p} = 2$ mA, $R_b = 5$ kΩ and $V_b = 1$ V, the bias voltage that needs to be applied is 21 V, 21 times higher than the required $V_b = 1$ V. For larger DC-feed resistors, this bias voltage rapidly increases to even more unpractical values, e.g. for $R_b = 10\,\text{k}\Omega$, the bias voltage is 41 V. Apart from the fact that it difficult to handle such voltages, there is also an additional power consumption as indicated by the final term of $S_{\text{bias-T,EAM}}$ in (3), which is the power reduction versus the single-ended EAM driver of the differential pair with bias-T in the presence of photocurrent. $P_{\text{bias-T,EAM}}$ is defined as the power consumption of the bias-T driver for an EAM.

$$S_{\text{bias-T,EAM}} = 1 - \frac{P_{\text{bias-T,EAM}}}{P_{\text{single}}} \approx 1 - \frac{1}{2}\frac{V_{dd}}{V_{dd,\text{single}}} - \frac{\overline{I_p}^2 R_b}{I_{\text{tail}} V_{dd,\text{single}}} \quad (3)$$

To obtain (3) we assumed that $V_{dd,\text{single}} I_{\text{tail}} \gg V_b \overline{I_p}$. This is a valid assumption because I_{tail} is required for the output swing and should be much larger than I_p for correct operation and $V_{dd,\text{single}} > V_b$ otherwise the differential pair is not correctly biased. The current of the single-ended driver was defined as $2I_{\text{tail}}$, with I_{tail} the tail current of the differential driver. The first two terms in (3) represent the power reduction of the bias-T driver for $\overline{I_p} = 0$ mA as shown in (2), while the last term is dependent on the photocurrent I_p. The photocurrent dependent part is not negligible due to the typically large R_b which reduces the power efficiency of the differential driver. Equation (3) can become negative for a large $R_b\overline{I_p}$ product, meaning that the bias-T differential driver consumes more power than the plain single-ended differential pair driver. The power reduction drops from 64% to 35% for $R_b = 3$ kΩ and is negative for $R_b > 11.25$ kΩ ($\overline{I_p} = 2$ mA and $I_{\text{tail}} = 20$ mA).

While the average photocurrent $\overline{I_p}$ causes a voltage drop and an increase in power consumption, the instantaneous EAM photocurrent influences the AC operation of the driver with an RC bias-T. The EAM modulates the light by changing its absorption coefficient according to the voltage $V(t)$ applied. This means that the photocurrent from the EAM is actually a time varying current $I_p(t)$. This time varying photocurrent can be decomposed in two components: a quiescent part earlier defined as the average photocurrent $\overline{I_p}$ and a time varying part $i_p(t)$ with $I_p(t) = \overline{I_p} + i_p(t)$. The time varying current $i_p(t)$ is proportional to the time-varying voltage $V(t)$ and the incident optical power P_o ($i_p \propto V(t)P_o$). Qualitatively explained, the high frequency component of i_p flows through the capacitor, discharging the capacitor. The current through the capacitor is now the sum of the current through the bias resistor R_b and i_p. If the bias-T is properly designed for a sufficiently low low-frequency cut-off, the current coming from the bias resistor R_b is negligible compared to the photocurrent, so the discharge of the capacitor is much faster with a photocurrent present than without. The faster discharge of the capacitor leads to a higher low frequency cut-off f_{LF} than the cut-off of the bias-T and a higher i_p amplifies this effect.

Equivalently, the current source $I_p(t)$ can be modeled as a non-linear resistor $R_p(V) = \frac{V}{2I_p(V)}$ in parallel with R_b. $R_p(V)$ is typically smaller than R_b (e.g. for $\overline{I_p} = 2$ mA, the average $\overline{R_p} \approx 250\,\Omega$), lowering the resistance of the RC-circuit, leading to the same conclusion that f_{LF} increases.

Besides the applied voltage, the optical power P_o in the EAM influences the f_{LF}, and likewise, a higher optical power increases the low frequency pole (Fig. 4).

Fig. 4 shows simulated transfer functions with changing low-frequency cut-off for different optical power or equivalently $\overline{I_p}$, where we assumed a responsivity $\mathcal{R} = 0.6$ A/W at the EAM bias voltage, which was the same for all curves. The low frequency pole goes from 1.63 MHz for $\overline{I_p} = 0$ mA to around 100 MHz for $\overline{I_p} = 4$ mA (∼8 dBm).

Similar conclusions can be drawn from Fig. 5, where a voltage step was applied to the biased EAM, which shows that higher optical power or average photocurrent, leads to a faster discharge of the bias-T or equivalently a higher f_{LF}, which will lead to DC-wandering when transmitting real data. This is also visible in

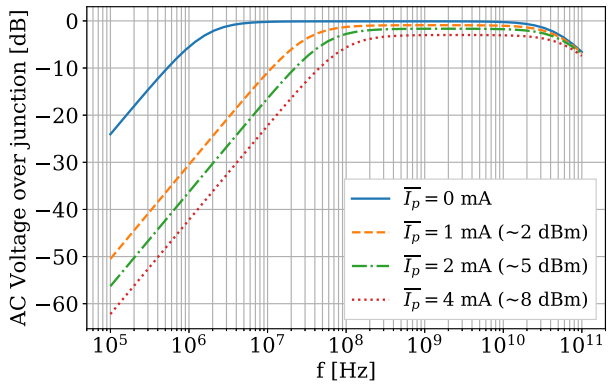

Fig. 4. AC voltage over modulator junction, normalized with the driver output voltage for a modulator with varying optical power or equivalently average photocurrent from $\overline{I_p} = 0$ mA to $\overline{I_p} = 4$ mA with a bias-T ($\mathcal{R} = 0.6$ A/W, $C = 10$ pF and $R_b = 10$ kΩ.)

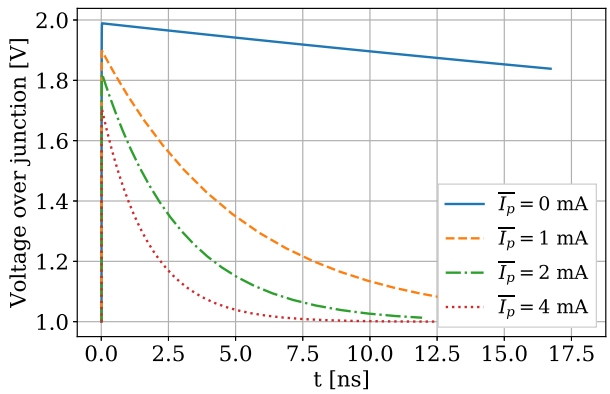

Fig. 5. Voltage over modulator junction when applying a step of 2 V_{pp} for a modulator with varying optical power or equivalently average photocurrent from $\overline{I_p} = 0$ mA to $\overline{I_p} = 4$ mA with a bias-T ($C = 10$ pF, $R_b = 10$ kΩ).

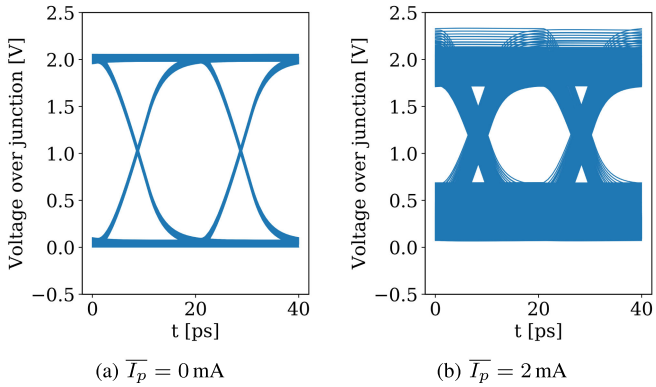

Fig. 6. Eye diagram of voltage over modulator junction when applying a 50 Gb/s 2 V_{pp} signal to a modulator with $\overline{I_p} = 0$ mA (a) and $\overline{I_p} = 2$ mA (b) with an RC bias-T ($C = 10$ pF, $R_b = 10$ kΩ).

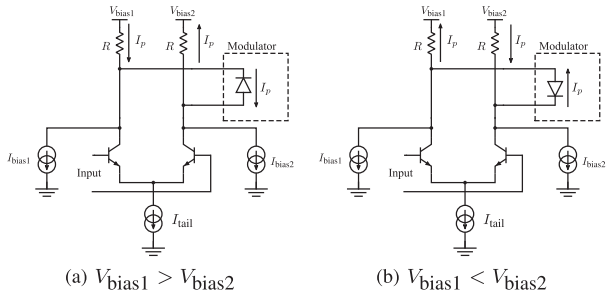

Fig. 7. The proposed DC-coupled fully differential driver output stage.

the eye diagrams (Fig. 6) of the modulator voltage, which show far higher amounts of DC-wander in presence of photocurrent than without photocurrent.

Another effect, visible on both Figs. 4 and 5, is that the high frequency component of i_p, flows through the drivers load resistors and reduces the gain and hence the drive voltage applied to the junction of the EAM. However, this effect is also present in the single-ended driver shown on Fig. 1 and is not related to the bias-T.

C. Proposed Differential Driver

In the previous section, we have shown that for an EAM, a bias-T is not a good solution to bias the modulator. We propose an alternative method to bias the modulator when using a differential pair as output stage. The solution still benefits from the improved power efficiency of the differential driver without the biasing problem of the bias-T. Moreover, the modulator is DC-coupled to the driver, making the proposed solution robust for data streams with a long section of consecutive identical bits as the biasing method does not include a low frequency cut-off (Fig. 7).

The bias voltage is generated by placing the top terminals of the driver's load resistors at different voltages V_{bias1} and V_{bias2}. In configuration (a) $V_{\text{bias1}} > V_{\text{bias2}}$ to reverse bias the modulator and in configuration (b) $V_{\text{bias1}} < V_{\text{bias2}}$. The proposed scheme is, as for a bias-T, flexible in the polarity of the modulator. This voltage difference is then directly translated in a voltage difference over the modulator, providing the bias voltage. Current sources I_{bias1} and I_{bias2} are added to fine-tune the bias voltage and to compensate for the transistor non-linearity due to the voltage difference across both transistors. This voltage difference induces two effects: a current difference in both arms of the differential pair and duty-cycle distortion. The current difference leads to a bias voltage reduction. Both the bias voltage reduction and the duty-cycle distortion can be counteracted by turning on the appropriate current source: I_{bias1} if $V_{\text{bias1}} > V_{\text{bias2}}$ and I_{bias2} in the other case.

The EAM photocurrent now flows into the load resistors of the driver instead of the large bias-T resistors. For high-speed applications, the load resistors of the driver are in the order of 50–100 Ω, therefore leading to a much lower voltage drop (~200 mV) instead of 2–20 V in the case of a bias-T with resistors that are rather in the order of 1 k–10 kΩ. The power reduction S_{proposed} of the proposed topology with respect to the single-ended differential pair is given in (4), with P_{proposed} the power consumption of the proposed topology and $V_{dd,\text{avg}}$ the average supply voltage of V_{Bias1} and V_{Bias2}. For $V_{dd,\text{avg}} = 3$ V

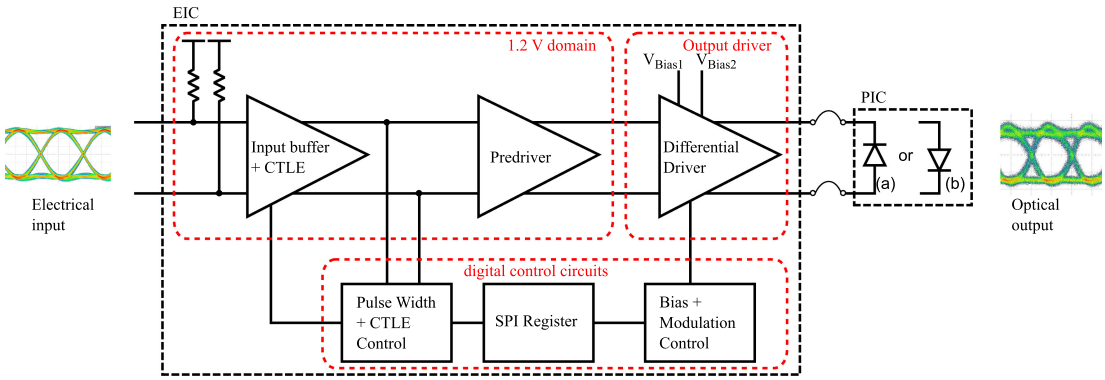

Fig. 8. The block diagram of the implemented driver on the electrical IC (EIC) and the two different modes (a) and (b) in which we can connect the modulator on the photonic IC (PIC) to the proposed driver.

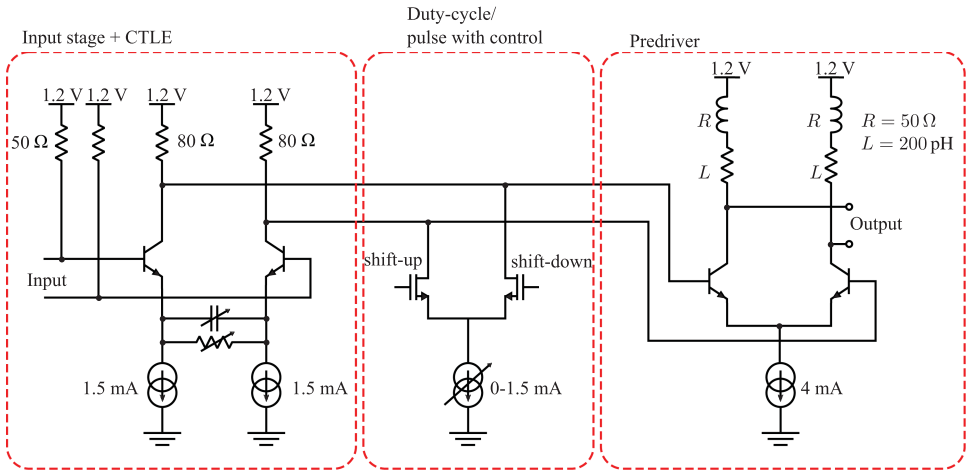

Fig. 9. The 1.2 V domain blocks of the driver: An input stage with CTLE in the form of tuneable degeneration, duty-cycle control circuit and predriver.

and $V_{dd,\text{single}} = 3.5$ V the power reduction is leads to 57%.

$$\begin{aligned} S_{\text{proposed}} &= 1 - \frac{P_{\text{proposed}}}{P_{\text{single}}} \\ &\approx 1 - \frac{1}{4}\frac{V_{\text{Bias1}} + V_{\text{Bias2}}}{V_{dd,\text{single}}} \\ &= 1 - \frac{1}{2}\frac{V_{dd,\text{avg}}}{V_{dd,\text{single}}} \end{aligned} \tag{4}$$

Again, we assumed $V_{dd,\text{single}} I_{\text{tail}} \gg V_b \overline{I_p}$. The proposed topology approaches the efficiency of a differential driver with bias-T and without photocurrent as in (2), while being DC-coupled and capable of handling the EAM photocurrent.

Note that for the several discussed driver topologies, different supply voltages are required. In a practical system, such supply voltages can be derived from a single supply using DC-DC converters. In the derivations above, we assumed DC-DC converters with 100% efficiency to keep the calculations simple. Realistic DC-DC converter efficiencies will decrease the power reduction, but the conclusions are still valid.

IV. ASIC Implementation

The driver was realized in a SiGe BiCMOS 55 nm technology [25]. The full block diagram is shown in Fig. 8. The output driver is preceded by an input buffer with continuous time linear equalizer (CTLE) to compensate for cable and PCB trace losses and a predriver with duty-cycle control.

A. Input Stage and Predriver

Fig. 9 shows the circuit implementation of the input stage with CTLE and the predriver. The variable resistor and capacitor are implemented as banks of respectively NMOS transistors in triode and NMOS capacitors, that can be switched via a digital interface, thus creating a CTLE with digitally programmable gain and peaking.

The pulse width control or duty-cycle control circuit is able to shift the crossing of the falling and rising edge of the driver upwards or downwards. This is accomplished by creating an imbalance in the input stage output voltage with a CMOS differential pair as shown in Fig. 9. This imbalance creates a DC-offset in the differential pair of the input stage. If this DC-offset goes through a highly non-linear, limiting amplifier stage such as the predriver, it is transferred into duty-cycle distortion and

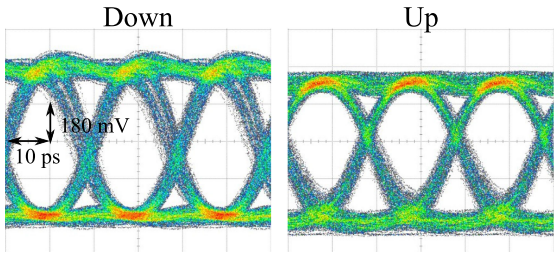

Fig. 10. Pulse width control: left the crossing is shifted down and right the crossing is shifted up.

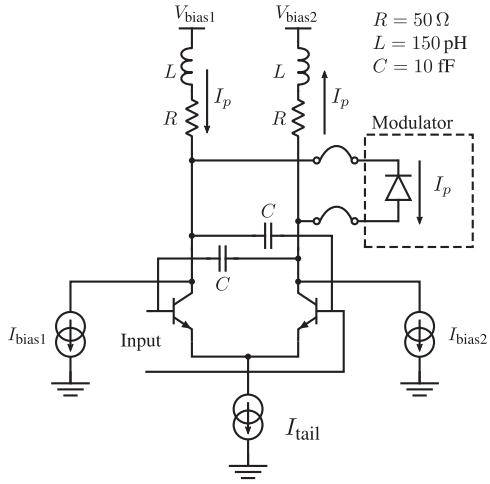

Fig. 11. The driver output stage.

a shift in the crossings on the eye diagram, see Fig. 10. The NMOS differential pair has a tuneable current source, which allows to program the amount of imbalance and hence the duty cycle. The gate voltage applied at the NMOS transistors determines whether the crossing is shifted up or down. Fig. 10 shows electrical measurement results of the duty-cycle control circuit, where we probed the output of the driver with a 67 GHz GSSG probe.

The predriver is the most bandwidth limiting component in this work since it has to drive the large input capacitance of the driver, while delivering the correct voltage swing. Applying a too large signal to the output stage can introduce unwanted jitter and distortion as transistors are pushed into saturation, while a too small signal will decrease the bandwidth of the output stage. Through simulations, an optimum value for the output swing for the predriver was found to be 400 mV_{ppd}, generated using a 4 mA tail current source and 50 Ω load resistors. To overcome the large input capacitance of the output stage while still maintaining a low power consumption, inductive shunt peaking with two 200 pH inductors was added. The simulated small signal gain of the cascade of the input stage and the predriver is 10 dB with a small signal bandwidth of 40 GHz.

B. Output Stage

The proposed topology in Fig. 7 forms the basis for the implemented output stage given in Fig. 11. The driver has an output voltage swing of 2 V_{ppd} while loaded by a capacitive modulator like the EAM. Cross coupled capacitors connect the collector of one transistor of the differential pair with the base of the other transistor. The cross coupled capacitor acts as a negative capacitor, reducing the capacitive loading of the output stage on the predriver. This effective reduction in load capacitance helps to reduce the power consumption of the predriver, since it allows to increase the predriver's load resistors while maintaining the same bandwidth. For the same voltage swing generated by the predriver, its bias current can be reduced. The current sources I_{bias1} and I_{bias2} are programmable with a maximum output current of 3.2 mA, allowing a modulator bias voltage shift of 160 mV in each direction. For the used EAM, this 320 mV total voltage shift is enough to fine tune the EAM bias voltage since the EAM only requires a reverse bias around 1 V.

Driving a capacitive modulator differentially has the disadvantage that the effective load on each arm of the driver is twice this capacitance. Note however, that the driver needs to drive also its own capacitance consisting of transistor and internal connections (20 fF), bondpad (30 fF), and ESD (20 fF) protection diode capacitance. The EAMs used in this work have a significantly smaller capacitance (20 fF) compared to the driver's capacitance (∼70 fF), which limits the bandwidth reduction of the differential driver compared to the single-ended driver. Besides a reduction in power consumption, differentially driving a modulator is beneficial for packaging inductances. For the differential mode of the signal, the effective bondwire inductance is halved compared to having both bondwires in series in case of the single-ended driver.

The bondwire inductance plays an important role in the design process of such an output stage for capacitive modulators. This inductance forms a resonance with the capacitance of the modulator, which can be used to increase the bandwidth of the driver-modulator interface. Although the exact bondwire inductance is is hard to predict accurately due to manufacturing tolerance, a fairly good estimate of the inductance can be made based on the distance between the bondpads of both chips. The Q-factor of this resonance becomes larger with increasing bondwire length and the resonance frequency shifts to lower frequencies [26]. If the resonance frequency shifts too low with respect to the target bandwidth of the driver, it becomes significantly more difficult to incorporate this resonance into the design. Shunt peaking can be added to the driver to further increase the bandwidth and to form a shunt-series peaked amplifier with the bondwire acting as the series peaking inductance. The bondwire inductance target was set to be 200 pH, which is an estimate for placing the the driver chip next to the Silicon Photonic chip containing the EAM. In practice, packaging tolerances will introduce a bondwire deviation, but this can be incorporated in the driver design. Depending on the Q-factor of the resonance, a broader bondwire inductance shift can be tolerated. Fig. 12 shows the simulated AC transfer functions of the output stage for the different peaking configurations: no peaking, shunt peaking only and shunt-series peaking with bondwire. The shunt peaking inductance $L = 150$ pH is chosen to have a maximally flat frequency response when there is no bondwire present [27]. The corresponding group delay simulations are given in Fig. 13. Up to 52.5 GHz (75% of 70 Gb/s), the total group delay variation is

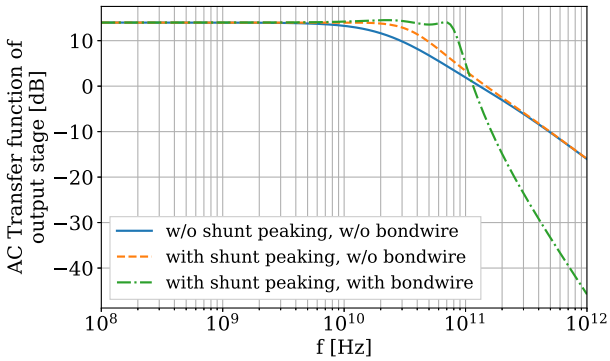

Fig. 12. Simulated AC transfer function of the output stage for different peaking configurations.

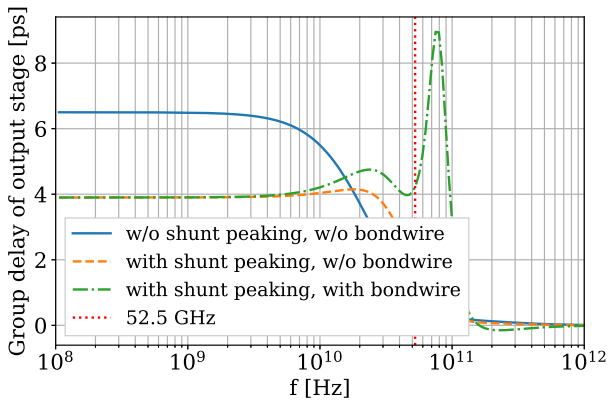

Fig. 13. Simulated group delay of the output stage for different peaking configurations. Up to 52.5 GHz (75% of 70 Gb/s), the total group delay variation is less than 1 ps, which is negligible compared to the bit period of 14 ps at 70 Gb/s.

less than 1 ps. This is negligible compared to the bit period of 14 ps at 70 Gb/s.

To isolate the effect of both resonances of the shunt peaking and series peaking, we will apply Middlebrook's Extra Element Theorem (EET) [28] on the output stage. The extra element theorem allows us to decompose the actual transfer function (H) into a transfer function (H_{ref}) with the extra element shorted or left open and a correction transfer function (D) that expresses the influence of that extra element so that the following is true:

$$H = H_{ref} \cdot D \tag{5}$$

For the remaining of this section, the simplified differential mode equivalent circuit from Fig. 14 for the output stage, modulator and packaging parasitics will be used. L_{BW} in Fig. 14 represents the bondwire inductance and C_p is the total parasitic capacitance at the drivers output node. C_j is the junction capacitance and R_s is the series resistance of the modulator.

To use this theorem to isolate the effect of the bondwire and shunt peaking, we have performed the EET twice: first with the bondwire shorted ($L_{BW} = 0$) and with the shunt peaking inductor as the extra element, afterwards we applied the EET on the bondwire with the shunt peaking enabled. This leads to (6) as a decomposition of the total transfer function H_{driver}, the transfer function of the output stage, including shunt peaking

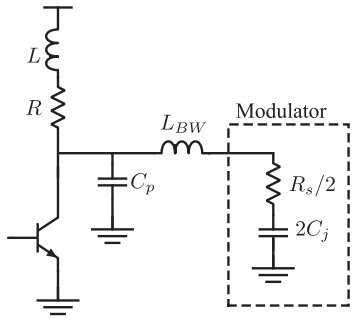

Fig. 14. The simplified differential mode equivalent circuit for the output stage, modulator and packaging parasitics.

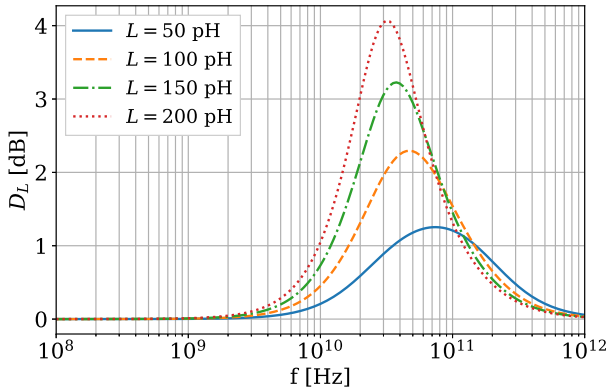

Fig. 15. The simulated correction transfer function D_L as a function of the shunt peaking inductor L.

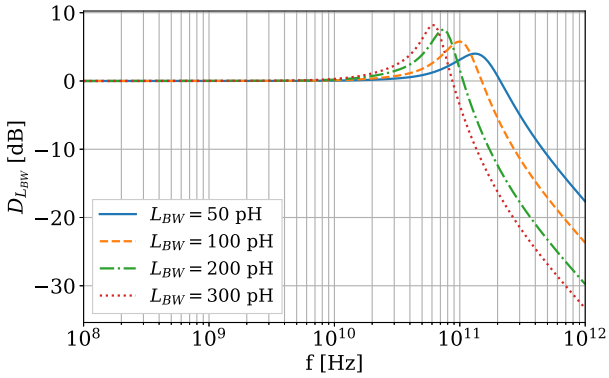

Fig. 16. The simulated correction transfer function $D_{L_{BW}}$ as a function of the bondwire inductance L_{BW}.

inductor and bondwire.

$$\begin{aligned} H_{\text{driver}} &= H_{L=0,L_{BW}=0} D_L D_{L_{BW}} \\ &= H_{L=0,L_{BW}=0} D_{\text{total}} \end{aligned} \tag{6}$$

With $H_{L=0,L_{BW}=0}$ the transfer function of the output stage without shunt peaking and no bondwire and D_L the correction transfer function of the shunt peaking on the total transfer function with the bondwire shorted and $D_{L_{BW}}$ the correction transfer function of the bondwire on the total transfer function. Figs. 15 and 16 respectively show the correction factors due to of L and L_{BW} for different inductance values.

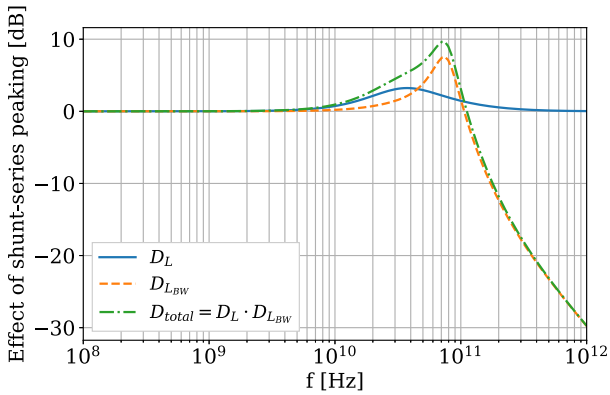

Fig. 17. The simulated total correction transfer function D_{total} for $L = 150$ pH and $L_{BW} = 200$ pH.

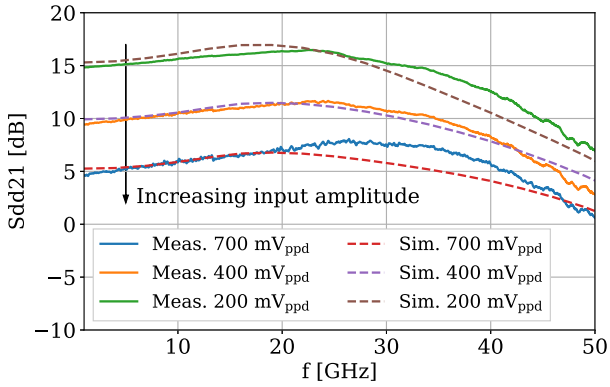

Fig. 18. Measured and simulated large signal S-parameters for different input swings. The driver is measured in a 50 Ω environment, slightly changing the bandwidth and reducing the gain with 6 dB. ($V_{\text{Bias2}} = V_{\text{Bias2}} = 2.5$ V).

Both correction factors exhibit as expected a resonance, with increasing Q-factor and decreasing resonance frequency with increasing inductance value. It is clear from Fig. 16 that the bondwire introduces a non negligible amount of peaking. This peaking can be partially resolved by choosing a larger load resistor. The larger load resistor reduces the bandwidth that is naturally compensated by the bondwire. A larger load resistor also means that for the same output swing, a lower power consumption is obtained because the current I_{tail} will be lower. This shows that to a certain extent, utilizing the bondwire inductance can lower the power consumption of the driver. After choosing the differential pair load resistance, the shunt peaking inductor needs to be chosen to bridge the gap between the differential pair bandwidth and the resonance frequency due to the bondwire. Fig. 17 illustrates the total correction transfer function D_{total}, where the resonance frequency of D_L is lower than the resonance of $D_{L_{BW}}$. The peaking of D_{total} compensates the roll-off of $H_{L=0,L_{BW}=0}$ as illustrated earlier in Fig. 12.

V. Electrical Measurements

The measured large signal S-parameters for the driver are displayed in Fig. 18. The S-parameters were measured with a four-port network analyzer configured in differential mode. We probed the input and the output with 50 Ω 67 GHz GSSG RF probes. To achieve the different curves, the output power of the network analyzer was changed so that the differential input swing at the driver went from 200 mV_{ppd} to 700 mV_{ppd}. The driver is not meant to be used in a 50 Ω environment at the the output, but because the load resistors of the differential pair are also 50 Ω, 6 dB additional loss in the S21 is expected compared to a capacitive load situation. For larger input swings, the driver's output swing is clipped to 2 V_{ppd} for a capacitive load and 1 V_{ppd} in a 50 Ω environment. This is why the large signal gain of the driver decreases with increasing input amplitudes. The bandwidth ranges from 38 GHz for small signals to 50 GHz for large signals. Simulation results are added to Fig. 18, showing a maximum deviation of 2 dB from the measured S-parameters.

VI. Electro-Optical Experiments

As mentioned before, the driver is wire bonded to a 50 μm GeSi EAM (Fig. 19). The EAM was reverse biased by placing V_{Bias1} on 3 V and V_{Bias2} on 2 V and the photocurrent sunk by the driver is 1.5–2 mA. A tunable laser at 1560 nm at 10 dBm output power was used, where the EAM has the best ER versus IL trade-off [2]. The electrical 200 mV_{ppd} differential input signal was applied to the driver by a GSSG 67 GHz RF probe. We used a 92 GS/s arbitrary waveform generator (AWG) to generate a pseudorandom binary sequence (PRBS) 2^9-1.

The light was coupled in and out of the optical chip by grating couplers with an IL of ∼6 dB, so the estimated power into the EAM is ∼4 dBm. The average transmit optical power in the fiber is −7 dBm, which was amplified by an erbium doped fiber amplifier (EDFA) to 9 dBm before entering the photodiode. Due to the lack of a suitable high-speed transimpedance amplifier (TIA), we used an EDFA to compensate and overcome the reduced sensitivity of a single 50 Ω matched photodiode. The photodiode has a responsivity of 0.6 A/W and a bandwidth of 70 GHz. Figs. 20 and 21 show the eye diagrams of the back-to-back link and after 2 km of standard single mode fiber (SSMF). The eyes at 70 Gb/s, the maximum bit rate for which the used AWG still generates a clean signal, are clearly open, even after 2 km SSMF. The measured ER is 4 dB with a driver output swing of 2 V_{ppd}. The power consumption of the driver is 61 mW, which leads to 0.87 pJ/bit at 70 Gb/s.

Bit error rate (BER) measurements were performed for the back-to-back case and after 2 km of SSMF (Fig. 22), showing that the transmitter is error free (BER $< 10^{-13}$) after 2 km of SSMF up to 56 Gb/s. Above 56 Gb/s, we were unable to measure the BER due to the limited speed of the used BER analyzer. For each BER measurement, at least 10 errors were counted and for a BER $< 10^{-13}$, we waited until 10^{-14}.

Horizontal eye openings for 50 Gb/s and 56 Gb/s were verified with bathtub curves (Fig. 23). For 50 Gb/s there is an error free (BER $< 10^{-13}$) window of 8 ps and for 56 Gb/s this is 5 ps.

Table I compares this work to other EAM and microring drivers with electro-optical experiments. We achieved the highest bit rate with a very low power consumption. The realized driver has the lowest power consumption compared to the other

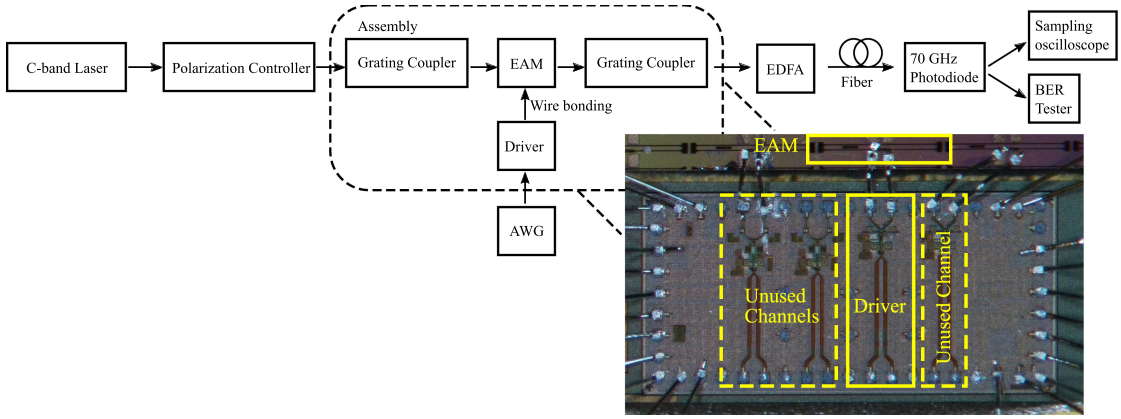

Fig. 19. The assembly and measurement setup used for the electro-optical experiments. The driver is wire bonded to a 50 μm EAM from imec's Silicon Photonics platform. The estimated distance between the driver's bondpads and the EAM's bondpads is around 180 μm.

TABLE I
COMPARISON OF REPORTED NRZ DRIVERS WITH OPTICAL EXPERIMENTS (BIT RATE > 50 GB/S)

Ref.	Power [mW]	Speed [Gb/s]	Efficiency [pJ/bit]	Swing [V_{pp}]	modulator	Modulator load	Chip Area** [mm^2]	Min. BER
[7]	40*	56 60	0.71 0.66	1	microring	capacitive	0.15	$2 \cdot 10^{-11}$ $2 \cdot 10^{-4}$
[8]	31*	50	0.61	1.5	microring	capacitive	-	-
[17]	1400	56	25	1.7	EAM	50 Ω	2.52	-
[18]	84	56	1.5	1.3	EAM	50 Ω	-	$\approx 8 \cdot 10^{-8}$
This work	61	56 70	1.1 0.78	2***	EAM	capacitive	0.37	$<10^{-13}$ -

*Driver only, without wavelength stabilization
**Including bondpads and IO-ring
***Differential swing

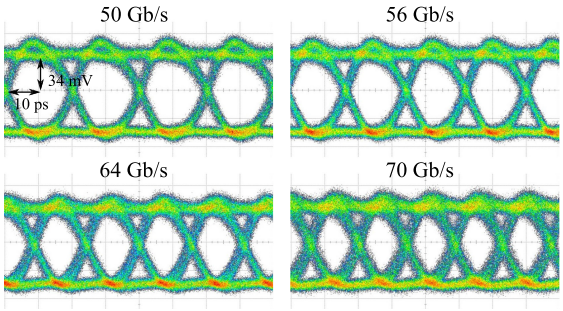

Fig. 20. Eye diagrams of the electro-optical experiments received by the photodiode (back-to-back).

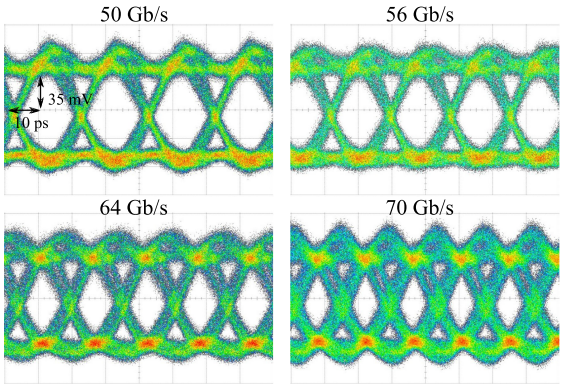

Fig. 21. Eye diagrams of the electro-optical experiments received by the photodiode (after 2 km of SSMF).

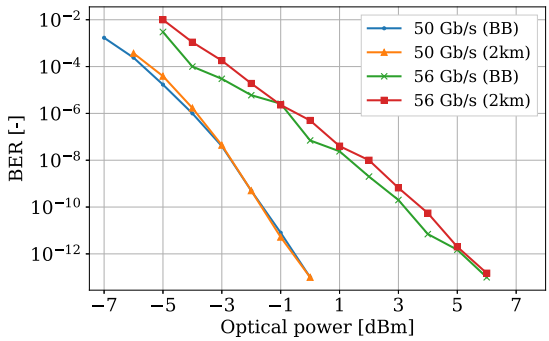

Fig. 22. BER curves as function of received optical power of the electro-optical transmitter for 50 Gb/s and 56 Gb/s.

EAM drivers. The reported microring drivers consume less power, but they didn't include wavelength stabilization circuits and heater, which will both increase the power consumption. Microring modulators suffer from process and temperature variations, shifting the resonance wavelength and reducing the modulation efficiency. Wavelength stabilization is therefore essential for datacenter applications. Depending on the implementation of the heater, the power efficiency ranges from a few milliwatt to 10 mW/nm [10], [29]–[31]. For a 7.5 μm radius microring, this leads to an added power consumption >10 mW to cover the free spectral range of the microring [10].

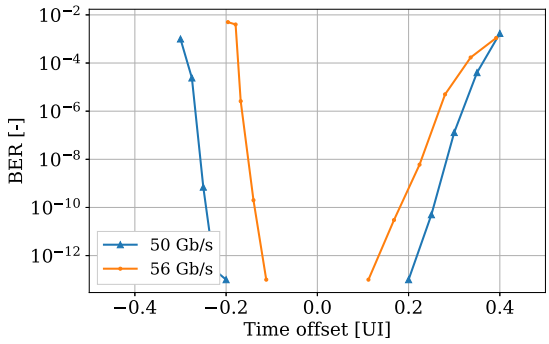

Fig. 23. Bathtub curves of the electro-optical transmitter for 50 Gb/s and 56 Gb/s.

VII. Conclusion

In this paper, we proposed a novel technique to differentially drive an EAM while simultaneously applying a reverse bias voltage. Application of the bias voltage is done without requiring bulky electrical passives. An analysis of the problems with bias-T connected EAM's was provided and a DC-coupled solution was proposed. This technique was implemented in a driver chip fabricated in a 55 nm SiGe BiCMOS technology. The driver consumes only 61 mW at 70 Gb/s operation, resulting in 0.87 pJ/bit efficiency.

Acknowledgment

The GeSi EAM devices were developed as part of imec's Optical I/O R&D program.

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