A Study of the Thermal Cycling Performance of Solder Joints in Area Array Packaging

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Abstract

For both the electronics manufacturer and consumer, reliability is an essential characteristic defining the quality of the electronic component and system. Gradual degradation of the electronic components decreases efficiency of the system, and lack of reliability can lead to a significant loss. Efforts at achieving better quality and reliability of electronic components involve the inspection of solder joints in area array packaging. It is of note that solder interconnections are the vulnerable parts of circuit board assemblies (CBA), because they are mainly subjected to various assembly process during electronic manufacturing as well as environmental exposure failures during service. Therefore, the reliability of solder joints is a major concern during the entire life of an area array packaging in order to minimize the electronic failure rate that may lead to large losses.

This thesis aims to provide a solution that helps to overcome some of the challenges that can occur during the reliability inspection of solder joints in area array packaging. Firstly, by successfully developing a non-destructive monitoring methodology to study the performance of solder joints under thermal cycling test. The quality of the solder joints in this research work from growth to failure was monitored by using a type of ultrasonic inspection called acoustic micro imaging (AMI). Results indicate that provided a suitable AMI parameters is applied, one can generate a 3D reconstruction of the solder joints images to allow and assess the solder joints' behaviour in flip chip packages. AMI inspection of solder joints show good agreement with the results obtained that was used to examine how the reliability was affected by the geometry and position of the joints.

An automatic segmentation technique was developed that allow to characterize and extract distinctive features of solder joints on different area array packages; such features include mean intensity, structural similarities model and histogram intensity of the region of interest of solder joints. The validation experimental results have been statistically implemented using novel geometrical and time domain features extraction methods like area, form factor and standard deviation. The result from these methods were used to extrapolate the solder joint's fatigue life at normal operating conditions. Moreover, the analysis of variance (ANOVA) was employed to determine the percentage contribution of solder joints parameters on the acquired images. The results indicated that the thickness of the printed circuit board can affect solder joint reliability.

Dedication

This thesis is dedicated to my wonderful family

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The completion of this thesis would not have been possible without the support and nurturing of people that has contributed positively to this work, I am deeply grateful for all your support.

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Adeniyi Olumide Ayodele

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List of Abbreviations

ºC	**Degree Celsius**
σ	**Applied Stress**
λ	**Wavelength of the ultrasound wave**
γ	**Shear strain**
$\Delta\alpha$	**Board to component CTE mismatch**
$\Delta Tfield$	**Temperature change in the field environment**
$\Delta Ttest$	**Temperature change during accelerated test environment**
Nf	**Weibull characteristic life**
Nf_field	**Cycles to failure in the field**
Nf_test	**Cycles to failure in the test**
3D	**Three Dimensions**
cm2	**Centimetre square (unit)**
mm2	**Millimetre square (unit)**
A	**Solder joint crack area**
A1	**Solder-dependent creep constants**
AAP	**Area array packaging**
AF	**Accelerated Factor**
ANOVA	**Analysis of Variance**
AMI	**Acoustic micro imaging**
ATC	**Accelerated thermal cycling**
BGA	**Ball grid area**
CALCE	**Centre for advanced life cycle engineering**
CBA	**Circuit board assembly**
CDF	**Cumulative distribution function**
CTE	**Coefficient thermal expansion**
DIP	**Dual flat package**
DOD	**Department of Defence**
DIC	**Digital image correlation**
ECU	**Engine control unit**
$F\#$	**Degree of achievable focusing**
FC	**Flip chip**
FE	**Finite element**

FR-4	**Flame retardant**
HASL	**Hot air solder Level**
I/0	**Input and output**
IEEE	**Institute of electrical and electronic engineering**
LJMU	**Liverpool John Moores University**
NDE	**Non-destructive technique**
NDT	**Non-destructive technique**
Pb	**Lead**
PCB	**Printed Circuit Board**
POF	**Physics of failure**
QFP	**Quad flat package**
ROI	**Region of interest**
Sn	**Tin**
TC	**Thermal Cycling**
VRM	**Virtual Rescanning Mode**

1 Introduction

Reliability of solder joints in area array packaging is one of the paramount qualities in characteristics of electronic systems. Generally, in today's technological world, almost everyone depends upon several electronic systems, for example our electric appliances, mobile phones, smart watches, computer systems, in banking industries, in aerospace industries and in the health care sector. Technology innovation has resulted in today's customer expecting those various electronic gadgets or systems to provide adequately designed functions when requested along with greater reliability. As you most likely have encountered, sometimes those electronic systems do experience certain failures that make them unable to function and deliver the desired quality as expected during usage. Unexpected failures occurring in those electronic systems always has a negative impact on the system reliability which can lead to excessive downtime and large losses such as high maintenance cost and loss of revenue. Nevertheless, the variety of materials in an area array packaging has led to the development of complex systems and increasingly retains a high level of reliability. It is clear that the reliability of solder joints is a major concern during the mission life of an electronic product, because they are the critical link in circuit board assembly. Hence, it is paramount to determine the factors that affect the solder joint reliability in area array packaging.

This chapter describes the definition of area array packaging and its necessity in electronic devices, the background of the research and some motivational key points on the performance of solder joints under thermal cycling test in area array packaging are described. In order to improve the reliability evaluation of solder joints, the study aim and objectives are set to facilitate better non-destructive techniques to monitor the reliability of solder joints in an area array packaging. Contributions to knowledge and novelty are presented. The content of each chapter in this thesis is outlined while a complete framework is proposed.

1.1 Background Knowledge of Area array packaging

The term area array packaging (AAP) describes the process of housing and interconnection of integrated circuits to form an electronic system. The packaging techniques can be classified in two different types' which are the through-hole technology and surface mount technology. In field electronic packaging, the precision and quantity of the different types of packages as shown in Figure 1-1 since the 1970's can be portrayed as a through-hole technology. For example, the dual in package (DIP) and quad flat packages (QFP). In which during the assembly process, the input/output (I/O) connections of the package or component leads are inserted through holes in the printed circuit boards and then transferred to the soldering machine for finishing process. Although, this type of technology provides strong mechanical bonds to the package and are more dependable, the restriction of the technology is that it only make use of the sides of the components of the board, leaving a substantial amount on the back side of the printed circuit board unutilized. In order to address the size constraints in through-hole technology, packages with solder joints were developed in the late 1980s. This new mounting technology was called surface mount technology. This technology have the advantages to provide high functional package density on the printed circuit board. Increasing transistor-gate counts based on the technology has constantly driven the growth and production of smaller packages with ever more input and output (I/O) connections. These I/O demands have driven peripherally leaded surface-mounted components to smaller lead to lead pitches (Milton et al., 2013). As a result of the added complexity, circuit board assembly yields and costs have been adversely affected. To address these problems a ball grid array package (BGA) was designed. The BGA package is a type of package that makes use of solder joints to connect the substrate to the PCB instead of pins, to have more convenient AAP for integrated circuits and large interconnects on the packages (Aryan et al., 2018). The continuous advancement on flip-chip technology has led the BGA and chip scale package (CSP) packages to develop into Flip Chip On board (FCOB) packages as shown in Figure 1-2(b), where the solder joints served as the first level interconnects, with the silicon die flipped over and mounted directly on the printed circuit board using soldering technologies.

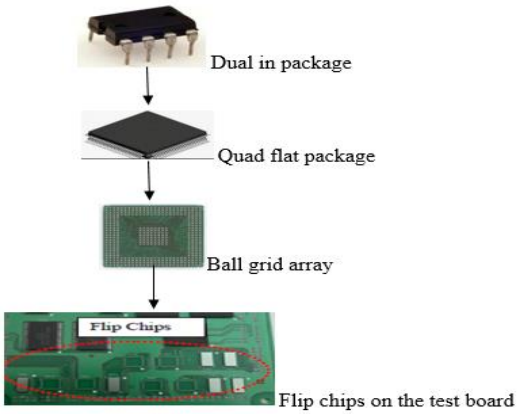
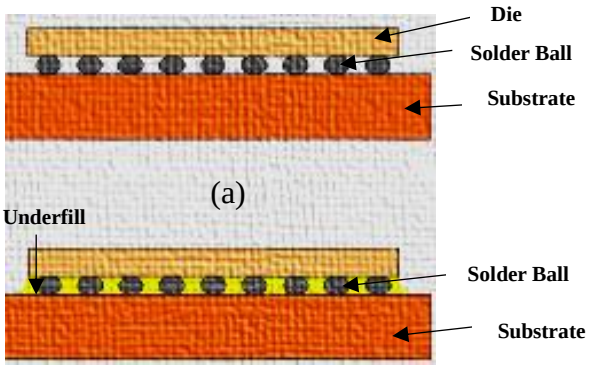


Figure 1-1: Types of packaging



(b)

Figure 1-2: Illustrates (a) Flip chip without underfill material and (b) Flip chip with underfill

The commercial use of surface mount technologies is motivated by various positive factors, like increasing the demands and supply of smaller die and packaging, increasing the heat dissipation and reliable interconnects. These factors have made the packages one of the most widely known growing technologies over the past few years (Wolter et al., 2007).

The area array packaging techniques provides the following advantages: (i) The AAP greatly increases interconnection density, and this is probably the most important driving force that has made it a widely known package today. (ii) The AAP are designed for high heat dissipation, in other words they are good in thermal management (iii) AAP are built

in solder source thus removing the need to apply paste for wiring board (iv) They could accommodate more than one chip. It is noted that area array electronics packages have been increasing in the interconnect density, and the substrate size, the increase in density will result in scaling down in package size (Vardaman, 2004, Harvey et al., 2007).

According to (Vardaman, 2004), it was cited that the packaging techniques of flip chip on AAP is becoming more complex in geometry and material properties with 50% annual growth in solder bumps while reducing the package size. The ever reducing package size results in smaller interconnect size (solder bumps) and unsurprisingly results in allied reliability issues experienced at the interconnect boundaries.

During usage, the solder joints on the manufactured flip chip packages are exposed to various environmental conditions, such as temperature, thermal shock, humidity and vibration, which contribute to their mechanical, chemical and electrical failures. According to Steinberg, (2000), reliability was defined as the probability that a system will perform it intended function at a specific period of time, when operated under a specific conditions. It was found out that 55% of the failures of electronic products related to their operating thermal environment during usage as shown in Figure 1-3, vibration is responsible for 20% of the failures, 5% of duct and another 20% were related to humidity.

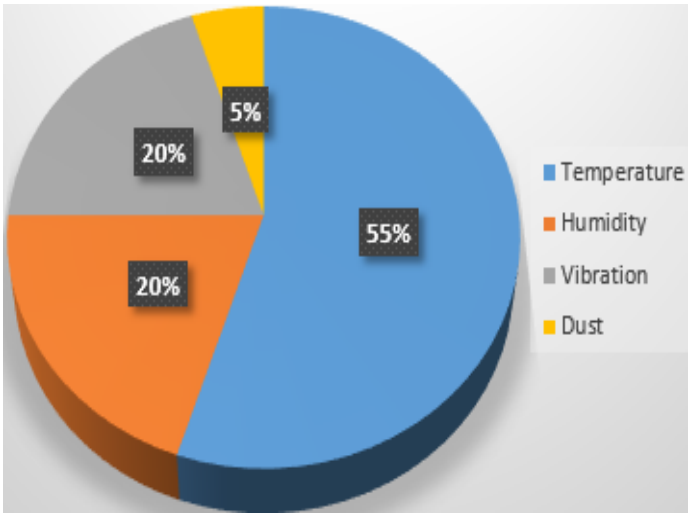


Figure 1-3: Failures of electronic products related to their operating environment

The reliability of solder joints is considered as the main concern for AAP since they are the vulnerable link in terms of circuit board assemblies' (CBA) reliability. This is

due in part to the coefficient of thermal expansion mismatch in materials used in the construction of components found on CBA, when exposed to thermal cyclic environmental conditions that in turn causes severe reliability issues and decreases the life cycle of the area array packaging dramatically. Additionally, many of these packages are constructed and required to operate in harsh environments for example in automotive and aerospace industries. Thus, the rate of change, exposure time and thermal excursion limits are dependent upon product application and usage known as 'Mission Life'.

In other words, the reliability of solder joints is a topic that has generated much interest over the last century and cannot be overlooked in the development of new area array packaging due to its varied application. It is very important to know that the vast amount of manufacturing engineering efforts goes into evaluating the reliability of solder joints, and trying to identify the fundamental causes of their failure during usage. The reliability of solder joints has become a major issue to be address because solder joints do not only provide excellent electrical connection, but they mechanically affix the component to the PCB that provides conduits for heat dissipation into the circuit board and help match expansion differences between PCB and components.

It is important to know that the reliability of solder joints has become a major issue of concern to electronic manufacturers because the package can also generate heat by itself as the current flows through it, also by an external environment to which it is exposed. For example, on an engine-mounted electronics control unit (ECU) in a vehicle that provides certain information on the dashboard, i.e. the speed, engine revolutions and fuel level, because of the different thermal properties of the materials involved during usage. The variations in temperature generated in the system cause coefficient thermal expansion mismatch between the substrate and the chip. Kulshreshtha and Chauhan, (2009) reported that due to this mismatch, distortion between the substrate and silicon die at extreme environmental operation will occur. Pang et al., (2001), also stated that the solder joints will begin to distort and cause creep to happen inside them when subjected to temperature loading. The creep distortion actuated by the temperature variations causes initiation and propagation of cracks in the solder joints. The level of propagation of cracks impairs the electrical functionality of the solder joints in the package. However, based on the need to observe and obtain solder joints' reliability data to better understand the failure rate and life characteristics, a novel approach presented

in this work, helps to assess the reliability of solder joints an AAP is able to withstand, by placing the CBA under thermal cycling test. The accelerated cycling test is used to generate rapid ageing of the flip chips' components on the printed circuit board, so that the effects of ageing or solder joint fatigue can be studied in a shorter period of time.

1.2 Motivation

As the components became much smaller, there is an absolute need to understand the critical reliability challenges of those area array packages. Over the past years, area array packages have become the most commonly used package for both design and manufacturing of electronic systems. The area array packages have become the package of choice to the electronic manufacturers because of their advantages such as the increase in capability and functionality of the circuit board assemblies. Apart from these, electronic manufacturers need to exceed customer design expectation by designing more reliable products with a very good performance before those electronic products go to the market. Nevertheless, in area array packages, such as ball grid arrays (BGA), solder joints interconnections are often the weakest link in terms of product reliability, which alone can provide coefficient thermal expansion (CTE) mismatch when subjected to environmental exposure. The CTE mismatch that occurs between the circuit board assembly and the packages, has a significant effect on solder joint reliability.

In order to reduce the solder joints failure rate and the time spent in performing reliability testing of solder joints in those components, the goal of this research project was to develop a new methodology for solder joints' reliability inspection in area array packaging based on an ultrasonic inspection technique called acoustic micro imaging (AMI). This technique has been used along with the accelerated thermal cycling (ATC) test to inspect the performance of solder joints under flip chips due to their great capability to detect anomalies within materials and interconnections.

Due to the limitation in life monitoring of solder joints, the research methodology will aid the design of solder joints through life validation tests, in which tests results from a reliability standard point in this project, can be used to create proper monitoring tests capable of generating adequate solder joints failure data that could occur during the desired service level.

1.3 Aims and Objectives

In order to obtain accurate and meaningful information on life distributions, reliability and failure rate of solder joints in area array packaging, it is critical to choose a proper failure criterion and use the appropriate measurement technique to monitor the failure events in the test. The aim and objectives for this research project are described briefly in the following sections.

1.3.1 Aims

The main aim of this research study was to estimate and monitor the failure rates of the reliability of solder joints under thermal cycling test using a non-destructive technique (NDT) called acoustic micro imaging (AMI).

1.3.2 Objectives

In order to achieve the overall aim of this research study, the following goals and objectives were set:

- To validation test solder joints in area array packaging using ATC which will enable an assessment and reliability analysis for electronic products.
- To establish a protocol for non-destructive inspection using techniques like Acoustic Micro Imaging and X-ray in order to ensure inspection of solder joints at set intervals, while maintaining the integrity of the package for further test cycles.
- To investigate the use of image processing techniques with the goal of extracting the features that represent the integrity of solder joints in the AMI images.
- To determine the reliability of the solder joints under validation test through evaluation using geometrical and time-domain feature extraction methods to estimate the fracture area, form factor and the standard deviation of the joints.

1.3.3 Novelty of this Thesis.

Despite the fact that a number of studies considering the subject of the reliability of solder joints exist in the literature, extensions of the concepts of through life monitoring of electronics is still rare. If one can assess the extent of the degradation from an expected normal operating condition for electronics then the data can be used to meet several goals, such as minimizing unscheduled maintenance, extending maintenance cycles, advance warning of failure and, reduction of life cycle cost of equipment by decreasing inspection and inventory costs.

A new thermal profile of -40ºC to +85ºC was designed in this performance study by balancing the test time and the number of data points requested for monitoring the crack initiation and crack propagation. This thermal profile developed led to a slower failure process, which enabled finer tracking of crack propagation in solder joints as depicted in chapter 6 of this thesis. The profile also facilitated the development of an image feature based joint fatigue degradation model for through life monitoring of crack propagation and prognosis of electronic devices.

An automated ultrasonic inspection and monitoring system of the solder joints on the flip chips was designed in this performance study that solved some existing issues in capturing the fatigue failures rate of solder joints under environmental exposure. This kind of techniques have been used along with the accelerated thermal cycling (ATC) test to inspect the reliability of solder joints due to their strong capability to detect discontinuities within materials.

The research presented in this thesis achieved the following tasks:

- Show how temperature affects the properties of large area array package solder joints' fatigue life. It is very important to examine and determine why the thinner board of 0.8mm is failing before the thicker board of 1.6mm when the contrary should have happened according to (Darveaux et al., 1998; Syed et al., 1999, Primavera, 1999; Lau et al., 2002; Vandevelde, 2004; Birzer et al, 2006; Ahmad et al., 2009; deVries, 2009). This research tries to find the trend of change of behavior for flip chips components on boards during the thermal cycling test, i.e., to see if a particular thickness with one kind of board is better or worse. It was found out that the fourteen flip chips on non-under filled

1.6mm hot air solder level (HASL) board has a prolonged life cycle compared to 0.8mm HASL substrate thickness board during the through life monitoring test.

- As the reliability for each flip chips component on different printed circuit board thickness is calculated for a specific time based on component age, this thesis aims to study the reliability of solder joints under thermal cycling test on those flip chips and validate the results against the appropriate simulation global model. Once validated, it also aims to design a robust image segmentation process that was implemented on the extraction solder joints images to understand the effect of various solder joints geometry and thermal parameters on solder joints reliability on area array packaging, and use such a study to develop the histogram difference, structural similarities difference and the intensity level that represent the performance of the solder joints under thermal cycling test.
- The research presented in this thesis proposed a new non-destructive methodology that can be used to acquire both 3D and 2D acoustic scans data during validation test. In the proposed method, ultrasound images were collected at different sets of intervals to verify the fatigue degradation and failure rate of solder joints occurring at the bump to silicon interface. These test results are extremely useful in investigating crack nucleation and propagation. Likewise, in the segmentation approach, the region of interest as shown in Figure 5-10 in the acquired solder joints during the environmental test is correctly detected from the background.
- In this research, analyses of the extraction results using geometrical feature extraction like area, form factor has demonstrated better stability in measuring the solder joints' defects in the acquired AMI images. Further analyses on those solder joints was done using analysis of variance (ANOVA) techniques that demonstrate how the PCB thickness affects the failure rate of solder joints.
- The research also determines and evaluates the variations in regions of interest in solder shapes under thermal cycling test using the form factor methods. Thus, the results depicted that if the region of interest shape is convex apex it

could lead to a big significant crack area, but a proportionally smaller crack area could occur when is it in concave apex form.

1.4 Thesis Outline

This thesis is a broad study of the performance of solder joints under thermal cycling test, consisting of seven chapters and some appendices. The contents of each chapter are as follows:

Chapter 1: Introduction and background – This deals with the background and inclusion of reliability of solder joints in area array packaging. It discusses the reliability prediction of solder joints of electronic components in previous research. The aims and objectives, contributions to knowledge of this research are also outlined.

Chapter 2: Literature Review - goes over different backgrounds and previous work done that are needed for this performance study, including thermal cycling inspection on electronic packaging and non-destructive inspection.

Chapter 3: Methodology that includes ATC testing and measurement – This provides insight into the thermal cycling experimental rationale, the various test samples, facilities, and design of experiments.

Chapter 4: ATC through life monitoring tests – This is a more important section, as it investigates the role of thermal cycling test on solder joints in PCB's, by performing a real life monitoring test on those solder joints that was based upon a low thermal profile. This method gives an adequate procedure for finding out reliability or time to failure of solder joints. ATC parameters associated with the testing will be focused on.

Chapter 5: AMI analysis of solder joints – This demonstrates how to ultrasonically examine the evolution and failure path analysis in solder joints. This approach has

been implemented to analyse and monitor the failure rate and reliability of solder joints under thermal cycling test. Using the application of industrial acoustic imaging systems available in Liverpool John Moores University (LJMU) ultrasonic laboratory, AMI images were taken throughout the validation tests for further processing. Inspection analysis using the AMI methods are also demonstrated.

Chapter 6: Crack evolution on different solder joints on the test samples – This study provides details about the results of the experimental study of crack growth in solder joints for different numbers of thermal cycles using AMI techniques on the PCBs. It presents the results of crack initiation using Matlab tools for solder joints under different post-process conditions like geometrical method (GM) feature extraction. This also provides detailed experimental investigation of crack propagation in solder joints, located under AMI techniques.

Chapter 7: Analysis of variance was used to determine the significant factors which affect the solder joints characteristic life under temperature cycling ranges.

Chapter 8: Conclusions and recommendation for future work – This provides summary/observations from the experiment and analytical studies, notes the contribution to knowledge and proposes future work and recommendations.

2 Literature Review

In order to understand solder joint reliability on area array packages under thermal cycling, then some background material is necessary. The background material covered in this chapter includes the fundamentals of area array packages; accelerated temperature-cycling tests on solder joints and non-destructive inspection techniques. Thus, only the successful integration of these various methods can lead to the successful development of solder joints' reliability inspection methodology that meets the overall research goal.

It is of note that area array packages (AAP) have gained popularity in major electronics applications due to their proven thermo-mechanical reliability and standard assembly techniques. In the processes of microelectronics manufacturing, electronic packaging provides electrical connection thermal and mechanical functions to semiconductor chips. Nevertheless, AAPs consist of solder joints that have proven to be valuable as a mechanical and electrical interconnect material in the electronics manufacturing industries due to their low melting point, wetting behaviour, electrical properties, and availability. However, solder joints on the packages have also proven to be very sensitive since they are the weak link in circuit board assemblies which exhibit such phenomena as age and cycle softening, grain-growth hardening, strain-rate hardening,(Wen et al., 1997). Despite many decades of characterizing solder joints' defects in AAPs, there are still some challenges in monitoring how the cracks in solder joints initiate and propagate. A very elementary view of solder joints' reliability was reviewed in this chapter, primarily to enable one to understand how to choose the right methodology to use when conducting a reliability test on solder joints on area array packaging.

2.1 Reliability issues in Area array packages

What is reliability of an electronic system from your own perspective? Take for example, switching on your mobile phone, would you consider your mobile phone to be perfectly reliable if it did not switch on immediately? Would you consider your mobile phone reliable if it takes more than two times to switch on? Based on your answer to the questions, it becomes more complex and hard to define and determine the reliability of the electronic system. Moreover, the reliability of the electronic components is increasingly becoming a paramount issue for electronics manufacturing engineers, as

mostly our everyday schedule and activities are more dependent on the functionality of those systems.

Although, it is of note that the reliability of electronic systems has generated much interest over the last century due to its varied applications and failure rates. The US Department of Defense (DOD) developed the reliability assessment of electronic system and circuit board assemblies to estimate the need for maintenance and logistics in the 1960's using prediction tables and software, documented in MIL-HDBK-217 (Pecht, 2001). It is common knowledge in literature that the developed method predict the expected useful life of electronic boards, incorporating certain components by using databases of electronic equipment failures.

Thus far, this class of traditional reliability approaches, known as the handbook method (MIL-HDBK-217), was recommended by (Pecht, 2003) to be abandoned after reviewing the development record and drawbacks in the technology of methods used for reliability assessment. A manual, IEEE 1413.1, 'IEEE Guide for selecting and using reliability prediction based on IEEE 1413', gives data on appraisal of the normal strategies for dependability expectation for a given application (IEEE standard 1413.1, 2002). It has been demonstrated that the Mil-HDBK-217 and the related handbook techniques, are not reliable. However, Pecht, (2003) developed the approach of design for reliability in the institution of Centre for Advanced Life Cycle Engineering (CALCE).

The reliability predictions, which were generated via the handbook, were based on basic heuristics, contrary to engineering design methods and the physics of failure (POF). However, the components in the handbook are out dated, which makes the job of keeping it updated very expensive. Due to this limitation, the reliability prediction is categorized into three classes of alternative method; these can broadly be classified as Physics of failure (POF), field data and test data from reliability test. The goal is to improve the understanding behind the reliability of electronic system which will enable designers, design more efficient products.

Firstly, a POF method technique uses the knowledge of mechanisms and processes to predict the reliability of a product analytically without having to resort to using the handbook method (Hendrick et al., 2015). This kind of approach dominates the reliability modelling, (Adithya Thaduri, 2013). POF actually models the root causes of failure such

as fatigue, fracture, wear and corrosion from the design phase to field data operation. (Hillman, 2002). This process has usually been done by gathering the information from the acceleration test and the statistical distributions (Perry, 1999 and ASM, 2004). The goal is to enable electronic reliability designers to gain more understanding on the reliability assessment of the product. Thus, the information and understanding derived from the use conditions and specific duration of thermal exposure helps the electronic design and manufacturers to make a remarkable note about the mission life of the products.

One of the key limitations of POF is that the algorithm is difficult to model and typically assumes a 'perfect design', (McPherson, 2010). In other words, the design engineers involved in the modelling should be able to understand and identify the system architecture and the effect of the validation test on the system. For example conducting an adequate study on the PCB material properties is critical step, in comprehending how the stiffness or the thickness of the PCB influences other parameters involved in the design. Thus, inadequate understanding could lead to the POF prediction being limited to end of life behavior.

Secondly, the field data method is important to the reliability engineering program. This type of design is required to improve the quality and implementation of the traditional reliability procedure used to describe the failure mechanisms, failure modes and failure sites in the MIL-handbook 217. The benefits of the field data method over the handbook method are significant, i.e. the data can be evaluated over the design before making a prototype, which will surely help to compare the existing reliability requirements with the current product in market (Adithya Thaduri, 2013). Thus, the kind of information received from the field data gives a specific measure of the expected product performance. The fundamental approach of this test data technique is necessary to assess and to be able to understand the reliability procedures expected from a product for environmental protection. For example, when the data from the similar field experiments are required, predictive equations for reliability study of the same product can be achieved.

Thirdly, the reliability testing of electronic products of components on the AAP in the early stage is important, to identify the mission life of the components, as it produces the

most significant information and data on the products. In order to assess the reliability of an electronic product, several approaches are involved. By going through the review of the work published by (White, 2008; (McLeish, 2010), it was suggested that this was a period in which the field data, test data and POF method were all competing to replace the traditional handbook methods as previously mentioned. it is important to know that each method has its merits and demerits, and if applied appropriately provides valuable results. Considering this, the IEEE (Institute of Electrical and Electronic Engineers) recently released a standard. (Jais, 2013) emphasized the reason for examining the three classes of alternative methods is that records of the failure occurrence, causes and prevention can be reviewed more precisely.

Reliability plays an important role in electronics manufacturing industries, due to the continuous reduction in package size. In packaging, modern electronic products are getting more flexible, composite, and thinner with higher interconnect density and speed, which must endure various stresses during their usage. These factors make it more difficult to design and develop a predictive solder joints' reliability process. Likewise, Floor plan layout, assembling and component quality all greatly influence the general reliability quality of a product.

Subsequently, precise analysis and reliability prediction of solder joints in area array packaging under thermal cycling test are considered tedious, due to a number of factors that could affect the solder joints' performance. Some of the factors are: (i) Mechanical stresses that cause delamination, fracture on the solder joints during usage, unintended stress from the intermetallic compounds , (ii) over constraint of the PCB's, and (iii) the soldering defects resulting in fracture, creep, diffusion voiding.

It is of note that one of the most common failures associated with solder joints is unexpected harsh environmental exposure during usage. Generally, temperature is the major causes of failure of solder joints in an electronic product. This particular failure occurs by inducing thermal stress in the solder joints, under normal operating conditions. This is because the solder joint is a eutectic alloy not an isomorphous solution (Kanchanomai et al., 2002). A eutectic alloy is formed between metals of very different parameters such as Sn-Pb, The failure that occurs in solder joint with a eutectic alloy during the validation test is mainly due to the high CTE (coefficient of thermal

expansion) mismatch deformation between the silicon die and organic substrate during environmental operation that leads to fatigue failures. As the temperature increases or decreases, materials having different CTE will shrink or expand, which result in stress in the interconnections. The creep strain distribution within the solder joints will vary depending on the relaxation of the joints. Both spatial and thermal gradients, coupled with the CTE mismatch generate the thermally induced strain and stress on those joints which is considered as the dominant failure mode in solder joints' interconnection.

Thus, one of the ways to assess the reliability of solder joints in AAP is by using accelerated cycling test (ATC). An accelerated cycling test is used to obtain information quickly on the desired usage level, failure rate and reliabilities of a product. For example, the design life of a car is typically 15 years. Therefore, it is unrealistic to expect 8,000 hours or 5000 to 1000 thermal cycles over 15 years. If a thermal cycle depending on the thermal profile in the field is 2 hours on average, then we are looking at 10000 to 20000 hours of testing. This is too long to be compared with design life cycles and hence we have to accelerate the testing. By using ATC, the prediction of solder joints' reliability must consider the aging effect on the component's life.

It is often found that in major electronics products, Eutectic tin lead solder (63%Sn, 37%Pb) has been used for area array packaging for more than 30 years because of its low melting temperature, excellent copper wetting and high heat dissipation, (Kanchanomai et.al., 2002). During the useful life of the solder joints on the packages, its reliability is a function of various stresses like thermal, mechanical and electrical stresses over time. (Edwards, 2012). Those stress applied to solder joints through thermal cyclic test fatigue were considered in the literature to result in the most dominant failure mechanisms. Several authors in literature have utilized ATC tests to approach subject matters, for example, Lodge and Peddar, (1990) conducted ATC tests to analyze the reliability of zirconium-titanium-stannate (ZTS) dielectric flip chip assemblies. Seyyedi ,(1993) also illustrated the use of ATC to study the thermal fatigue behaviour of low melting point solder joints. Ghaffarian, (2000) reviewed the reliability of BGA and CSP assemblies by making use of several thermal profiles.

Meanwhile, in other publications reviewed, authors have taken an experimental approach to address the subject matter in order to study the reliability of electronic systems. Schubert et al., (2002) conducted a test in which the mechanical and physical

properties, the tensile stress / strain rate, and the microstructure appearance of two lead free solder alloys, Sn96.5Ag3.5 and Sn95.5Ag3.8Cu0.7 was studied using ATC tests (Schubert et al., 2002). Bhate observed that 'in essence this is fatigue crack growth problem' (Bhate, et al., 2007) and it is frequently studied empirically. Likewise, (Han, 2005) explains that an increase in thermal stresses of an electronic circuit board increases the failure rate and decreases the reliability through electrochemical degradation processes. High temperature can also cause melting of the solder joints of the flip chips on PCBs and can slow progressive impairment of the performance levels due to degradation effects (Turek, 2012).

Thus, the fatigue behaviour of solder joints has been studied under the premise of plastic deformation that involves the physical phenomenon of grain boundary separation following the grain coarsening because of thermo-mechanical stresses. Previous research carried out by Park et al., (2007) on a study of ATC on various BGA designs, utilized a Digital Image Correlation framework (DIC), they were able to observe the anisotropic orientation of the few grains in the joints, and observed the effect of the intermetallic compounds in the solder joints. This enabled them to observe how this could lead to plastic deformation along the grains boundaries close to the compounds that could initiate the crack in the solder joints.

The work done by Sun et al., (2015), stresses the need to improve the understanding as stated in literature; he conducted a test to investigate the influence of temperature on PCB responses. A set of combined tests of temperature was designed to evaluate solder interconnect reliability at 25 °C, 65 °C and 105 °C. Results indicate that temperature significantly affects PCB responses. More work could be done in this area by considering a softer thermal profile, in order to investigate how the crack gradually tends to initiate and propagate in a harsh environment and more in the bulk solder. Upadhyayula et al., (2001), conducted a thermal cyclic study and accounted for the process of combined effects of thermal and mechanical stresses. Thermal cyclic creep was also addressed in the above-mentioned work extensively. The creep that occurs during the test is essentially a thermal stress induced phenomenon that is associated with the homologous temperature of the solder joints' material properties. The "Viscoplastic" nature of solder joint conditions due to high homologous temperature was considered for analysis in the

above research work. This works suggests that the nature of deformations considered in the above study is predominantly in the plastic domain.

It is of note that the solder joints fatigue failures that occur in the flip chips assemblies are often reported at the chip-to-bump interface and not likely to occur at bump-to-substrate interface as shown in Figure 2-1, Frear et al., (2001 and Pang et al., (2001), reported that during the thermal cycling tests, the chip-to bump interface has the highest plastic strain concentration because of the distribution of stresses over each thermal cycle.

The image originally presented in Figure 2-1 cannot be made freely available via LJMU E-Theses Collection because of 'copyright'. The image was sourced at Braden, D.R., 2012. *Non-destructive evaluation of solder joint reliability* (Doctoral dissertation, Liverpool John Moores University).

Figure 2-1: Pictorial representation of flip chip interconnection (Braden, 2012)

Randoll et al., (2014) conducted a study on the thermal behaviour and isolation properties of Flame Retardant FR4, which is a grade designation, assigned to glass-reinforced epoxy laminate sheets, tubes, rods and printed circuit boards (PCB). Test materials were investigated for application in embedded power systems. Its goal is to minimize and evaluate different PCB materials. The temperature dependent thermal conductivity of each material was measured to show the thermal behaviour and isolation properties of FR4 materials.

Furthermore, Wan et al., (2015) explains that thermal-mechanical fatigue is one of the main failure modes for electronic systems, particularly for high-density, electronic systems with high-power components. Moreover, he cited that solder joints are often the cause of failure in electronic devices. Baik, (2008) illustrated the challenges encountered in the estimation of electronic reliability based on warranty data and recommended a technique for estimating PCB's component reliability using an accelerated life test model. Kariya *et al*. (2004) also observed that the delamination or failure commonly

started in the corner solder joints, global location depended on whole sample geometry and solder joints' geometry influenced strain within the joint. It is often assumed that an interconnection on the outermost row of a BGA on a PCB will see most accumulated strain and is the site of failure initiation (Lee et al., 2014).

Malik et al., (2011) explains more about the useful time of electronic products in his paper; he cites that the lifetime of solder joints could decrease significantly because of the large thermal stresses that occur at the chip to bump interfaces. In other publications also reviewed, authors also used a numerical approach towards predicting the reliability of PCBs. In a paper documented by Fan Yang et al., (2013), a numerical approach was used, to develop a new and computationally efficient multi-level approach to investigate board level drop reliability of a printed circuit board (PCB) assembly. Their approach was composed of two levels of finite element (FE) simulations: solder joint level and board level. Initially, static simulations of the solder joint level were used to obtain the homogenized property of the solder-under fill interconnection; explicit FE simulations of the board assembly followed this. Although he stated that some work needs to be reviewed on this part, by locating critical areas of the entire board, this could be achieved by investigating the interconnection stress on the PCB.

Ameer et al., (2015) explain the criteria and methodologies of a simulation tool that predicts the reliability and remaining lifetime of circuit boards, where the criteria of determining the position of the failed components on the board layout and their effect on the entire test sample was demonstrated. Pan (1994) used an energy-based model to compile strain energy density for eutectic SnPb solder. The model considered the crack initiation in the joints and growth by removing elements from his finite element method when they reached the threshold strain energy density value. Logsdon et al., (1990) explored Sn-Pb material parameters, such as stress intensity factor and strain energy release rate, and Fatigue Crack Growth Rate (FCGR) under isothermal fatigue tests. A survey by Jacob, (2015) in his recent tutorial paper, describes an approach towards how to improve root-cause finding of electronic component failures by means of a system-related failure anamnesis approach. While traditional failure analysis tries to analyse on the device level, this system-related method starts by providing a failure anamnesis on a system level, systematically continuing downwards via subsystems, wiring, and printed

circuit boards (PCBs) towards the device level in an opposite approach to that of subject (device)-related failure analysis.

In electronics product the integrity of solder joints on packages is very paramount and also remains the backbone for ensuring that the products perform the intended function. It is stated clearly that product reliability is related to it through life performance during mission life. In other words, the most common and feasible way to assess the operating life time of the product is by extrapolating the accelerated test results using an Acceleration Factor (AF). This could be refer to as the analytical modelling method. Accelerated factor is expressed as the ratio of cycles to failure in the field (*Nf_field*) to cycles to failure in the test (*Nf _test*). There are several methods to calculate and analyse the acceleration factors, the most common and also used as a basis of other models is the refer to as Coffin-Manson (Masson, 1996) depicted in Equation 2-1.

$$AFcm = \frac{Nf\_use}{Nf\_test} = \left(\frac{\Delta T test}{\Delta T\ use}\right)^{n} \qquad \text{Eq. 2-1}$$

Where AF is the Acceleration Factor, ΔT_{test} is the Test temperature difference (°C), ΔT_{use} is the Use temperature difference (°C), n = Fatigue or Coffin-Manson exponent.

This is used explains the crack propagation phenomenon since it addresses only the plastic behaviour and therefore this type of method but does not adequately involve the through life monitoring process on the crack initiation phase in solder joints in which the significant contributor could be thermo-mechanical stresses that could over time initiate a crack. For example, assuming the test boards which are going to be used for this experiment undergo 5 daily temperature transitions from 20 °C to 60 °C (ΔT_{use} = 40 °C), while they are normally being used, the following acceleration will occur if the product is thermal cycle tested using a high temperature of 80°C and a low temperature of -20 °C (ΔT_{test} = 100°C), assuming a typical Coffin-Manson exponent (m) of 2. The work has been calculated by using equation 2-1.

$$AF = (100 / 40)^2 = 6.25$$

Testing this electronic product for 500 temperature cycles using the accelerated conditions would therefore be equal to about 2 years of life based on the stated use conditions.

(6.25 x 500 cycles) / ((5 cycles per day) (365 days per year)) = 1.71 or 2 years

The downside to the numerical approach as illustrated by Riduot and Bailey (2007) is that the mechanistic effects such as crack initiation and propagation are ignored. Another limitation of fatigue model is that they don't adequately captured microstructural effects. As has been mentioned repeatedly in this literature review in chapter 2, corresponding to this, the solder joints' thermal fatigue testing that occurs during thermal cycling is a process that needs to continuously improve. However, accordingly Yang, (2012) illustrated in his thesis that reliability of a solder joint in a product is the probability of a product to hold its quality with the movement of time, in other words, the reliability is used as a measure of the system success in providing its function properly during its design life. Thus, reliability still remains a major concern during the lifetime of a product and is subject to continual improvements. Nevertheless, previous studies on reliability have shown that no electronic product has an interminable operational lifetime. Keeping in mind the end goal to plan a product design and show operation without failure, expected product lifetime must be determined. The critical reliability challenges of solder joints in AAP is considered as a paramount point in this research work because they play a major part in product reliability. Moreover, a broad variety of factors could affect the joints' reliability, which can also contribute negatively to the lifetime performance. However, conducting a reliability test on those solder joints using a through life thermal cycling test can reduce a lot of early problem and failure they could encounter during their operational lifecycle. ATC is achieved by subjecting the components on the test vehicle to test conditions such that failures occur sooner. So that the prediction of the reliability of the product can be made within a shorter period of time. By considering these merits, a quantitative ATC test was performed in this research in Delphi Automotive Industry. Thus, two different test samples of 0.8mm and 1.6mm thick circuit board assemblies with the proposed thermal profile of -40ºC to +85ºC to quantify the reliability of solder joints were used, to accurately project (extrapolate) what the cumulative distribution function (CDF) at use will be. Obviously, the lower the stress the longer the time needed for the failures to occur in those packages. In respect to the aim, it is imperative to conduct and evaluate the reliability study of solder joints on AAP, also to construct the life performance of solder joints' fatigue models. A wide variety of solder joints' delamination and defects exist that can negatively affect reliability. The need to perform a non-destructive evaluation (NDE)

and validation test on solder joints is critical before AAPs reach the production stage, to ensure that manufacturing quality metrics have been achieved.

Table 2-1 depicted six solder joints fatigue models, which are summarized and arranged by class.

Table 2-1: Summary of solder joints fatigue models (Lee et al, 2000 and Fan et al., 2006)

Fatigue Models	Model class	Description
Coffin-Masson (Qian et al, 1998)	Plastic strain	Based on the apply stress to the component.
Solomon (Syed, 2004)	Plastic shear strain	Low cyclic fatigue model relating to plastic shear strain. Which is focuses on the time-independent plastic effect
Engel Mainer (Syed, 2004)	Total shear strain	The total number of cycles to failure is related to the total shear strain
Darveaux (Darveaux et al, 1995)	Energy density based	These models predict fatigue failure based on a hysteresis energy system or type of volume-weighted average stress and strain history.
Stolkarts (1999)	Damage accumulation based	Involves calculating the overall damage done to solder joints.
Dasguspta (Dasguspta et al, 1992)	Total strain energy	Based on creep phenomenon or strain energy criterion. Focuses on time-dependent effect.

All of the fatigue models depicted in table 2-1 require some form of crucial information related to the specific geometry of the joints. It is important to know that most of the fatigue models produce different prediction results as certain assumptions are made in every different model. In order to apply those models as stated by Lee et al. (2000) baseline low cycle fatigue testing is paramount to acquire the values of the fatigue model constants. This baseline acquired data could be refer to as geometry specific to the region of interest of the solder joint. Hence, early fatigue model of the solder joints could fail to capture the ATC conditions like the ramp rate, dwell time, thermal range and strain amplitude because the model assumes the parameters to be empirical. Thus the practical uses in solder joint modelling is limited, because the thermal profile and the parameter's used in the validation test is consistent through the test.

2.2 Review of Solder Joints Non-Destructive Inspection Techniques.

The attachment of flip chips on area array packaging has been carried out over the past decade by solder joint technologies (Braden, 2012). The inspection of solder joints on those packages using non-destructive inspection techniques has played a noteworthy part in the improvement of better process and analysis control in the performance study of those solder joints in AAP manufacturing industries. This kind of technique has aided the internal and external inspection of those solder joints during various environmental tests. Traditionally, the inspection of solder joints has been performed manually as shown in the flow chart in Figure 2-2, for example using electrical testing as illustrated in a paper by Madhav et al., (1996). This method cannot be used to identify the exact defect on the solder joints during inspection.

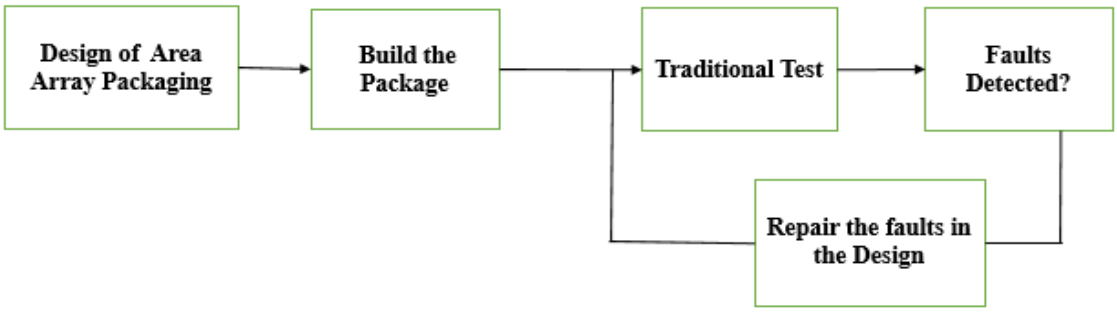


Figure 2-2: Flow chart showing traditional testing of area array packaging

Currently, the available and the most common non-destructive inspection techniques are X-ray inspection, Laser inspection, visual inspection and ultrasound inspection. These types of techniques are used to analyse the reliability and solder joints' failure rate on those components on AAP. For example, for companies deploying AAP in their products, in sensitive industries like automotive, aerospace and military, the cost of failure of those various component can be unsustainable in terms of product recall, which could actually lead to damage of the company's brand.

Likewise, according to some findings from research done by the Motor Industry Research Association, according to Square (2012), it was found that electrical problems

sum up to 70% of consumer complaints, which increased the warranty claims doing that period. Also from a previous study done by Square Trade, (2012), it was reported that 7.5% of smart phones, 6.6% of high definition cameras, did not perform the required function due to failure from non-accidental malfunctions. Therefore, the non-destructive evaluation (NDE) inspection of solder joints under various field conditions has become an important process that must be undertaken in the manufacturing industries in order to prevent early failure of those joints and ensure the quality of the end products.

During the performance study of solder joints, one of the prominent ways to ascertain the integrity and reliability of solder joints in those components is through non-destructive reliability testing. Therefore, using an NDE method, to determine and assess through-life performance of solder joints during thermal cycling's and to accurately measure product reliability, becomes a needed tool for products designers. It also gives engineers the opportunity to evaluate manufactured Circuit Board Assemblies (CBA) without physically cross-sectioning components, thereby preventing them from destructive impact. Thus far, several non-destructive techniques have been developed to investigate the defects present in solder joints in AAP, some of the techniques include X-ray microscopy (Moore, 2002), Visual inspection, Acoustic Inspection, and Laser ultrasound coupled to interferometry.
The survey methods for non-destructive inspection techniques that can be applied in the solder joints are discussed in the following sections 2.2.1 to 2.2.4.

2.2.1 X-ray Inspection

The X-ray inspection is a non-destructive evaluation (NDE) technique, developed for use in various imaging applications like AAP package and medical inspections (Yang, 2012). Thus, the X-ray system consists of an X-ray source, an X-ray collector to receive the penetrated radiation, and a camera to convert the photons on the collector to a digital form and imaging interpretation software during the inspection (Gong, 2016). When the x-ray travels to a test sample, the material absorbs x-rays proportional to its atomic mass and density (Bernard, 2003). The images from those material being used shows different image pixels because of different absorption due to the short wavelength. X-rays have a wavelength in the range of 10 to 0.001 nanometers. This short wavelength allows them

to penetrate test samples' materials. This type of technique is a contrast imaging technique that has a resolution about one to two microns, depending on the X-ray wavelength (Pacheco, 2011).

However, there are three different types of X-ray inspection namely the laminography, the tomography and the radiography. Thus, Gong, (2016) stated that most 2D X-ray systems use radiography techniques and are considered the most cost effective systems that have been used for inspection for years in many industries for inspecting volumetric defects on the packages. However, it has difficulty in detecting cracks because of the positioning of the solder joints and the presence of interfering features such as the multilayer interconnects on the substrates (Pacheco, 2011). Nevertheless, X-ray tomography and laminography are considered as 3D X-ray techniques. Figure 2-3 shows the schematic operating principle of Xradia 520 versa 3D x-ray, which are able to overcome some challenges that occur using the traditional tomography since they rely on a single stage of geometric magnification.

Figure 2-3: Schematic operating principle of *3D* X-ray ZEISS Xradia 520 Versa

The inspection microscope in Figure 2-3 uses a combination of geometric and optical magnification to produce a high resolution image of the sample. With this, the system allows to study a wide range of sample and also produces resolution at a distance (RaaD) this enable to maintain a submicron resolution at large and flexible working distance. The technique achieve images with a spatial resolution of 0.7 µm and minimum achievable voxel of 70 nm. This type of technique have the ability to inspect solder joint defects that occur in area array packages , but the test samples like printed circuit boards with large dimensions need to be trimmed and be rotated during the inspection due to the scan limit in the test chamber. As a results of the size limitation, x-ray inspection

techniques remain unsuitable because of the limitation in test samples' size and it requires long time data acquisition and image reconstructions.

2.2.2 Visual Inspection

This type of non-destructive inspection has played an important role in inspection of PCB in electronic manufacturing environment. These types of techniques are available in 2D and 3D systems; an example of 3D is laser triangulation techniques that provide faster data acquisition (Ryu et al., 1997). A 2D visual inspection system includes an illumination source to power up a device, a camera to record the acquired image and a processor to produce an output image. Thus far, Capson et al., (1988) conducted an experiment and introduced an illumination source, which uses two circular colour lamps and a camera to analyse the solder joint structure. The lamps are mounted so that their centre lies on the same axis. One lamps ring emit red light mounted at the lower angle and the other emits blue light mounted at the higher angle. As shown in Figure 2-4, the author further stored the acquired images using the RGB image capture board. The colour of the lamp is chosen to aid in the segmentation of the acquired solder joint images from the PCB itself which usually appears green (Zhang, 2006). The visual inspection as illustrated in Figure 2-4 can also be used to generate colour contours on the solder joint during the inspection in order to detect and analyse various defects like voids, delamination. However, the application of this type of inspection is limited to the peripheral column of the flip chip in the package as the light beam is affected by the outer rows of solder joints.

Figure 2-4 Image of tiered-colour illumination solder joint inspection system with two light sources (Zhang, 2006)

2.2.3 Ultrasound Inspection

This important NDE inspection technique has been employed in medical applications, and for flaw detection in packages. This type of technique refers to sound waves at frequencies higher than the range of the human ear, for example a frequency higher than 20 KHz. There are several forms of the technique but, as schematically shown in Figure 2-3, they all rely on generating acoustic waves with a piezoelectric transducer and then propagate them into the test sample under inspection via a focal lens and coupling fluid medium (e.g., de-ionized water). The same piezoelectric transducer used for the inspection then records the reflected waves and converts them into electrical energy. Thus, both penetration and image resolution are determined by the operating transducer frequency. For example, at low frequencies a transducer of 20–50MHz enables coarse ultrasonic scans of images with low resolution, but greater penetration of imaging (several mm). At the other extreme a higher frequency transducer like 230MHz generate a better spatial resolution with a lower penetration of a few micrometers. Hence, the higher the frequency waves, the shorter the wavelength, the lower the frequency, the longer the wavelength.

A basic principle of ultrasound imaging is illustrated in Figure 2-5(a), while Figure 2-5(b) depicts an AMI system. In Figure 2-5(a) the piezo electronic transducer both sends and receives the reflected waves, which is also known as pulse echo mode. This technique is carried out by immersing the transducer lens in de-ionized water. The de-ionized water that serves as acoustic impedance is mainly used as a medium to transmit the ultrasound waves. There are different types of imaging modes used to provide different inspection techniques during acoustic imaging inspection; one is the pulse echo and the second one is the through transmission modes (Sonoscan). However, the pulse echo mode could provide a better spatial resolution than the trough transmission mode, which make it more necessary in the inspection of area array packaging.

Figure 2-5 a) A basic Schematic diagram of Ultrasound imaging (Sonoscan) b) Image showing Gen6™ C-Mode Scanning Acoustic Microscope (Courtesy Liverpool John Moores University Imaging Lab)

Furthermore, the AMI techniques in Figure 2-5(a) have been used in area array packaging inspection in detecting gap-type defects such as cracks, delamination, artefacts, and voids. In a number of literature reviews, scanning acoustic microscopy (SAM) has been shown to be very useful in studying failures of plastic packages. Thus far, Yang et al., (2012) stated that they used ultrasound-imaging techniques to study how joint position and constraints can influence the reliability performance of solder joints in area array components. Likewise, Braden, (2012) stresses the need for improved solder joint reliability, based on this technique. In his work, an ultrasonic technique was proposed for through life non-destructive evaluation, in which a key solder feature, nucleating at the bump to silicon interface, which was propagating along the laminar crack plane, was captured using Acoustic Micro Imaging (AMI). The measurement data was compared to Finite Element Analysis (FEA) studies in order to understand the differences in reliability prediction. Furthermore, it was found in this study that FEA simulations that take into account floor plan layout and constraint points (resulting from gluing or screwing CBA's to a metal housing) showed a difference in predicted reliability outcome compared to traditional simulation methods. The work done was improved on by considering the shape and the size of the greyscale image of the region residing both at the centre and the outer image of the solder joint. Since the intensity values of every pixel contain some spatial information about the defect, the data obtained

can be included in the calculation to obtain the failure location more precisely and to track the crack in the joint.

Semmens et al., (1997) presented an ultrasonic based process technique concerned at improving the application of the ultrasound method to the detection of crack depth. The results obtained have provided useful information about the severity of the damage. The depth was estimated with good reliability for some of the most evident cracks presented in the sample. The maximum depth was evaluated at approximately 20 mm in the package. Shirahata et al., (2014) also proposed a methodology that determines the difference between fatigue cracks by the ultrasonic non-destructive test. They came up with the tandem array ultrasonic testing method that could figure out an incomplete penetration; the transducer used for the tandem array could determine the reflected wave at the incomplete penetration and the bottom of the irregularity structure.

Ganpatye et al., (2006) developed a detection matrix for the detection on the ultrasonic testing. Originally, the ultrasonic data were being taken over the specimen. Then the data were confirmed with the results obtained using the conventional methods like optical microscopy. Their results show excellent correlation between the comparisons. Using the ultrasonic back scattering technique, they have found the matrix cracks which are not optical images as in photography instead those are grey-scale representation.
However, it is noteworthy to know that AMI techniques are widely used in inspecting the discontinuities on the components of area array materials. Thus, more information concerning how to use AMI technique to monitor the performance of solder joints under area array packaging is depicted in chapter 4 of this thesis

2.2.4 Laser ultrasound

This type of inspection technique helps in examining the solder joints' defects. One of the limitations of this kind of technique is that they do not provide more detailed information about each joint's failure. This system makes use of a pulsed Nd: YAG (neodymium-doped yttrium aluminum garnet) laser to induce ultrasound in the flip chip packages in the thermoelastic region to prevent any damage to the packages (Liu et al., 2001). It then measures the transient out-of-plane displacement response on the package

surfaces using a laser Doppler vibrometer. Liu et al., (2001) stated that the displacement response during the test reacts differently when there are abnormal solder joints lying under the measurement points. Erdahl et al., (2004), carried out a study and the developed laser system has been successfully applied to detect solder joint defects including missing, misaligned, open, and cracked solder bumps in flip chips, land grid array (LGA) packages and multilayer ceramic capacitors (MLCCs).

As previously mentioned, there are various non-destructive inspection technique used to evaluate the integrity of an electronic products but due to some limitations in properties of each NDT, the capability of inspecting and monitoring the performance of solder joints under thermal cycling test is discounted. For example, Optical inspection has the ability to detect surface cracks, but the indication of small failures are difficult to analyze. 2D x-ray techniques is unable to monitor defects in solder joints during thermal cycling tests, whereas 3D X-ray techniques is unfavorable due to its long throughput time. Laser ultrasound might be a good techniques to inspect the performance of solder joints, but the detection is verified indirectly by analyzing the vibration responses which is error prone and relies on skillful and experienced operators (Yang, 2012). Some common non-destructive inspection techniques are reviewed in table 2.2.

Table 2-2: Comparisons of commonly used non-destructive techniques

NDT technique	Advantages	Disadvantages
Optical Inspection	Ability to detect macroscopic surface defects.	Small defects are difficult to detect, no subsurface flaws.
X-ray	Can detect subsurface defects.	Test sample size limitation and long data acquisition and reconstruction.
Microscopy	Ability to detect small surface flaws	Package size limitations
Eddy Current	Ability to detect small cracks on the surface.	Limited penetration. Inability to detect of the flaws lying parallel to the probe coil winding and probe scan direction.
Dye penetrate	Ability to detect surface defects	Inability to detect subsurface defects.
Ultrasonic	Ability to detect surface and subsurface flaws	Samples must be good conductor of sound.
Infrared thermography	Ability to detect subsurface defects and anomalies.	Limited depth penetrations

2.3 Chapter Summary

From the literature cited so far in chapter 2, there were many efforts deployed to investigate reliability problems of the solder joints in modern electronic circuit boards. Due to the difficulty in performing the life-monitoring experiments of those joints, most of the studies on solder joint reliability are computational modelling used for locating and characterizing defects. Likewise, it soon becomes apparent that existing non-destructive evaluation and life monitoring of modern electronic circuit boards are limited in their application as stated in table 2-2 for use in electronics industries. In order to fill this knowledge gap, and meet better level of quality inspection of solder joints reliability, the performance of this work is concerned with investigating how to implement the use of ultrasonic imaging called Acoustic micro imaging. This type of techniques has demonstrated a strong ability to locate and characterize materials conditions and defects. AMI inspection will help to improve the resolution of solder joints' images under thermal cycling test needed to get adequate failure data of solder joints in area array packaging, in order to be able to study the performance and reliability of those joints. In addition, as a very helpful, convenient and versatile NDT, AMI inspection method has the following advantages; sensitivity to both surface and subsurface discontinuities in the test sample materials, can penetrate test samples for solder joints defects measurement, ability to access for pulse-echo technique, high accuracy in determining reflector position and estimating size of the scan sample, instantaneous scan results, detailed scan imaging with automated systems. A more detailed analysis concerning how to undertake the performance study of solder joints under thermal cycling test is depicted in the research methodology section that follows as chapter 3.

3 Research Methodology

To carry out a reliability research study on solder joints, it is important to choose a well-defined methodology. This performance study concerns applied research with a purpose to apply a validation test and AMI inspection technique to find the time-to-failure of the solder joints on area array packaging (AAP). Based on the current knowledge gathered from an extensive literature study and academic consultations, this helps to achieve the impact of environmental exposure on the reliability of solder joints on AAP. Figure 3-1, shows a research flowchart methodology to study the performance of solder joints under thermal cycling test. The framework in this section also provides details of how to use non-destructive inspection tools to monitor the performance of solder joints during the validation test.

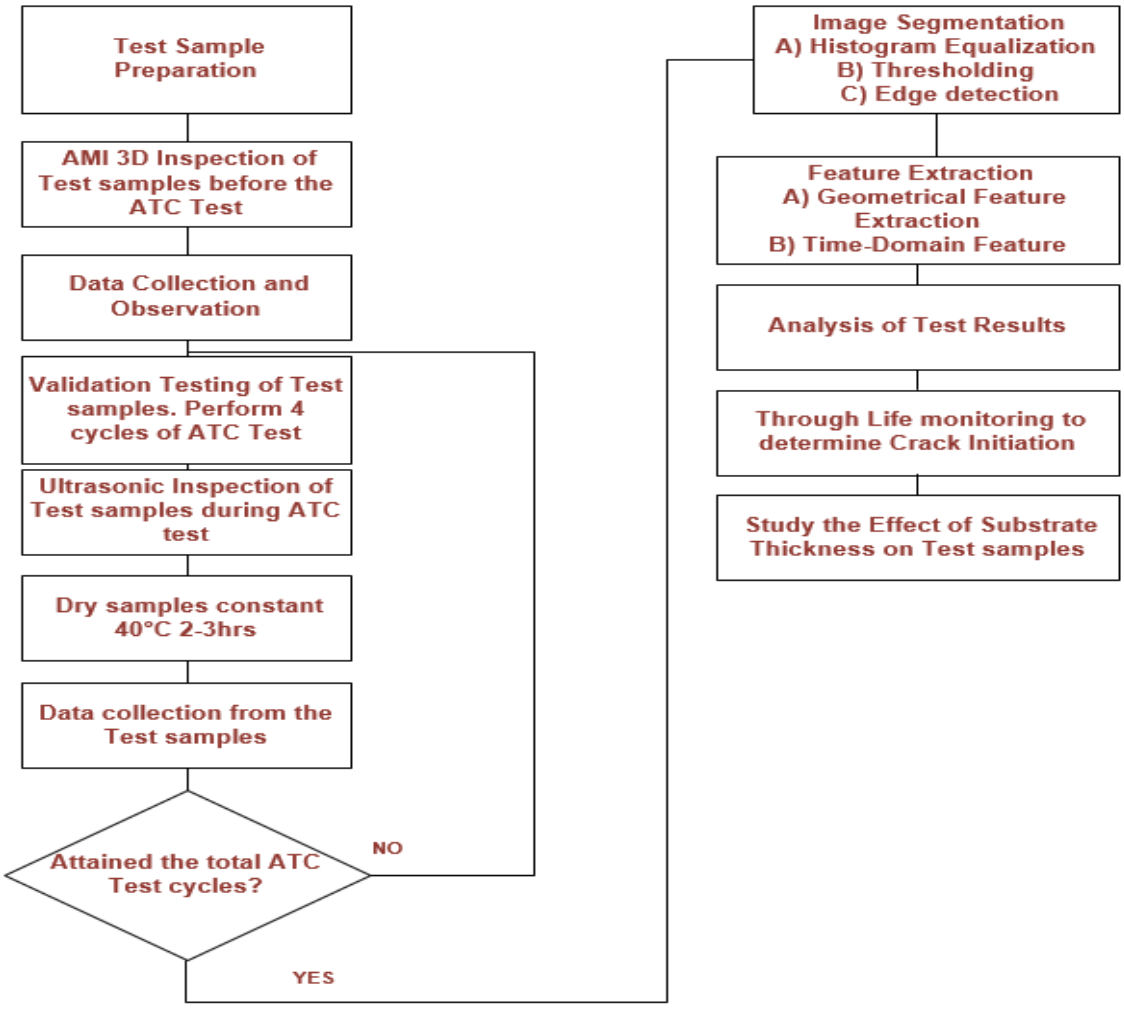


Figure 3-1: A framework for Research Methodology

Likewise, in other to satisfy the research methodology in the proposed framework, the procedure followed for the research methodology tasks approach is detailed and appears in Table 3-1.

3.1 Research Set-up Table

Table 3-1 : Table of Research Tasks

Number	Task Name	Task Descriptions	Reasons for Task
1	Validation Test	Individual testing of the PCB in the chamber	To understand and test the ability of the solder joints under thermal cycling
2	Non-Destructive Testing	Ultrasonically testing the whole fabricated PCB using AMI techniques	To understand and to check the performance of the solder joints at different cycles.
3	Development of imaging processing techniques for through life monitoring of solder joints	To segment and extract the features that represent the integrity of solder joints in the ultrasound image.	Novel feature extraction was applied to all AMI images captured during the thermal cycling tests. To track the initiation and propagation of cracks in the solder joints

3.2 Research Methodology Strategies Steps

This research work deals with the reliability of solder joints in AAP using a thermal cycling test as the validation test. Thus, experiments in this research work were conducted via the methodology illustrated using the flow chart as in Figure 3-1.

3.2.1 Test Boards Design

In order to investigate the potential and feasibility of studying the through life performance of solder joints in AAP under thermal cycling, test boards were designed for this research work as shown in Figure 3-2. Two, thickness of printed circuit board typically used in industry were chosen. So test boards of 0.8mm and 1.6mm were designed with copper pads having a hot air solder levelling (HASL) finish before the flip chips are assembled on them. This industry standard HASL finish was used in this research study because of its excellent wetting during component soldering. The use of two different thickness HASL test boards is critical to assessing the optimum performance of the solder joints on different board thickness under thermal cycling.

The test boards designed for this experiment are multipurpose PCBs, with various AAP, different surface finish configurations and substrate thickness to enable validation experiments, which are suitable for accelerated cycling test (ATC) test in this study. In this study, FR-4 (Flame Retardant Class 4) PCBs were chosen as the testing board material. One set of the boards was populated with 14 flip chips with PCB thickness of 1.6mm HASL, while the other test boards also has 14 flips chips with PCB thickness of 0.8mm HASL. On each PCB 8 other area array ball grid array (BGA) chips not used in this study were attached. Each flip chip package contains 109 solder joints of 125μm height in two main rows positioned at the periphery of the package. The rectangular die were 3948um x 8898um in size having a thickness of 725um. The solder material used was Sn 52.9%, Pb 45.9% and Cu 1.2% with the bump diameter of 140μm. The flip chip packages were assembled without under fill between the substrate and chips in order to generate failures at a shorter period. Images of the test boards sample used for this research work can be found in Figure 3-2. In addition, Table 3-2 interpret the flip chips configurations on both 0.8mm and 1.6mm boards. Parts were placed on either side of the circuit board in two configurations as depicted in Figure 3-2 in order to study the effects of floor plan layout and PCB dynamics on solder joint reliability under thermal cycling test, as illustrated in Figure 3-2. The configurations comprised double-side mirror (back to back) assembly, double-side mirrored placement 50% offset relative to one another and single-side assembly.

Table 3-2 : Showing the configuration data 0.8mm and 1.6mm flip chips

FLIP CHIPS	CONFIGURATION
U19 and U35	Double side assembly
U20 and U36	Double side assembly
U27 and U39	Double side assembly
U28 and U40	Double side assembly
U23 and U26	Single side assembly
U31 and U43	Double side assembly
U46 and U34	Double side assembly

The test boards in Figure 3-2 depicted manufactured organic substrates industrial test boards, designed for both 0.8mm and 1.6mm PCB thickness. Each PCB were populated with fourteen flip-chips namely U19, U35,U20, U36, U27, U39, U28, U40,U23,U26, U31, U43, U34 and U46 and eight other BGA chips not used in this study.

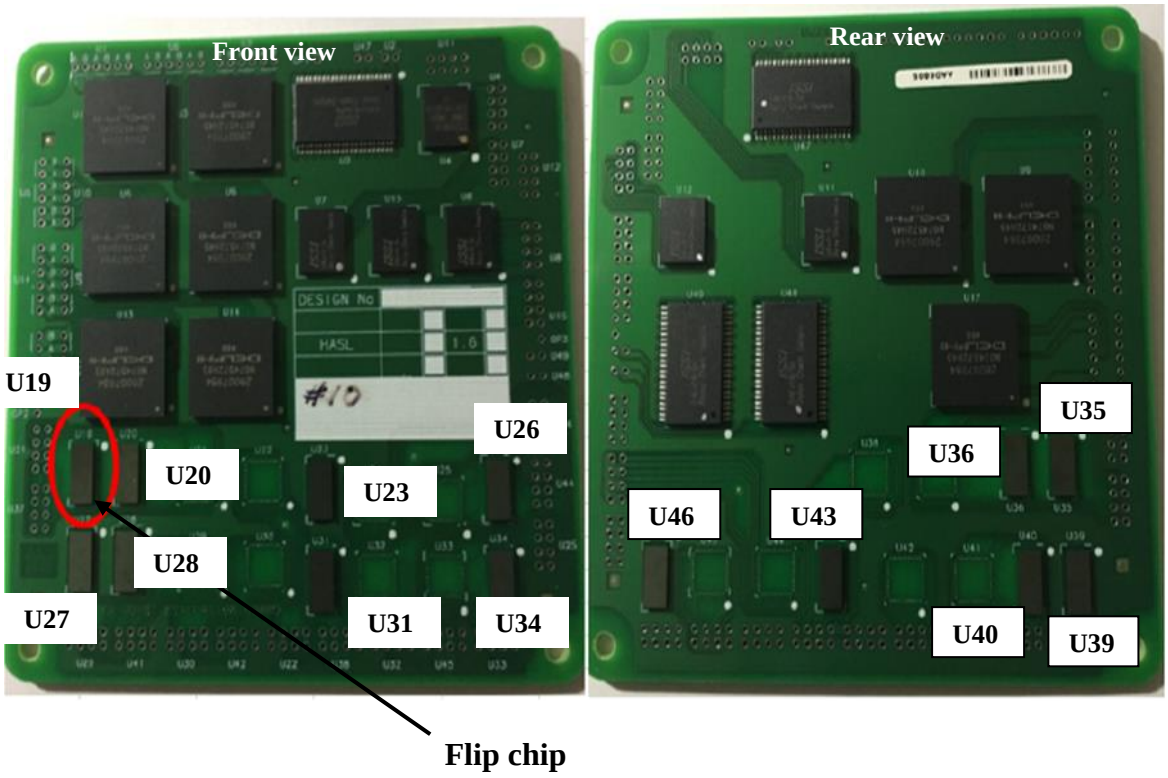


Figure 3-2: The flip chips locations shown in both sides 0.8mm and 1.6mm test samples

3.2.2 Nomenclature of the Test Boards.

The starting point in image acquisition involved using AMI techniques to monitor the performance of those joints at intervals, by removing the samples from the thermal chamber for scanning, throughout each thermal cycling test. During this stage, a consistent scanned solder joints image-numbering scheme was introduced throughout the image acquisition and image analysis to provide unique identification for each solder joint.

The test boards and labelling Scheme are as follows:

(i) Test Boards have a naming scheme of Board number _Finish type initial _Thickness

Test Boards: 0.8mm HASL finish boards with board name DKTESTBD09 (BD09) has been named as H1_0.8_ BD09.

(ii) In addition to this naming scheme, the scanned AMI images have been named:

Scanned Images: Board name_Transducer use_Component no_Test cycle no_ Scan type

For example: for a 0.8mm HASL board where Flip chip number U46 is being C-scanned after 4 thermal test cycles the image name for the 1st scan will be : BD09_230_U46_C4

(iii) For Virtual Rescanning mode (VRM) 3D scan, it will be BD09_230_U46_C4_V1.

Note: Virtual Rescanning mode has been used in this research work in order to access the scanned image data without completely rescanning the flip chips all over again.

In this performance study, there are a large number of flip chips on each test board, each flip chip consist of 109 solder joints. Thus, it is paramount to label each solder joint as shown in Figure 3-3, under the flip chips for better clarification during the data acquisition and feature extraction. The labelling scheme for each solder joint is depicted in Figure 3-3, which helps in providing crucial information about the position of solder joints for performance study.

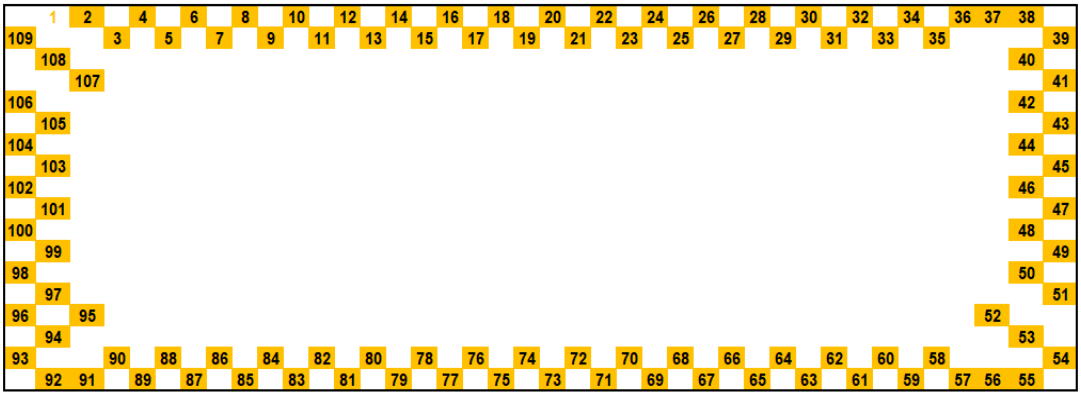


Figure 3-3 Solder joints labelling Scheme

3.2.3 Validation Testing

In this research, validation test were computed for various purposes and in view of various goals doing this performance study in order to evaluate the reliability of solder joints on flip chip. Thus far, in electronics manufacturing, understanding the evaluation process of those packages in the early stage is important, as it aids in developing a

better/more efficient reliability requirement for the product. Most PCB's assembly producers go for excellent standards to surpass client requests and desires. For example in avionics, defence or automotive industries, those packages requested by the clients may operate in very harsh environments during usage, so the reliability of those packages is a huge concern to the manufactures in order to prevent early failure and waste of raw materials in those products. To convey an adequate performance study of solder joints, validation testing is a critical step in understanding reliability of those packages. It is vital to detect poor quality solder joints in those packages because these will cause poor electrical connection between a chip and a substrate, which can additionally affect the mechanical bonding that supports a chip to a substrate. Consequently, it is essential to recognize such damaged solder joints in PCBs at an early stages of the assembling procedure as the location at later stages will be more tedious, costly to repair and time consuming.

In order to fill in this research gap, an experimental validation system has been developed in this performance study to explore the degradation process of the solder joints for diagnosis failure analysis purposes. The goal of this real life experiment is to design a thermal cycling technique for predicting the remaining useful life of solder joints on the flip chips of .8mm and 1.6mm thick circuit board assemblies as shown in Figure 3-2.

Previous work in this research area conducted by Yang, (2012) and Braden, (2012), involved a thermal cycling experiment with an aggressive thermal profile from -40ºC to +132ºC. The purpose of this highly accelerated profile was to generate and obtain information fairly quickly on the life distribution and failure rate of the solder joints.

Moreover, in this performance study, ATC is used to generate less rapid ageing of the flip chips components so that the effects of ageing of the solder joints can be studied over a longer period. In other words, the main purposes of validation tests in this project is to use a softer thermal profile of -40ºC to +85ºC, typically used by some industries, in order to obtain more accurate measurement data spread over a longer test time, since the solder joint were expected to deteriorate more slowly allowing more accurate point by point assessment. These long-term solder joint reliability measurements were planned to provide a process verification and validation regime that can be usefully related to the operating environment in the field. This thermal profile has been implemented on all the

test samples of 0.8mm and 1.6mm HASL boards specified in this research work; it acts as a basis for through-life monitoring tests of solder joints to generate fatigue defects on custom designed test boards, and perform AMI scanning every 4 test cycles over a total period of 220 thermal cycles.

The validation test reported within, was performed in Delphi Automotive Plc, which is one of the leading designers and manufacturers of automotive electronic controller units. The design of the experiments was conducted to induce different failure modes in those solder joints and also to determine the extreme stresses that the solder joints experience in order to improve their design.

The thermal profiling data was measured by using type T thermocouples as shown in Figure 3-4. In this validation test, eight (8) Copper-constantan type T thermocouples were used, illustrated in Figure 3-5. These thermocouples were placed in each corner of one square block as shown in Figure 3-7 and one was placed on the centre of the test sample for monitoring temperature change.

In other to monitor the air temperature chamber one thermocouple was also inserted in the chamber, as shown in figure 3-7 below. This type of type T thermocouples as shown in Figure 3-4 are suited for measurements in the −100 to 350 °C range (Agilent technologies manual). In addition, they are often used as a differential measurement since only copper wire touching the probes were connected to the bench link data logger 3 as shown in Figure 3-6, which were also inserted on the printed circuit board. The thermocouples were arranged in such a manner that one was located in the air of the chamber and the others were attached to the two test samples as demonstrated in Figure 3-5. From the thermal profiling, the logged temperature data was recorded using an Agilent 34972A data acquisition system.

Figure 3-4: Type T thermocouple used for the thermal cycling test

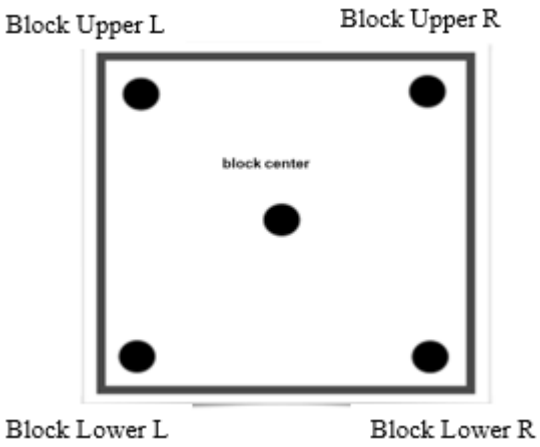


Figure 3-5: Thermocouple Position on the Test Fixture during the validation test

The graphic in Figure 3-6, shows the user interface of the configuration contains all of the instrument settings, scan settings and the graph settings of the Data logger 3 used in the validation test to study the performance of solder joints under the thermal cycling test.

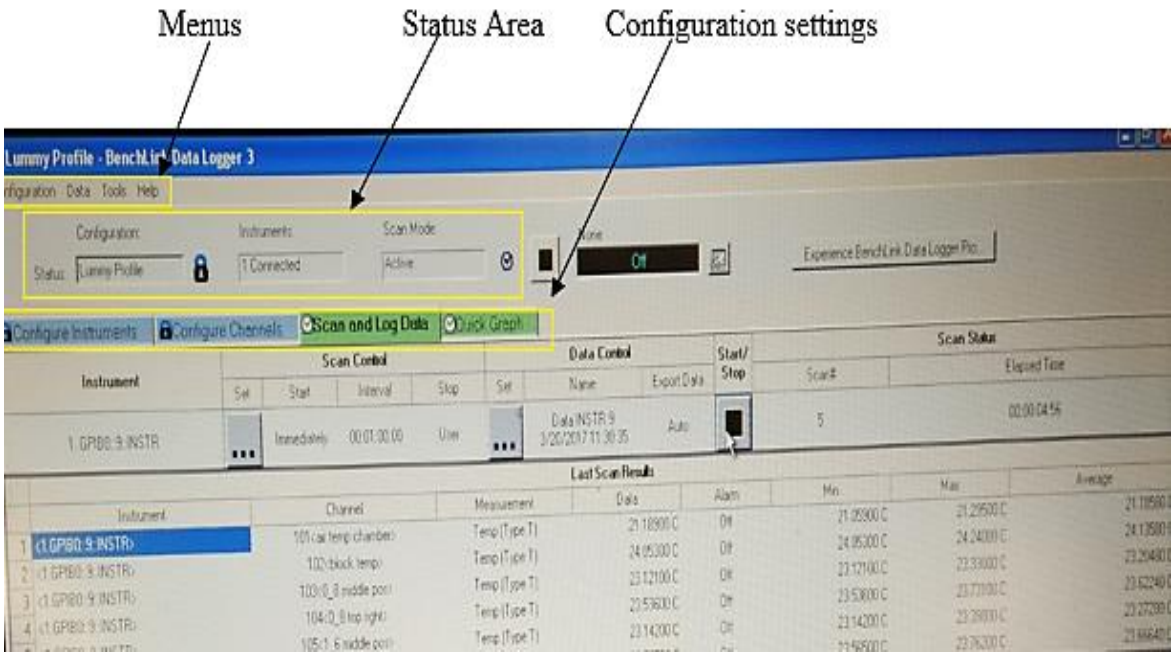


Figure 3-6: Image of Bench link data logger 3 used for the validation test

3.2.4 Validation Experimental Procedures

To estimate the reliability of solder joints in area array packaging in this research, a method was proposed for an accelerated testing set-up, in which printed circuit boards (PCB) with two thicknesses were subjected to life monitoring test to obtain the life failure data. When the experimental plan was created to evaluate the procedure of how to implement tests within a thermal chamber, the followings steps were essential in setting up the experiment:

(i) A chamber program for the experiment had to be developed. One of the requirements for the thermal chamber is that it has the capability of changing and maintaining the same thermal profile within the tolerances specified.

(ii) The chamber set points used in the program were checked to get close to the theoretical profile; the thermal profile should start and finish at ambient.

(iii) There were be no less than four TC in every test. The maximum temperature, minimum temperature and dwell time of every accelerated thermal cycling in the test must be constant.

(iv) During the preliminary test, four thermal cycles were run to understand if the chamber is getting to the set point.

(v) During the period of the test, non-destructive evaluations such as scanning acoustic microscopy have been conducted every four cycles to prudently evaluate the through life performance of the solder joints.

3.2.5 Test Set-up in the Thermal Chamber

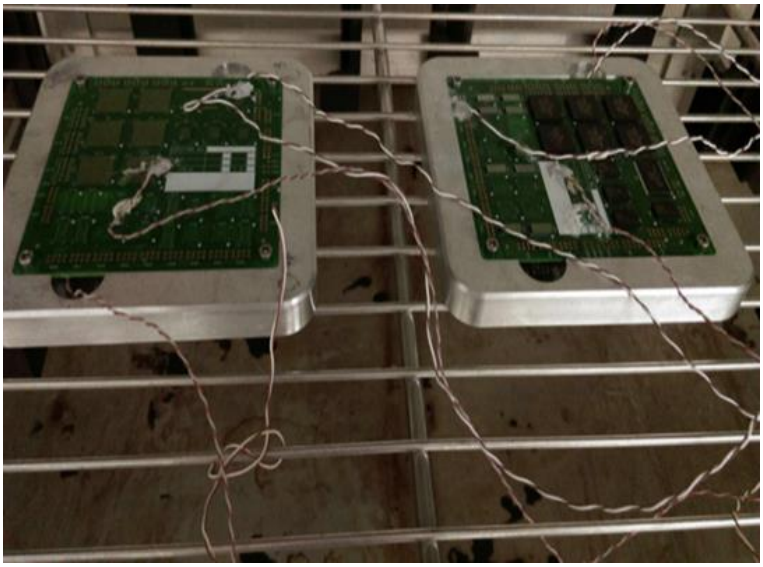
Different environmental conditions have a major impact on the reliability and durability of PCBs. Accelerated temperature cycling testing is the dominant test used to assess the performance of solder joints and to understand the mechanism behind future failure. The main objective rising from ATC is to subject the packages to thermo-mechanically induced stress, this results in creep and thermal fatigue- related failures that are usually the most significant factor behind failures of interconnections in most conditions where

electronics are used. This part of this section aims to improve the current understanding of the reliability of solder joints using ATC. Such understanding will also aid the through life experimental setup for TC that is require for the performance test.

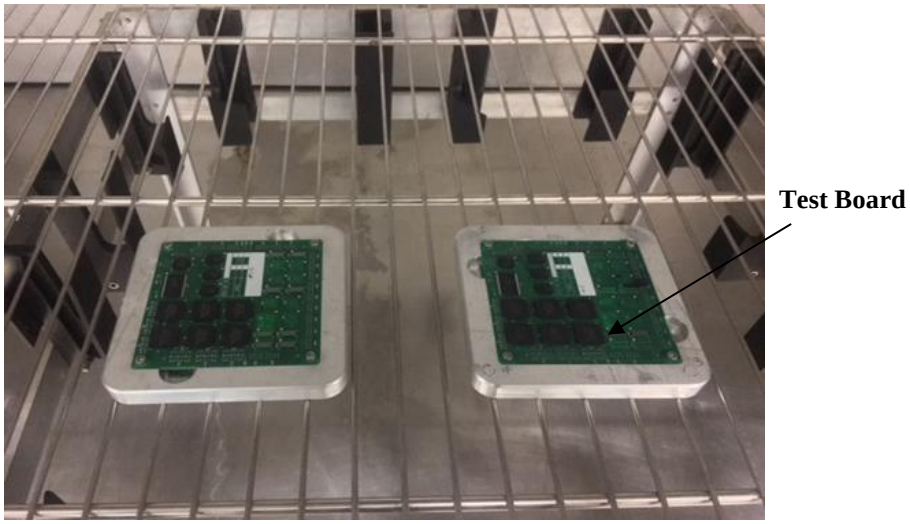
Thermal cycling test was conducted in an Envirotronics thermal cycling chamber in which the environment temperature periodically changes from hot to cold, with a minimum and maximum achievable temperature of -70, to 180 °C, with no humidity, the ramp rate for the chamber was 12°C and controller 7800. As shown in Figure 3-7 (a) and (b), the test boards with different substrate thickness were attached to a test fixture, placed horizontally in the thermal chamber in order to reduce the thermal lag they may induce and to obtain maximum flexure of the board. Bending the board in the \chamber causes displacement between the board and the components on it resulting in board failures or component interconnection.

To estimate the reliability of solder joints in AAP, two set of test samples PCBs with various substrate thicknesses as shown in Figure 3-7(b) were subjected to several accelerated thermal cycling to obtain the life failure data. Figure 3-7(a), demonstrates the ATC preliminary test, with un-populated and populated PCB's coupons, that were subjected to thermal cycling, to test the performance of the thermal chamber based on the thermal profile proposed.

Having selected the required thermal profile of -40°C to 85°C, the next stage in the process is to ensure and verify that those test boards attain the desired temperatures. The results from this preliminary test are consistent with tests performed using the thermal profile. Based on these results, it was decided to conduct solder joints' reliability tests using the same parameters proposed. The validation test was conducted by subjecting the flip chips on the test sample in Table 3-7, to less severe conditions, than those that the samples will be experiencing at the normal operating environment. Thus, some of the important factors to keep in mind doing the test are the temperature extremes, the ramp and dwell time. The cycles had 30-minute dwell times, because the longer the dwell time is, then there is a larger amount of accumulated creep damage, the ramp down was 25 min resulting in 5 °C/min ramp rates, respectively, with 1 cycle for 60mins. The tests were conducted according to JEDEC standard JESD22-A104 recommendations.



(a)



(b)

Figure 3-7: : Image a) Showing the unpopulated test boards in the thermal chamber and b) showing the populated test boards attached to a fixture in the environmental chamber at Delphi automotive industry

3.2.6 Thermocouple System Related Error during the Validation Test.

The accuracy specifications in this validation test includes measurement error, switching error and transducer conversion error. Thus, calculating the total thermocouple reading error is quite straightforward with the Agilent 34972A data acquisition system. This calculation has been done by adding the listed measurement accuracy to the accuracy of

your probe. For example, according to Agilent technologies data manual the input reading for type T thermocouple measurement is 100 °C, and the standard accuracy is the thermocouple probe accuracy + 1.0°C., Likewise the probe specifies accuracy of 1.1°C or 0.4%, whichever is greater. Then the total error is the addition of the standard accuracy and the probe accuracy, which is equal to 2.1°C or -1.4%. In order to carry out the validation test, Table 3-3 shows the temperature profile used in industries according to several applications.

Table 3-3: Accelerated temperature profile for modern electronic products

Usage	Thermal Profile (°C)
Consumer electronics	0 to 65
Wireless and Telecommunications	-40 to 85
Commercial Aircraft	-40 to 95
Military Aircraft	-40 to 125
Automotive-passenger	-40 to 65
Automotive-under the hood	-40 to 160

Likewise, in order to estimate and describe the fatigue performance lifetime of those solder joints in AAP, utilizing the methodology of the ATC experiment is paramount to age the life cycle of the AAP through the manner of placing the test sample in TC parameters conditions as show in the table 3-4.

Table 3-4: Thermal Cycling parameters

Low Temperature (°C)	-40
High Temperature (°C)	+85
Ramp Rate (°C/min)	5
Dwell Time	30mins
Number of cycles	4 cycles
Number of test samples	2

The parameters of the thermal cycling regime used in this evaluation study have been listed in Table 3-3 and Table 3-4, which provides the parameter representation of a thermal cycle profile that has been used for the validation test monitoring test.

The main objective of using this kind of method is to induce failures or degradation of the solder joints on flip chips components of the test samples. In addition, to use the failure data and degradation observations during the validation test to estimate and study the reliability of the joints on different test samples as discussed in chapter 5 of this thesis.

Although AMI inspections were performed at every 4 thermal cycle intervals as depicted in table 3-4, in order to get enough adequate failure data points. Due to the large amount of data and solder joints images obtained during the validation and inspection tests, only solder joints images taken at 0 cycles and 220 cycles are considered. A full dataset upto 5terabyte is archived on electronic media located at the back of this thesis. The primary case studies investigated in this research work were:-

(a) Single side flip chip placement (U23 and U46).

(b) Double flip chip component placement (U19 and U35) and (U27)

(c) PCB thickness of 0.8mm and 1.6mm HASL for scenarios (a) and (b), in order to study the influence of thermal cycling test on PCB thickness.

3.2.7 Non-Destructive Inspection Methods using Acoustic Microscopy Imaging

Acoustic Microscopy Imaging (AMI) used in this performance study as shown in Figure 3-9 uses a piezoelectric ultrasound source to scan across the test sample. This kind of ultrasound technique uses high-frequency ultrasonic energy, typically from 10 MHz to 300 MHz pulsed from a focused lens, through a coupling medium such as distilled or deionized water (Yang, 2012). Hence, by integrating the AMI technology in this performance, non-destructive defect detection of solder joints throughout thermal cycling tests can be achieved. In order to monitor and inspect those solder joints to determine air gap type defects such as cracks, voids, or delamination, the reflected pulse on the user interface of the AMI system as shown in Figure 3-8 was used to generate ultrasound C-scan images. The subsurface reflected echo information about the test samples is obtained by moving the transducer lens vertically in the z direction, causing the point of focus to

vary in concert. Figure 3-9 shows the image of PCB test samples in the AMI system during the non-destructive inspection.

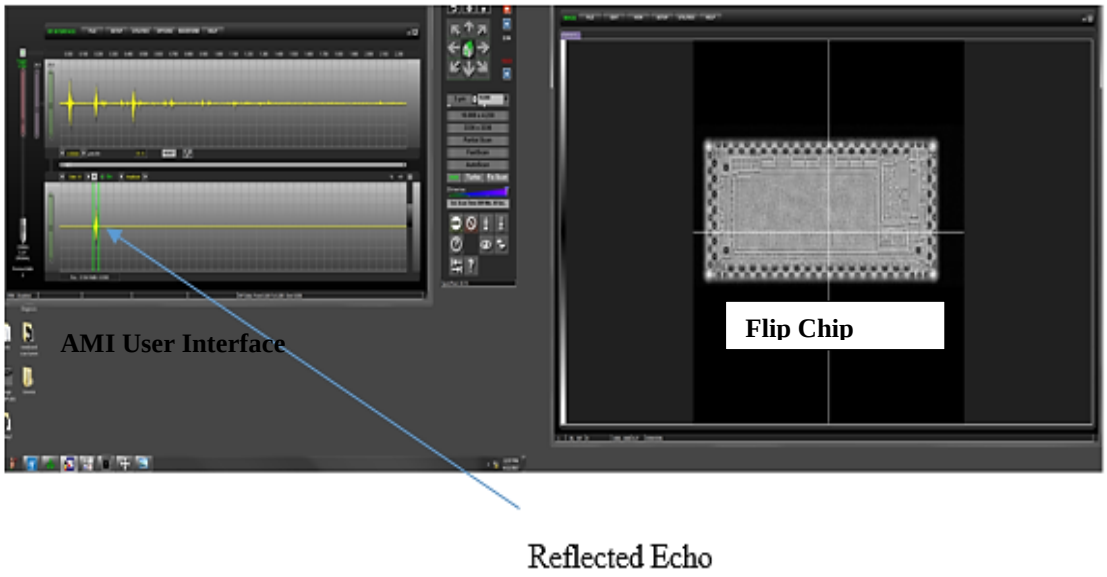


Figure 3-8: Shows the user interface of the AMI system with a scanned image

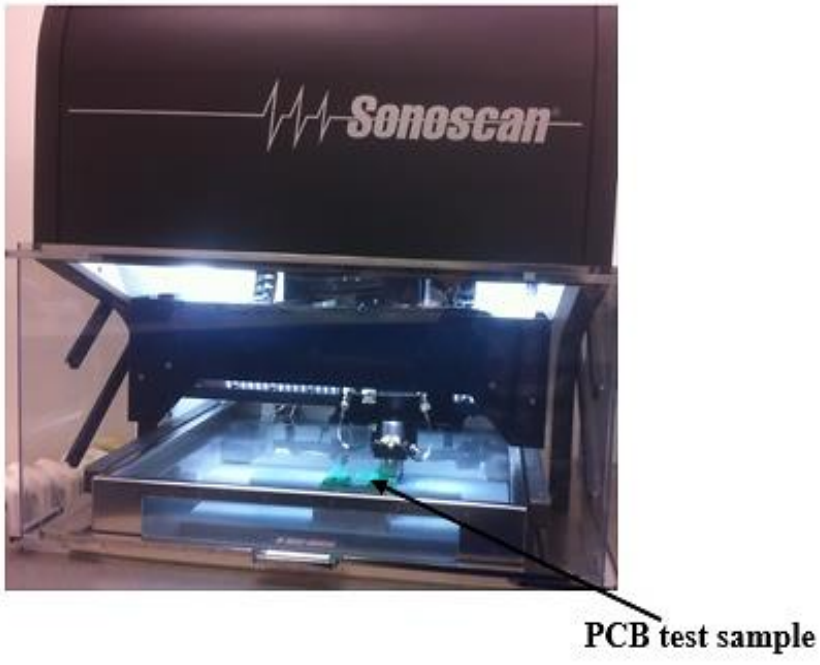


Figure 3-9: Shows the Image of Test sample during the AMI inspection

3.3 Procedure established based on the AMI inspection

In successfully carrying out the required experiment to study the thermal cycling performance on solder joints using ultrasound inspection, it is imperative to run experiments for known ultrasound inspection on solder joints, to affirm the technique. Thereby ensuring that a safe performance study is conducted during the validation process and repeatable /accurate experimental data set from the experimental work must be obtained.

Thus, in order to conduct an AMI inspection to monitor the performance of solder joints under thermal cycling test, the following procedures were established:

- A 230MHz piezoelectric transducer was used and placed in a fixed position. (The same for all measurements). The selected transducer was required because high solder joints image resolution and sensitivity can be achieved by using a high frequency transducer as shown in Figure 3-10(c). The 230MHz transducer was also the highest frequency available on the Sonoscan Gen 6 systems in the laboratory. The highest possible resolution of the C-SAM images of the solder joints is crucial to accurately quantify the performance of the solder joints images during feature extraction.
- The set-up was first experimentally optimized resulting in chosen values as a trigger value of 0.590, channel gain value of 24.5, and front-end gain of 24 were used and held constant throughout the experiments, in order to ensure repeatable/accurate inspection dataset.

Hence, using a piezoelectric transducer with the highest probable frequency is desirable. In order to select the most suitable transducer for this research work, preliminary scans were conducted using three different types of transducer 50MHz, 100MHz. and 230MHz on test samples as shown in Figure 3-10, which enabled images to distinguish various features and get information like the package thickness of the test samples.

The Figure 3-10 below shows images of solder joints with different transducers:

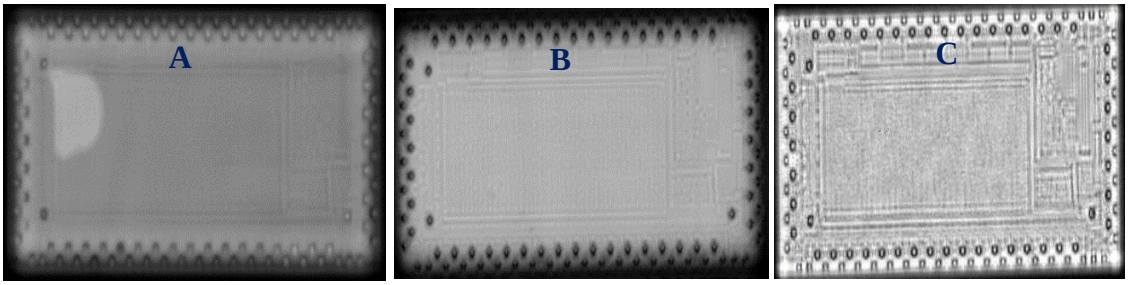


Figure 3-10: : Ultrasound image of solder joints(a) 50MHz transducer, (b) 100MHz and (c) 230MHz transducer

As shown in Figure 3-10(a) and (b), low piezo electronic frequency transducers (50 MHz and 100MHz) were chosen in the first place to evaluate the solder joint quality at the expense of high resolution, in order to guarantee that our AMI would be able to penetrate through the flip chips. However, the image resolution on the ultrasound images acquired was too low to investigate the performance and the quality of those joints. Due to the limitation, of these low frequency transducers to evaluate the test samples, 230MHz was used. It is of note from the inspection that the operational frequency transducers such as 230MHz provide better images with excellent resolution, but have a shorter wavelength than the lower frequency transducers. The acoustic energy in the signal does not penetrate very deeply and makes them limited to very thin samples due to lack of depth penetration. Likewise, the low operational frequency transducers provide lower resolution with longer wavelength as illustrated in Figure 3-10 above. Lower frequency allows more signal transmission through materials providing deeper penetration. Furthermore, the choice of transducer to be used for any non-destructive inspection is determined by the specification of the test board and flip chip design and the flaw spot size and depth of the sample materials.

The highest frequency transducer available in the Liverpool John Moores University Ultrasonic lab was the 230MHz, 0.25" focal length transducer, which provides excellent image resolution as illustrated in table 3-5. Likewise, $F^{\#}$ in table 3-5 is the degree of focusing achieved by the lens of the transducer, and is determined by the lens diameter and its focus length. The $F^{\#}$ is used to exhibit the beam focusing characteristic, for instance, if $F^{\#}$ for two transducers are identical, the transducer will have similar resolution and depth of field if they have same centre frequency. In Table 3-5 that follows, typical resolution and penetration depths for the chosen transducer listed:

Table 3-5: Transducer parameters

Frequency (MHz)	Focal length (inches)	Diameter (inches)	F#	Resolution (mils)	(mm)	Depth of focus (mils)	(mm)
10	1	0.25	4.00	20.375	0.518	670.866	17.04
15	0.75	0.50	1.50	5.094	0.129	62.894	1.598
20	0.75	0.25	3.00	7.641	0.194	188.681	4.793
50	1	0.25	4.00	4.075	0.104	134.173	3.408
100	0.5	0.25	2.00	1.019	0.026	16.772	0.426
230	0.25	0.125	2.00	0.443	0.011	7.290	0.185

Table 3-6: AMI test inspection parameters

Transducer frequency	Focal length	Resolution (Pixel)	Trigger level	Front end gain	Channel gain	Scan size	Quantity to be scan
230MHz	0.25inches	3um	0.590	24.0	24.5	10	28 chips

The inspection were conducted using the parameters in Table 3-6, likewise, the time used to scan the test sample was 15 minutes per flip chip and was recorded. The image size of each flip chip used was 3336 x 3336 pixels, throughout the experiment to maintain the consistency of the experimental results. However, as mentioned in section 3.2.1, that the flip chips die thickness on the sample is 725um and the focal length of 230MHz transducer is 6.35mm (0.250 inch), the selected transducer is able of penetrating the test samples and imaging the chip to bump interface. The results from the AMI inspection using those parameters accurately showed the differences of the effects of variation in thermal cycling as relating to the ultrasound inspection of solder joints. Once the AMI images have been obtained from different cycles, the crack initiation, propagation, voids and defects on those joints can be analyzed and learned.

3.4 Data Collection and Observation

This research involves a series of simultaneous experiments to analyze and measure the reliability of the solder joints in area array packaging. The data acquired during the course

of study helped to support the novelty of this research work. The data collection approach can be summarized as below:

i) Solder joints' life in this research work was defined by the number of accelerated thermal cycles experienced before failure, recorded data during the test was exported from the thermal chamber using Agilent 34972A to excel for full data storage and analysis

ii) To evaluate the solder joints conditions, Test boards sample were taken out of the thermal chamber to perform the ultrasound scans, the recorded data has been exported from the AMI using VRM (Virtual rescanning Mode) for data analysis.

iii) AMI scans were perform every four cycles in this study on each test boards, in order to observe the cracks initiation on those joints, the data was exported to MATLAB for full data analysis, conclusions were derived from the acquired data.

To successfully carry out the required validation test, a preliminary ATC test was performed on two unpopulated and populated PCBs circuit board assemblies with different thickness and the same material properties as shown in Figure 3-2, supported by appropriate data collection method as mention above. Thereby ensuring that a safe validation test is conducted and repeatable/accurate experimental dataset are obtained.

3.5 Image Segmentation and Feature Extraction

In this research work, image-processing techniques were used to extract and segment distinctive solder joints image characteristics and features. In order to get the region of interest in the solder joint images, two image-processing steps were used in this research work. Hough Transform was used to detect the solder joints in the acquired AMI images. Then, image segmentation was performed on the solder joints images considered as the process of dividing an image into different regions with the same homogenous properties. In this case, the region of interest are derived on each solder joint in order to estimate the reliability of the joints. Analysis of this extraction method is presented in chapter 6 of this thesis.

3.6 Through-Life Non-Destructive Monitoring of Solder Joints

This research aims to develop a non-destructive monitoring system using ultrasound technology to assess solder joint through-life performance during thermal excursions. All the degradation data set acquired from the performance study were plotted to identify any distinctive failure pattern that occur during the validation test. During this stage, various failure phrase cycling durations are been estimated from the graphical results to find the crack initiation time of the solder joints using fracture mechanic- based models. These kind of fatigue models are based on the principle of defects existing in any solder joints during the validation test. From this, when a crack initiate, it can propagate through the solder joints area during the application of an applied stress, in this case thermal cycling. Nevertheless, by using these methods, the reliability of the solder joints may be derived according to (Liu, 2001) for characterising crack propagation behaviour through stress that occur as a function of time geometry and environmental conditions as suggested by Liu. Analysis of the test results are presented in chapter 6 of this thesis.

3.7 Chapter Summary

This chapter features the methodology and techniques employed to monitor and estimate the reliability of solder joints under thermal cycling test. It is of note that solder joints are considered one of the vulnerable parts in area array packaging. Therefore the analyses and inspection of solder joints on those packages has become an important process in electronics manufacturing industries in order to adequately achieve the desired used level reliability during the mission life of those products. The above methodology and requirements have magnified the need for providing more accurate performance results on the reliability of those joints. This was achieved by conducting a validation tests on test samples and monitoring and estimating the reliability of those solder joints during the various ATC non-destructively using an AMI technique.

4 Inspection of AAP throughout Thermal Cycling Tests using Scanning Acoustic Microscopy

4.1 Introduction to the Inspection Requirements of AAP

Despite over forty years of rapid technology advancement and exponential increase in electronic demand, the specialty of using SAM in life monitoring of the performance of solder joints under AAPs continues to receive scant attention in most reliability studies. In this chapter, the goal of using this type of technique is its ability to monitor and assess the through-life performance of solder joints during thermal cycling (TC) tests, in order to track any defect conditions, such as voids, delamination and cracks. Also to effect some understanding on how the imaging techniques work, including how the principle of operation involved could influence the test samples.

As the demand for AAP functionality is getting higher, the packages are getting smaller, more complex to design and more prone to faults during manufacturing. Increasing demand and supply of AAP in industry tends to increase the number of advanced reliability research projects, based on the reliability and testing methods of those packages. This type of research could actually prevent any type of internal, external and functional faults or delamination on those packages in the future. In reliability studies of AAP, solder joints' reliability tests are considered of paramount importance, because they are the items most affected by stress, under cyclic loading these causes unclearly seen laminar cracks, and solder bump defects on packages during their mission life.

Likewise, during usage, the cracks that occur in solder joints in the field always reduce local stiffness and cause material discontinuities in the AAP. However, if these solder joints' defects are detected early using a non-destructive technique (NDT), some preventive measures can be implemented to avoid damage and possible failure in their mission life (Braden, 2012). Although, there are two different ways in which cracks in those packages can be detected: destructive testing and non-destructive testing. The destructive type of techniques involves physical damage of the test sample, and quantitative data is obtained, while the non-destructive type of techniques inspects the test sample without physically damaging it and also provides both qualitative and

quantitative data. These types of techniques have played a crucial role in the electronics manufacturing industries.

Moreover, the NDT crack detection analysis has been demonstrated using some of these techniques such as infrared testing, Ultrasonic testing, Laser testing, and Radiographic testing as mentioned earlier in chapter 2. Consequently, ultrasonic inspection a type of Non-Destructive Evaluation (NDE), was developed in the 1940s by Floyd Firestone (Nobile, 2015). This type of inspection, played a pivotal role in the development of more improved and efficient processes, and their control measures employed in production and manufacturing.

The ultrasonic inspection procedures use acoustic waves as a source to create Confocal Scanning Acoustic Microscopy (C-SAM) images of variations in the mechanical properties in AAP. During NDT inspection, the quality of the solder joints' interface, delamination, cracks and other types of unexpected defect may be examine before and during the ATC tests. Based on technological evolution, simultaneous increasing in functionality of electronic products, always leads to scaling down in package size, which is consider as a major challenge in electronic manufacturing industries (Bogatin, 2015). Moreover, it has also been predicted by Ghaffarian, (2016) that the structural size of those packages will be in the order of few nanometers in the future. As reported by Chean, (2014) flip chip packaging alone is facing rapid growth owing to the present methods developed by the private sector. Therefore, based on the increase in the performance of the products, the actual technology gap between the AAP and the type of resolution required during the non-destructive inspection of those packages is getting wider and more complex.

Figure 4-1: Technology gap between IC package size and NDT resolution methods (Aryan et al., 2018)

Therefore, one of the key aspects based on the current gap to NDT inspection techniques of those packages is the evaluation of voids, delamination, defects, cracks and artefacts using AMI. Assessing package reliability regularly requires the capacity to consider package interiors without destroying the packages. Ultrasonic (SAM technique) permits the user to examine various interfaces and determine the mechanical integrity of the assembly. The use of this acoustic microscopy for solder joints investigation of microelectronic packages has gained wide popularity. There are different types of acoustic microscopes that have been utilized in most common applications to study and evaluate interfaces in microelectronics devices, (Maev, 2008, Hafsteinsson and Rizvi, 1984). Two are Scanning Laser Acoustic Microscope (SLAM) and Scanning Acoustic Microscope (SAM).

SAM is the well- established method that has been used to inspect packages since 1970. SAM is a non-destructive technique that has the ability to measure defects such as delamination, cracks and voids in particular materials, and has been found successful for evaluating the reliability of AAP. A main part of the SAM technique is the transducer used during the inspection, which converts electrical signals into acoustic signals and vice versa. Although all of the instruments make use of techniques that use high frequency ultrasonic energy (typically 10MHz and higher) to look into objects to detect defects or internal discontinuities in microelectronic packages. The most commonly used devices for ultrasonic receivers and transmitters are the piezoelectric transducer.

In order to meet the necessary demands for higher resolution, accuracy, and fast and reliable surface defect analysis on those packages, the ultrasonic inspection (SAM) procedure with low power acoustic energy was used in this project for crack detection so that the samples are not damaged by low energy SAM/ acoustic scanning. This technique introduces high frequency ultrasonic waves into the test samples to obtain adequate information about the samples without damaging or altering them in any way.

Thus far, several authors in literature have utilized NDT inspection methods to approach the matter of crack detection techniques, one such example was research work performed by Braden, (2012) in which NDT was used in through-life evaluation of solder joints. In this work, a key solder feature nucleating at the bump to silicon interface was captured.

The experimental results were further validated by comparing them with the Finite Element Analysis (FEA) to gain more understanding on the reliability prediction.

Accordingly, this Ultrasonic inspection step involves the performance study of the stress imposed on the solder joints during the validation experiment, with respect to the failure criteria. Thus, based on the applicability and availability of the latest ultrasonic machine, which is the Gen6™ C-Mode Scanning Acoustic Microscope available at Liverpool John Moores University, the AMI inspection technique was used successfully in this project to inspect and study the solder joint through life monitoring. The technique could actually inspect the micro bump soldering of various parts of the AAP.

4.1 Principles of Ultrasonic transmission

This type of technique operates on the principles of ultrasonic waves. Ultrasonic waves are sound waves whose frequency is above 20 kHz and have been used for non-destructive evaluation in various inspection environments. These kind of waves have the capability to penetrate optically opaque surfaces so outperforms optical inspection for hidden solder joints. However, the depth of penetration decreases with increasing frequency, so the best resolution is only available for thin samples such as flip chips. Thus , AMI also known as SAM is an example of an ultrasonic system which makes use of the properties of the ultrasound waves, which are mainly mechanical waves that transmit energy through oscillations of discrete particles in liquid or solid (Chean Lee et al., 2012). These waves are generated by a piezoelectric transducer in AMI, which are focused and transmitted to the test sample through a couplant in the form of distilled water (Aryan, 2018). There are two types of ultrasound waves, transverse and longitudinal waves, However, due to the inability of transverse waves to propagate through gases and liquid, AMI makes use of longitudinal waves, which propagate in the same direction as the particle motion. (Yang, 2012). These types of waves move from left to right and oscillate about their individual equilibrium positions. Longitudinal waves, also referred to as compressional waves, can be found in liquids, solids and gases.

However, when an ultrasonic waves travel through different test materials, it is reflected back to the transducer as echoes. The transmits wave to further is scattered with respect

to the differences in acoustic impedance, which is the ratio of the acoustic pressure to test sample velocity as it passes through per unit area. Hence, the acoustic impedance of AAP materials is describe in details in Figure 4-2

The image originally presented in Figure 4-2 cannot be made freely available via LJMU E-Theses Collection because of 'copyright'. The image was sourced at Sonoscan (n.d.). The Value of C-SAM® Acoustic Micro Imaging (AMI). Available at: < http://www.sonoscan.com/technology/ami-basics1-2.html> [Accessed: 20 July 2018].

Figure 4-2: Typical Acoustic Impedance Values (Sonolab, user manual)

For inspection, it is noteworthy that the acoustic impedance that governs the amount of transmitted and reflected energy of dissimilar material interfaces can affect the amplitude and polarity of the reflected echo detected by the receiving transducer. Thus, in successfully carrying out the required inspection for imaging purposes, the main interest is the echoes reflected back to the transducer. These echoes have different amplitudes, polarities and time locations, which can give crucial information about the test sample being inspected. Important aspects of the information are density, layer thickness and flaws on the internal structures of the material.

In this research, a technique called Acoustic Micro Imaging (AMI) has been used to monitor the performance of solder joints under ATC testing. Ultrasound C-scan images were obtained from the *Gen6™ C-Mode Scanning Acoustic Microscope*, which has a most comprehensive range of accuracy and resolution, using a 230MHz transducer with 0.250-inch focal length to scan all test samples. The selection of the type of transducer to be used to scan test sample is based on the package thickness and the expected size of the defects.

Meanwhile, the available SAM is able to provide extraordinary resolution to detect the internal and external discontinuities in the test sample materials and the flip chip components on it. It is also important to know that acoustic image resolution varies with the sample material as well as the frequency of the sensor. A tradeoff between a low- and a high-frequency transducer is in the depth of penetration and resolution. The high

resolution and sensitivity during the inspection could be achieved by making use of high frequency and focused transducer, at the expense of reduced penetration.

4.2 AMI Preliminary Study

Ultrasonic transducers can be defined as a device that converts electrical energy to mechanical energy. Conducting an adequate study on the transducer is a critical step, in understanding the AMI inspection based on the penetration, resolution and focal length. Based on this phenomenon, the selection of the type of transducer to use for this particular inspection is an important factor that could affect the quality of solder joint image produced during the inspection.

There are various type of piezo electronic transducers designed for a variety of applications in the real world. The capability of transducers can be defined and analyzed by the focal length and the frequency.

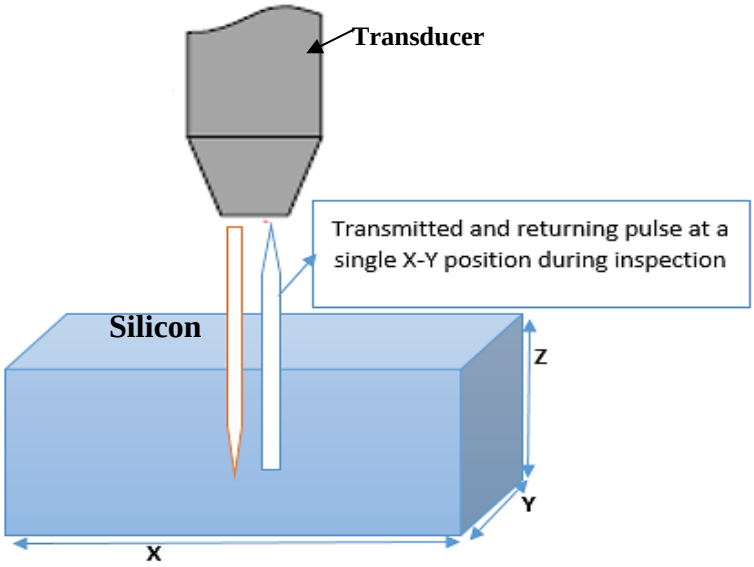
The transducer resolution for an inspection has generated a lot of interest over the last century due to its application. Kino, (1987) suggested that the determination of a transducer to be used for a measurement can be selected based on Kino's approximation equations, which is illustrated below

$$\text{Beam Diameter} = \frac{(\text{FL} * \text{V})}{(D * F)} \qquad \text{Eq. 4-1}$$

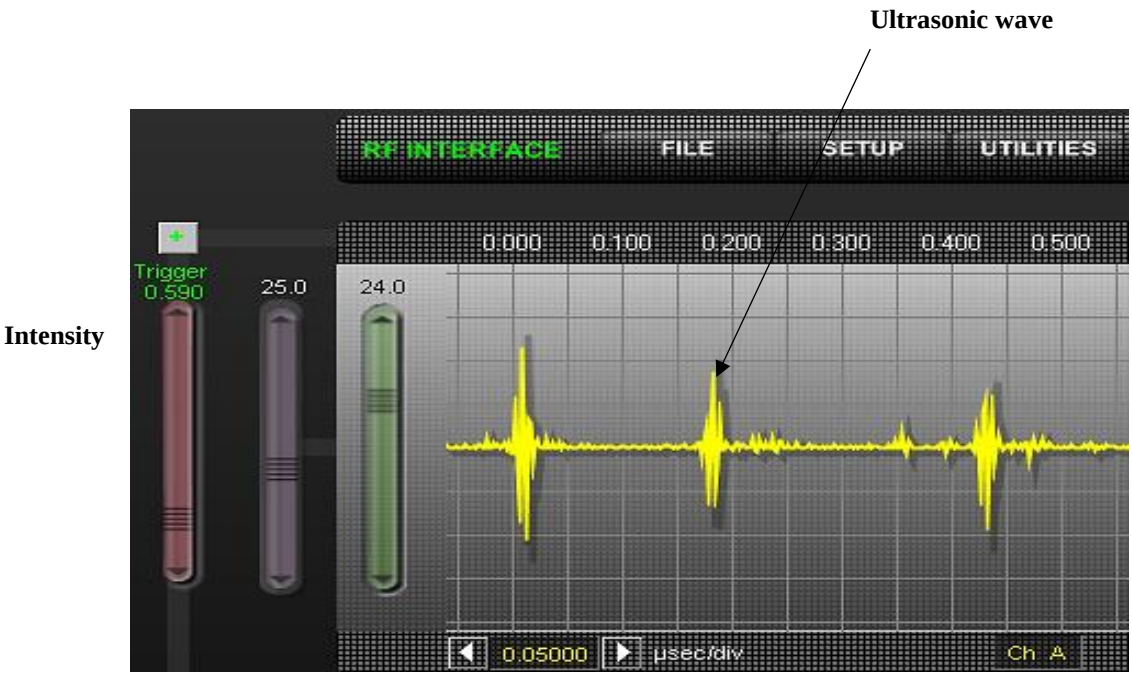
In the equation FL is the focal length of the transducer, *V* is the acoustic velocity of the material to be inspected, F is the centre frequency of the transducer and *D* is the diameter of the piezoelectric crystal. By definition, the focal length of a transducer is the distance from the face of the transducer to the point in the sound field where the signal with the maximum amplitude is located (Olympus NDT, 2006).

Thus, the AMI can provide adequate information on defects of x, y, and z coordinates without re-scanning for every single layer with the transducer. The reflected ultrasound signal known as the A-scan as shown in Figure 4-3(b) contains various reflections in the

signal, which represent different layers in the test sample. The time-axis can depict the time of flight information of the test sample, while the intensity-axis can give crucial information about the amplitude and polarity of the signal components in the A-scan. Likewise, in order to get adequate desired depth the transducer needs to be moved from up and down in the z-direction. This feature, as shown in Figure 4-3(a) below has two advantages: it allows automatic focus adjustments to ensure all depths are in focus and it allows multiple electronic gating to provide images or slices at many different levels during a single raster scan.



(a)



(b)

Figure 4-3: (a) Schematic of the C-SAM AMI Technique (b) showing the relationship between sound intensity and Time

It should be noted that the polarity of the echo can be determined by the equation 4-3 below:

$$\%\, Transmitted = \frac{2Z_2}{Z_2+Z_1}\ , \qquad \text{Eq. 4-2}$$

$$\%\, Reflected = \frac{Z_2 - Z_1}{Z_2 + Z_1} \qquad \text{Eq. 4-3}$$

Where Z_1 and Z_2 are the acoustic impedances of the top and bottom of the sample materials respectively.

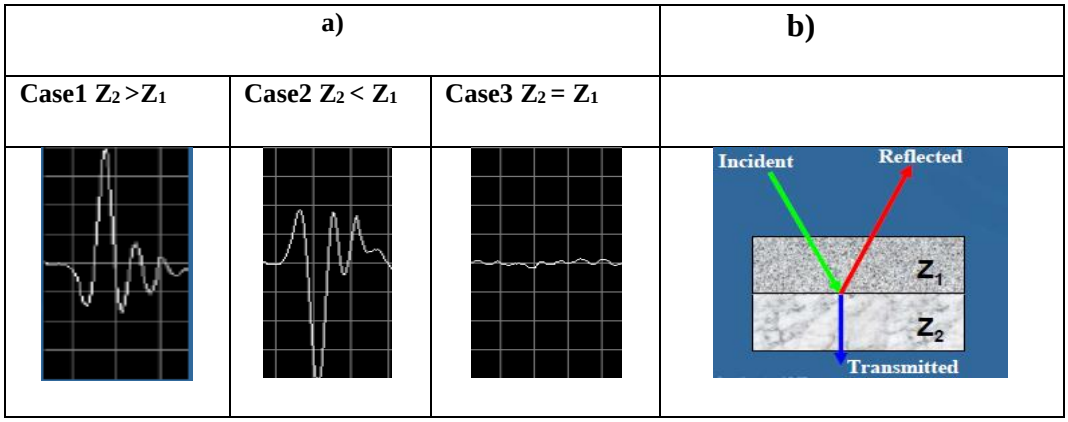


Figure 4-4: a) Ultrasound echo polarity (b) Image showing the incident pulse

Thus as shown in Figure 4-4(a), summation of the reflected and transmitted signal that is generated by the transducer is called the incident point, which is later analysed to produce an ultrasonic image as shown in Figure 4-4(b)

4.2.1 Advantages of Acoustic micro imaging inspection

The main advantages of AMI inspection compared with other methods of inspection are as follows:

- Excellent penetration of ultrasound waves into test sample boards allows the detection of variations such as delamination, voids and defects. Test samples from a few micrometers thick up to several metres long have been examined based on the transducer used (Yang, 2012).
- AMI method is considered to be very accurate and sensitive and can locate many small artefacts on test sample as shown in Figure 4-5 that could actually contribute to the reliability of the test sample.

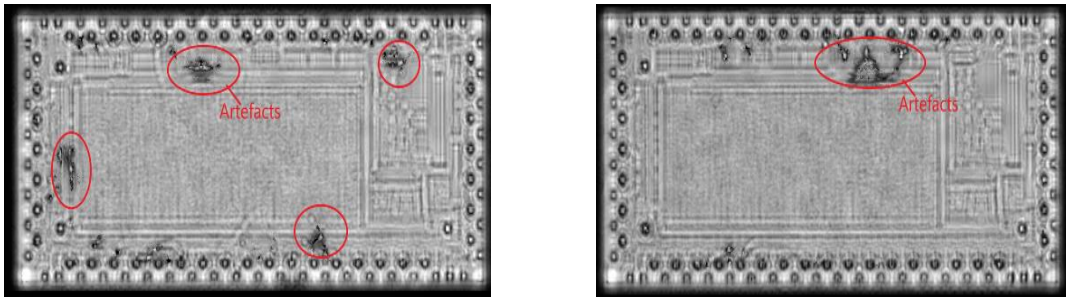


Figure 4-5: Images of some artefacts on U23 and U20 flip chips on 1.6mm board during AMI inspection

- The method uses a pulse-echo technique, which enable access from only one side of a component, as required, by sending and receiving the ultrasound signals beneath the surface of the sample.
- By using the Virtual-rescanning mode available on the AMI system, a 3D acoustic data record of the scanned samples can be digitally stored for evaluation and reconstructed later without rescanning the test sample thereby helping in time management.
- The whole test sample can be scanned from the front to the back surface using the A scan signal generated by the ultrasonic system.
- Acoustic signal data stored using the virtual rescanning mode, can be later processed using both acoustic frequency and time domain images (Zhang et al 2010), which allow delamination, cracks voids or any artefacts to be better characterized and analyzed.

4.2.2 Disadvantages of Acoustic micro imaging inspection

The limitations and the disadvantages of AMI are listed below:

- It is quite hard to interpret and analyse a cluster echoes on the A-scan during the inspection.

- AMI techniques require experienced operators to handle the machine, thus, the training required can be time-consuming to understand the mode of operation, and collect the best data when scanning the samples
- Preparation and development of AMI inspection procedures is not straightforward and good scientific knowledge is needed for the analysis.
- Some BGA components and other test samples are difficult to perform an inspection test on due to complex multilayer structures.
- To analyse any delamination, defects or voids on any test sample an additional processing technique is needed. Likewise, to calibrate the machine, the standard operational manual is required.

4.3 Data presentation of Acoustic micro imaging

Ultrasonic data using SAM could be acquired and analysed in various formats. This section will briefly introduce the commonly used formats like A-scan, B-scan, and C-scan.

4.3.1 A-scan Representation

Amplitude scan (A-scan) is the clearest technique in AMI that gives the fundamental information about the test sample. It is the basic approach to store the received raw signal. In other words, an A-scan in an AMI is defined as a graph of sound intensity against time. The profundity of a reflector in the test sample can be analysed from its echo in the A-scan as demonstrated in Figure 4-6. An A-scan shows the propagation time for the sound to travel to the test samples and back, the polarity and amplitude of the received signal.

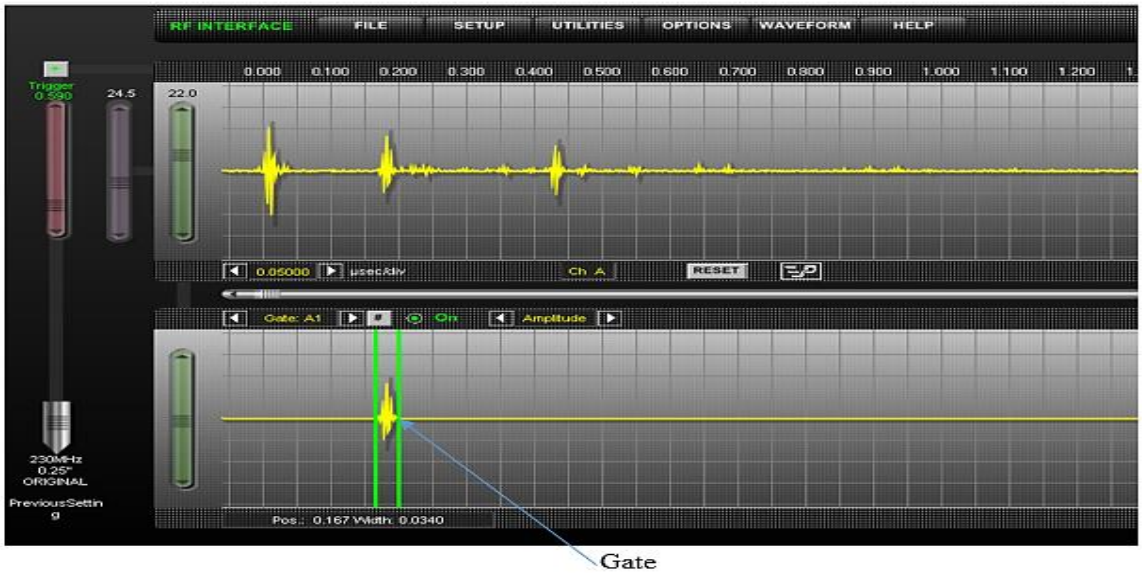


Figure 4-6: Typical A-scan Image from Gen6™ C-Mode Scanning Acoustic Microscope

Any identified layer of interest can be gated from A-scan signal. Thus, an electronic gate was been placed on the sub-surface echo in Figure 4-6, which enables selection of a portion on the A-scan. The width of the gate in this case is actually wide enough to cover the top surface silicon and the innermost structure of the flip chip. In addition, by applying an electronic gate on the echo, only the desired image of a specific interface is revealed in the lower trace window as shown in Figure 4-7 below.

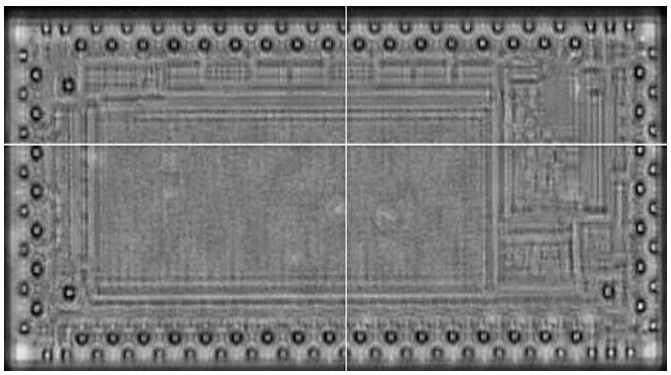


Figure 4-7: Typical C-SAM image acquired using the selected gate in Figure 4-6

Figure 4-7 displays the C-SAM image of solder joints obtained from the selected gate in the A-scan of Figure 4-6. From those C-SAM images acquired from A-scans of a layer

of interest, the failure modes in solder joint interconnection on those flip chips could be studied.

4.3.2 B-scan Image

The B-scan is a 2-D profile image. it displays the directional view of the test sample, as illustrated in Figure 4-8 (Sonoscan, 1999), the operational frequency transducer is connected to two displacement sensors, which measure x and y position coordinates to the test samples. The x-axis can show the time of flight information or the depth information. The y-axis is the signal amplitude and polarity information. This, enables the location of a void at a particular thickness of the test sample. This kind of technique is usually employed to analyse the image appearance of a bulk test sample. The B-scan image is visual and has been used to provide distorted dimensional information of the sample if the object appears much thicker than the original size.

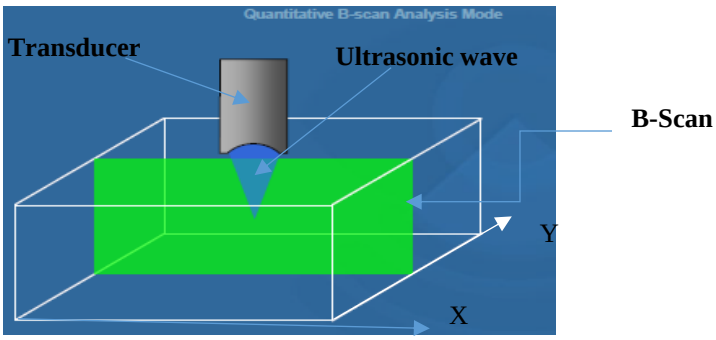


Figure 4-8: B-scan in a cross section along an x-y plane

4.3.3 C-scan Image

This is an image of the test sample in the x-y plane, which is known as C-scan mode, as shown in Figure 4-7, only the echoes restrained by the gate at that particular plane are used to generate a CSAM image as illustrated in Figure 4-6. This type of inspection scan is widely used in package evaluations and for failure analysis, and enables the analysis the differences between one images from another. This tool is non-destructive, which gives the reliability engineers more opportunities to widen their knowledge in reliability testing. The available scanning acoustic microscopes are used to monitor the performance

of solder joints. Sonoscan and other systems are capable of providing extraordinary resolution. However, the image resolution of the system varies with the scanned sample material and most appropriate, the transducer selected for the work.

4.4 Image Analysis of solder joint Using AMI

AMI uses high-frequency ultrasonic energy, typically from 10 MHz to 400 MHz. The pulsed from a focused transducer through a coupling medium such as distilled or deionized water into the unit to be tested were used to determine air gap type defects such as cracks, voids, or delamination. The reflected pulse acquired in the A-scan during the inspection study has been used to generate ultrasound C-scan images in this project. The important feature of this tool its non-destructive probing that gives continuous opportunities to monitor the performances of solder joints during thermal cycling tests, and with a high image resolution.

There are so many solder joints images in this project that look the same on the surface, but within their compositions lie different characteristics that constitute their texture and appearance. The ability to compare two or more images and finding delamination, cracks or voids on those images in a large collection is a tricky matter and it takes a careful procedure for the task to be successful. In order to carry out the analysis, AMI solder joints images were acquired based on reflected echoes on the A-scan, where the intensity level is proportional to the ultrasound signal reflection strength. If there is a defect in the solder joints during the validation test, the intensity will be higher due to larger reflection strength. Therefore, intensity level of each joints and the shift in histogram of the region of interest which is the grey region at the centre of the joints are key features which help to classify defects in this research study.

4.4.1 Images of Solder joints under flip chip at different ATC using AMI

Based on the current knowledge about thermal cycling test on PCB, an experimental framework to acquire the solder joints images under ATC test was designed as shown in Figure 4-9. The first stage is the test board's preparation, whereas in the second stage, non-destructive inspection was performed on the test boards using a SAM system before

the preliminary test. To further investigate the performance of those joints under the PCB's, a validation test was conducted on 0.8mm and 1.6mm HASL test boards on every four cycles, and the solder joints' digital images were acquired using SAM simultaneously as shown in the flow chart in Figure 4-9. By using that SAM technique, the microscopic images were obtained and recorded.

Nevertheless, the ultrasonic machine as illustrated in Figure 2-3(b) in chapter 2 has a novel 3D scanning mode technique called Virtual Rescanning Mode (VRM) that could collect high quality acoustic images data. It does this by scanning the test samples at every coordinate and collecting and storing the array of A-scan signals. The main advantage of using this kind of scanning mode is that the stored A-scan signals can be analysed as a 3D cube of data samples at the later date, virtually reconstructing the AMI images without the presence of the test sample.

In order to collect high quality AMI images consistently throughout the whole experiment, an acoustic scanning strategy was designed as mentioned in chapter 3, which includes the type of transducer used, scanning resolution, scanning area, focusing position, image size, and data organisation that really helps in the analysis of the data. Likewise, the resolution and penetration of the digital images depends on the type of transducer used. However, in different AAP the types of delamination in the package require different AMI configuration settings during their non-destructive inspection. In this research work, a 230MHz transducer was used to collect the acoustic data, because this kind of transducer is preferred in flip chip solder bump, and stack die inspection for optimum resolution.

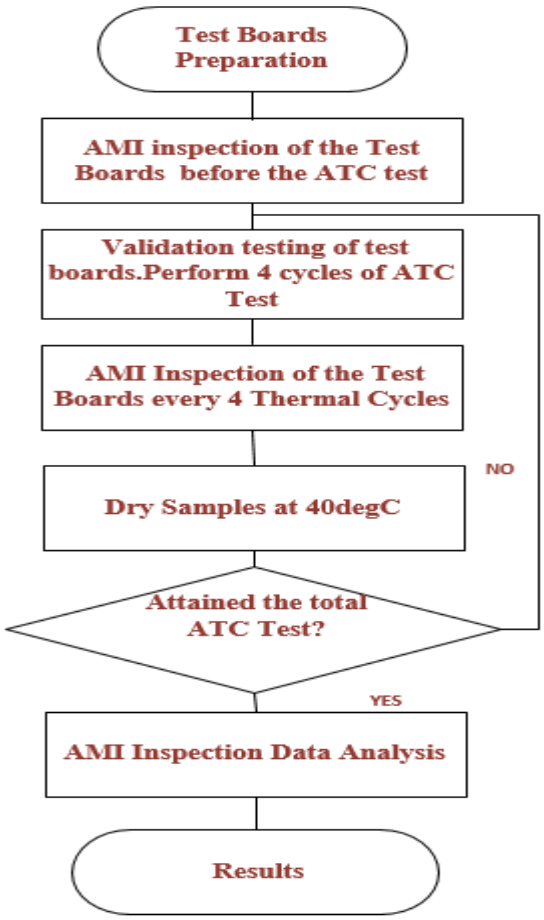


Figure 4-9: Test Framework showing the AMI acquisition strategy

Before the scanning of the test samples began, the selected 230MHz piezo electronic transducer was carefully placed in the system in order to prevent the transducer cable from resting on the splashguard. Hence, in order to get accurate measurements of the samples the transducer was moved up and down in the axial (or z) direction, to adequately permit the focal length of the transducer being used to penetrate the silicon die and focus on our region of interest.

After the test samples were subjected to each ATC test cycle , this technique was confirmed by the AMI scans of the solder joints on the flip chips of the test samples, after 0,28,40,48,128, and 192 thermal cycling test using 230MHz frequency transducer as demonstrated in Figure 4-10 . As depicted in Figure 4-10, each scanned image contains

109 solder joints of 125um height position at the periphery of the package. The solder material used was Sn 52.9%, Pb 45.9%, and Cu 1.2% with a bump diameter of 140um.

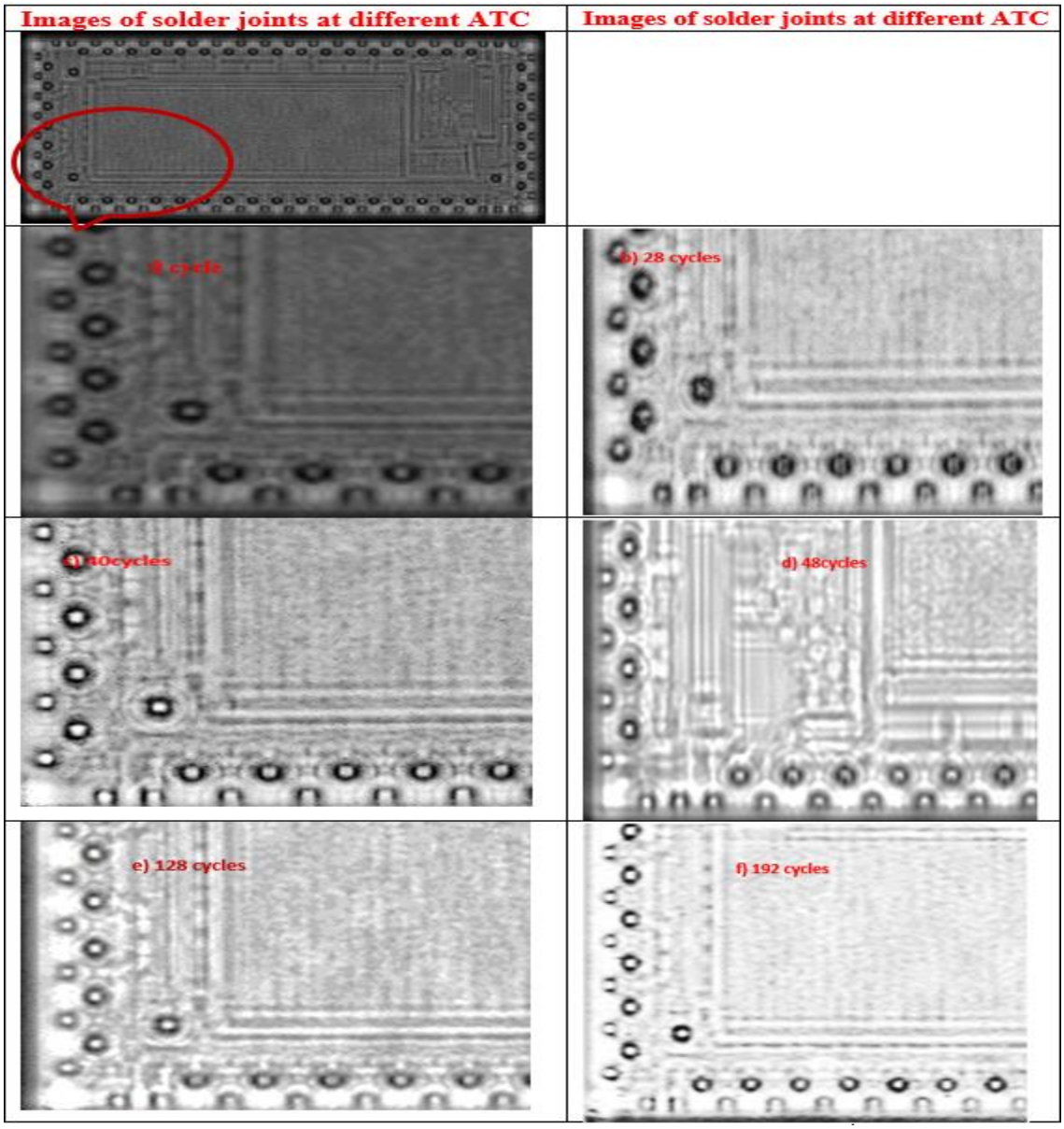


Figure 4-10: Images of solder joints after different thermal cycles

From Figure 4-10 images b, c, d, e and f, evidence from the images above has showed that the grey region in the middle of the solder joints appear brighter than at 0 cycle in Figure 4-10(a), as the ATC increased. Also looking at bright circled solder joints at the corner of the flip chip in figure d, it can be observed that the innermost grey area of the solder joint also appears to be getting brighter as the thermal cycle increases and the same can be said for the middle and the outermost part of the solder joint in Figure 4-10(f)

which has turned into a brighter and greater spot. Which illustrated that the corner joints on those flip chips have the lowest levels of reliability during the validation test. It is also important to know that the cap size is larger when defects occur, thus the area and the form factor of the region of interest is another important feature to aid in clarifying the performance of solder joints under thermal cycling test.

Although, the complexity of the whole procedure during the inspection is time consuming but has successfully helped to enable to the differentiation between good and fractured joints. Thus, helps to verify and keep tracks of the through-life monitoring process as the thermal cycle increases, that later helps to track the failure or cracking propagation in them.

Furthermore, the ultrasonic inspection method will be of great benefit to the electronic industries. By improving the understanding behind the in-depth analysis of the performance of solder joints under various thermo-cycling scenarios using AMI. This will enable engineers to have the necessary requirement for evaluating the reliability of the solder joints in AAP.

4.5 Chapter Summary

This chapter provides the background knowledge and theories that constitute an acoustic micro imaging inspection system. It illustrates the use and purpose of C-mode scanning acoustic microscope (C-SAM) in order to generate the acoustic images needed for the performance study. It is of note to know that the quality of the monitoring of the performance of solder joints during ATC test also relies on the image resolution that could be acquired by the AMI system. In order to get a better resolution, the system makes use of high frequency ultrasound to detect internal discontinuities in materials and components. The three modes of operation of the system was described. It is of note that the low frequency transducer has lower resolution and the high frequency transducer has a finer resolution. The merit and demerit of using the AMI system were been mentioned. A more detailed analysis and discussion about the through-life monitoring of solder joints using AMI under thermal cycling test is presented in Chapter 5.

5 Through Life Monitoring of Solder Joints using ATC

Chapter 5 is devoted to accelerated thermal testing and reliability of solder joints manufactured on flip chips to PCB. The performance evaluation of solder joints under ATC using image-processing techniques were also presented and discussed. Thus far, the reliability of solder joints in area array packaging is the probability that the various components on those packages perform their intended function without any failure and within specified performance boundary for a specified period in their life cycle application environment. Reliability prediction according to Rao, (1996), has the following advantages: (i) To prevent production loss including outage repair and labour costs, (ii)To optimize maintenance cycles and spares holdings, (iii) To maintain the effectiveness of the components on the products through optimized repair actions, (iv) To help in the design of future products, by improved safety margins and reduced failures.

Generally, reliability testing starts with selecting the test method to study the performance of the test samples. In this project for instance, the concept of accelerated temperature cycling (ATC) test was used, because a product is exposed to daily temperature variations resulting from environmental conditions, localized heating and self-heating. The temperature fluctuations can produce fatigue in the product and this will accumulate over time. This kind of validation testing focuses on these phenomena to help evaluate the effectiveness of solder joints in AAP. Likewise, among the many environmental testing methodologies for assessing reliability of a product, ATC has becomes more paramount and is the most commonly used for the characterization test of various devices as well as interconnections.

Reliability of solder joints in this performance study is considered as a function of thermal cycling time that has been estimated by observing the life cycle of solder joints on the flip chips components surviving at a particular time. For instance, the continuous process and the constant loading of solder joints during thermal cycling tests cause them to degrade over time. Nevertheless, the reliability data obtained during the through-life monitoring test of solder joints are then utilized to study the effects of thermal cycling

tests on various test samples for predicting the reliability of the flip chips under normal operating conditions using statistical analyses.

5.1 Accelerated Thermal Cycling Test to Study Solder Joints' Reliability

In order to investigate the study of solder joints' performance in through-life monitoring tests under ATC, the ATC test was conducted in order to achieve the desired thermal profiling on the 0.8mm and 1.6mm test samples with a hot air solder levelling (HASL) finish. HASL finish was used in this performance study because of its excellent wetting during component soldering. Understanding the use of different test boards of the same finish but different substrate thickness is critical to getting the optimum performance of the solder joints under thermal cycling. An example of a thermal profile is depicted in Figure 5-1.

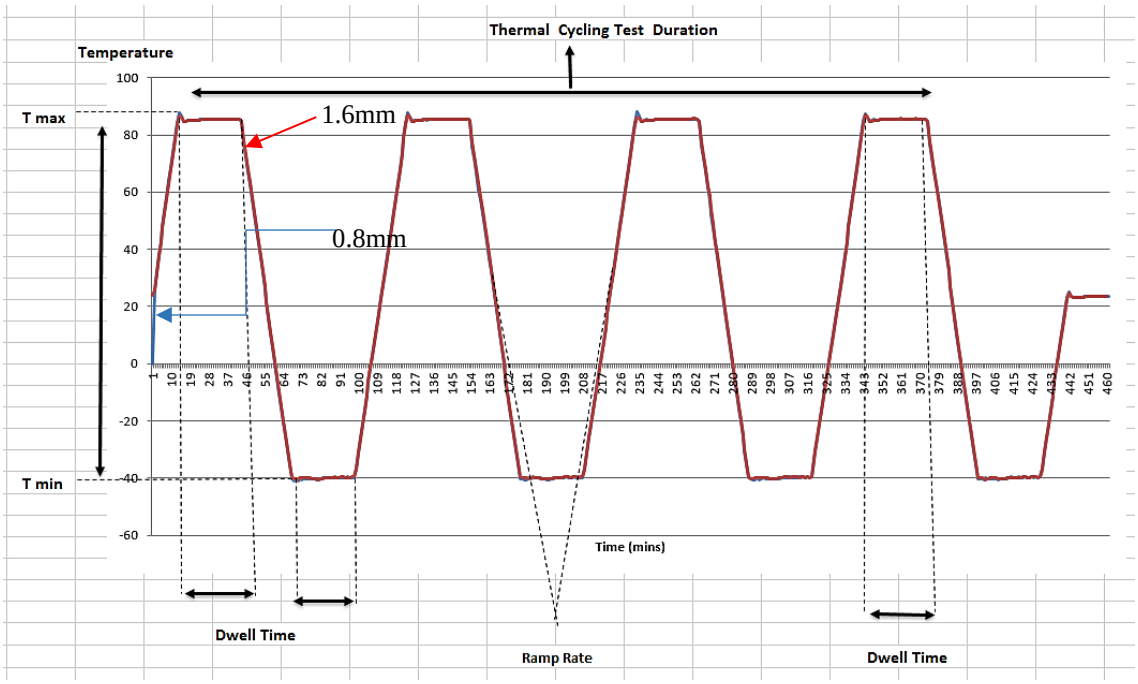


Figure 5-1: Shows the thermal profile used for Validation Tests on 0.8mm and 1.6mm Boards

Subsequently, the thermal cycling test was conducted at Delphi Automotive Plc, to help understand the impact of thermal profiles on the test samples. Previous work conducted by Yang, (2012) and Braden, (2012), carried out a life monitoring test on solder joints

under very harsh conditions, with the thermal profile -40ºC to +132ºC, which resulted in total solder joints failure after about 100 thermal cycles. Their main purpose of using a highly accelerated profile was to generate the cracks, on those solder joints in the shortest possible time. Thus far, the sample intervals were insufficient to track the failure modes with sufficient accuracy. Due to the limitation of failure data of solder joints in the previous work done, a new profile of -40ºC to +85ºC was developed in the performance study of solder joints under thermal cycling test; that led to a slower failure process, which enabled finer tracking of crack propagation in solder joints. It also facilitated the development of an image feature based joint fatigue degradation model for through-life monitoring of crack propagation that may lead to prognosis of electronic devices.

Before commencing the validation test, an initial ATC test was conducted by subjecting the unpopulated and populated 0.8mm and 1.6mm test boards as discussed in chapter 3 to verify that those test samples can achieve the thermal profile designed. The test vehicles were subjected to four thermal cycling tests to understand if the thermal chamber is getting to the set point. The preliminary results as depicted in Figure 5-4 and 5-5 confirmed that both the unpopulated and populated 0.8mm and 1.6mm thick circuit board assemblies can achieve the thermal profile. Subsequently, a non-destructive evaluation technique such as scanning acoustic microscopy was used to examine the flip chips components on the boards before the ATC test. The effectiveness of the SAM inspection techniques on the flip chips is shown in Figure 5-2 to reveal the nature of those solder joints before the validation test.

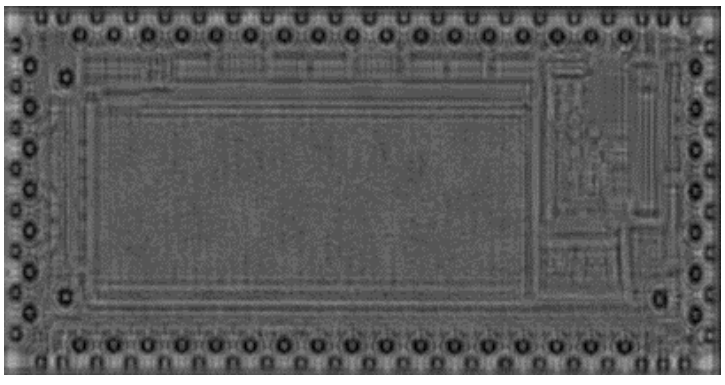


Figure 5-2: Initial Scan of Solder Joints on flip chip before ATC Test

In addition, Figure 5–3 shows the mounted flip chip of U19 in the test sample (a) and 3D X-Ray image (b), which shows the ball grid array design.

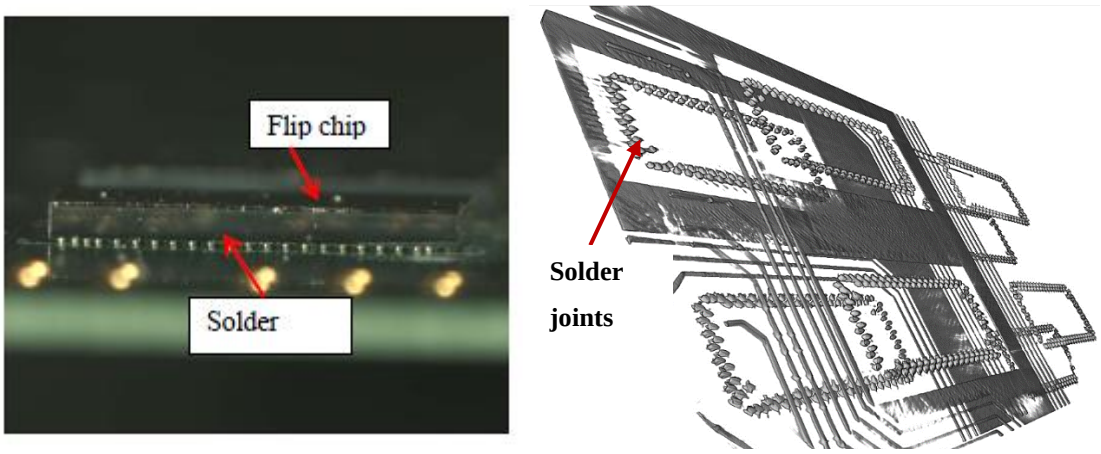


Figure 5-3: (a) Optical image of the solder joints (Yang, 2012), (b) 3D X-ray image of the solder joints

In addition, 3D X-ray was also performed initially on the ball grid array demonstrated in Figure 5-3, to depict the performnace of solder joints before the ATC test. The X-ray inspection as previously mentioned, is one of the NDT inspection techniques for inspecting the internal struture of the flip chips on AAP. This technique was used to ascertain the nature of those solder joints. The reason for this test may be summarised as product performance through life test, comparison of different substrate thickness on test boards, and quality assurance for the remaining useful life of the test boards. Finally, the experimental results are presented.

5.1.1 Thermal Cycling Result Response of Unpopulated 0.8mm and 1.6mm HASL Boards under ATC Test

Mostly electronic devices often operate under varying thermal conditions. An example is that of cyclic thermal excursions in the automobile engine compartment, railway traction system and wind turbine. Thus, during this thermal cycling, failure of solder joints on the electronic devices could occur for various reasons during their desired useful life. For example, the coefficient of thermal expansion mismatch between the substrate and PCB

causes creep of the solder joint. Thus, in order to improve the failure rate the performance of solder joints during thermal cycling test must be determined and estimated.

The validation test presented in this section was based on unpopulated 0.8mm and 1.6mm thick circuit board assemblies. This thermal test was conducted on the unpopulated test samples to demonstrate whether the desired thermal profile are achieved. Analyses from the test results were used to monitor and estimate the reliabilities of different test samples. Nevertheless, the thermal cyclic interface response of the test samples as shown in the Figure 5-4 depends on a number of factors. Some of the factors are the thermocouple locations, the temperature profile, the stress-free condition, the ramp time, dwell time, the composite of the packages. Therefore, the unpopulated 0.8mm and 1.6mm HASL finish test samples as shown in Figure 3-7(a) were subjected to a thermal -40°C to +85°C for every four thermal cycles. The resulting profile of unpopulated test samples as shown in Figure 5-4 has the temperature (Degree C) on the Y-axis, the time (minutes) on the X-axis .The graph also shows that 30mins-dwell time, and the new thermal profile of -40ºC to +85ºC is sufficient for the PCB to reach the temperature of the chamber.

The thermal profiling data collected from the validation test of unpopulated 0.8mm and 1.6mm board thickness was collected by using a type T thermocouple as mentioned in chapter 2. Hence, the accuracy of the interface response in unpopulated 0.8mm and 1.6mm HASL PCB has a profound effect on the reliability estimates and in decision making on the performance of solder joints under ATC.

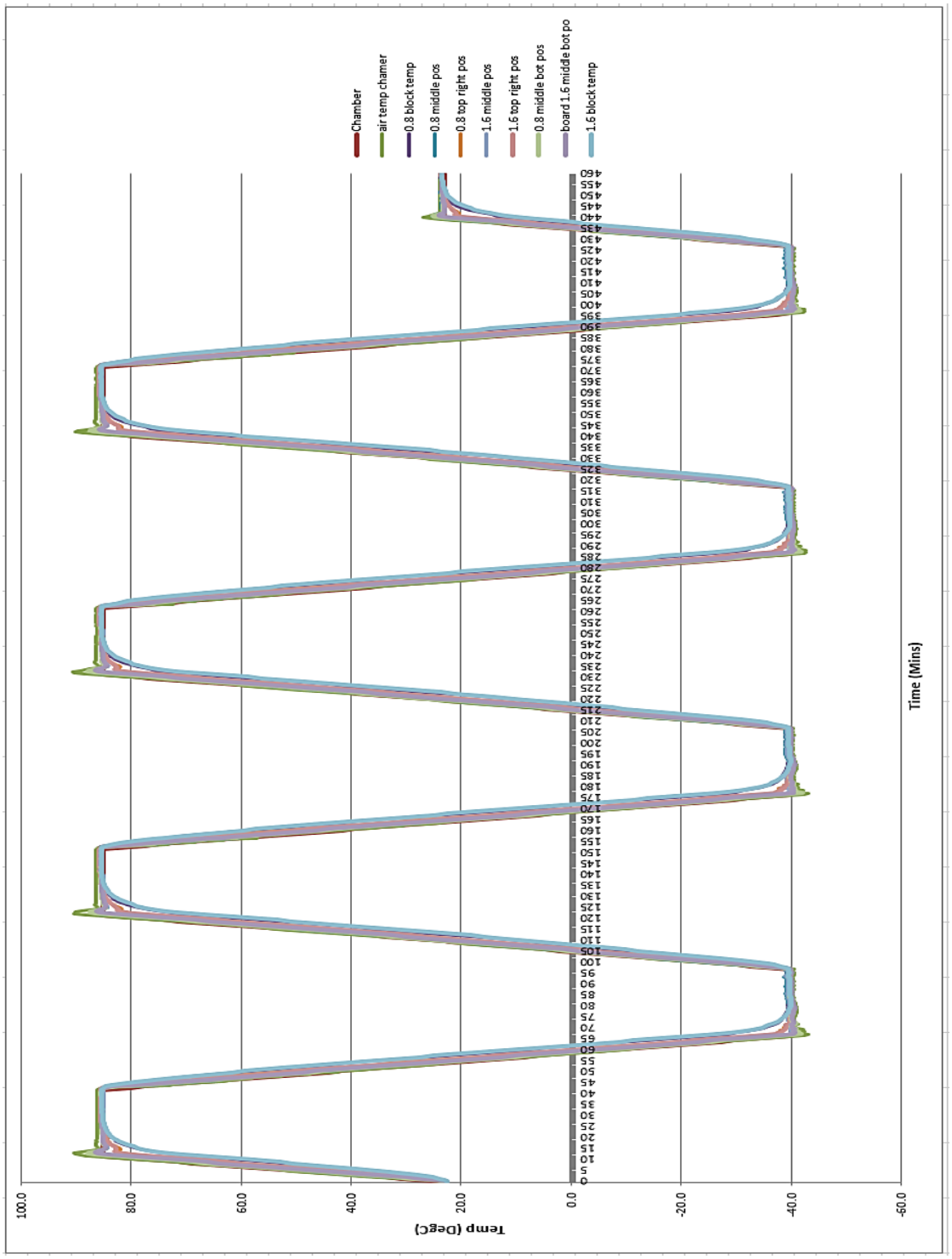


Figure 5-4: Thermal profile for unpopulated 0.8mm and 1.6mm test board

5.1.2 Thermal Cycling Result Response of Populated 0.8mm and 1.6mm HASL Boards under ATC Test

Understanding the thermal profiling process in the initial accelerated life test of unpopulated 0.8mm and 1.6mm test samples has really helped to conduct this validation test on populated PCB. As it aids in developing a more efficient validation test procedure. In this section, a subsequent attempt was conducted on the populated test samples. The thermal profiling logged temperature data results for populated 0.8mm and 1.6mm HASL finish thick circuit board assemblies which are presented in Figure 5-5. The analysis of the test results presented in this section was based on the populated test sample of 0.8mm and 1.6mm thick circuit board assemblies that are used to monitor and estimate the reliabilities of on the solder joints on the flip chips. As previously mentioned, in section 5.1.1, that TC test is mainly used to evaluate the life performance of solder joints subjected to thermal profile.

The thermal profile data used to compare both populated 0.8mm and 1.6mm HASL finish test boards was acquired from the thermal chamber by using a type T thermocouple as mentioned in chapter 2. The test parameters as illustrated in table 3-4 in chapter 3 remain constant throughout the whole validation test, with thermal profile -40ºC to +85ºC, the dwell time for both maximum and minimum temperatures was 30 minutes. This test was carried out on the populated test samples to mainly monitor and demonstrate whether the desired thermal profile can be achieved. The thermal profile data used for populated test samples is depicted in Figure 5-5. It is precisely clear that the graphical results accelerated thermal profile is suitable to evaluate the components on the test samples.

From the presented results in Figures 5-4 and 5-5, it has been found that the desired thermal profile could be achieved using the same thermal chamber. The analysis steps described above, depicted that the new thermal profile -40ºC to +85ºC selected for this study will lead to a slower failure process during the performance study, which enables finer tracking of defects in solder joints on the circuit board assembly.

The resulting graph in Figure 5-5 ramps perfectly with the thermal chamber. Based on these validation test results, the ATC test was conducted on the test samples using the same thermal profile throughout the test in order to verify and analyse the reliability of solder joints in AAP. Thus, the AMI inspection was also considered in this performance

study to be carried out every four (4) cycles interval, in order to monitor any initial delamination on those solder joints during the validation test

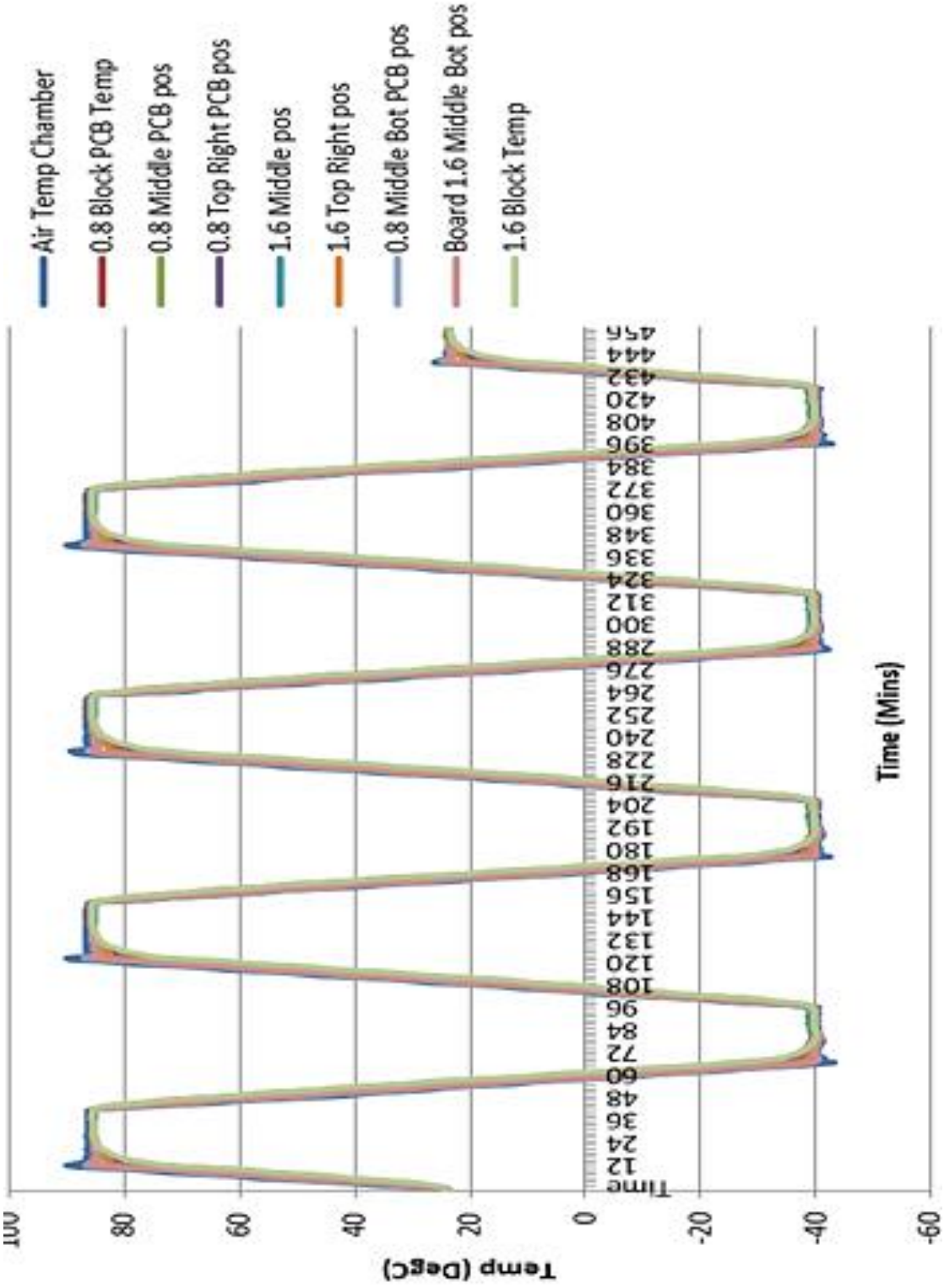


Figure 5-5: Thermal profile for populated 0.8mm and 1.6mm test board

5.2 The Effect of 0.8mm and 1.6mm HASL Thick Circuit Board Assembly Thickness on Solder Joint Life

Different electronic markets and applications nowadays often require manufacturers to use different designs for the final stage of their products in order to exceed customer demands and expectation, one of which could be the thickness of the PCB. The methodology of using ultrasonic inspection techniques employed in this research has enabled the effect of substrate thickness on the reliability of 0.8mm and 1.6mm HASL PCB floor plan layout to be studied and analysed.

The substrate thickness effect analysis presented in this section was based on the fourteen flip chips on the 0.8mm and 1.6mm HASL test samples as shown in Figure 3-2 in chapter 3. The thermal profile used was -40ºC to +85ºC. The solder joints reliability data obtained from this ATC test are time-to-failure measurement for each test sample at different tests. However, results from this study were used to extrapolate the flip chips components characteristic of each test sample needed to study the reliability of solder joints on them. The effect of thermal cycling on the test samples was achieved by subjecting the components to 220 thermal cycles. The analyses of the test results between each flip chip on 0.8mm HASL test samples is plotted in Figure 5-6 which was used to estimate the reliabilities and failure rate of the AAP in order to achieved the desired objective.

Although the results obtained from the test suggested that the solder joints' performance on the flip chip on 0.8mm HASL board is limited to different thermal cycling on the Y-axis, additionally, the analysis in Figure 5-7 shows the variation of the cycle to failure as a function of solder joints on the flip chip component. This indicates that the flip chips on the 1.6mm HASL board have a better reliability compare to 0.8mm substrate thickness board during the through-life monitoring test because the duration of the fatigue failure on the flip chips is relatively long.

Thus, Figures 5-6 and 5-7 depict the thermal cycling failure rate results of 0.8mm and 1.6mm HASL thick circuit board assemblies, obtained through the validation test on the fourteen flip chips components. The bar analysis in Figure 5-6 and 5-7 denotes that the flip chip is more fragile when there is an increase in thermal cycling.

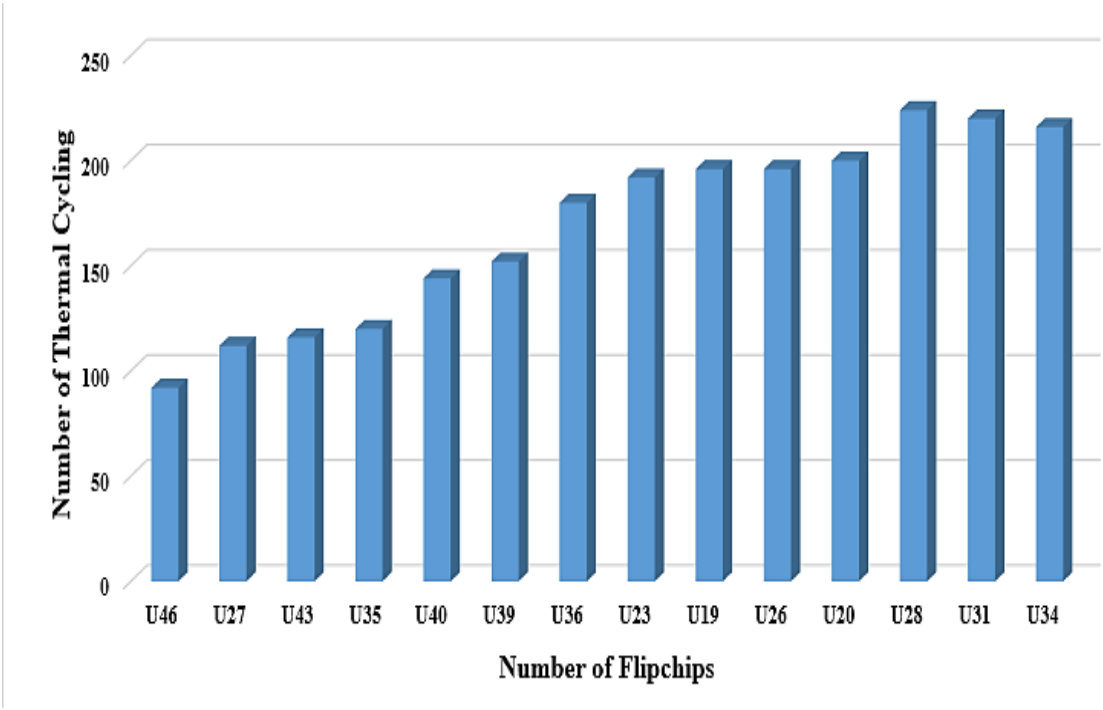


Figure 5-6: Failure rate of 14 flip chips on 0.8mm board thickness under thermal cycling

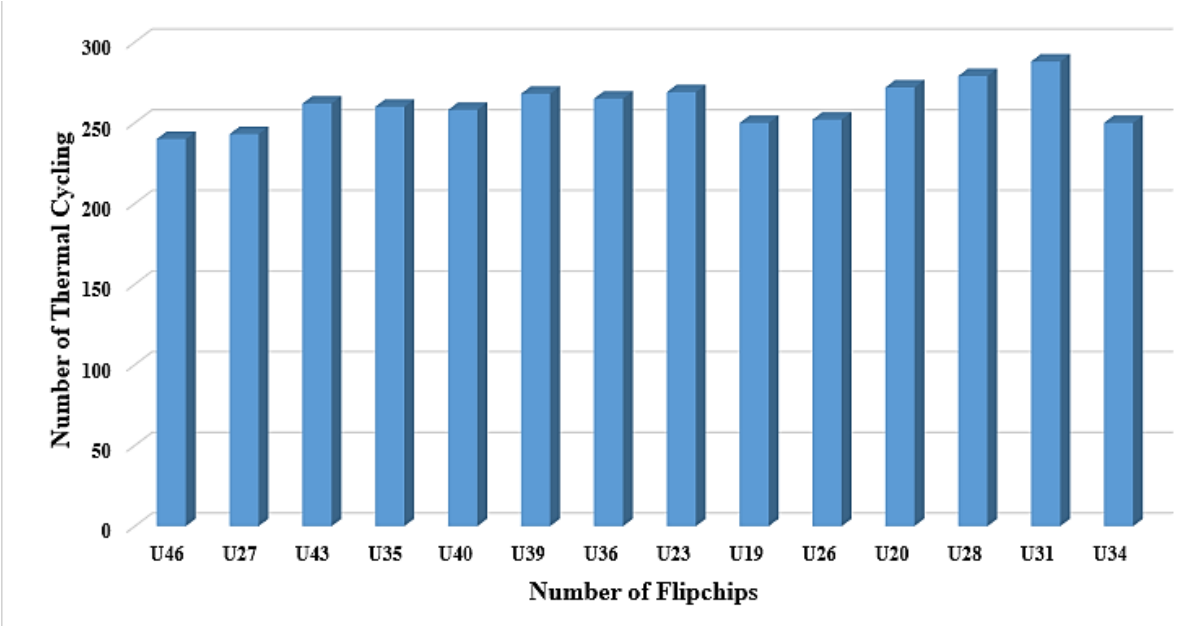


Figure 5-7: Failure rate of 14 flip chips on 1.6mm board thickness under thermal cycling

5.1.3 Findings based on the effect of PCB thickness on solder joint life

The thickness of the PCB board and the materials used changed the overall performance of the board under environmental exposure. Thus, it is of note that many PCB parameters can affect reliability of solder joints on the flip chip components. Apart from the PCB thickness as mentioned earlier, other parameters that could affect them are the floor plan layout and physical constraints placed on the PCB. Hence, the physical constraints considered in this performance study of solder joints under thermal cycling tests were due to five mounting screws placed at the corner of each test fixture during the validation test.

In this research study, solder joints with the same height of 125 micrometres and solder bump diameter of 140 micrometres were investigated to study the effect of PCB thickness on solder joint life. These studies have been carried out on two different HASL boards of thicknesses of 0.8 mm and 1.6 mm PCB. The monitoring data used to differentiate them was generated using a -40 to +85 °C, with 5 minute ramp and 30 minute dwell times as shown in Figure 5-5, because the longer the dwell time during the ATC test, the longer the time to failure. The shorter the ramp rate, the longer the time to failure. The shorter, the thermal profile, the longer the time to failure. Hence, combining good dwell times, suitable ramp rate and low thermal profile range can optimize the performance testing of solder joints' interconnects' durability.

From the analysis results, it can be observed from Figure 5-6 that the solder joint's life on the flip chips component decreases as the PCB thickness decreases. In addition, the package shows a better performance on a thicker board under thermal cycling tests, which is because the thicker boards are more compliant, that helps in reducing the amount of viscoplastic work in the solder joints. Hence, when comparing the reliability of 0.8mm HASL thinner PCB and 1.6mm HASL thicker PCB, there is a two-fold difference in fatigue lives of solder joints under some flip chips of U46, U27, U43 and U35, an example of this is depicted in Figures 5-6 and 5-7.

Furthermore, the reliability of flip chips components are often expressed in numbers of stress cycles by using the Engel Maier fatigue model (Xiaoyan et al.**,** 2017) which is an improved version of Coffin-Manson model as shown in Equation 2-1, and takes the thermal cycle frequency, temperature effect and elastic-plastic strain into account.as shown in the Equation 5-1 below:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon f}\right)^{1/c} \qquad \text{Eq. 5-1}$$

Where N_f is the number of cycles (fatigue life), εf is the fatigue ductility coefficient, c is a constant that relates the average temperature of the solder joints and the time for stress per cycle and Δγ is the total shear strain range. However, a 3D failure simulation results for the predicted fatigue life of 0.8mm HASL board for each solder joint on flip chip components using the same thermal profile of -40-+85 °C , is depicted in Figure 5-8. The Finite element model and analysis using global approach was developed by industrial partner.

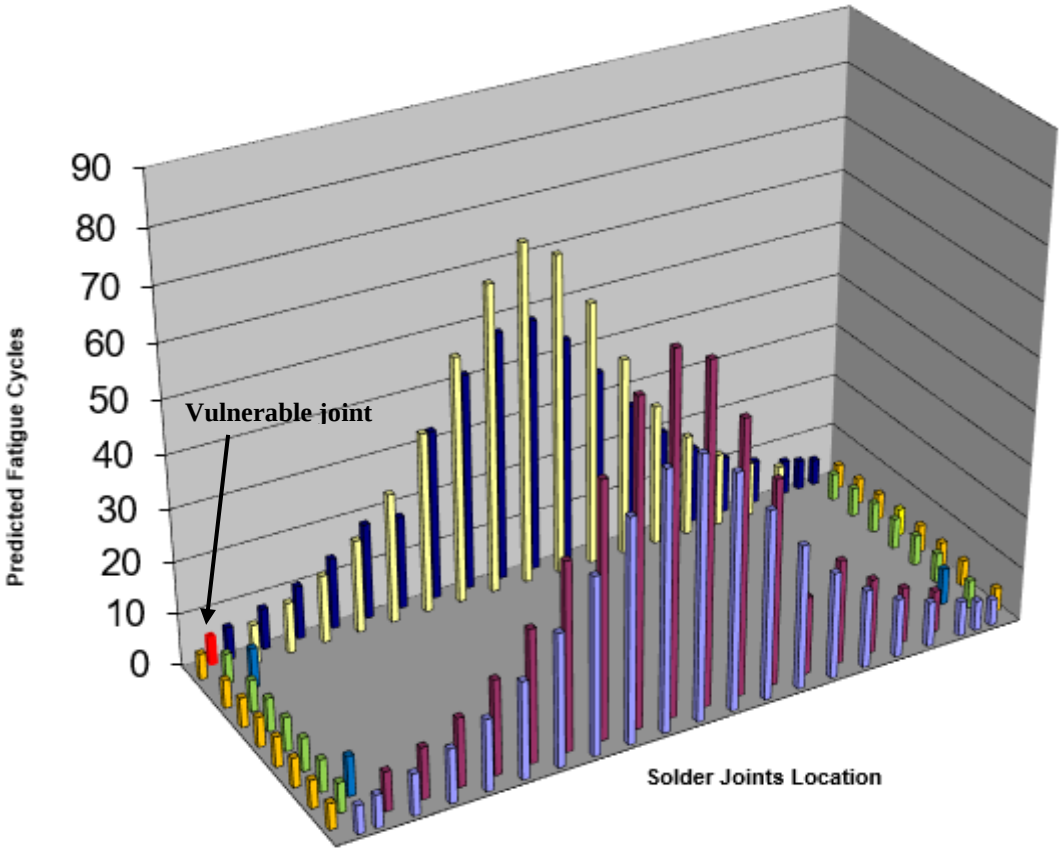


Figure 5-8: 3D predicted plot showing cycles to fail of solder joints on 0.8mm CBA

Nevertheless, the analysis simulation results depicted in Figure 5-8 help to make some novel findings on differences between AMI life measurement under thermal cycle test and the predicted fatigue cycle on 0.8mm HASL board. In the simulated results in Figure 5-8, joints number one is highlighted in red and located in the upper left of the graph. The predicted simulation results depicted consistency with the theory that solder joints that have lower level of reliability are always located at the corner of the package, and have least number of thermal cycles. However, more corner joints failed during the AMI monitoring test of solder joints as illustrated in Figure 5-9. The inner joints and outer solder joints are plotted in two different colours for better illustration. A 3D failure distribution for all 109 solder joints for U46 flip chip of 0.8mm board, which was a double assembly flip chip was constructed and is depicted in Figure 5-9. The AMI failure cycles result shows that all the corner joints have significantly lower levels of reliability during the validation test as different thermal cycles.

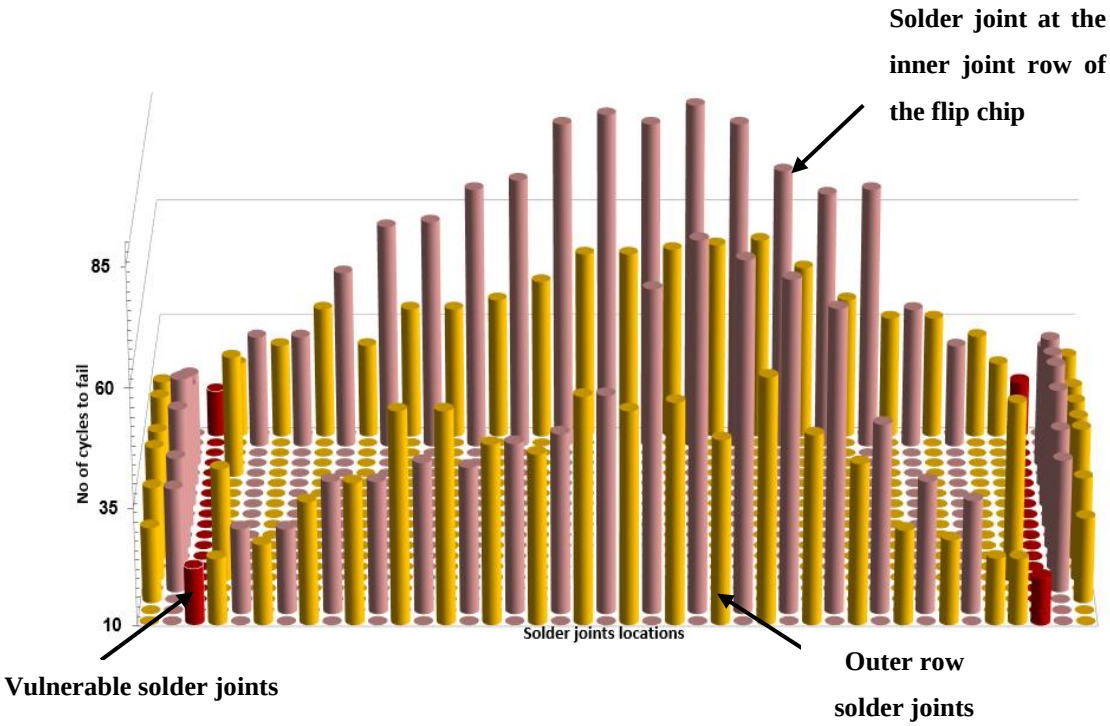


Figure 5-9: Depicted AMI failure cycles of 109 solder joints under U46 Flip chip on 0.8mm HASL board

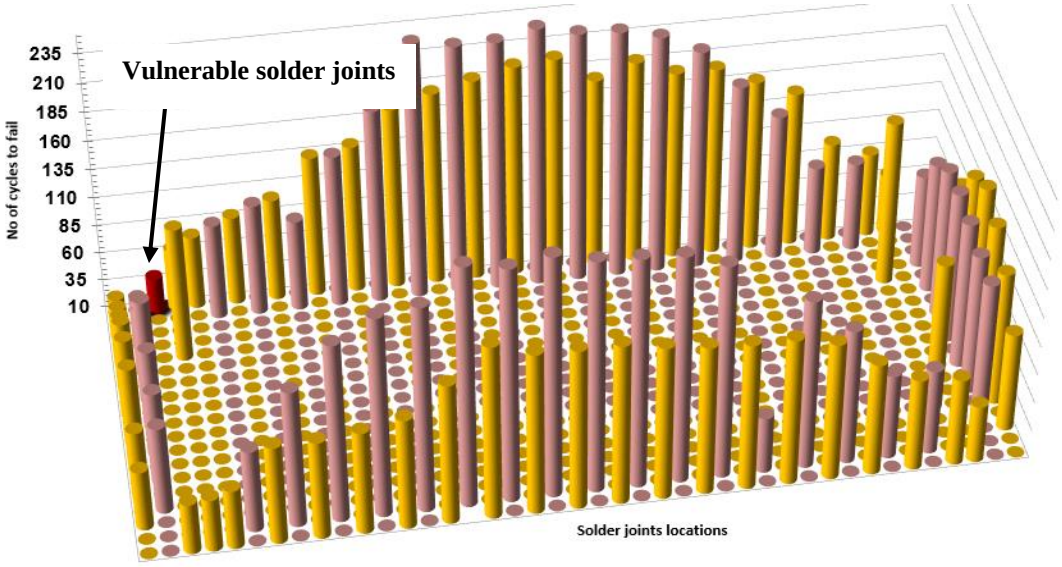
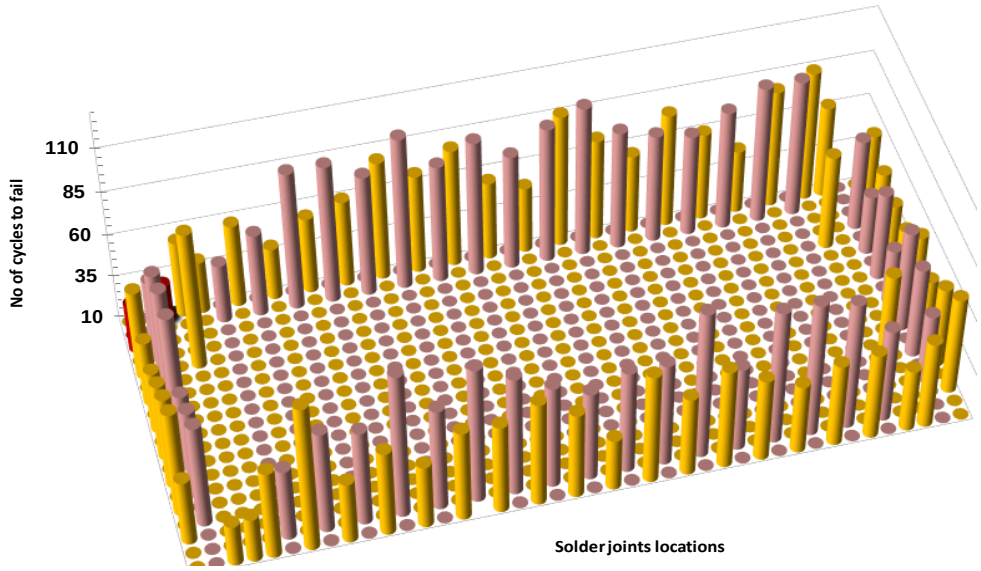


Figure 5-10: Depicted AMI failure cycles of 109 solder joints under U46 flip chip on 1.6mm HASL Board

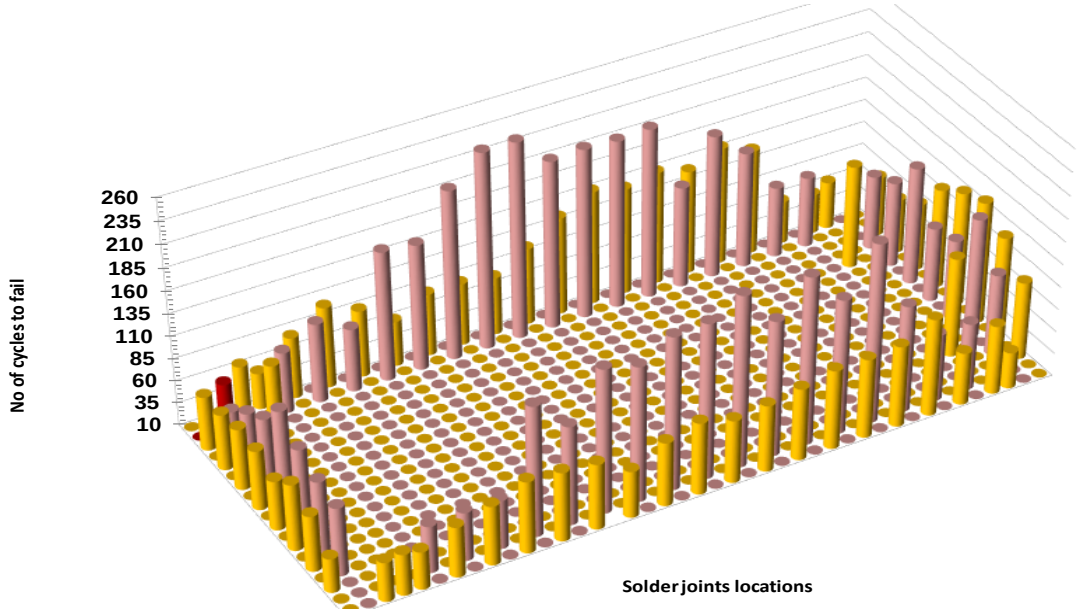
Figures 5-9 and Figure 5-10, demonstrated that the reliability of solder joints on the flip chips under thermal cycling test degrades at different failure rates. The solder joints with the red bar at the corner of the flip chip package as depicted in Figure 5-9 and Figure 10, are considered as the vulnerable solder joints. In the simulation results, it was found that the vulnerable solder joint that shows the lowest level of reliability at a very low thermal cycling test is joint number one as labelled in Figure 3-3. Hence, the AMI measurement depicted in Figure 5-9 was used to verify if the prediction global model is accurate. Based on AMI results, the vulnerable joints that show the lowest level of reliability at a very low thermal cycling are joints 1, 92, 55 and 38. It can be seen that failures of the corner joints in Figure 5-9 initiated after 16 to 20 thermal cycles. This shows that the AMI measurement is more accurate to detect the performance of the solder joints at different failure rates corresponding to the joint location on the flip chips. Thus, the reliability of those solder joints is generated with respect to the thermal profile being used in this research study.

For this work the AMI results presented in Figure 5-11 to 5-14 compare the results of 0.8mm and 1.6mm HASL boards in terms of relative reliability using U35, U19, U27 and U23 flip chips as case study. Consequently joint 1 (highlighted in red on the 3D graph

plots) on the flip chip for is considered as being a vulnerable joints under thermal cycling test. It is important to know that mostly the corner joints has the least number of cycles to failure during validation test. The reliabilities for all other bumps are calculated with respect to increase in thermal cycling test. Also from the monitoring graphical results, it is noteworthy to know that solder joints suited under the flip chips exhibit different thermal cycling rates and different levels of reliability. The reliability levels can vary due to the floor plan layout and influences of some other components.

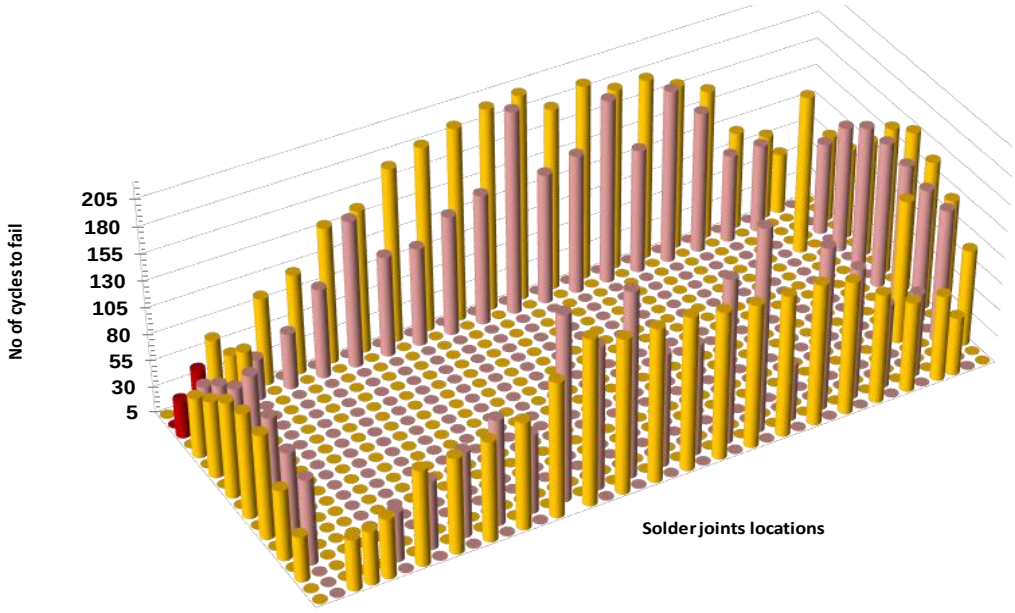


(a)

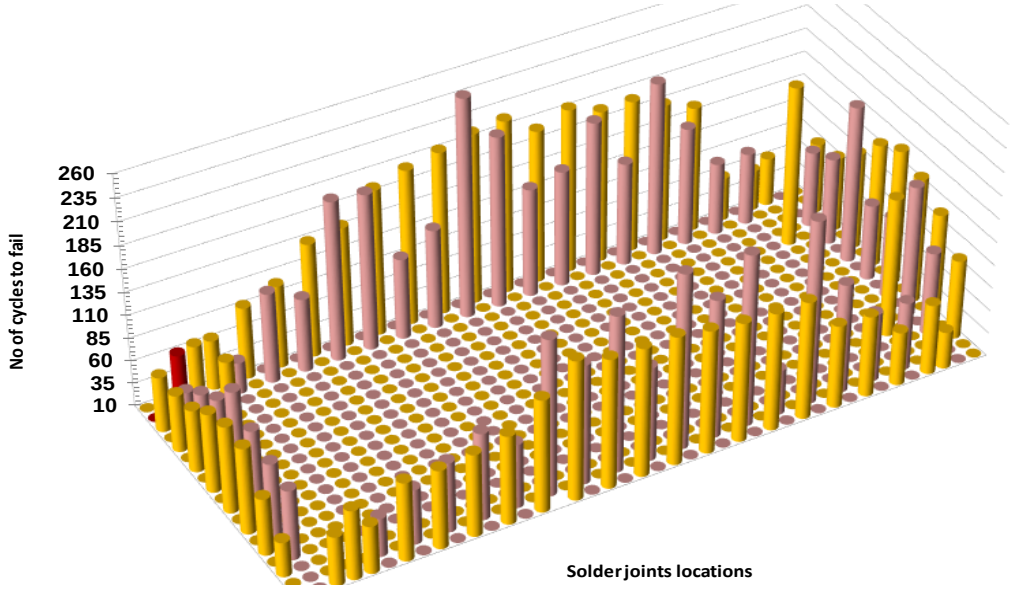


(b)

Figure 5-11: AMI 3D plots showing thermal cycles to failure for (a) U27 flip chip on 0.8mm and (b) U27 flip chip on 1.6mm board

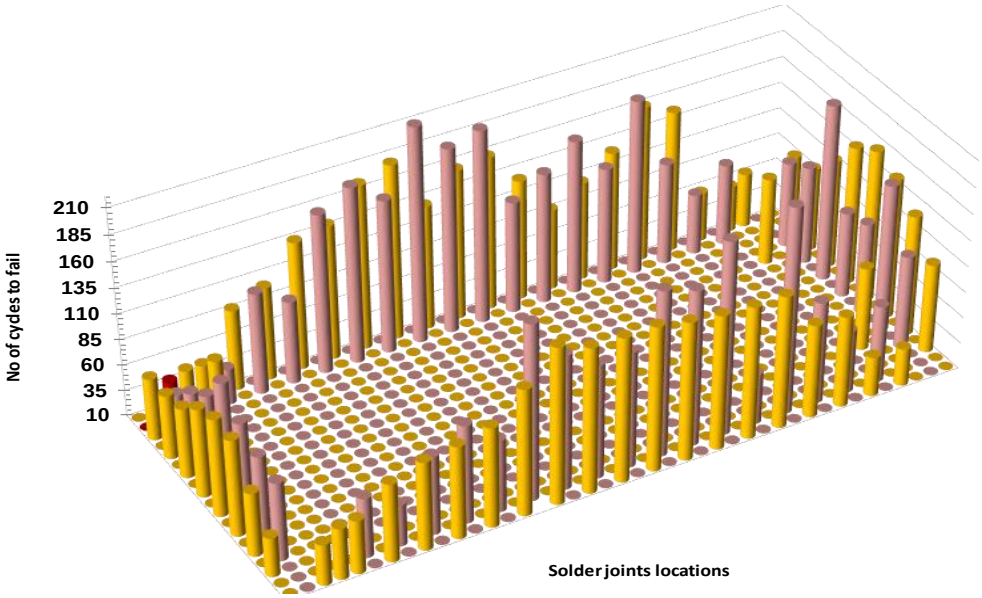


(a)

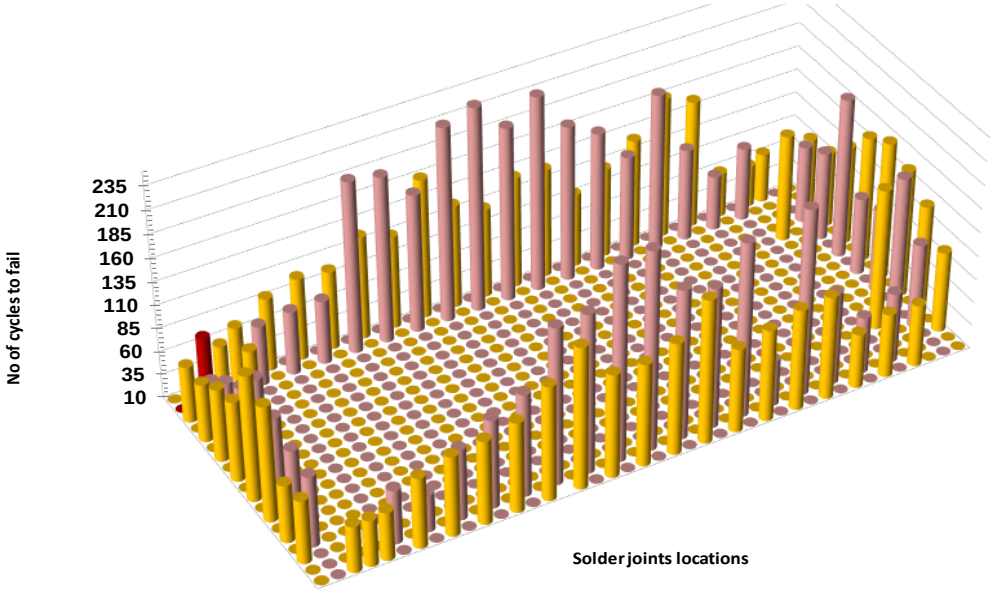


(b)

Figure 5-12: AMI 3D plots showing thermal cycles to failure for (a) U23 flip chip on 0.8mm and (b) U23 flip chip on 1.6mm board

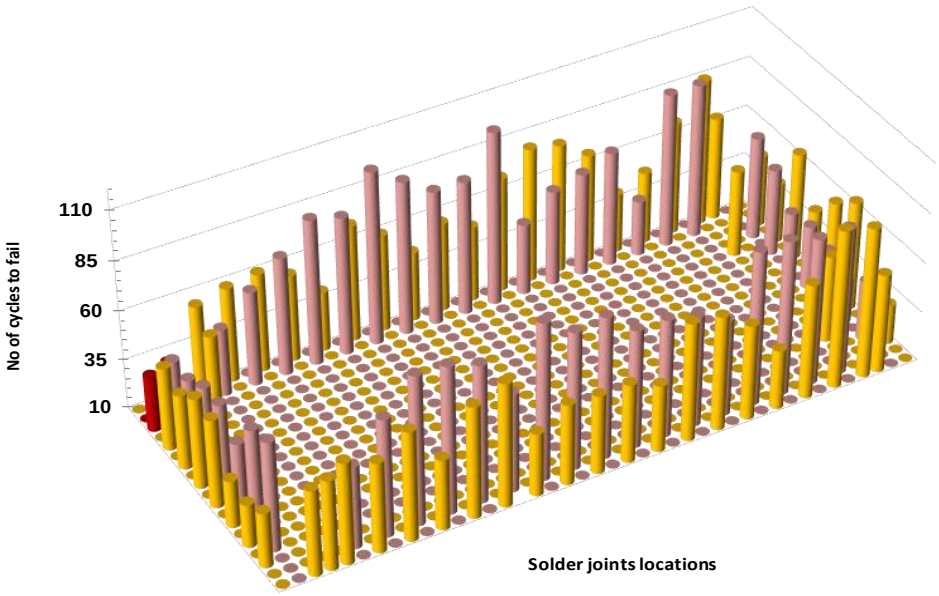


(a)

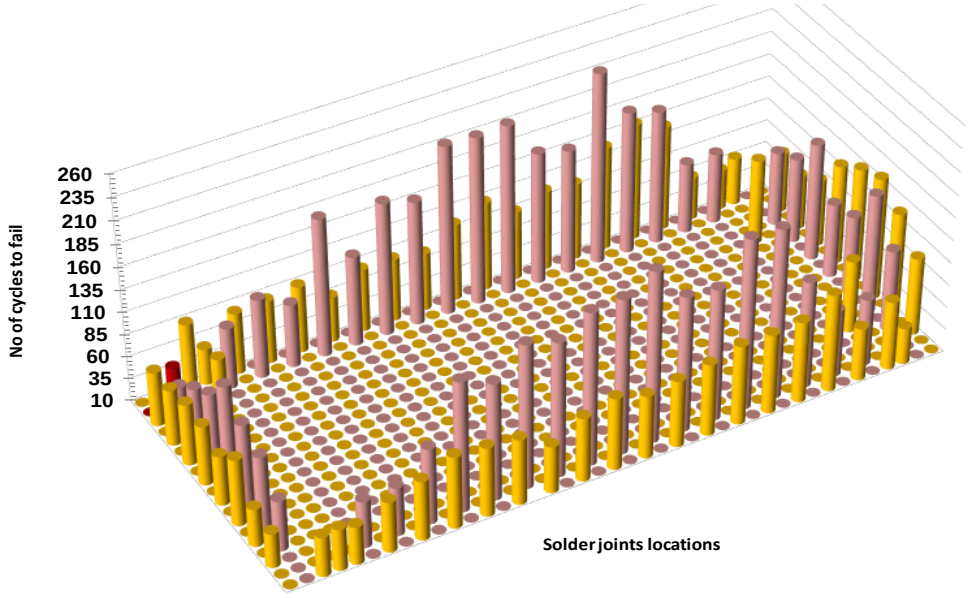


(b)

Figure 5-13: AMI 3D plots showing thermal cycles to failure for (a) U19 flip chip on 0.8mm and (b) U19 flip chip on 1.6mm board



(a)



(b)

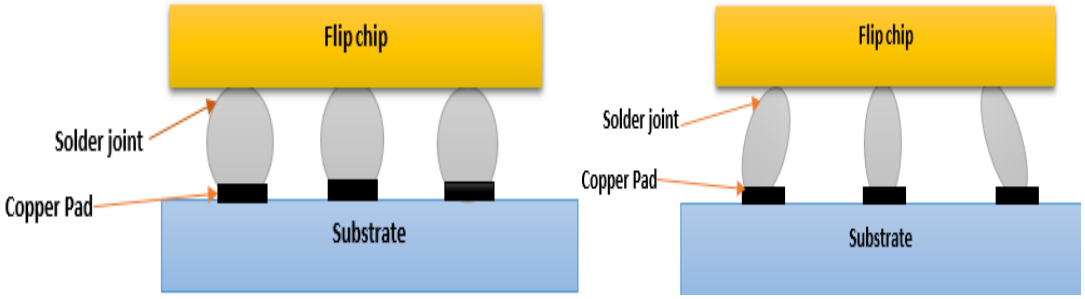
Figure 5-14: AMI 3D plots showing thermal cycles to failure for (a) U35 flip chip on 0.8mm and (b) U35 flip chip on 1.6mm board

5.1.4 Discussion based on the Result of the Effect of PCB thickness on solder joint

In this subsection, the following discussion shows how the validation experimental methods has been established in finding the variability of the ATC parameters and its effect on the reliability of different test samples of 0.8mm and 1.6mm HASL boards. However, the time of failure of many flip chips on the area array packaging was estimated based on conducting a validation test using the constant ATC parameters and by using the theoretical basis shown in Figure 5-11 to analyze the failure mode. It is of note that solder joints are eutectic alloys, for example tin and lead. The material behavior of those joints under various thermal cycling tests, leads to changes in their mechanical properties. At this moment, the CTE mismatch between the substrate and the die generates the failure of the solder joints on the flip chip components carrying the applied thermal stress, which leads to deformation.

However, understanding the role that thermal cycling has on the different test samples on HASL finishes was used to estimate and monitor the reliabilities and failure rates of those flip chips as shown in Figures 5-6 and 5-7. The graphical plots in Figure 5-6 and 5-7 shown that the performance of the solder joints under thermal cycling test is greatly affected by different floor plans layout of the components. As mentioned earlier in Figure 3-3 in chapter 3, the 0.8mm and 1.6mm with HASL finish test boards have 109 solder joints at different locations under each flip chip on each test sample. The flip chip components are all rectangular in shape, hence, the location and geometry of each joint on the flip chips may also dictate the failure mechanisms based on the thermal stress. According to Yang, (2012) in his thesis, the distance of each solder joint to the neutral point in this case, could also lead to thermal strain. Nevertheless, other factors can also affect reliability of the solder joints on the flip chips during the ATC test, for example, the temperature range during the test, the dwell temperature, geometry of the solder joints and the co-efficient thermal expansion mismatch between the substrate and the silicon chip as shown in Figure 5-15.

Thus, by considering the extent of the coefficient thermal expansion mismatch as the main factor in which the substrate expands more than the chip, in this manner the tensile stress is moving towards the direction of the substrate and the opposite direction of the chip side.



(a) **(b)**

Figure 5-15: (a) Solder joint before ATC test
(b) Deformation in solder joint due to ATC.

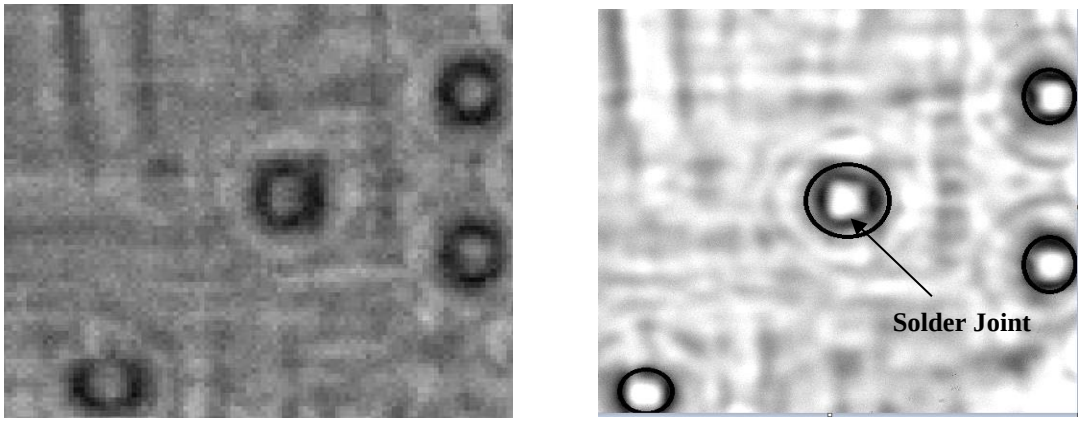
Moreover, the difference in the thermal expansion rate imposes a thermo-mechanical stress on the solder joint between the die and substrate (Pang et al., 2001). The constraint to silicon chip expansion is much greater on the cooling process than the heating process (Rao Tummala, 1996*)*. Thus, based on the inspection analysis, previous research in this field (Yang,2012) has stated that the defect in between the chips and the substrate will provide a large acoustic impedance mismatch, which in return will produce higher intensity images during the AMI inspection.. Moreover, from previous research (Clech et al., 1996, 2005, 2009) (Teng et al., 2002; Shih et al., 2004; Wu et al., 2014), there are many differing opinions on the effect of board thickness on solder joint reliability. According to those authors, modelling indicates that thicker (stiffer) boards afford less mechanical compliance and shorter ATC life, but the work in this section, which has been based on the effect of thermal cycling test on 0.8mm and 1.6mm HASL finish with non -under fill solder joints is vice versa to the findings.

5.2 Performance Evaluation of Solder Joints' Life under ATC using Image Processing Technique.

In this performance evaluation section, part of the main objective is to be able to track and study the rate of increase in intensity of those solder joints, which may occur from the continuous ATC test, performed on the test samples. Thus, once all the solder joints' images have been acquired completely from the performance study, the image must be analyzed using the feature extraction techniques in order to identify and study the crack initiation, propagation rate and the time of failure during the ATC test. Therefore, using image processing techniques is critical to getting the optimum performance of solder joints from those acquired C-SAM images.

Consequently, the first step involved after image acquisition is by selecting the area of interest in the solder joints' scanned images. In this study, the centre of the joints as shown in Figure 5-16 were selected in the solder joints images to be the region of interest (ROI), because they are the main area of interest in the joints that provide all the functions needed to perform their operation in mission life. Therefore, the rate of change in the intensity level of those solder joints have been considered as the main features that will aid in

classifying the performance of those joints. However, in order to extract the region of interest, segmentation techniques were used at the initial stage. Performing a segmentation technique on those joints to get the region of interest is straightforward as it has clear boundaries to process as illustrated in Figure 5-17. Likewise, taking a closer look at the extracted circle ROI in Figure 5-17, there are a number of interesting events that occur in the region that should be involved in the evaluation of those images.



(a) **(b)**

Figure 5-16: a) Shows the nature of several solder joints before ATC test
(b) Shows the nature of similar solder joints after ATC test

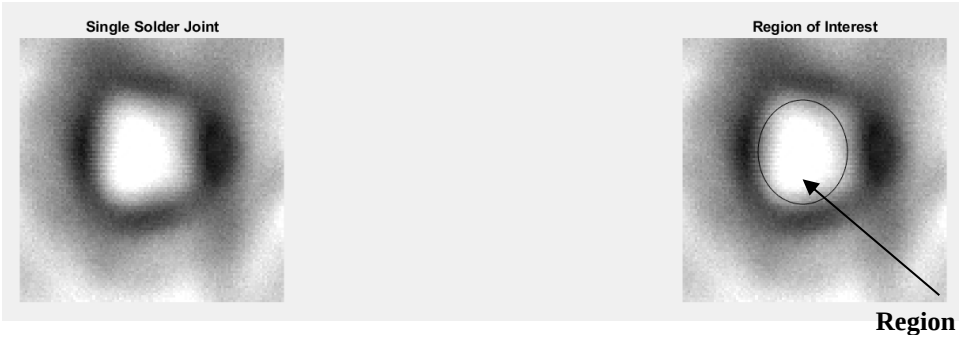


Figure 5-17: Shows a region of Interest of a defective solder joint after ATC Test respectively.

Figure 5-17 shows the region of interest of a single joint on U46 flip chips, 1.8mm board at 88 cycles. Furthermore, the thresholding segmentation method was employed in the image segmentation, which aims to separate the grey levels of pixels belonging to an image that are substantially different from the grey levels of the pixels belonging to the background. This type of technique is an important image segmentation method, which is termed as the main basic preprocessing step in feature extraction analysis and has become an effective tool to separate objects from the background. Some of the examples of thresholding applications used in image processing for non-destructive testing have been documented by (Chen et al., 2009).

Several authors in literature have also utilized the threshold technique according to the type of information they want to exploit. Some of those authors are Solihin et al., (1990), in which this technique was applied to an image by using histogram based thresholding segments to divide an image into various regions based on pixel intensities, which is later applied to handwritten character identification. Likewise, Sang et al., (2007) utilized this kind of technique in their work based on the knowledge based adaptive thresholding segmentation of digital subtraction angiography images. Otsu, (1979) proposed a method for choosing the optimal threshold to minimize the within-class variance. Thus far, Kapur et al.,(1985) introduced a method for determining the optimal threshold to maximize the entropy. Meanwhile Hou et al., (2006) also suggested an optimal threshold method to minimize the sum of class variances. However, among the types of thresholding techniques cited, Otsu's thresholding method could be referred to as the most popular method due to its non-complex and efficiency during segmentation (Jung-Min et al, 2014). This method has been represented by using Equation 5-2:

$$\mathrm{P_i}\ \frac{ni}{MN}\ ,\ \mathrm{P_i} \geq 0\ \ \sum_{i=0}^{L-1} P_i = 1 \qquad \text{Eq. 5-2}$$

Represent let M × N pixels of a given image by L grey levels $\{0, 1, 2\ldots\ L-1\}$. The number of pixels at level i is denoted by n_i and the total number of pixels is denoted by $MN = n_0 + n_1 + \ldots.. + n_{L-1}$. The grey-level histogram is then normalized and regarded as a probability distribution.

The segmentation technique has been implemented in those solder joints in Figure 5-18 to separate out regions of an image corresponding to objects, to analyse. Thus,

segmenting the region of interest of the solder joint with a full black ring is straight forward as it has a clear boundary to process. This separation technique has been based on the variation of intensity between the object pixels and the background pixels of those single solder joints.

The figure 5-18 shows the typical single solder joint C-SAM images that demonstrate the process of increase in the intensity in ROI of solder joints number nine 9 subjected to different thermal cycles, under U19 flip chip of 0.8mm substrate board.

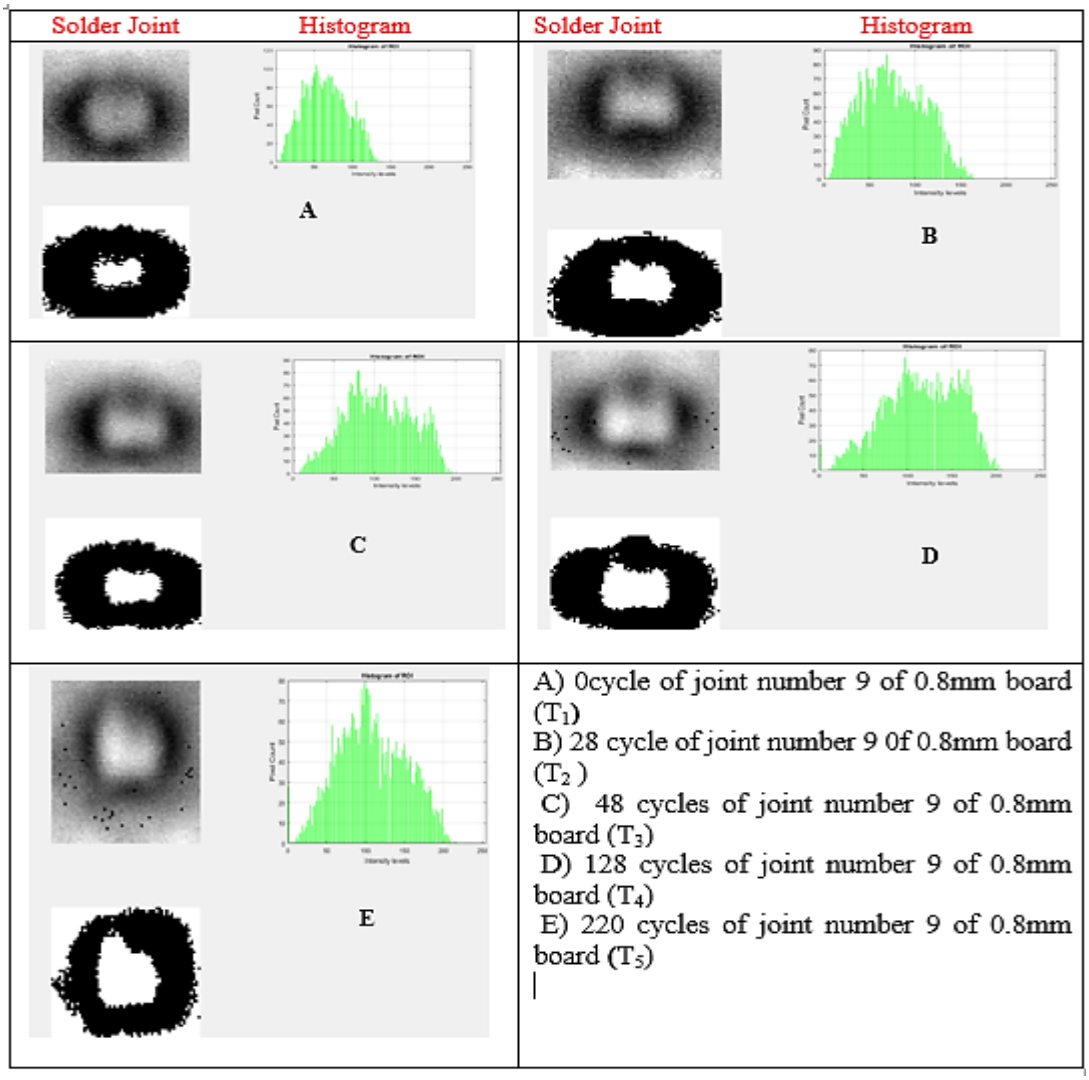


Figure 5-18: Intensity level and histogram of region of interest of joints number nine (9) after a) 0, b) 28, c) 48, d) 128 and e) 220 cycles of U19 flip chip of 0.8mm board.

With respect to the objective, the intensity level of ROI's of the solder joints before and after the TC test have been demonstrated in Figure 5-18. When examining the

performance of the solder joints image, according to the work conducted by Yang, (2012) the intensity of the solder joints will be higher if there is a defect on the joint. Thus, the histogram graphical results justify the performance degradation of those joints generated by the validation test. It has been found that increasing thermal cycling test, has a range of effects on the intensity around the grey area at the centre of the solder joints. In addition, by observing those single solder joints' images, it shows that there is distortion and structural changes of the ROI under thermal excursions. Another observation is that the intensity of the histogram keep shifting and increasing from low intensity to high intensity as the TC increases. This has been considered as an indication that the crack could occur in this region.

As I mentioned earlier, the round grey area in the middle of every joint represents the integrity of the joints, which denotes the bonding between the die and the solder bump. However, from the observation noted from the acquired C-SAM images, it is going to be more difficult to analyse the level of cracks or delamination in those joints by just using human visual inspection. Hence, using feature extraction methods will make it much easier to analyse and segment the solder joints images during performance analysis.

5.2.1 Using Structural Similarity Index to Analyze the Solder Joints

To further investigate more about the difference and to examine the difference in those solder joints at different thermal cycling tests, a numerical index comparison using statistical methods is employed to determine the degree of similarities between the images got from each variation in the test. The principal idea underlying the structural similarity approach is that the human visual system was adapted to extract structural information from visual scenes and therefore a measurement of structural similarity should provide a good approximation to perceptual image quality assessment (Wang, 2002)(Al-Najjar, 2012).

The SSIM index is a function of images denoted $\mathbf{T_5}$, $\mathbf{T_4}$, $\mathbf{T_3}$, $\mathbf{T_2}$ **and** $\mathbf{T_1}$ in Figure 5-18 respectively. Assuming one of the images to have a good quality, the SSIM index in this scenario has been regarded as a quality measure of the other images. The algorithm computed in MATLAB separates the task of the image quality measurement into three parts: structure, contrast and resolution. The image of the solder joint at T_1=0TC was used as the reference or template image while the images of solder joints at T_2=28TC,

T_3=48TC and T_4=128TC and T_5= 220TC were being used as the matching/distorted image.

Below are the results as got from the MATLAB Toolbox

The SSIM Index between the reference image '0' and distorted solder joints image '220TC' is 0.949.

The SSIM Index between the reference image '0' and distorted solder joints image '28TC' is 0.987.

The SSIM Index between the reference image '0' and distorted solder joints image '48TC' is 0.972.

The SSIM Index between the reference image '0'and distorted solder joints image is '128' is 0.966.

For more information regarding the MATLAB code for this work please refer to the Appendix B in the CD at the back of this thesis

In addition, in order to improve human knowledge in the classification process, and for correlating the performance of solder joints under TC test, the mean intensity value scattered analysis graph was constructed. Due to the symmetry feature, flip chip location, and likewise the effect of the thermal cycling test on those test samples, U46 flip chip of Board number 09 of 0.8mm substrate thickness was used for the analysis. From the resulting diagram in Figure 5-19, the image features obtained by the AMI techniques such as intensity can easily distinguish between a healthy and fractured joint. The graphical results shows the typical mean intensity increases of all the 109 solder joints under the test sample during temperature cycling. Thus, for performance analysis, the graph has been divided into two periods, before and after the ATC test. The maximum intensity value was around 180 at 88 thermal cycles, while the mean intensity of the good joint is in the range of 43- 85 for 0 TC.

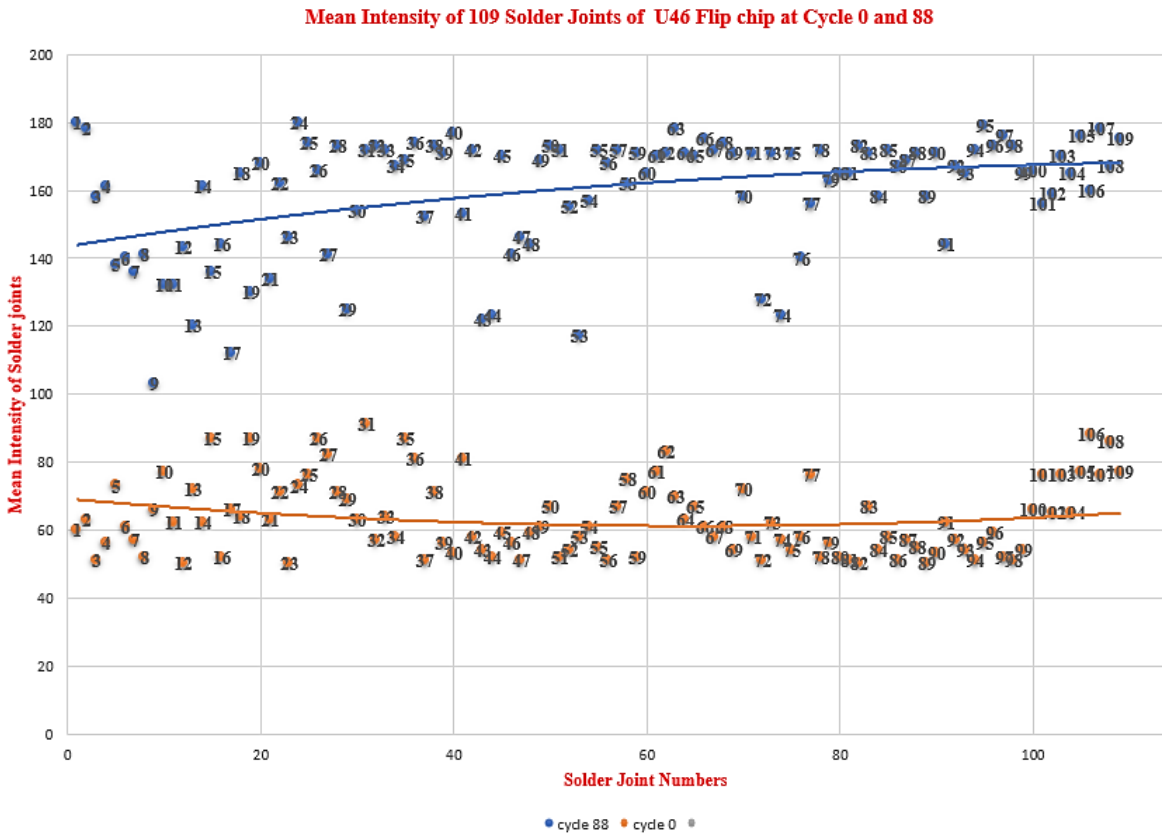
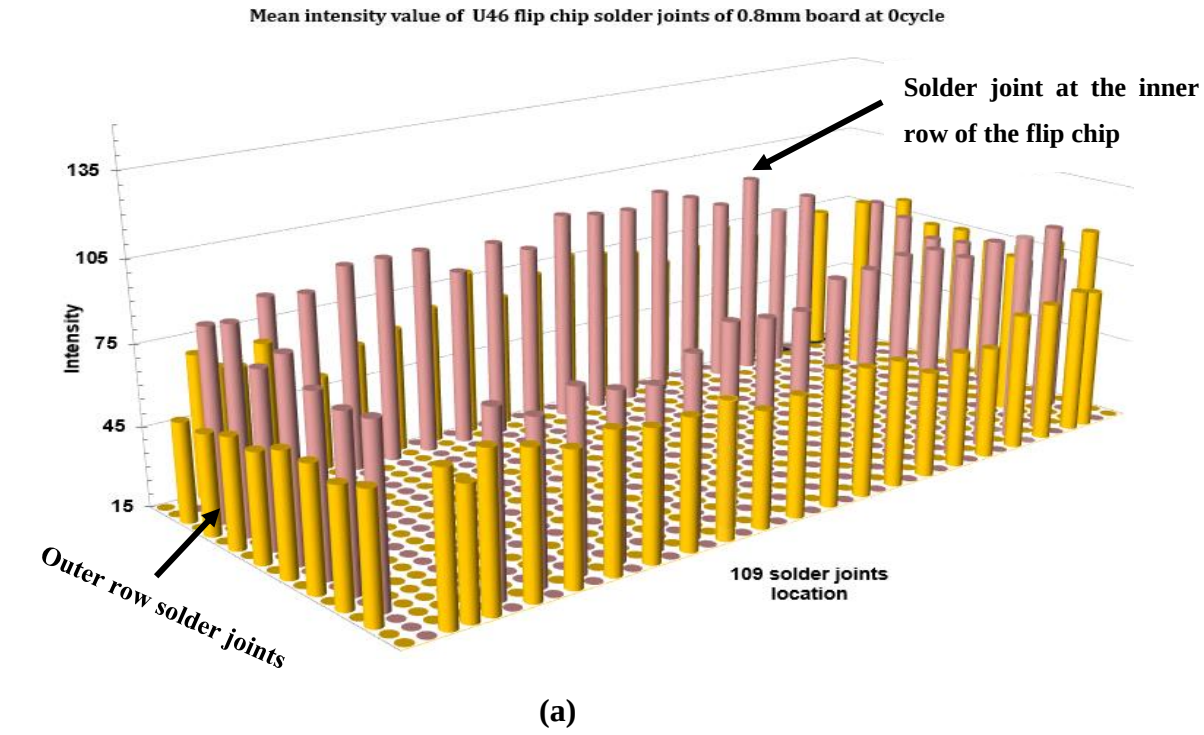
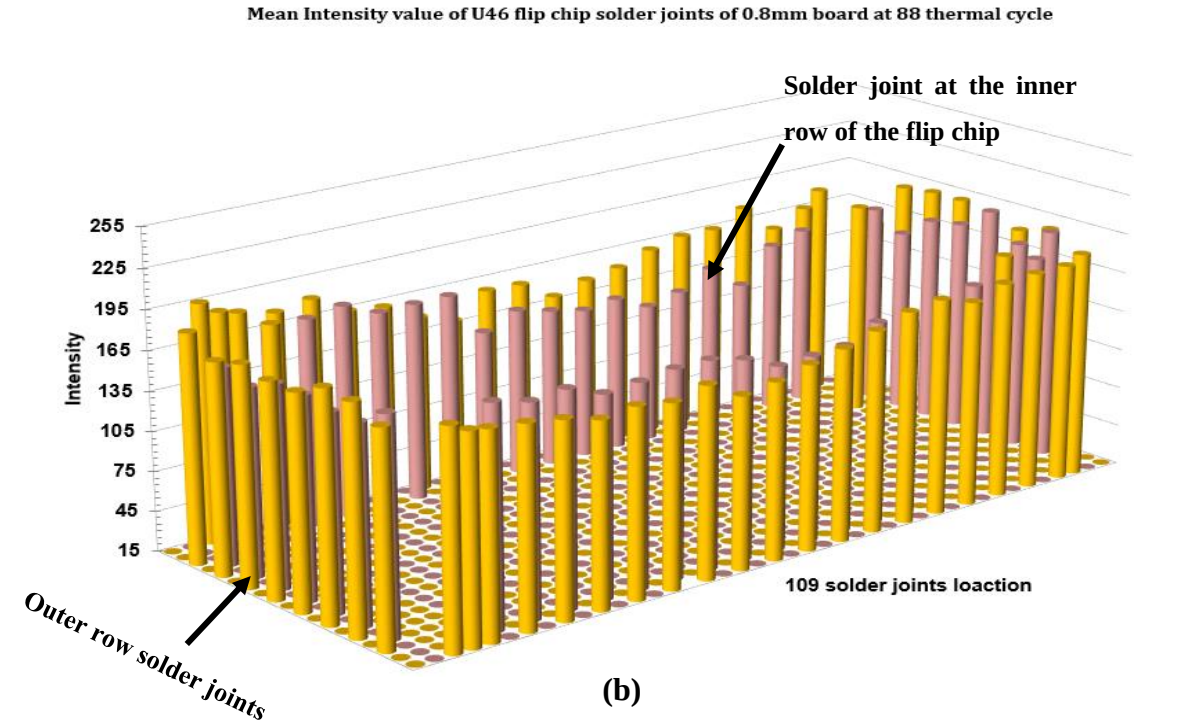


Figure 5-19: Scattered graph showing the mean intensity of 109 joints under BD09 U46 Flip chip, 0.8mm at 0 to 88 Thermal Cycling

However, the figure in 5-19 depicted the intensity plot of U46 flip chips solder joints at 0 and 88 cycles. With regard to the 3D diagram as shown in Figure 5-20, the changing trend for each solder joint intensity rate is similar at low thermal cycling, whereas the intensity of those solder joints increased drastically as the thermal cycling increased. However, due to the geometry position of the U46 flip chip on the circuit board assembly as shown in Figure 3-2 and the substrate thickness of the board being used, all solder joints failed at 88 thermal cycling, which led to the removal of the flip chip on the test sample. In other words, as the board thickness and overall stiffness decreases, the resulting stress the solder joint, without under fill experiences, increases.



(a)



(b)

Figure 5-20: Depicted the Mean Intensity of 109 joints on U46 Flip chip of 0.8mm Board, at 0cycle to 88 Thermal Cycling

5.3 Chapter Summary

In summary, a validation test was conducted in Delphi automotive industry for a whole year in order to quantify the reliability of solder joints on different test samples. By using available industry standard thermal chambers. Thus, in order to estimate and determine the reliability of solder joints on area array packaging, an appropriate printed circuit board for the test was designed as shown in Figure 3-2. For different test samples designed for this experiment, the test samples had various area array packages configurations, different surface finish and two substrate thicknesses to enable reliability testing, so that the failure rates of those components can be monitored to achieve the desired specifications.

A thermal cycling test with the thermal profile -40ºC to +85ºC was conducted on the test samples as illustrated on the resulting graphs in Figure 5-4 and 5-5. Analysis of the test results was used to monitor and estimate the relationship between the unpopulated and populated PCB under different thermal cycling tests in other to achieve the desired specifications. The thermal profiling data were analysed as shown in Figure 5-1 to demonstrate the accelerated cycling test used to acquire information quickly based on the life testing of those joints. This was achieved by subjecting all the test samples to the validation test such that a slow enough failure process, enabled finer tracking of crack propagation in solder joints, was observed will be discussed in chapter 6.

It is of note that the thermally induced stresses in those solder joints are the result of CTE mismatch of the various materials in the area array packaging (AAP). Thus, analyses of the test results as shown in Figure 4-10(d), noticed that after 44 thermal cycles, defects begins to occur on the corner joints of 0.8mm board, due to the increase in the reflected acoustic wave intensity of those joints as shown in figure 5-20. A novel finding was that the thicker the substrate thickness, the longer the solder fatigue life for the results from 0.8mm and 1.6mm PCBs used. Hence, solder joints on the thicker board show significantly high solder joint reliability.

With respect to the objective, evidence from this study has depicted that the corner flip chip solder joints have the lowest reliability on both the PCB's as shown in Figure 5-6. However, findings also demonstrated that the failure distribution on those solder joints is often influenced by the floor plan layout of the components.

Finally, by studying the variation in the acquired data, the test results will be used in chapter 6 next, for reliability monitoring of solder joints. Then to produce an extrapolation analysis to try to predict reliability of solder joints at use.

6 Crack Initiation in Solder Joints of 0.8mm and 1.6mm Test Boards

After the validation test, the next step involved in this research is to detect, analyse and estimate any solder joints' defects that could contribute negatively to the reliability of solder joints in the packages. This chapter also presents and examines a novel method for solder joints defect evaluation using geometrical and time-domain feature extraction methods. This was demonstrated to analyse the reliability and failure rate results of solder joints under validation test. Thus, the AMI solder joints images acquired during the validation test was used to affirm the reliability of those solder joints in the test samples.

6.1 Solder Joints Crack initiation measurements in AAP

One of the major challenges in the reliability study of solder joints under ATC is to be able to determine when the cracks will initiate, propagate or when a solder joint will fail completely in AAP. As previously mentioned in chapter 2, the defects on those solder joints are very difficult to identify using some of the NDE like X-ray because of their test samples' size limitations, and a long data acquisition and image reconstruction makes it a challenge during the monitoring of solder joints under thermal cycling test. However, in order to analyse and estimate the defects in those solder joints, real AMI solder joints were collected at different ATC times to monitor the fatigue degradation rate of those joints. Thus, due to the large amount of data collected at various intervals during the thermal cycling test, only the solder joints shown in the Figure 6-1, was selected for reliability analysis study.

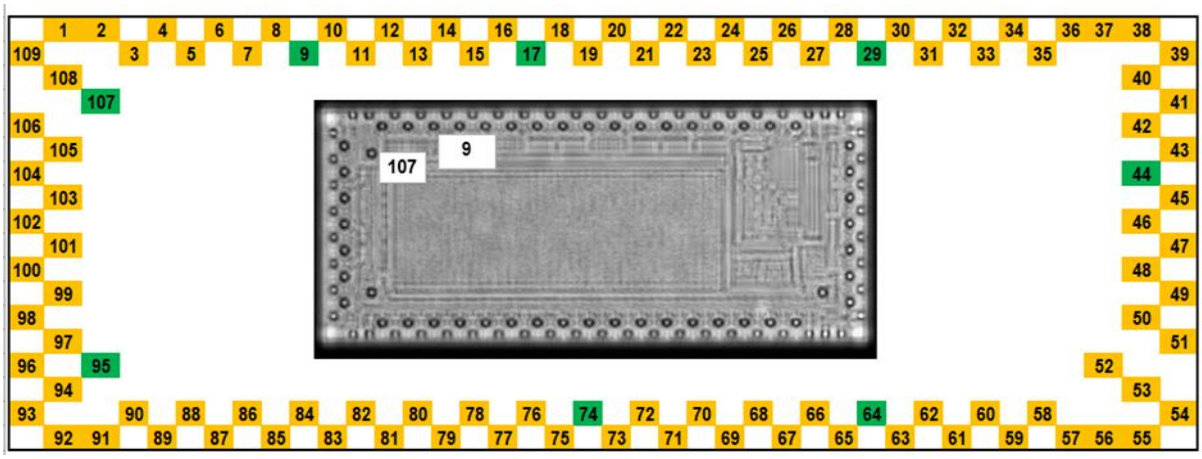


Figure 6-1: Layout of the solder joints in the flip chips

In this reliability study, there are 109 solder joints on each flip chip, the labelling of each joint has been depicted in Figure 6-1, and the selected solder joints marked in green colour are used for performance analysis. Hence, those solder joints were selected based on the distance to the neutral point. It is noteworthy that the thermal strain on those solder joints was related to the distance of the solder joints to a neutral point (Clech et al., 2009). Nevertheless, the solder joints at different locations on the chip may also have different fatigue behaviour and failure mode this is mainly due to the thermo-mechanical, which is dependent on the joint position (Magnien et al., 2017). Based on the AMI images acquired during the validation test and monitoring test as shown in Figure 4-10 (d) it is noted that the solder joints on the flip chips begin to fail at the corner joints, this factor is also considered when selecting the joints in the solder joint assembly during thermal test.

Thus far, various approaches have been used in this research work to study the fatigue life of those joints as discussed in section 6.2.

6.2 Solder Joints Crack Initiation Detection Using Image Processing Techniques

Estimating the crack growth in solder joints allows for determining the load bearing area of the joint as a function of service lifetime (Nielsen, et al., 2014). However, according to Huang et al., (2010), by using fractured mechanisms, the cracks that occur in solder joints can develop in two stages, namely crack initiation and crack propagation to failure

during usage. Nevertheless, Darveaux, (1993) shows that crack initiation under thermo-mechanical loading occurs in the first 10% of the fatigue life. His approach was based on using the sum of a crack initiation period and crack growth in the test sample to predict the lifetime performance of the product which is referred to as the Energy-based method using non-linear Finite element analysis (FEA). Some researchers as previously mentioned in chapter 2 of this thesis, who have studied the reliability of solder joints so far rely on detecting the failure in them through measuring the Finite element analysis or based on assumption.

Now the actual question is how to characterize, monitor and estimate the failure rate and reliability of AMI solder joints images under thermal cycling test. Thus far, different researchers have used different criteria to work on the field. For example, in previous works (Yang, 2012;Braden, 2012), two image features named as crack plane diameter and intensity were examined. The initial results showed that the image features have a strong relationship to the crack size. Nevertheless, in order to determine and estimate the reliability and the failure rate of AMI solder joints images in this research work, massive expansion of image data as shown in Table 6-1 was acquired using the acoustic micro imaging technique.

Table 6-1: Shows the solder joints data acquisition table

Scenario	Transducer MHz	Resolution	Scan Type	Flipchips to Scan		Time/Scan (Mins)	Total Scan Time	Image Size Pixels		
				Qty	List			X	Y	Z
1	230	3um	C-Scan	14	All	15	210	3366	1024	1
2	230	3um	Virtual Rescanning Mode	6	U23,U19, U35,U27, U39,U46	22	132	3366	1024	256
3	230	1um	C-Scan	1	U23	115	115	10000	3400	1

After the image acquisition, classifying and analyzing those images were considered mainly as vital research issues for detection of cracks. A significant contribution of this research was to automate the solder joints' extraction methods and employ it for effective reliability analysis of solder joint under environmental testing. This was accomplished by using two feature extraction methods namely the geometrical and the time domain

features as described in this chapter. The analysis results were used to demonstrate the reliability of solder joints.

The analysis was achieved after the segmentation process as illustrated in Figure 6-2, in which the reliability and the failure rate of the solder joints was extracted by using a fracture-based model. The objective of using this type of model in this research work was to characterize the crack propagation time, which was used for detailed solder joint failure analysis. Consequently, the geometrical feature extraction methods such as form factor and area were extracted from the AMI images obtained, the objective is to verify and estimate the reliability and fatigue degradation of solder joints during ATC test in order to achieve the desired conditions. Although, the result accuracy obtained in defects detection in this reliability analysis can be useful in defects analysis.

6.2.1 Strategies used in estimating solder joints behaviour under validation test

Estimating the reliability of solder joints under validation test in this research work involves various series of steps. In other words, the solder joint images must be analysed prior to the feature extraction process illustrated in chapter 3 in order to estimate and identify the distinctive image features. This consequently requires multiple image processing steps for the extraction of meaningful quantitative information. An outline of a strategy used to analyse the solder joints images in this research is presented below:

i) Load solder joints images from the file directory

ii) Applying Histogram equalization to improve the contrast in images

iii) Image segmentation.

After performing the histogram equalization on the solder joint images, the next step is to perform image segmentation. Segmenting the grey area of those solder joints with a full black ring is straightforward as it has a clear boundary to process. Puneet et al., (2013) stated that image binarizing is a process that divides the image into two different parts namely black and white. Thus, the solder joint images acquired comprise of two parts during the validation test as illustrated in Figure 5-10 in chapter 5, and has a bright background over a dark background. One way to extract the background is to

automatically determine and select a threshold T that separates these regions, using the equation 6-1:

$$G(x, y) = 1 \text{ If } f(x, y) > T \qquad \text{Eq. 6-1}$$

$$= 0 \text{ Otherwise}$$

Where g(x, y) is the thresholded binary image of f(x, y). We can implement the thresholding operation in MATLAB by the following function:

$$g = \text{im2bw}(f, T) \qquad \text{Eq.6-2}$$

The first argument f gives the input image, and the second argument T gives the threshold value. The level value of 0.5 corresponds to an intensity value halfway between the maximum and the minimum value. This level value was found to work well with all the solder joint images. The threshold value was set based on the contrast between the solder joint back outer background and its surrounding ROI's.

(iv) Using Hough Transform to detect the solder joints in the AMI images.

This type of method aims to find circular patterns within an image. If a circle in an image is described by using the equation 6-3:

$$(x-a)^2 + (y-b)^2 = r^2 \qquad \text{Eq. 6-3}$$

Where (a, b) in the equation 6-3 are the coordinate of the circle centre and r is the radius, then an arbitrary edge point x and y will be transformed into the circular cone in (a, b,r) parameter space (Mohamed et al., 2005). This method was implemented in the acquired AMI images by using the Opencv library (Bradski, 2008) in python as shown in Figure 6-2. Opencv is good for image processing and computer vision tasks, which is user friendly. Figures 6-3 and 6-4 show and verify the use of Hough transform in detecting the solder joints.

```
#detect circles in the image
solder_joints = cv2.HoughCircles(mask, cv2.HOUGH_GRADIENT,2, 1,param1=100,param2=10,minRadius=2,maxRadius=5)
print solder_joints
# ensure at least some solder_joints were found
if solder_joints is not None:
        # convert the (x, y) coordinates and radius of the circles to integers
        solder_joints = np.round(solder_joints[0, :]).astype("int")
        # loop over the (x, y) coordinates and radius of the circles
        for (x, y, r) in solder_joints:
                # draw the circle in the output image, then draw a rectangle
                # corresponding to the center of the circle
                cv2.circle(gray, (x, y), r, (0, 255, 0), 4)
                cv2.rectangle(gray, (x - 5, y - 5), (x + 5, y + 5), (255, 255, 0), -1)

        # show the output image
        cv2.imshow("output", np.hstack([resized_img, gray]))
        cv2.waitKey(0)
```

Figure 6-2: Image showing the command for detecting solder joints in AMI images using Open cv

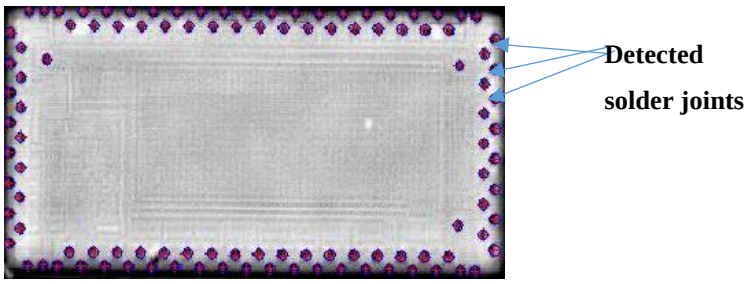


Figure 6-3: Results obtained by using Hough Transform to detect solder joints

iv) Clearing border object (Imclearboarder) has been used to obtain the region of interest as an indication of solder joint bonding quality in the ultrasonic images.

v) Feature Extraction: feature extraction is the step taken to segment and extract features that represent the integrity of the solder joints' images. Two features extraction were used namely:

i) Time Domain feature: using standard deviation

ii) Geometrical feature : Using the area and perimeter to find the form factor which is Form Factor =(4πX Area)/(Perimeter)^2

The Figure 6-4 show basic block diagram of image binarization.

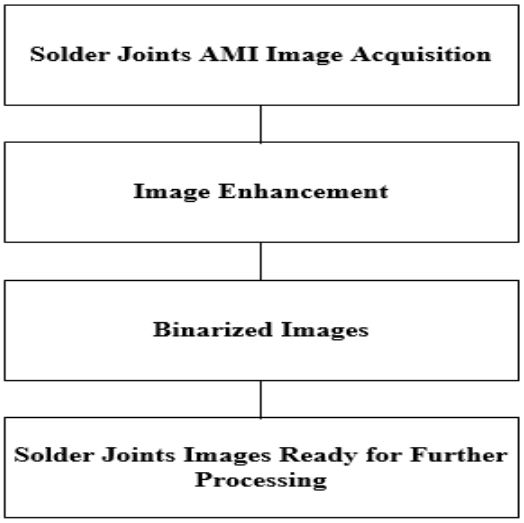


Figure 6-4: Block diagram of Image binarization

6.3 Image Segmentation and Feature Extraction

The proposed integrated crack initiation and propagation methodology were divided into various section as shown in the flow chart Figure 6-5:

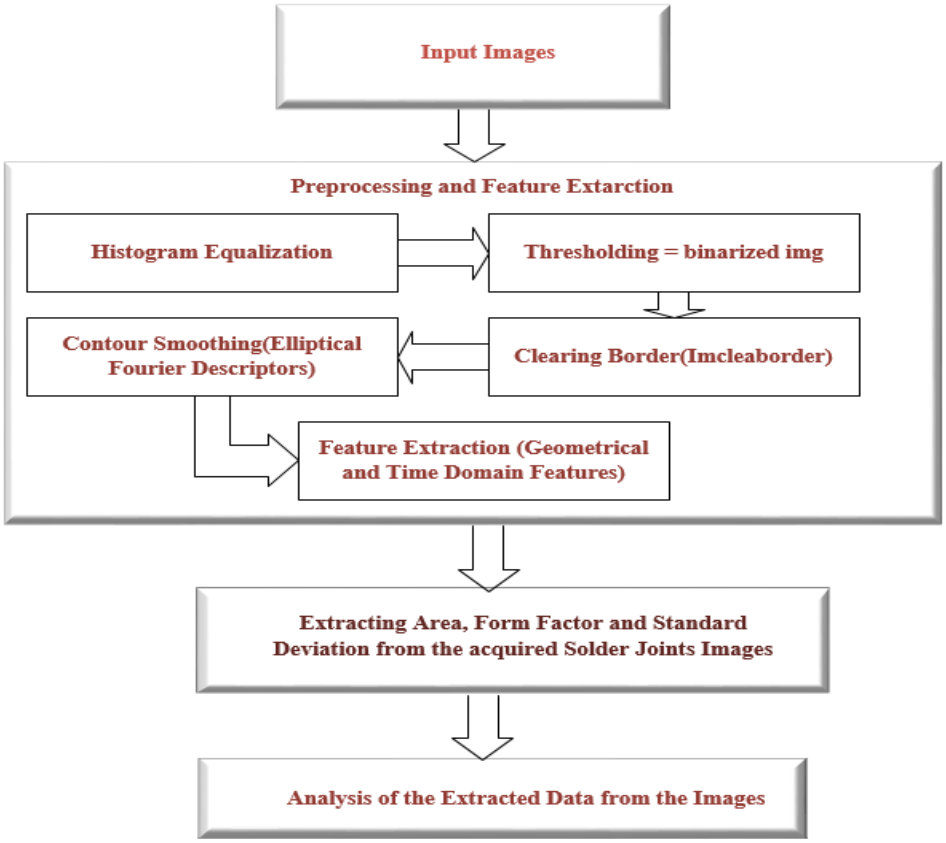


Figure 6-5: Framework showing Pre-processing and feature extraction Algorithm

This section presents a novel approach to monitor the performance of solder joint using the time domain feature and the geometrical feature, with the objective to determine the extreme stress that those solder joints experience before failure that portrays the fatigue crack initiation and propagation life of solder joints under thermal cycling tests. During the statistical analysis stage as depicted in Figure 5-9 in chapter 5, it is observed that the effect of temperature cycling on fatigue evaluation only for one solder joint, on the flip chips on different test samples, is not enough to determine and compare the reliability of other solder joints under the validation test. Obviously, this is due to different stress states experienced by various joints that actually affect the fatigue life of solder joints.

Moreover, when examining the solder joints images in detail, it was discovered that the images in Figure 6-6 contained different backgrounds and formed different geometrical patterns under thermal cycling test. For preprocessing purposes, there are two stages involved in the segmentation process of those solder joint images, firstly, all the selected

solder joints: in order to highlight the region of interest thresholding was done in order to eliminate the background noise as discussed in chapter 4.

Image processing as shown in Figure 6-4, secondly is to extract an image of the ROI from each solder joint. The relationship between the solder joints during thermal cycling in the image and the initiation time is derived and analysed using the image processing technique in MATLAB toolbox. During the segmentation process, the first technique used was histogram Equalization as illustrated in Equation 6-4. For example, the intensity of a pixel in an image is represented by 'I 'and the integer pixel intensities ranging from 0 to L − 1. Where L for an 8 bits image will be $L=2^8=256$, Thus, possible intensity values going from zero representing black to L-1=255 representing white.

$$pn = \frac{number\ of\ pixels\ with\ intensity\ n}{total\ number\ of\ pixels} \qquad \text{Eq. 6-4}$$

Where n = 0, 1, L-1. In addition, p is the normalized histogram of image.

This technique was performed to enhance the contrast in the acquired images and to equalize intensity in an image so that the details in those images were observed more easily. Next step is Image segmentation, which is a process of partitioning the acquired images into different segments as depicted in Figure 6-4. There are two stages involved in the segmentation process. The first stage is extraction of solder joints from the acquired image as shown in Figure 6-3. Note more extracted solder joint images for 0.8mm and 1.6mm thick circuit board assembly are available in the disc at the back of this thesis. The second stage is to extract the region of interest from them Figure 6-4. However, this type of method is considered as the first important step in the pre-processing. According to Frew (1997), this technique was carried out by assigning a particular label to each pixel in the image such that each pixel with the same class shared common characteristics (Frew et al., 1997). In other words, in performing the segmentation on those images, the pixels which represent both the background and the bright region are grouped into meaningful regions.

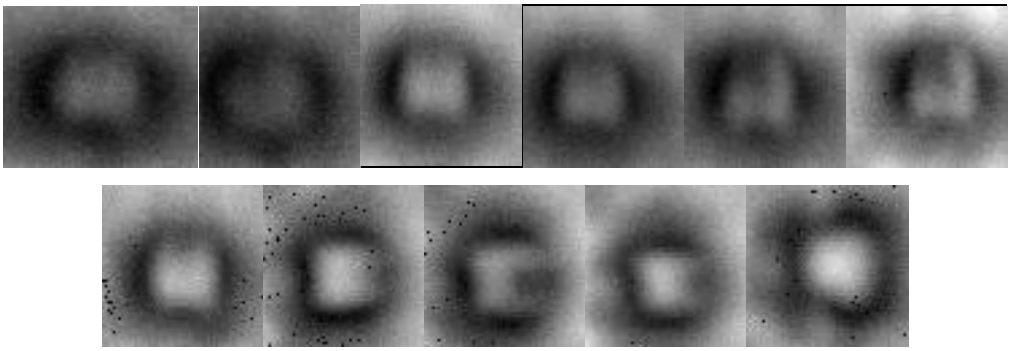
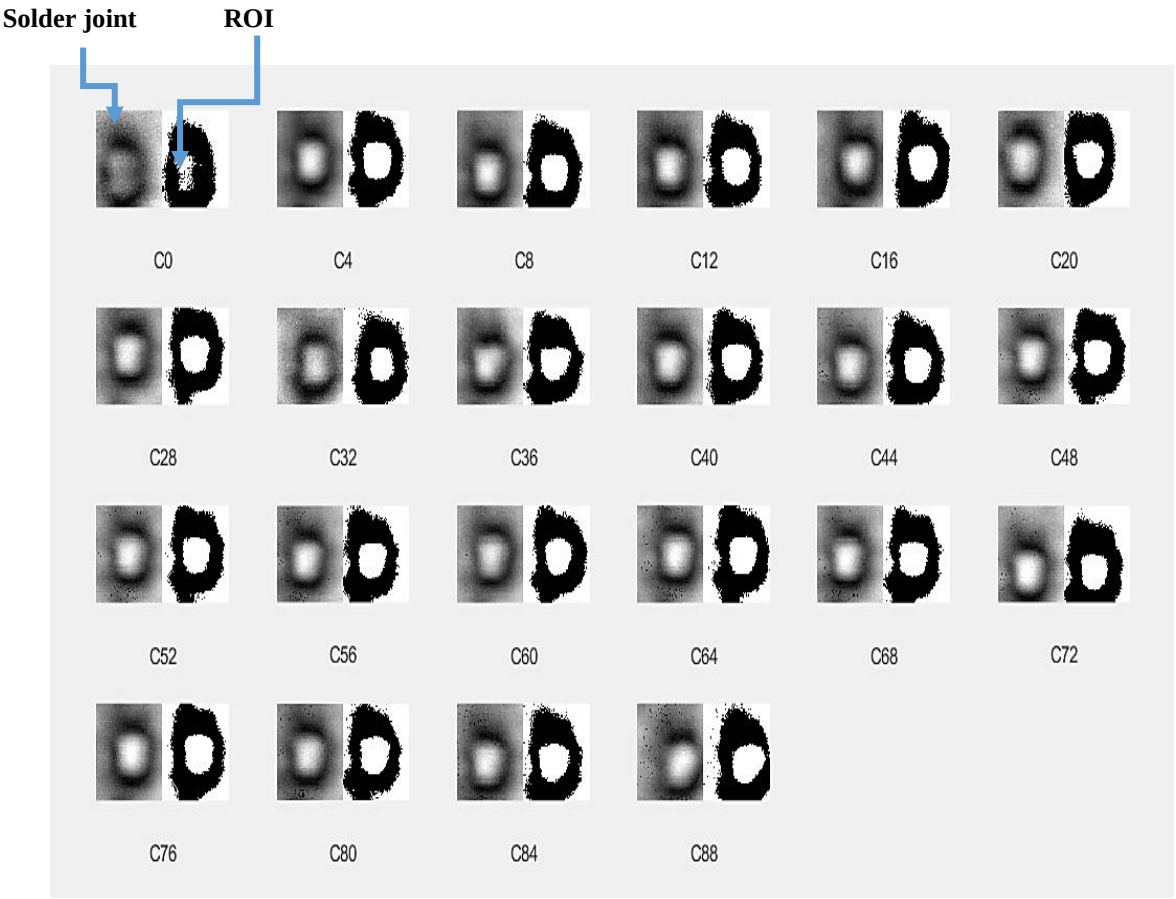
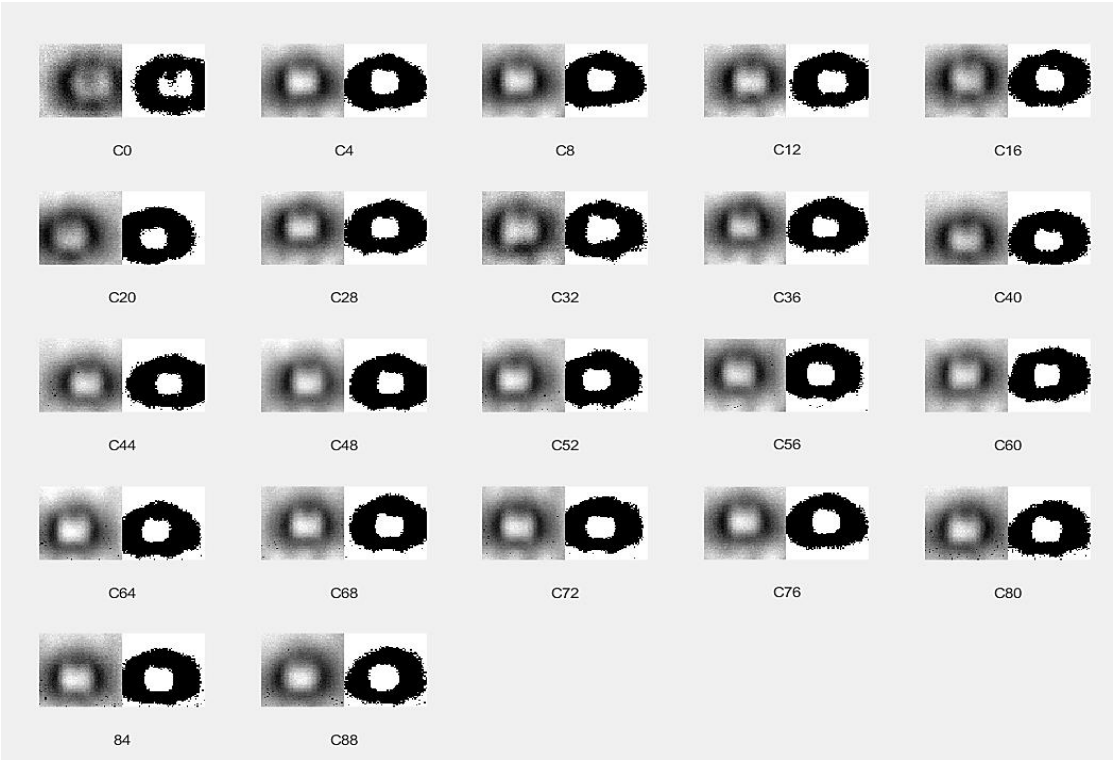


Figure 6-6: Examples of extracted single solder joints images

The result in Figure 6-7 a, b, c and d shows the thresholded images of U46 flip chip of 0.8mm HASL thick circuit board assembly. Note: The U46 flip chip was the first chip that came off from the 0.8mm board during the thermal test after 88cycles. This shows that the solder joints at U46 flip chip of 0.8mm HASL board has a low level of reliability during the thermal test.


Solder joint
ROI
C0
C4
C8
C12
C16
C20
C28
C32
C36
C40
C44
C48
C52
C56
C60
C64
C68
C72
C76
C80
C84
C88

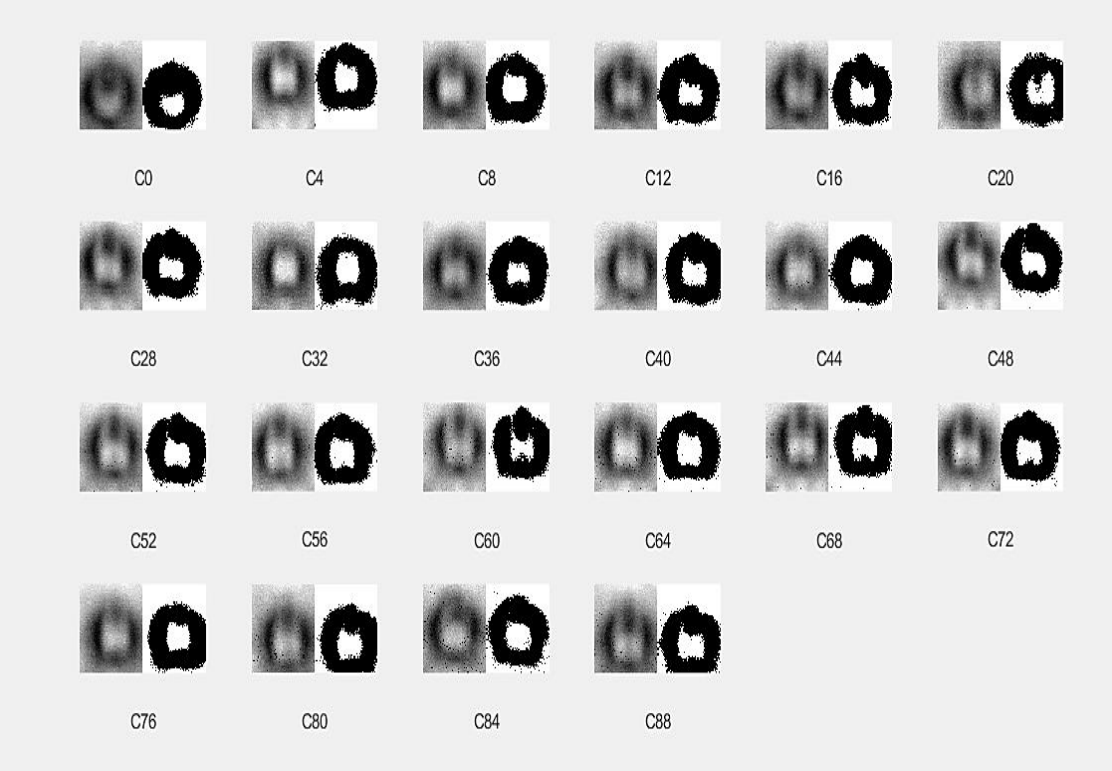
(a)


C0
C4
C8
C12
C16
C20
C28
C32
C36
C40
C44
C48
C52
C56
C60
C64
C68
C72
C76
C80
84
C88

(b)


C0
C4
C8
C12
C16
C20
C28
C32
C36
C40
C44
C48
C52
C56
C60
C64
C68
C72
C76
C80
C84
C88

(c)



(d)

Figure 6-7: Variations of joint numbers a) 64, b) 44 c) 95 and d) 17 of U46 Flip chip, on 0.8mm board at different Thermal Cycling test cycles

In order to facilitate image segmentation after the first step, the next step is to eliminate the black spots on the extracted solder joints that could contribute negatively to the performance analysis of the joints; this could be termed as the cleaning stage. Figure 6-7, shows that the extracted solder joints are composed of regions of interest with black inner spots. The black spots inside those images are the result of small pits in the solder. These black holes in the ROI were mended by using region filling, so that all the ROI can be extracted from the background more correctly.

Thus far, the regions of interest of the solder joints have been extracted using segmentation, closed or open holes as illustrated by Somasundaram. K., et al, (2010), could occur on those acquired solder joints after image segmentation, because of the shape of those joints. This happens because the solder joint has passed through various TC conditions. Likewise, those holes can be more confusing when analyzing the

performance of those joints during thermal tests. Therefore, dilation and erosion of morphology was used to eliminate those holes as shown in Equation 6-5 and 6-6. According to Sreedhar et al., (2012), dilation of A by the structuring element B that defines the neighbourhood of the pixel of interest is expressed by:

$$A \oplus B = \underset{b \in B}{U} A_b \qquad \text{Eq.6-5}$$

The dilation function assigns a value of the corresponding pixel in the output image. In a binary image, if any of the pixels is set to the value one, the output pixel is set to one. While the erosion of the binary image of A by the structuring element B according to Sreedhar et al., (2012), can be expressed using the equation 6-6

$$A ! \ B = \left\{ z \in E \middle| B_{=} \subseteq A \right\} \qquad \text{Eq.6-6}$$

In a binary image, if any of the pixels is set to zero the output pixel is set to zero. Furthermore, the region filling was applied after the elimination process to mend and close those spots. These techniques are based on a set of complementation, dilation and intersections (Gonzalez et al., 2002). Gonzalez further illustrated that the centroid of the region usually describes the contents (or focus points) which are surrounded by a boundary, which is referred to as the region's contour. This was carried out by using a built-in library function from the MATLAB image processing toolbox. Thus, the main contour function of bwlabel was also implemented in MATLAB that labels all the contours in the images and compared and finds the area of the largest contour in the images. It is of note from previous research (Pande Ankita 2013) that contour also known as border, is a kind of technique in image processing, that is applied to digital images in order to extract their boundary. This preprocessing technique according to Pande Ankita (2013) was performed on the acquired solder joints images in this study, in order to extract significant information about their general shape after going through different thermal cycling tests.

Based on this, a built-in function of region-props function command has been implemented in MATLAB that finds out the area of the joints. The calculation of region props done with MATLAB was performed using the Equation 6-7 (The math works Inc):

$$A_L = \frac{1}{S^2 F} \text{ [regionprops ('}I_L\text{, Centroid')]} \quad \text{Eq.6-7}$$

Where: S^2_F is the constant square of image xy- resolution and I_L the label image

Likewise, in order to find the maximum diameter of the Region of Interest in the solder joints, all the boundary points of ROI were determined using bwboundries command. The MATLAB Image processing function used for this purpose is shown in the equation 6-8 below:

$$C = [(y_c, x_c)] = \text{bwboundaries } (I_B, N_b) \quad \text{Eq.6-8}$$

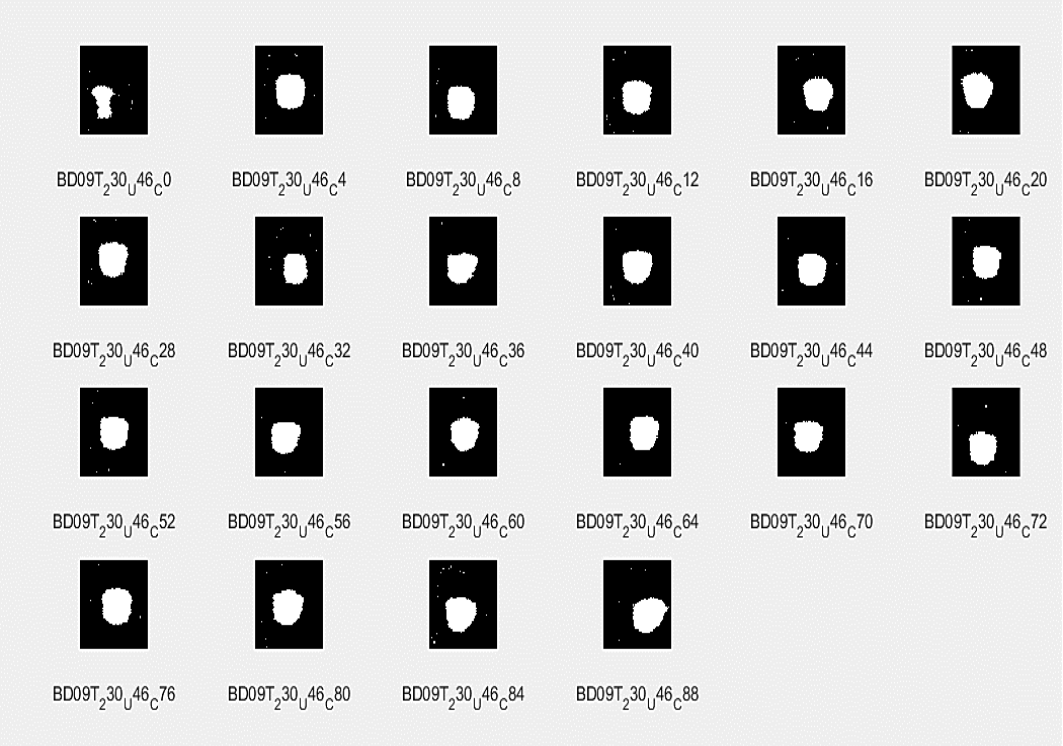
Which is defined by: C is the array of the contour points; I_B is the imfill, while N_b is the neighbour pixels (Joanna Sekulska et al, 2011). Nevertheless, contour smoothing was carried out in the closing process by applying the Elliptical Fourier Descriptors (EFD) in Equation 6-9 and 6-10 (Joanna Sekulska, 2011)

$$x'(c) = a_0 + \sum_{n=1}^{N} \left(a_n \cos \frac{2\pi nt}{T} + b_n \sin \frac{2\pi nt}{T} \right) \quad \text{Eq.6-9}$$

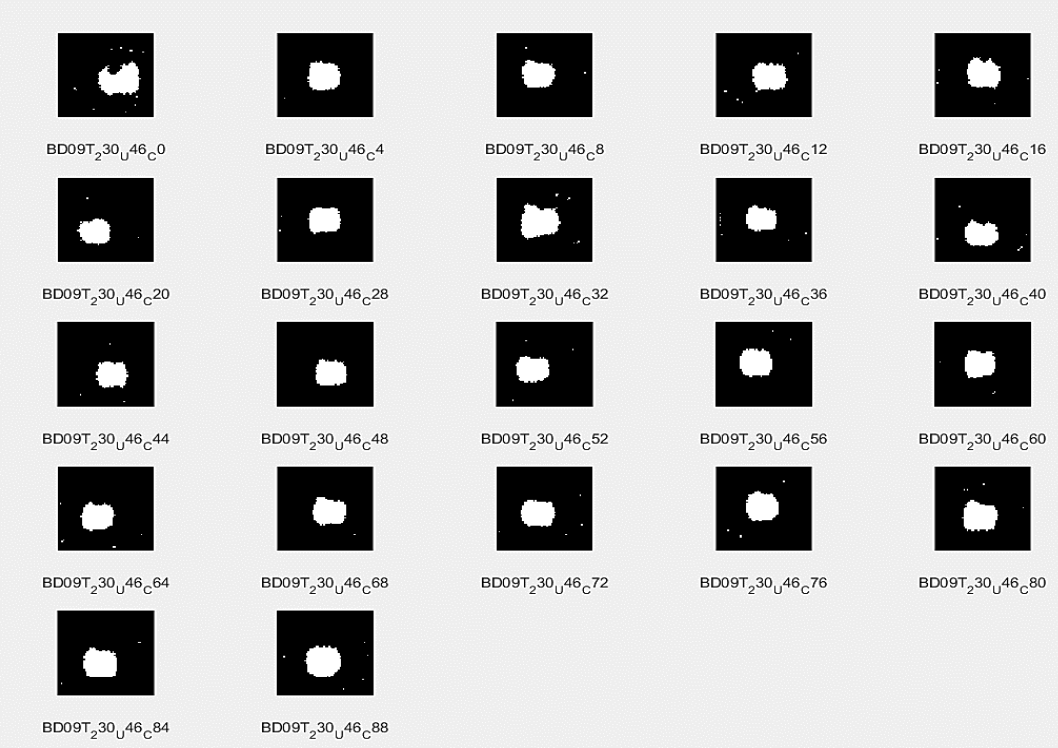
$$y'(c) = c_0 + \sum_{n=1}^{\infty} \left(c_n \cos \frac{2\pi nt}{T} + d_n \sin \frac{2\pi nt}{T} \right) \quad \text{Eq. 6-10}$$

Which is defined as 'T' is the number of steps required to traverse the entire contour in an image, while a, b, c and d *(n)* is the frequency coefficients to create a smooth boundary. The rules for calculating the values have been demonstrated in Neto et al., (2006). Where (t) is, the step needed to traverse pixel along the contour. Once the contour of a given pattern is extracted, its different characteristics will be further examined and used as features which also plays a key role in the measurement algorithm for geometrical classification. Therefore, correct extraction of the contour in those solder joints will produce more accurate image features, which will increase the chances of correctly classifying a given pattern.

However, in order to evaluate the variation in solder joints shape, a further analysis was carried out in this work. According to a reliability study conducted by Rahman, et al (2014) the quantity of solder paste and the soldering conditions could contribute to the irregularity of the shape of those solder joints during thermal cycling tests. In addition, "Imclearborder" is a function in MATLAB, that was also required in the image processing to search for the border and when it finds it, removes all the other structures connected to it. This gives a pixel value of one to the ROI in between and suppresses all the other values around the region. Further analysis of the region of interest in the acquired solder joints during the feature extraction phase, is shown in the Figures 6-8 a, b, c and d. These describe the elimination process by using region filling and also show every characteristic of what one could actually refer to as 'ROI's shape irregularity phase' where there are several ROI's shapes during the thermal excursions.



(a)


BD09T2 30U 46C 0
BD09T2 30U 46C 4
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BD09T2 30U 46C 12
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BD09T2 30U 46C 28
BD09T2 30U 46C 32
BD09T2 30U 46C 36
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BD09T2 30U 46C 44
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BD09T2 30U 46C 64
BD09T2 30U 46C 68
BD09T2 30U 46C 72
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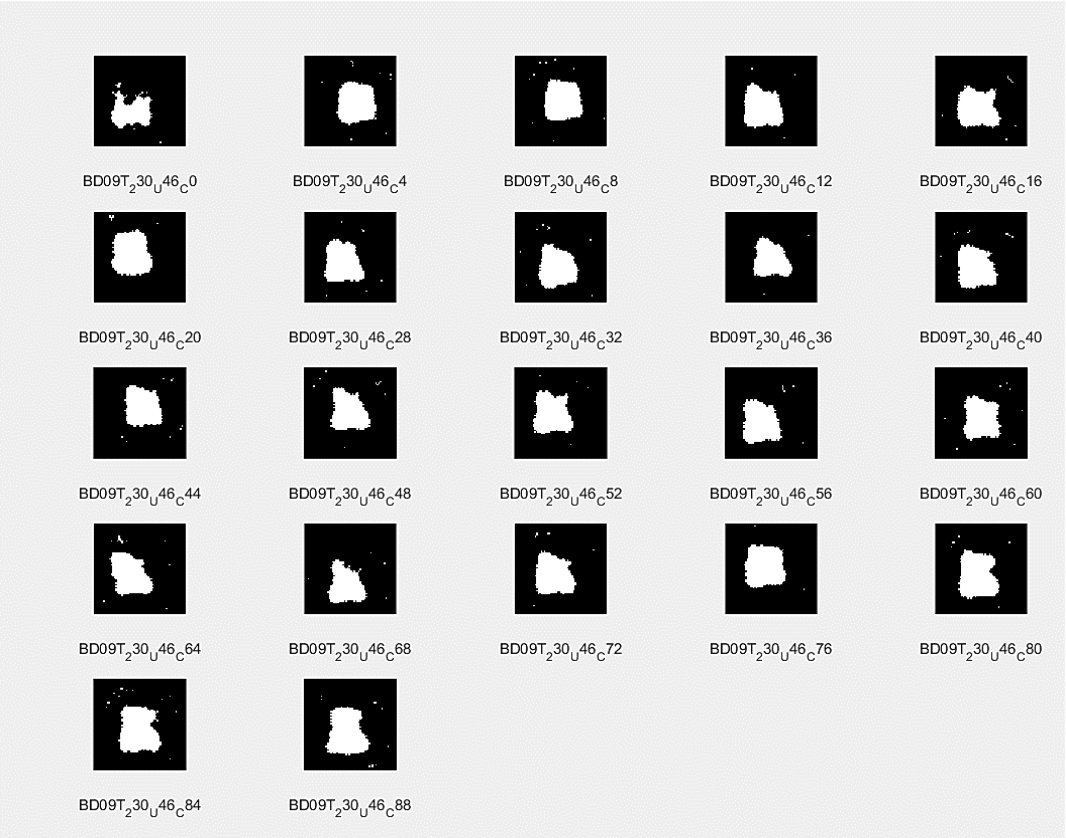
BD09T2 30U 46C 80
BD09T2 30U 46C 84
BD09T2 30U 46C 88

(b)


BD09T2 30U 46C 0
BD09T2 30U 46C 4
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BD09T2 30U 46C 64
BD09T2 30U 46C 68
BD09T2 30U 46C 72
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BD09T2 30U 46C 80
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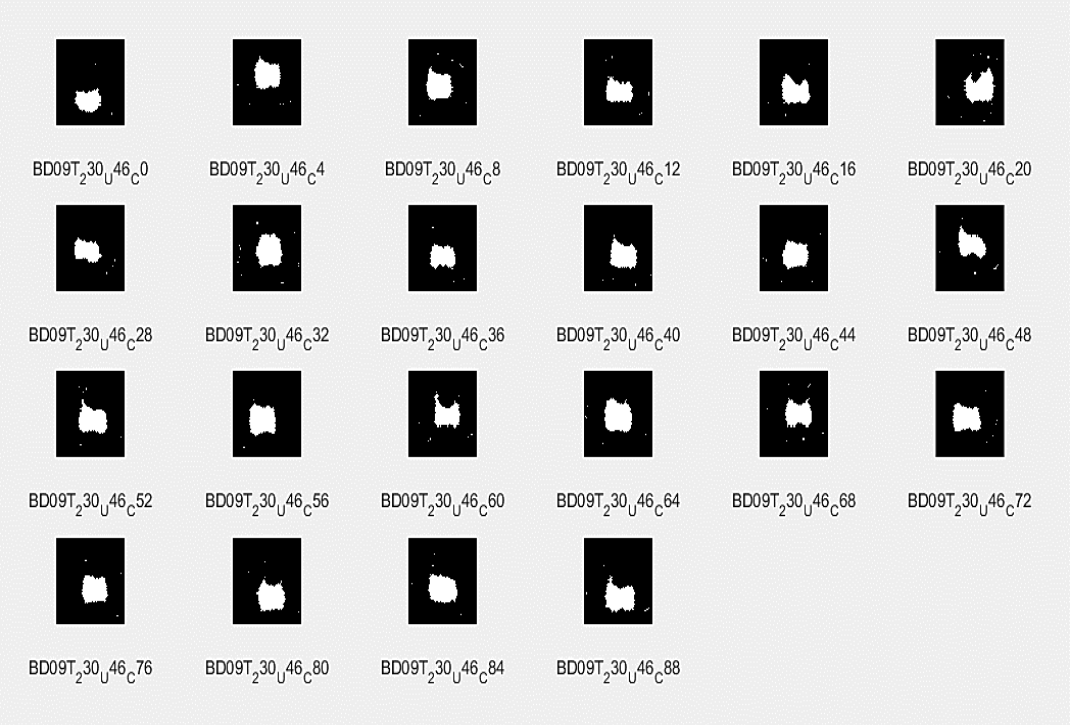
BD09T2 30U 46C 88

(c)



(d)

Figure 6-8: Different shape patterns Region of Interest of joints a) 64, b) 44 c) 95 and d) 17 of U46 Flip chip, 0.8mm board at different Thermal Cycling test cycles

Those images above disseminated the preprocessing carried out on the acquired solder joints images. The feature extraction techniques were applied to those images, which can efficiently remove the effect of reflection that occurs during the test while keeping all the properties of the acquired image constant. Thus far, it is noteworthy to know that the major cause of fatigue failure in the solder joints is the TC deformation of the joint by the stresses encountered during the ATC test combined with the CTE mismatch. These cause the fracture in the solder joints to propagate until complete discontinuity.

However, based on the discontinuities in the solder joints during the TC test, the shape and the width of the ROI exhibits phase segregation, which certainly reduces the joint geometry. This phenomenon is due to the concentration of stress at the centre of the joints. Thereby, the spatial shape of the particular region is considered as an important criterion for classification in this study.

Subsequently, since the solder joints under TC have no fixed shape, their features indicating the bonding quality such as intensity and area of the ROI's should be extracted and considered as the basis of the next feature classification process. Therefore, in order to achieve better accurate CDF curve of crack detection during this performance study, the extracted ROI's of the solder joints from those images above were further processed to determine the geometrical and time domain features of those joints.

Please note, for the segmentation images on 1.6mm PCB please refer to the appendices 3 in the CD at the back of the hard copy of the thesis.

6.3.1 Implementation of Watershed Based Image Segmentation Method in AAP

The aim of this section is to implement the watershed segmentation algorithm, on the acquired solder joints images. These type of techniques have been implemented in MATLAB to generate the segmentation output of those images.

These techniques were used for solving the image segmentation problem. Digabel and Lantuéjoul initially proposed this type of technique. However, Beucher and Lantuéjoul (1979) later expanded this technique to a more broad structure. Meyer et al, (1993) demonstrated in their research how the watershed transformation techniques could be applied to greyscale images. This makes an image easier to analyse in the image processing analysis. However, in this type of segmentation, which is the process of dividing images into regions according to their characteristics, the images have been scanned from the top to the right, to provide a complementary approach to the segmentation of objects. During this process, a unique label is given to each region detected by regional minima.

The watershed segmentation is always used to search for regions of high intensity gradients in an image (Salman et al, 2003*).* The techniques have mainly two classes. The first class is flooding based water algorithm, while the second class contains the rain falling water algorithms. The work of Pierre Soille and Luc M. Vincent, (1991), stresses the need for improved understanding as stated in other literature, which involves segmenting greyscale images using flooding simulations.

By considering the sample image as a topographic surface, which could be ed peaks and valleys, respectively in topographical terms (Thouray, 2014*),* the grayscale images of the

test samples were treated as a 3D array. The first and second ordinates represent the pixel's position, and the third ordinate represents the change in thermal cycling of the ROI. Figure 6-9 below describe the watershed segmentation of the joints in Figure 4-10 .These algorithms are based on sorting out pixels in increasing orders of their grey values around the ROI, followed by the flooding step consisting of a fast breath-first scanning of all pixels in order of their grey levels.

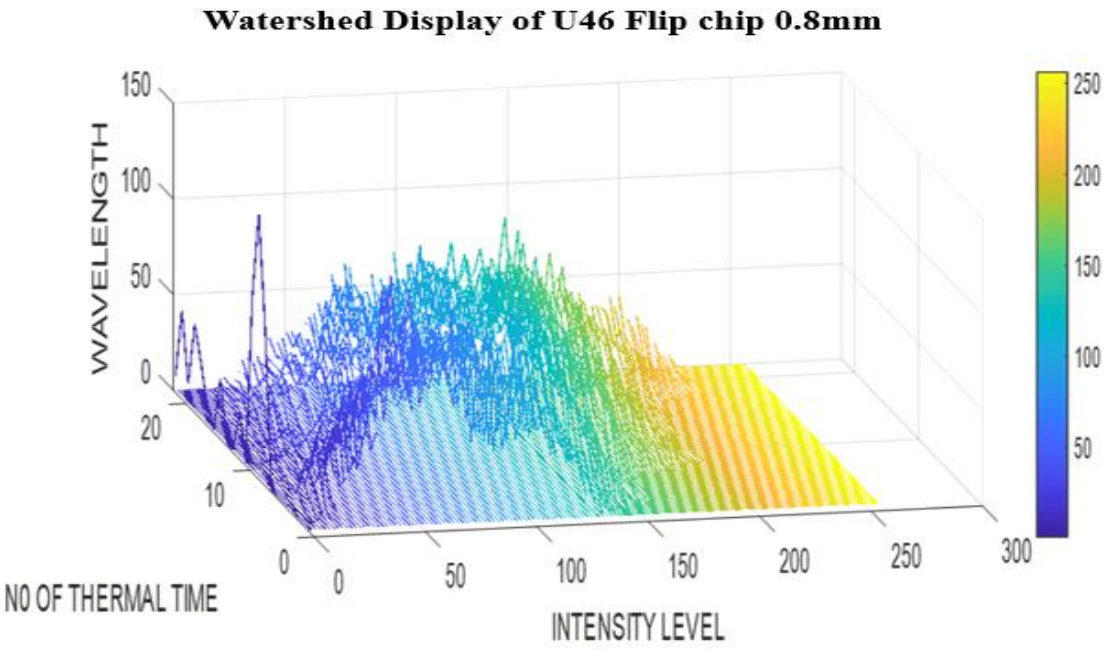


Figure 6-9: Watershed Segmented images of solder joint on U46 flip chip of 0.8mm board

Watershed segmentation in Figure 6-9 and 6-10 is depicted by interpreting the intensity of the scanned AMI image as a landscape. This segmentation process deals with and help to differentiate the propagation of the intensity in the ROI. As the thermal cycle increases, the pattern of the intensity distribution of the watershed graph changes.

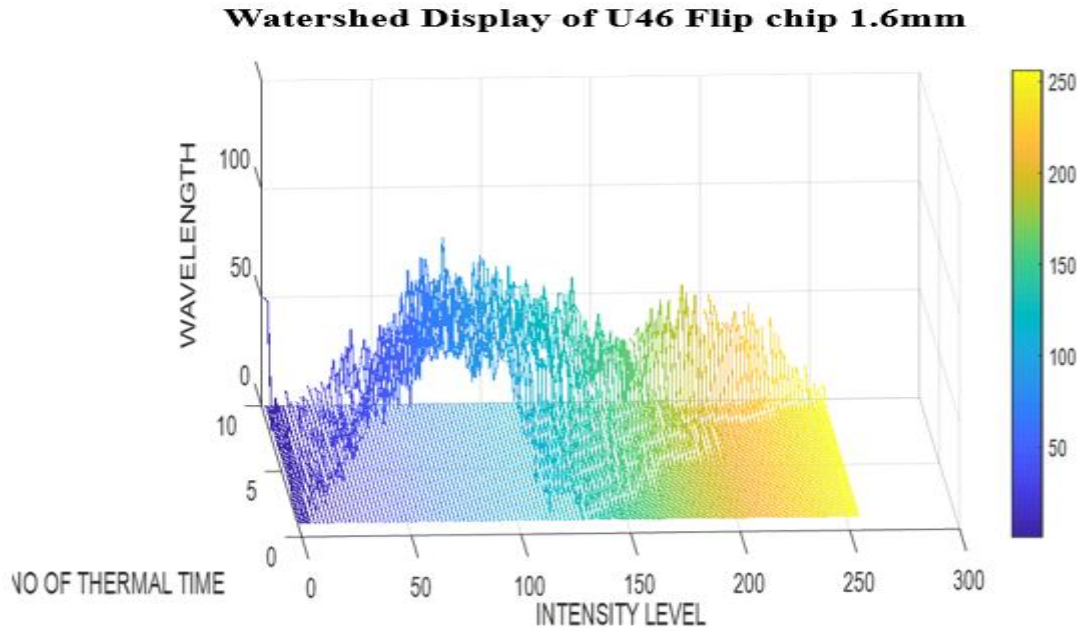


Figure 6-10: Segmented image of ROI in solder joint number 9 of 1.6mm board by watershed technique

This type of technique has also provided a good match to differentiate and analyse the acquired solder joint images of 0.8mm and 1.6mm HASL boards. Furthermore, the merit of using this kind of method is that it enables us to extract the ROI's and analyse them,

The segmentation results show that the proposed approach can monitor and estimate the increase in the intensity of the region of interest of solder joints on area array packaging. With several experimental studies in this research work, it was concluded that the high intensity in the area of ROI's of the joint images, could describe the solder joint failure rates.

6.4 Results from Feature Extraction on the reliability study of solder joints

In this section, the next phase of using feature extraction is to be able to analyse and detect any solder joints' delamination encountered during the TC test, which could affect the performance of the board during mission life.

From previous research as mentioned earlier, it has been noted that the physics of failure reliability method alone does not provide adequate failure data information needed on the AAP (Adithya Thaduri, 2012). Thus, using other techniques in assessing the performance

of solder joints could also contribute to its reliability. Some of this includes the through-life monitoring of the solder joints. Hence, using image feature extraction to extract distinctive characteristics of those solder joints after the inspection could give crucial information on the fatigue degradation. A feature in this case is termed a data representation that describes the structure of an image, which is represented by area, shape, intensity level, histograms etc.

Nevertheless, applying feature extraction on those solder joints will adequately improve the effectiveness of the reliability prediction on the performance of those joints. Thus, in order to improve the processing techniques, this section examines how a new feature extraction technique was demonstrated, designed and implemented to measure the properties of the solder joints to achieve a better performance analysis.

Thus far, the preprocessing solder joints data acquired after the image segmentation process, describe that there may still be many solder joints images that appear as delamination or crack. In order to differentiate between the healthy joints and fractured joints, feature extraction methods become the major problem to be solved. Thus, using some feature extraction methods like geometrical and time domain features, the reliability and performance analysis of those solder joints can be studied and the graphical analysis results can be generated.

The selected geometrical feature extraction method is proposed to perceive the differences between the area and form factor of both the healthy joint and fractured joints. Likewise, the time domain feature extraction method is also proposed by using standard deviation as a criterion for describing and analysing the degree of irregularity of an ROI's shape during various TC tests. The sections below elaborate more on the features extraction which have been used.

6.4.1 Geometrical Features Extraction

Images could be represented by various forms, but robust representation must maintain the features that describe the images and enable further analysis and decision-making (Faraq, 2014). As the solder joints images may not have a specific geometric description during the validation test, the image features in the acquired AMI images may not be easy to specify. Thus far, physical observations after reviewing the variations observed in

those solder joints images, showed that the image data sets should be analysed to generate linear crack growth rates at each thermal cycling test using geometrical features. Meanwhile, it is paramount to investigate the area of the crack length in the ROI in the first place to find a primary expression for the fatigue degradation rate in the joints.

Geometrical features extraction in this stage provide critical information about shape and other features of the acquired images like the root cause time analysis. By implementing this feature extraction methodology and in order to find specific features, the complete image processing is done by using MATLAB.

From the previous work carried out by Braden, (2012), it was reported that those joints are spherical and the UBM is circular in shape, it is reasonable to simplify the crack plane surface to a circle, but ROI's in those solder joints are not perfectly round in shape. Thereby to find the level of defect in those images we need to find and calculate the area of the ROI's.

6.4.2 Calculation of an area in the solder joints images

As describe in chapter 3 earlier, each flip chips consists of 109 solder joints. The solder joints are at different locations on the flip chips of the test samples and they all behaved differently during the validation test, thus depicting various characteristics in the graphical results as show in Figure 6-10. From the validation test conducted in this performance study, it is noted that the thermal strain on those solder joints was related to the coefficient thermal expansion (CTE) which is mainly dependent on the distance of the solder joints to neutral point by using the Equation 6-11 (Clech et al., 2009). This is because of the shear and strain forces applied on solder joints during the thermal cycling test. Thus, taking the position of solder joints on the flip chips and their relationship to the neutral point as a factor and important parameter to consider when determining the cycle to failure during the performance test, eight solder joints were selected and divided into various group for further analysis.

$$C = A_1 \cdot \frac{1}{L\Delta\alpha} \cdot \frac{1}{h^m} \cdot \left(\frac{A}{K}\right)^{1+m} \qquad \text{Eq. 6.11}$$

Where: C is the coefficient calculated from the component assembly, h is the stand-off height, K is the assembly stiffness, A is defined as solder joint area, $\Delta\alpha$ is the board to component coefficient thermal expansion mismatch, L is the largest distance to neutral point and A_1 is defined as the solder-dependent creep constants. From the equation 6-11 above, it is shown that the crack area of the solder joints on those packages is one of the paramount factors to estimate the CTE.

The selected solder joints in Figure 6-1 are eight in number and divide into three groups namely, Joint 29, 9 and 64 is one group, which are located at the middle of the flip chip assembly and is almost symmetrical to the neutral points. Joints 95 and 107 are grouped together since they are the single joints in the centre of the flip chip and symmetrical to the neutral point. The third group included in this performance study are 17, 44, and 74 since they are symmetrical to the neutral point and have very good positioning (located at the middle) on the flip chips.

Furthermore, the ability to measure the area of the ROI's, which are considered the grey region in those solder joint images as shown in Figure 5-10 , is an important feature for evaluating the levels of delamination or cracks in solder joints. The extracted area measurement of the solder joints on different test samples will be used alongside the form factor to provide spatial information of the crack initiation and crack propagation to failure.

To start the Feature extraction process, firstly, the standard of judging whether a particular solder joints belongs to healthy, partial fractured or fractured joints in this research work should be determined. To my knowledge concerning the through-life monitoring of solder joint under TC test, the solder joints defect area is made through assumptions as there is no efficient method to actually define and measure the crack initiation and propagation time, in relation to the study carried out by Yang, (2012). Therefore, in order to verify the fatigue degradation on the solder joints under the flip chips of two different test samples of 0.8mm and 1.6mm HASL board, the following

steps apply: (1) the extracted solder joint crack area increases significantly as the TC increases; (2) the form factor is less than 0.5; (3) has a low standard deviation.

However, the lifetime of the selected solder joints are determined by how the crack propagates as a result of cracking mechanisms. In this case, fractured mechanics-based models play an important role in characterizing the solder joints' behaviour and can lead to the formulation of the reliability prediction of those joints. These mechanics fatigue models are based on the principle of defects existing in any solder joint and having the ability to form a nucleation site. From this, a crack may propagate through the solder joints area during the application of an applied stress, in this case thermal cycling.

It is of note that the solder joints' life predictions under thermal cycling tests can therefore be derived from characterising crack propagation behaviour through stressed materials as a function of time geometry and environmental conditions as suggested by Liu (Liu, 2001). Thus, the propagation of the crack and growth rate through any stressed material is a function of time, interconnect geometry and the applied environmental conditions. A basic velocity equation cited by Liu, (2001) is given in equation 6.12

$$\frac{da}{dt} = B(Y\sigma\sqrt{\pi a})^n \qquad \text{Eq.6.12}$$

In this case a is the crack length, *a* is the applied stress, Y is an interconnect geometry parameter, *B* and *n* are empirical constants which are thermally dependent.

The rate of cracking can be correlated with the ATC parameters as stated in the literature by the Paris-Erdogan equation. Hence, based on the graphical results in Figure 6-10, the crack initiation time, crack propagation time and failed time of the selected solder joints on those flip chips relate to the crack length propagation per cycle and were estimated using Paris Law in Equation 6.13 (Branco et al., 2008), which actually measures the crack propagation as a function of thermal stress.

$$\frac{da}{dN} = C\Delta k^m \qquad \text{Eq. 6.13}$$

Where ΔK is the range of the stress intensity factor, and C and m constants that depend on the stress ratio and temperature. According to Branco et al., (2008), it has been found that the stress intensity ratio can be defined as in equation 6.14.

$$R = \frac{K\ min}{K\ max} \qquad \text{Eq.6.14}$$

It is noted that the failure in those solder joints during thermal cycling tests always begins at one of these high stress points at the corner joints as illustrated from the image which shows the preferred stress locations on those joints in Figure 4-10. For example, consider a flaw with increases in the intensity of the solder joints in Figure 4-10 that grows with ATC time. This indicates that once a defect or crack is formed due to the fracture mechanism, the applied stress on the solder joints on those packages due to thermal cycling acts as a driving force to propagate the crack in those joints until a catastrophic failure occurs.

Based on this mechanism of crack nucleation, the solder joints named in Figure 6-1 above were used as an example throughout the solder joints' reliability studies respectively. From Figure 6-11, it is shown clearly that the area of the fractured solder joints rapidly increases compared to the healthy joints. It is noted that the area of the ROI increased via a rise in the thermal cycling due to the presence of a crack and completely failed on the flip chip by joint separation or when the joint reaches a particular thermal cycle. However, given the failure criterion, the thermal fatigue life of the solder joint subjected to stress from the first set of the results in Figure 6-11, was predicted using the equation 6-13. Hence, based on the analyzed results from Figure 6-13, that identified different types of joints, statistical analysis was also done in the depicted results on area of the joints to observe the statistical behavior with increase in thermal cycling.

This indicates that the solder joint in Figure 6-11 begins to fail on U23 flip chip of 0.8mm HASL board for joint 9 around 60 cycles, joint 29 around 70 cycle while for joints 64 around 56 cycles and then fails completely at 200 Thermal cycling. It has been observed that crack initiation and propagation time are about 65% and 35% in joint number 9, likewise 40% to 60 % in joint number 29 and finally, 29% to 61% in joint number 64 of the total fatigue lifetime, respectively.

Nevertheless, the plot of a fractured solder joint in Figure 6-11 generated a sharp jump when cracks are present compare to the healthy joints due to the present of defects. Which indicates that the higher the increase rate in the crack area, the higher the failure rate, since a lower contact area is left during the TC test and due to the crack area propagation phase.

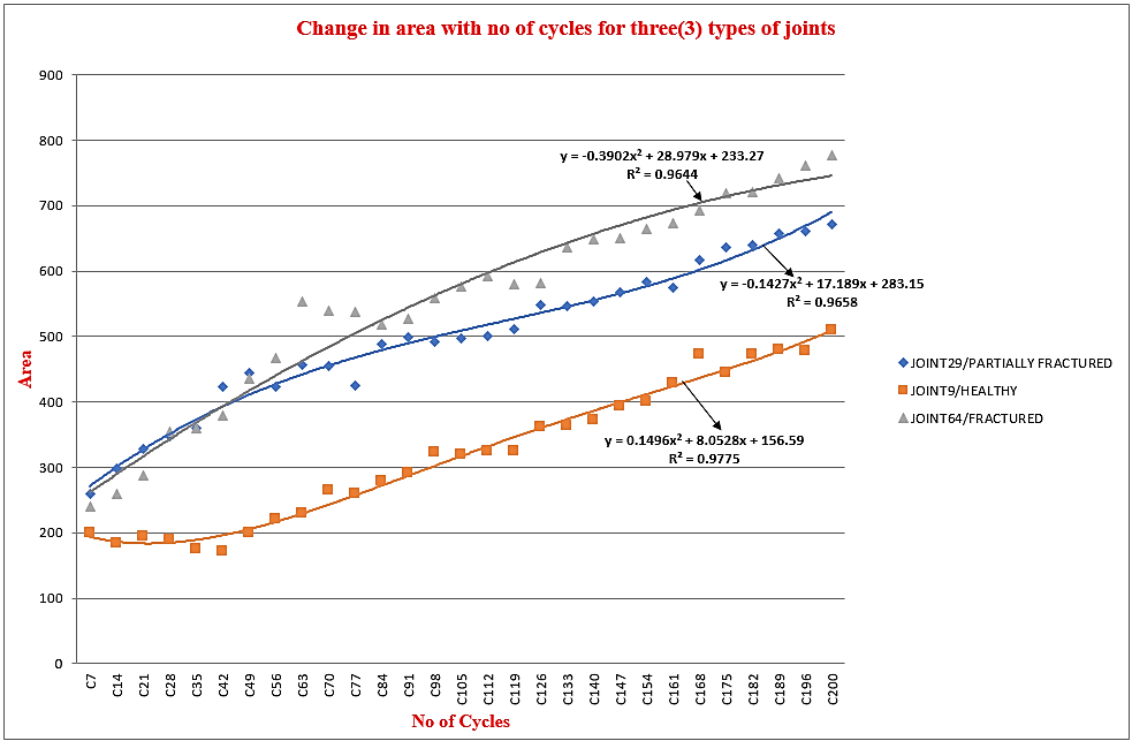


Figure 6-11: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 0.8mm board for Joint number 29, 9 and 64

Furthermore, the resulting graphs in Figure 6-12 to 6-13, also illustrates the failure modes in the extracted area of different types of joints on the flip chip at every thermal cycle of 0.8mm substrate thickness board. However, individual graph analysis was also drawn to make some conclusion about the solder joints' performance. Thus, the selected fractured joints in Figure 6-12 have different area value due to the position of each joint on the flip chips, which makes the crack area of those joints increase and proportionally to increase in thermal cycling. The generation of failure in solder joint based on fractured

mechanisms in Figure 6-12 to 6-13 was divided into various stages, which are the crack initiation, crack propagation and the failed using Equation 6.13, which could help analyse and provide certain parameters affecting the joints. The second set of results in Figure 6-12, depicted two solder joints' graphical results. The two solder joints are at different locations on the flip chips. Thus, from the results it is of note that there is a highly significant difference in the behaviour of the solder joints under thermal cycling tests. Based on the failure criterion, cracks begins to initiate in Figure 6-12 around 91 cycles in joint number 95, while they begin to initiate in joint 107 at 70 thermal cycling. It is noteworthy that the total life of solder joints on the flip chips on both test samples at different locations are not the same. The average total fatigue life of those solder joints is about 200 cycles, which is the total number of thermal cycling tests that the flip chip experiences before failure. From the results depicted in Figure 6-12 , the major difference between the thermal fatigue behaviours of those selected solder joints is the ratio in the crack area propagation to the overall fatigue life. The averages of the crack area for crack initiation and propagation times on 0.8mm board thickness of non-underfilled solder joints are about 40% and 60% in joint number 95, likewise 60% to 40 % in joint number 107 of the total fatigue lifetime, respectively.

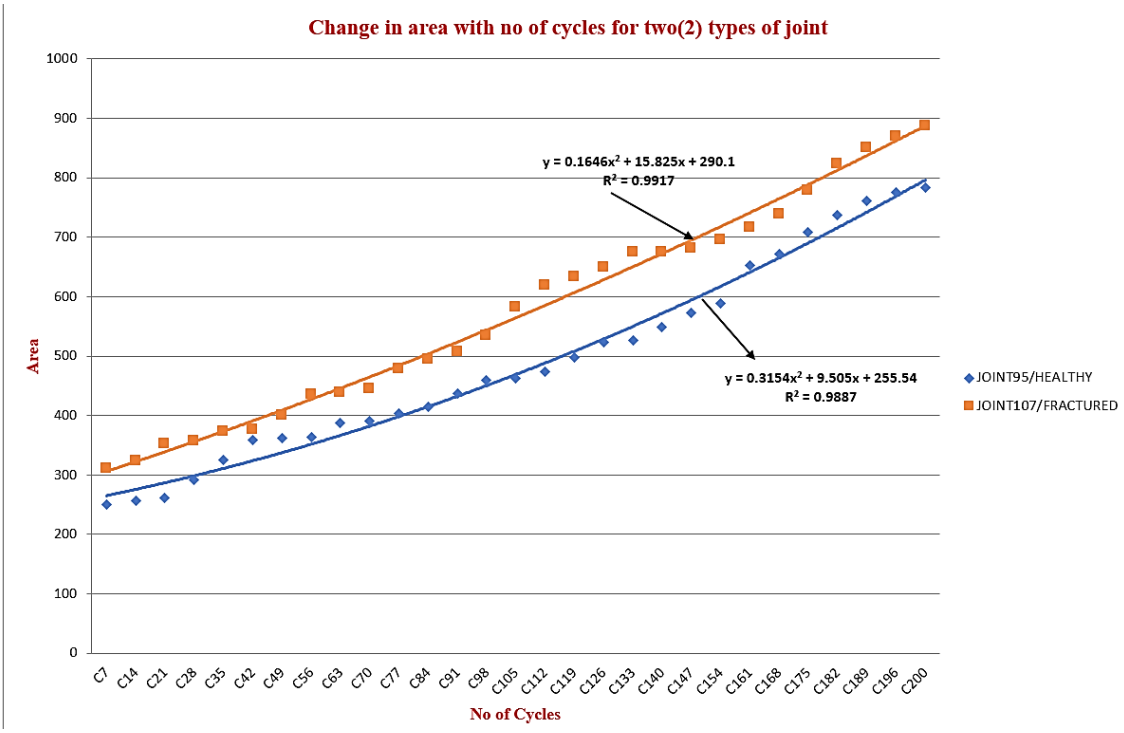


Figure 6-12: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 0.8mm board for Joint number 95 and 107

The third set of results in Figure 6-13, depicted three solder joints graphical results. The two solder joints are at different locations on the flip chips of 0.8mm board. Thus, the crack area in Figure 6-13 also indicates that there is a large crack area in joint number 44, but lower crack area in the 17 joint. The total average of the fatigue life of those solder joints without under fill is 200 cycles also. It is of note that there is much difference in the area size of those joints, once the area increases to a certain point as the flip chips failed. However, it is depicted from the results that joint area propagation time is more than the initiation time. Hence, the results based on the fatigue life of those solder joints can also be evaluated using the crack area size. It is noted that when the cracks in the solder joints grow to a critical size then fractured occur. Based on the failure criterion in equation 6-8, the initiation time and the propagation time of those three selected solder joints are about 35% to 65% in joint number 17, 60% and 40% in joint number 44, finally 50% to 50 % in joint number 74 of the total fatigue life of those joints. Based on the

graphical results depicted in Figure 6-12 to 6-13, the calculation of the area of the solder joints can be used to verify the fatigue degradation of the solder joints under thermal cycling tests.

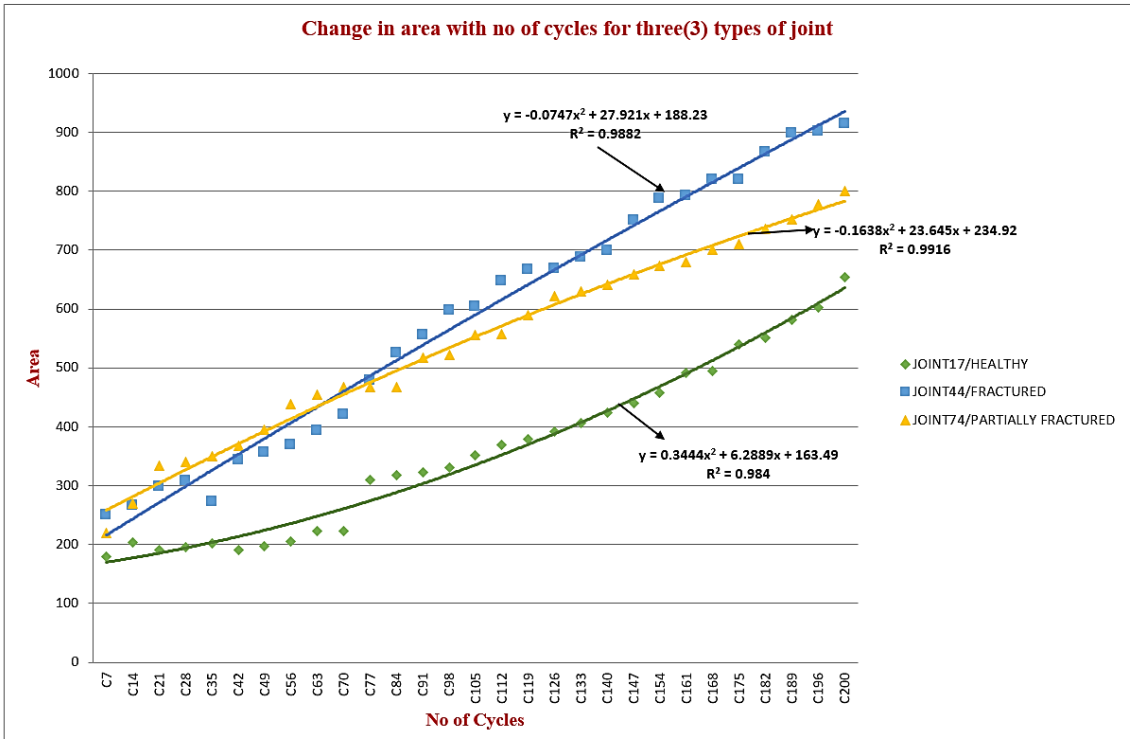


Figure 6-13: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 0.8mm board for Joint numbers 17, 44 and 74.

6.4.3 Results of solder joint area in 1.6mm HASL Board

In the reliability evaluation, the temperature cycling analysis on Board 10 with 1.6mm substrate thickness was used to study the performance of solder joints under thermal cycling tests. The data was collected by performing the feature extraction technique on the same joints used in 0.8mm board and plotting the crack area in an intuitive meaningful way, as shown in Figure 6-14 to Figure 6-15. Hence, given a failure criterion as illustrated

in equation 6-8, the thermal fatigue life of the solder joints subjected to thermal stress can be predicted from the first set of results in Figure 6-14 using the fracture mechanisms.

The graphical results show that the area begins to increase dramatically in joint number 64 around 70 thermal cycles, while in joint number 9 around 105 cycles. However, at 125 cycles, joint number 29 begins to increase in crack area. This also indicates that the crack initiation time for 1.6mm is quite long compare to 0.8mm board. For comparison purposes, the total average of the fatigue life of those solder joints without under fill is 200 cycles for the selected joint of U23 flip chip on 1.6mm board. Furthermore, it is also noted from the validation test that it took so long for the 1.6mm board to fail. Thus, as shown from the results from 0.8mm and 1.6mm, the joint number 64 is still the fractured joints on both boards due to the higher stress displacement around the location of the joint. Thus, the average increases in area of those selected joints based on initiation and propagation are about 65% and 35% in joint number 29, 40% and 60 % in joints number 64, finally 55% and 45% in joint number 9 of the total average of the lifetime respectively. The figure 6-14 illustrates the results for board number 10 ten U23 flip chip

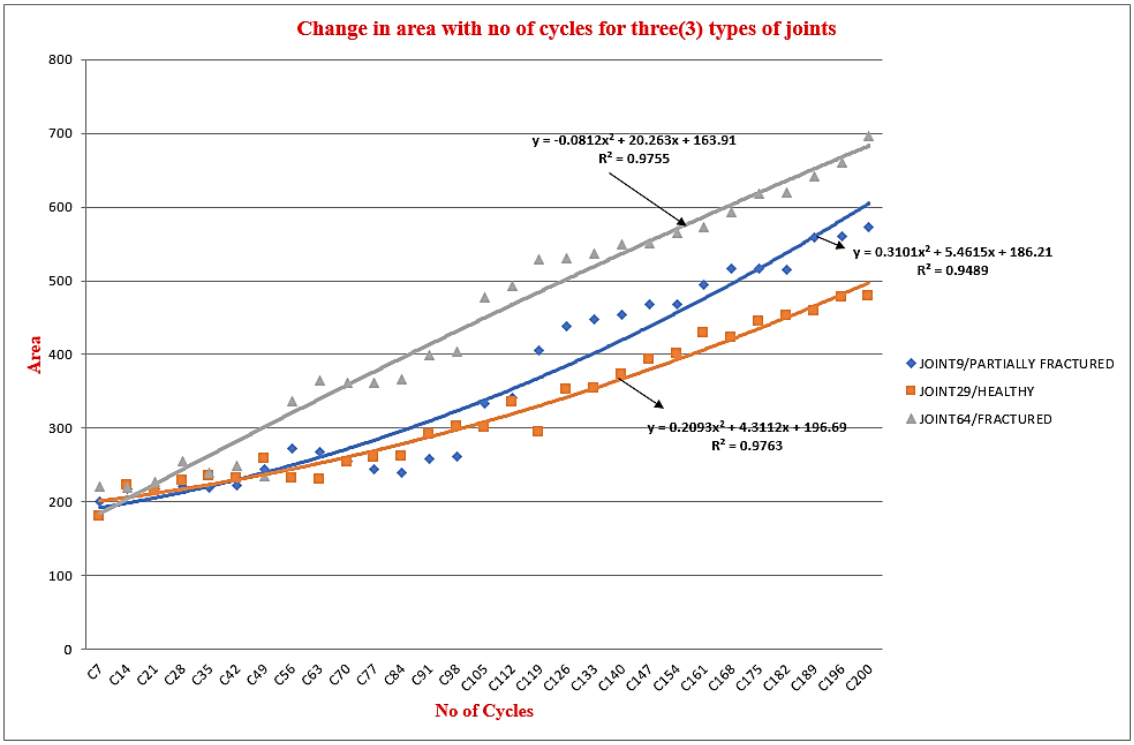


Figure 6-14: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 1.6mm board for Joint number 29, 9 and 64.

The second set of this extraction analysis has two solder joints at different locations on the flip chip. Considering the solder joints' location and their distance from the neutral point, joint 95 and 107 are in one group in Figure 6-15. It is of note that the area begins to increase as the thermal cycling increases. Likewise, the propagation rate on both selected joints are almost at the same rate. However, the average increase in area of those selected joints based on initiation and propagation are about 45% and 55% in joint number 95 and 60% to 40 % in joint number 107 of the total average of their lifetime respectively.

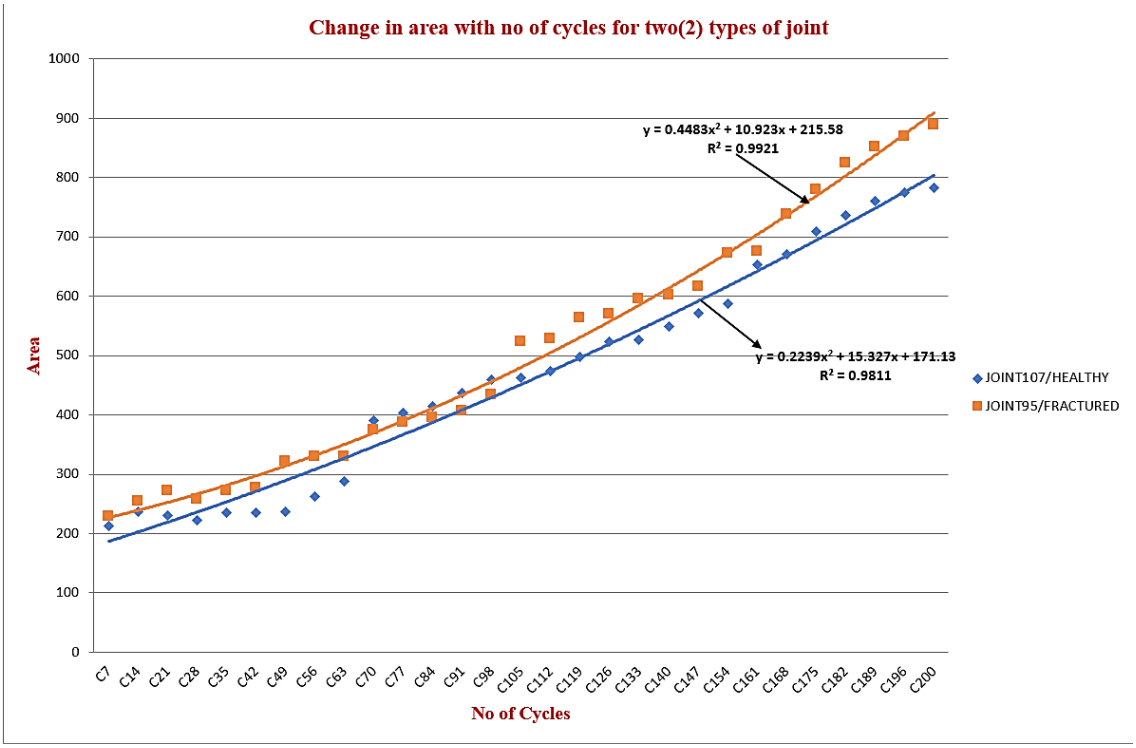


Figure 6-15: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 1.6mm board for Joint number 95 and 107.

The third set on 1.6mm board compute three solder joint area analysis. Figure 6-16, shows the crack area of the number 17 , 44 and 74 in 1.6mm board, from the graphical results, as discussed earlier that increase in the area is due to crack formation or growth in those solder joints. From this we can summarise that the crack initiates at 84 thermal cycles for joint 74, while in joint number 44 the crack initiates around that 98 thermal cycles and also in joint number 17 the crack initiates at 119 cycles. However, the average increase in area of those selected joints based on initiation and propagation based on the failure mechanisms are about 70% and 30% in joint number 17, 55% to 45 % in joint number 44 and lastly, 40% and 60% in joint number 74 of the total average of their lifetime respectively.

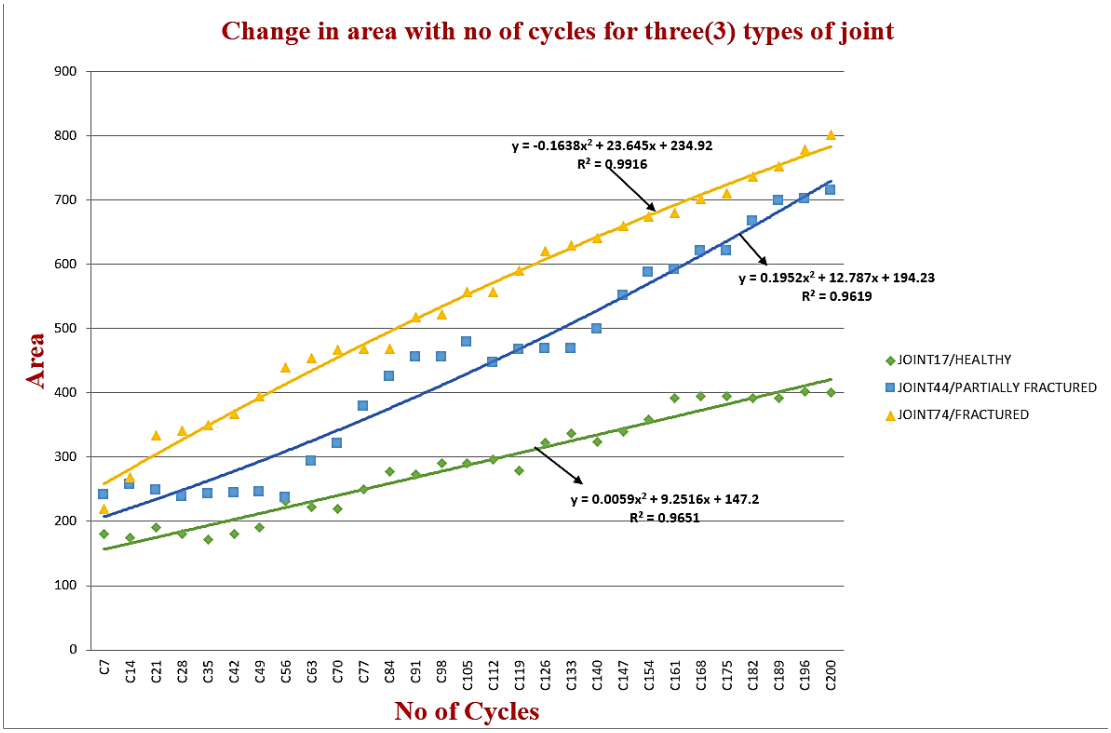


Figure 6-16: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U23 flip chip on 1.6mm board for Joint number 17, 44 and 74.

6.4.4 Results of solder joints area on 0.8mm Board BD09 U46 Flip chip.

The U46 flip chip on 0.8mm board was the first chip that came off during the study of the performance of solder joint under TC test. It can be inferred that the rate of change in the crack area is quite different from others. Thus, from Figure 6-17 to 6-18, it is observed that the crack begins to initiate in joints number 29, 9 and 64 as thermal cycling increases.

However, the acquired acoustic images confirm that the rate of increase in intensity of those selected joints is dramatically high. However, at 88 thermal cycles the flip chip came off on the test sample during the validation test. Thus, the total average of the fatigue life of those solder joints without under fill is 88 cycles for this particular flip chip.

Furthermore, the graphical results during the performance analysis confirms that, the average increase in area of those selected joints based on initiation and propagation, are about 35% and 65% in joint number 9. Thus, 55% to 45 % in joint number 44 and lastly, 42% and 58% in joint number 64 and 40% to 60% in joints number 29, of the total average of their lifetime respectively.

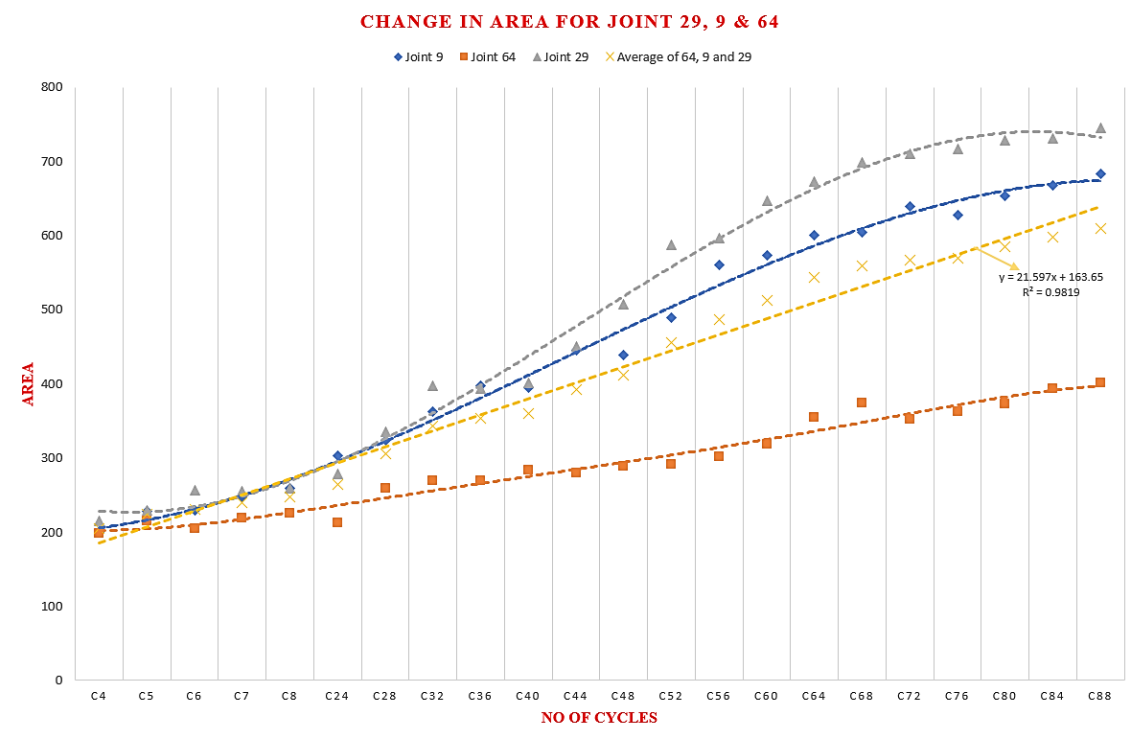


Figure 6-17: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles for U46 flip chip of 0.8mm board for Joint number 29, 9 and 64.

Figure 6-18 shows the typical crack area increases of those selected non-underfilled solder joints during thermal cycling tests. The average fatigue life of the selected flip chip is 88 thermal cycles.

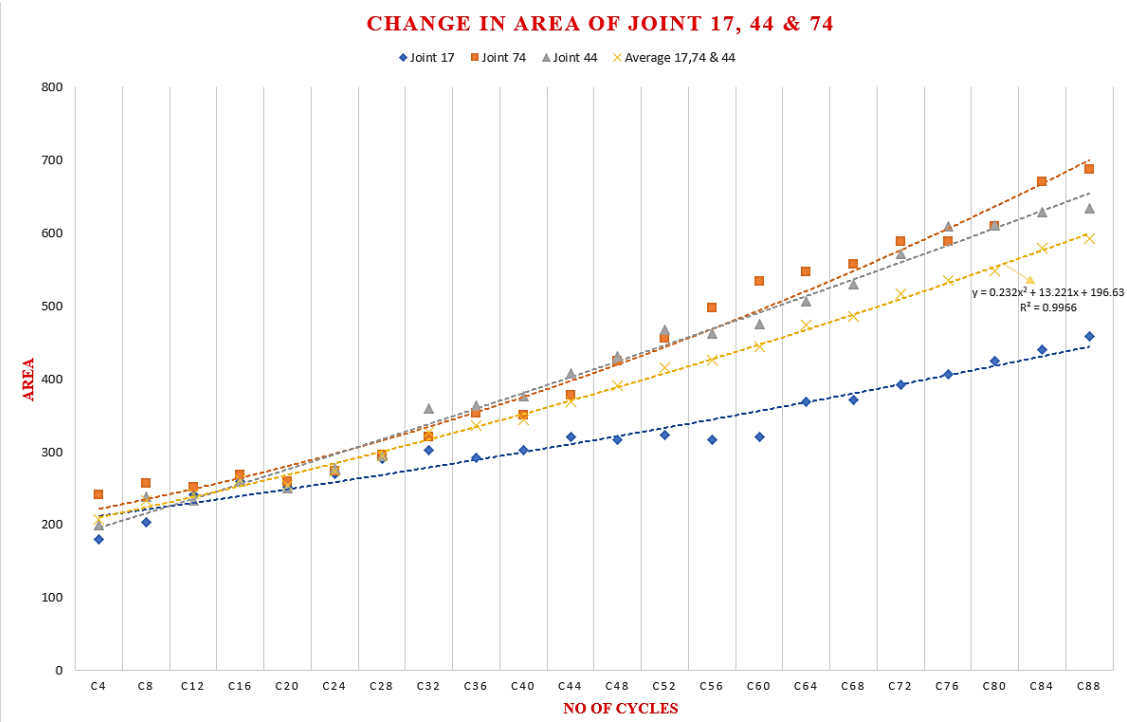


Figure 6-18: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U46 flip chip on 0.8mm board for Joint number 17, 44 and 74.

For comparison of results, the Figure 6-19 shows the area and the temperature-cycling curve for the selected solder joints 95 and 107. However, it is of note that the fatigue life of those joints during the TC test tends towards the same direction and almost similar, due to the locations of those joints on the flip chips. However, the average life of those solder joints is estimated to be 88 cycles. The increase and propagation in area of joint number 95 are 60% to 40 %, while joint number 107 are 35% to 65% of the average of the total lifetime of the flip chip respectively.

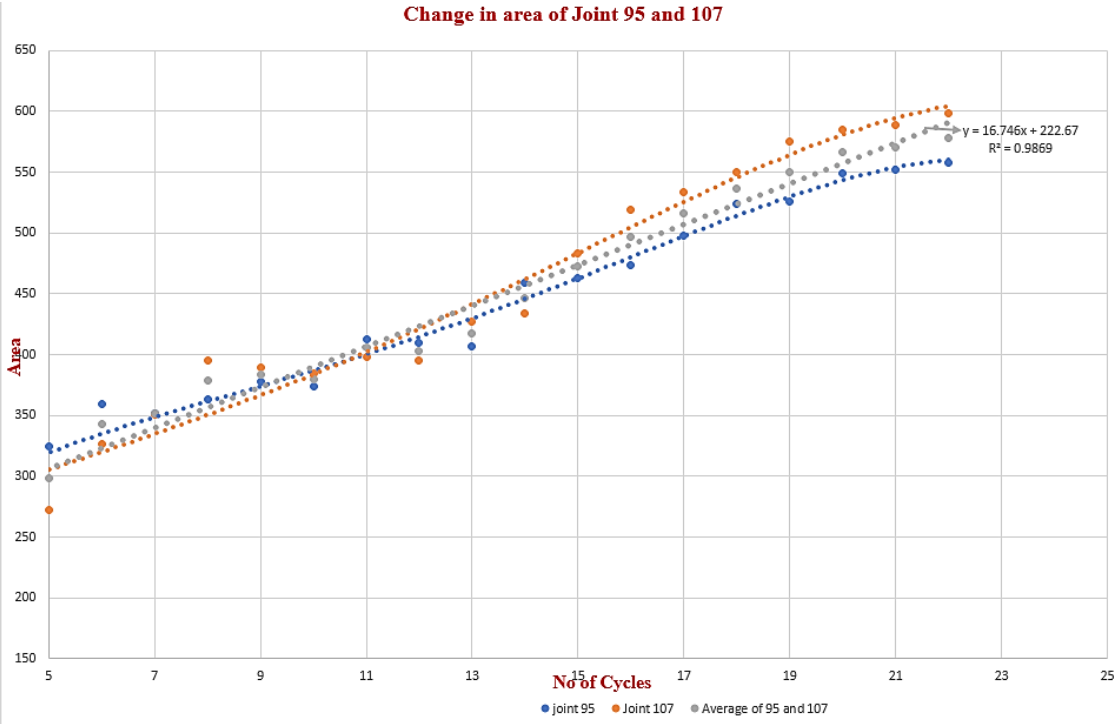


Figure 6-19: Area for healthy, partial fractured and fractured solder joints over number of thermal cycles of U46 flip chip on 0.8mm board for Joint number 95 and 107

6.4 Crack Area Summary

For solder joints in the area array packaging, differences in the coefficients of thermal expansion of the different materials in the electronic assembly and a changing thermal environment are known to be major factors for inducing strains. Defects or cracks form and propagate in those solder joints due to thermal fatigue as illustrated in this chapter, and this propagation rate is reported to be the main failure mechanism that affects solder joints' life. In this research study, the results indicate that continuous increase in the area values of those solder joints under thermal cycling tests demonstrates a decrease in the strength and performance of those joints, which led to the discontinuity of the flip chips on the test samples. Thus, from the graphical results, a failure crack area value is specific to each joint. Every joint having a different failure characteristic as illustrated in Figure 6-14 and Figure 6-21, when comparing the characteristics of the selected joint in Figure 6-1. A linear regression analysis was performed on all the area graphs. It is observed that

a strong correlation exists (R^2=0.98 to 0.99) in all the area graphs on 0.8mm and 1.6mm boards. It is noteworthy that some solder joints experience variations in crack area size as a results of the flip chip position on the AAP, interconnect geometry and manufacturing assembly. This is most noticeable for example on the corner joints. However, other factors such as the PCB thickness and the component population on the PCB could also influence the crack area size response of the joint under thermal cycling test. Comparing aging conditions, the differences in the propagation of % crack area for 0.8mm and 1.6mm HASL packages were statistically different.

6.5 Crack Evaluation using Form Factor in the Solder joints Images

In this evaluation study of solder joint, the purpose of this analysis is to demonstrate how the variation in region of interest shapes, rather than only the diameter, can affect the solder joints' life under thermal cycling tests. It was observed that the deformation of the region of interest (ROI) shape of the aged SnPb (Sn=52.9%, Pb=45.9%) joints in Figure 6-7 on both test samples of 0.8mm and 1.6mm were rather round. In order to carry out this evaluation study on how the ROI affects the solder joints' life, experimental results on the extracted region of interest have been analysed by using a new geometrical (form factor) feature extraction method, with the goal of improving the current understanding regarding the subject area and to determine the defect form factor value of each solder joints in the acquired ultrasound images. However, the analysis of the results has shown that the reliability of solder joints could be affected by variations in the solder joints' shapes during temperature cycling tests. It is of note that the bump is spherical and the under bump metallization for the flip chip packages is circular, it is rational to assume that the defect plane surface to a circle, from which the form factor of the ROI was calculated by using the Equation 6-7 in MATLAB software from Math works. Studies on the form factor feature extraction method has been successfully implemented in medicine to differentiate between a normal cell and a sickle cell in Figure 6-20. The form factor is computed using the equation 6-15 to determine whether the cell is sickle or not (Alotaibi, 2016). According to Alotaibi, the method of using a form factor to differentiate a cell is 90 percent more accurate than the existing method in medicines.

Figure 6-20: (a) and (b) Shows different shapes of cells (Alotaibi, 2016)

In other to account for the experimental data results, the acquired image data were correlated by using this kind of feature extraction method which characterizes and differentiates the shapes of the regions of interest on the solder joints images. The failure distribution pattern of the form factor methods is an important feature for evaluating the levels of deformity in the shape of those ROI's, since the ROI's are not perfectly round in shape under thermal cycling test. Nevertheless, this can be mainly understood when carefully considering the shape of the region of interest of the solder joints during thermal cycling in Figure 6-7 and 6-8.

Thus far, from the literature review in chapter 2, it is common knowledge in literature that in area array packaging, the coefficient thermal expansion difference causes the materials on the circuit board assembly to expand and contract at different rates, and when the thermal stress exceeds the break point of the solder joint, fatigue failure occurs, the fatigue could actually cause the shape of those ROI joints to deform. As stated in section 3, solder joint images were acquired during different thermal cycling test using an AMI machine. Hence, the shape geometry of the ROI in the acquired solder joints images can be determined by form factor method, which assumes that the ROI of solder joints are round without considering the effect of TC on it. The value of the form factor is calculated from the ROI's based on the deformations caused by these cycling test on the images that lead to various stress state in the joints. From the analysis results in Figure 6-23, conducting this type of feature extraction on solder joints has helped to observe the phenomenon that irregularity in the ROI's is mainly linked to solder joints as the TC increases.

The form factor operation is expressed by using Equation 6-7. Thus, this operation defines that the ROI have different degrees of roundness because they appear

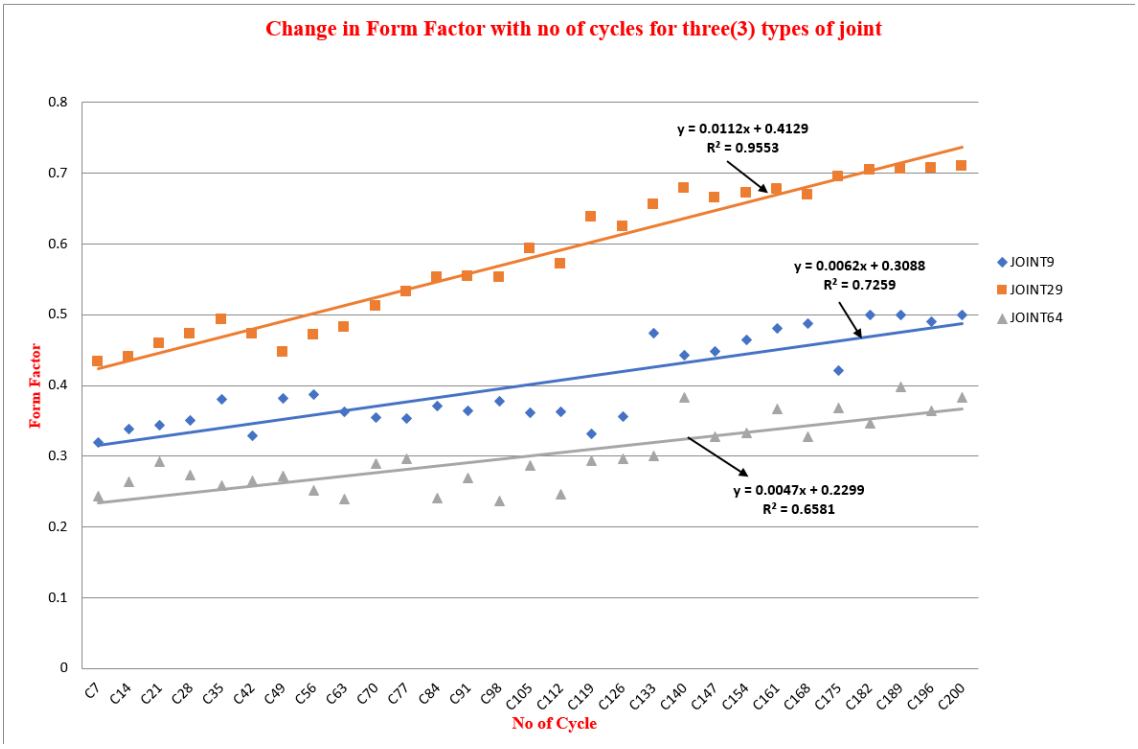
heterogeneous in terms of their shapes. It is noteworthy to know that this type of feature extraction makes use of two other parameters: i) changes in area and ii) changes in the perimeter of a sample to determine the shape of the ROI. According to the equation 6-15, for a perfect circle, the form factor value is equal to 1 (one).

$$(4\pi \times A)/ (P)^2 \qquad \text{Eq. 6-15}$$

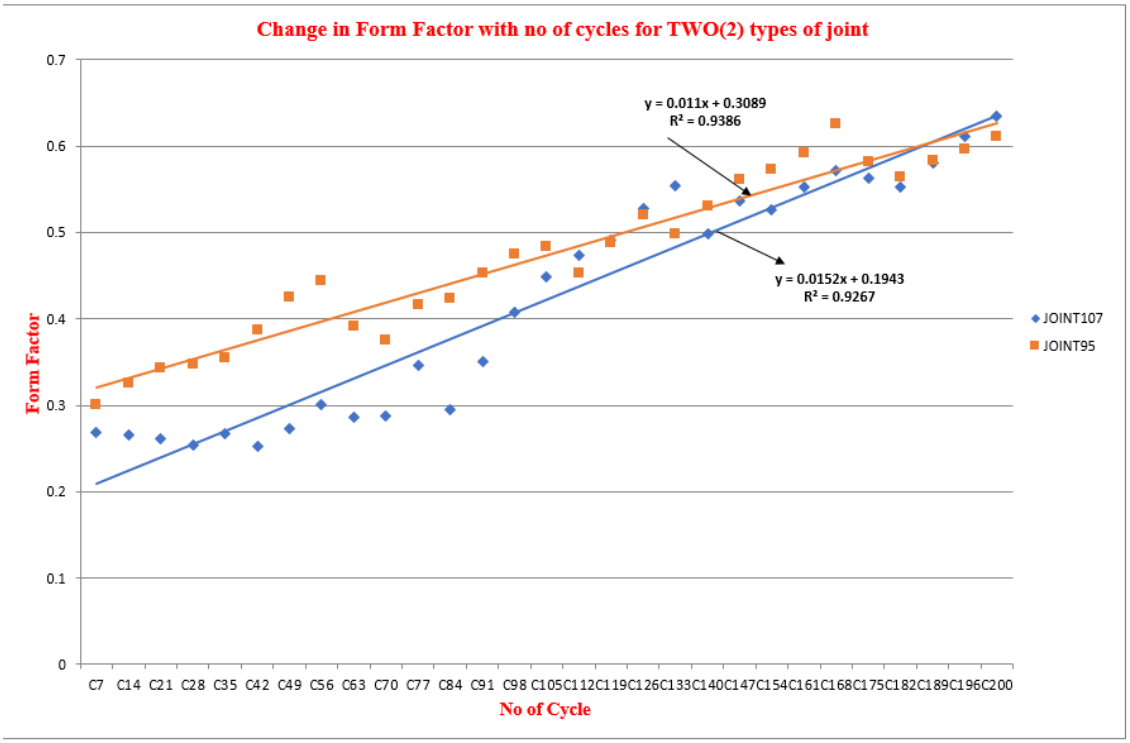
Where A is the area and *P* is the perimeter of the region.

Conversely, as the shape of the ROI becomes less round, the circularity should decrease and tends to approach zero. Based on the graphical observation from Figure 6-21 to 6-23, it is of note that as the cyclic temperature transition induces a thermo-mechanical stress to each solder joint, it was postulated in this research study that the differences in the ROI are attributed to the presence of defects in the joints. If the ROI shape is convex as illustrated in Figure 6-7, this could lead to a significant crack area as graphically depicted in section 6.4.2, but a proportionally smaller crack area could occur when is it in concave form, the graphical results below compare the shapes of the regions of interest of solder joints to see if one correlates better with solder joint life under thermal cycling tests.

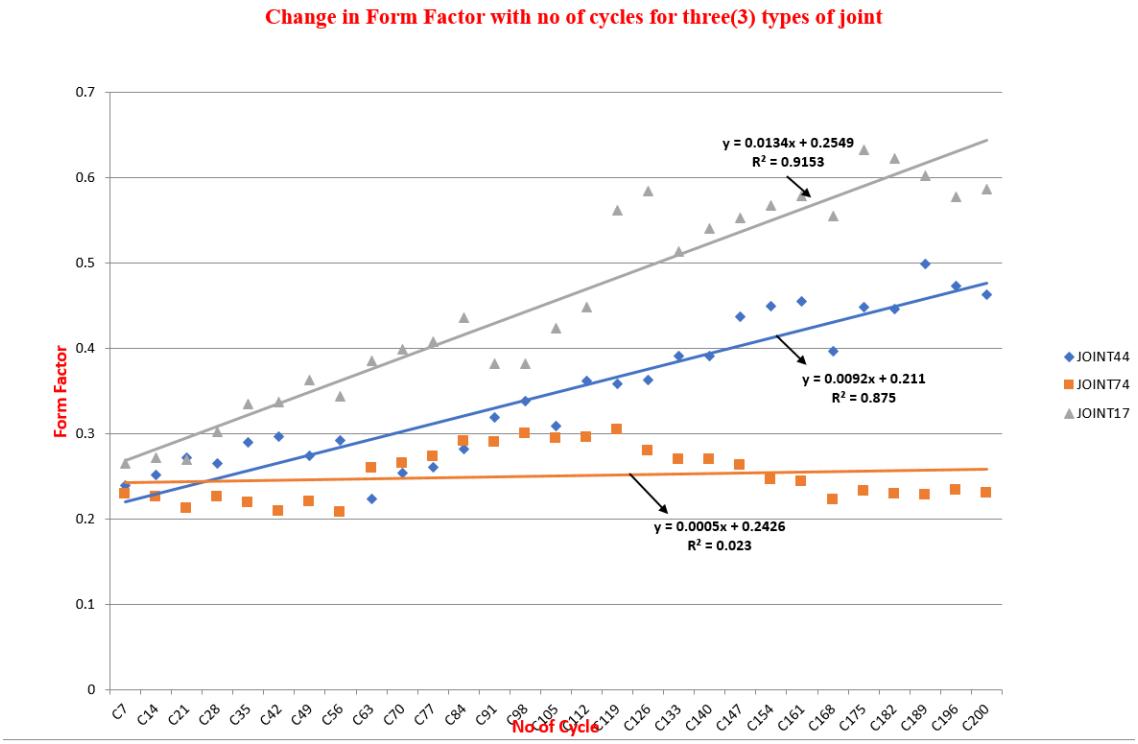
6.5.1 Results of form factor of 1.6mm Board, U23 Flip chip



(a)



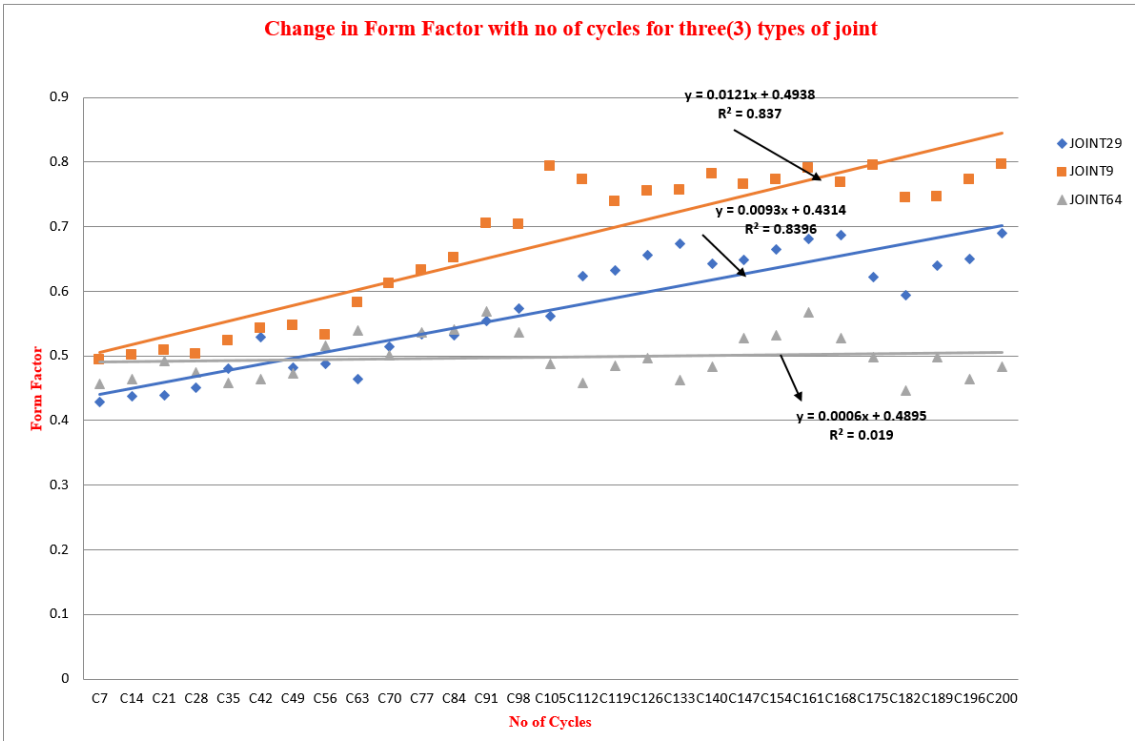
(b)



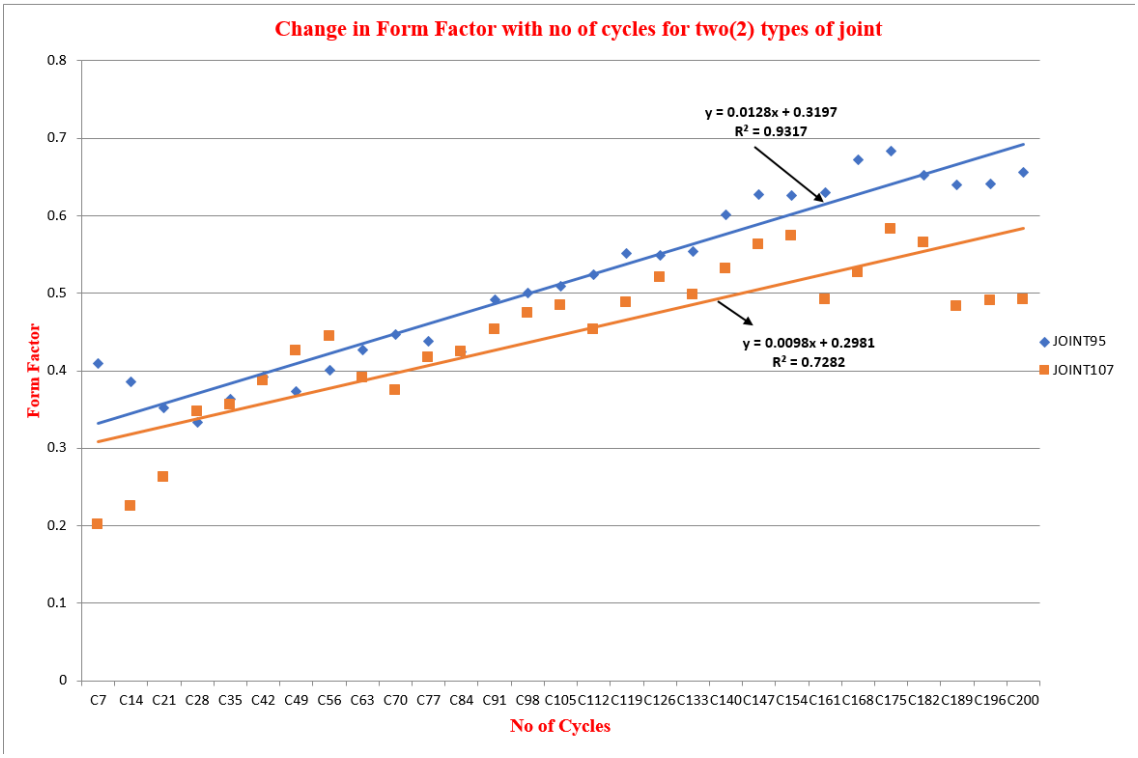
(c)

Figure 6-21 : Depicted the form factor of 1.6mm substrate thickness on U23 flip chip under different thermal cycling, with non-underfilled solder joints at different locations (a) 29, 9, 64 (b) 95 and 107 and (c) 17,44,74

6.5.2 Results of Factor of 0.8mm Board, U23 Flip chip



(a)



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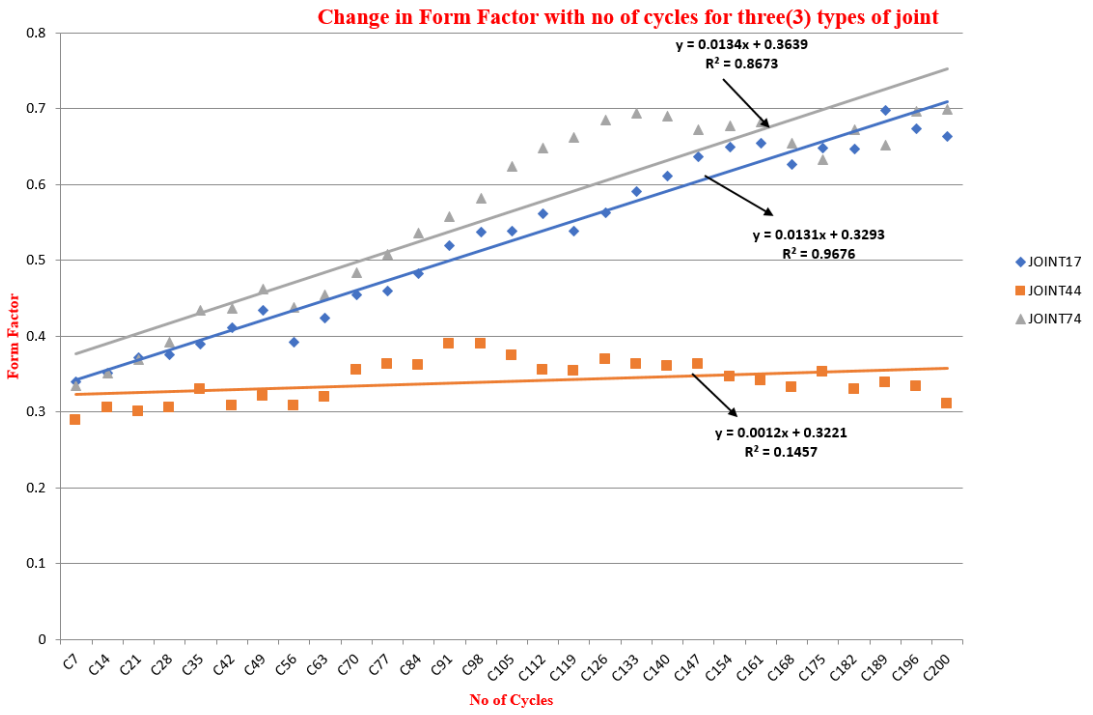
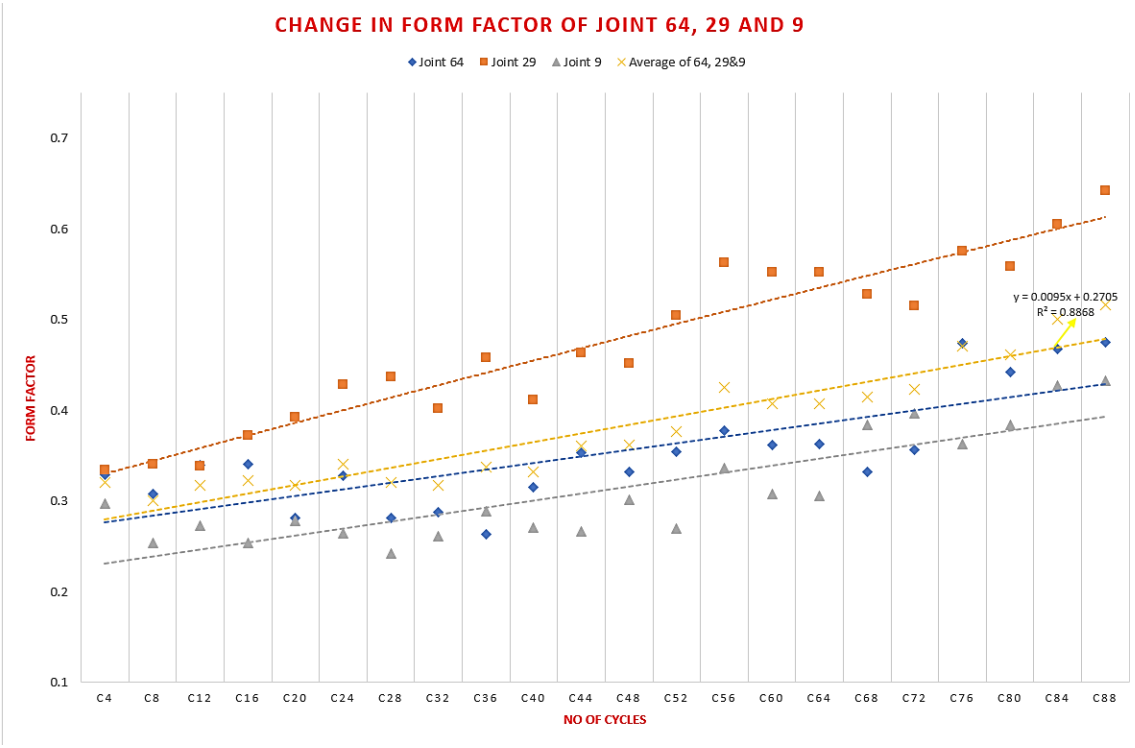


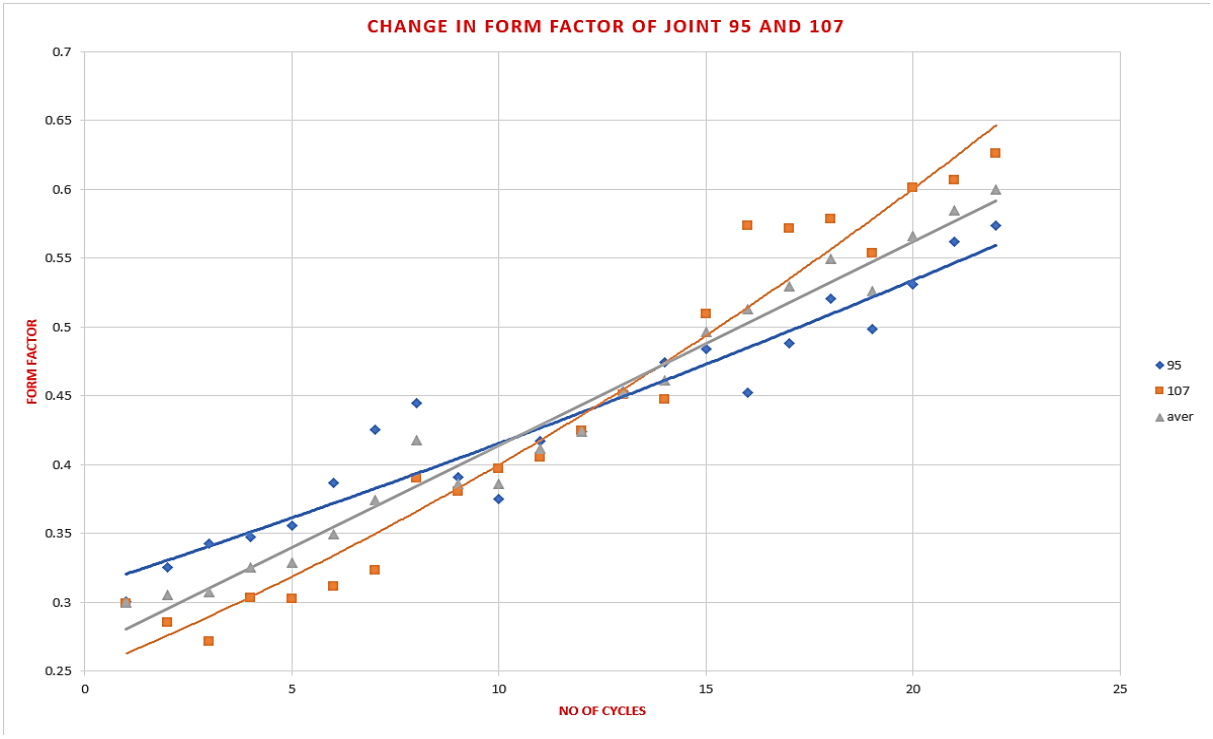
(c)

Figure 6-22: Depicted the form factor of 0.8mm substrate thickness on U23 flip chip under different thermal cycling, with non-underfilled solder joints at different locations (a) 29, 9, 64 (b) 95 and 107 and (c) 17,44,74

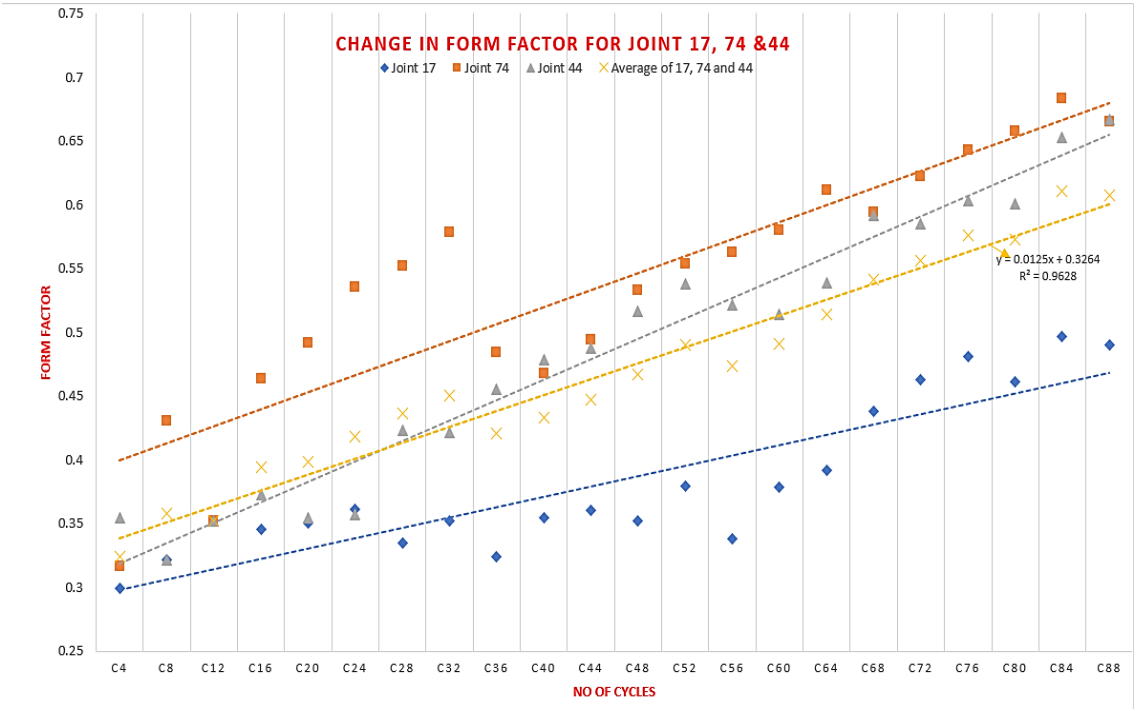
6.5.3 Results of Form Factor of BD09 U46 flip chip



(a)



(b)



(c)

Figure 6-23: Depicted the form factor of 0.8mm substrate thickness on U46 flip chip, under different thermal cycling, with non-underfilled solder joints at different locations (a) 29, 9, 64 (b) 95 and 107 and (c) 17,44,74

6.6 Findings

The shape formation of the solder joints has been analyzed from a statistical points view point, and the effects of the shape on the fatigue have been investigated. The findings from this section are based on using form factor as depicted in Figure 6-21 to 6-23. It is observed that as the thermal cycling was increasing, the reliability of the package was decreasing. Figure 6-21 to 6-23 shows the variation of cycles to failure in relation to ROI shapes. This is because as the diameter of the solder joints increases during the thermal test, the distance from neutral point increases which leads to more strain in the solder joints. For corner joints, defects were initiated at the point with lower form factor which are considered to have a convex apex region of interest shape as shown in Figure 6-8, for the shape of convex apex, the stress level was comparatively high, because the high stress

area concentrates at the interface that are not closer to the neutral point in the centre of the flip chip. In analyzing the form factor effect on the remaining selected joints 9, 29, 64, 74, 107 and 95 in figure 6-1, it was found that the results in Figure 6-23 clearly denote the dependence of the solder joints' failure data on the extraction method when the region of interest shape diverges from spherical under thermal cycling tests. The results practically coincided with the segmentation techniques in chapter 5, suggesting that the shape of the region of interest is randomly oriented i.e. concave shape. For the solder joints shape of concave and tiny concave, the stress level was relatively low, because the high stress area are not located at the interface that are more closer to the neutral point of the flip chip. However, based on the analyzed results on form factor, it is of note that the region of interest in solder joints' images is more vulnerable to thermal fatigue. It is also found that during the ATC, the deformation of the ROI in all direction increases with the decrease in thickness of the PCB board.

6.7 Time Domain Features using standard deviation

In past years, inspection of certain defects or delamination on electronic boards was done through simulations, a method that is term subjective and hardly efficient. However, due to the effect of some environmental factors such as thermal expansion, vibration, humidity, solder joints suffer from defects in their internal structures. These kinds of delamination or defects are referred to as cracks, which could directly affect their functionality during usage. Thus, adequate and accurate through-life monitoring information about those defects is crucial for their performance.

Therefore, using the standard deviation (SD) method during the study of the performance of solder joints is one of the useful ways to monitor and evaluate their fatigue life. (Pan, et al 2011). The standard deviation of the solder joints is an effective criterion for describing and measuring the variation of irregularity of a spatial shape of the ROI of the solder joints. Thus, the work presented in this section endeavours to use the standard deviation feature to evaluate the solder joints' defects caused during the thermal cycling. It is of note that the spatial shape of a particular image is an important criterion for image analysis (Yang et al, 2012). A low standard deviation indicates that the data points tend

to be very close to the mean, whereas high standard deviation indicates that the data points are spread out over a large range of values (McDonald et al, 2015).

However, based on the perspective on the segmented results of using visual observation, you will have a clear idea that the joints consist of a pattern of irregular shapes during the TC test, but you probably would not be able to tell what was happening in the ROI's of those images. Thus, one paramount characteristic of those test images is how much variation there is between them. In this performance study, a standard deviation in terms of feature extraction is presented to measure and show how much variation or dispersion of the component is in each pixel. This method has been defined as the square root of the fraction of the summation of mean deviations of a set of values. Thus, a standard deviation filter has been used to calculate the standard deviation, which enables it to assign this value to the ROI in the image which helps in detection of irrelevant or irregular objects in an image.

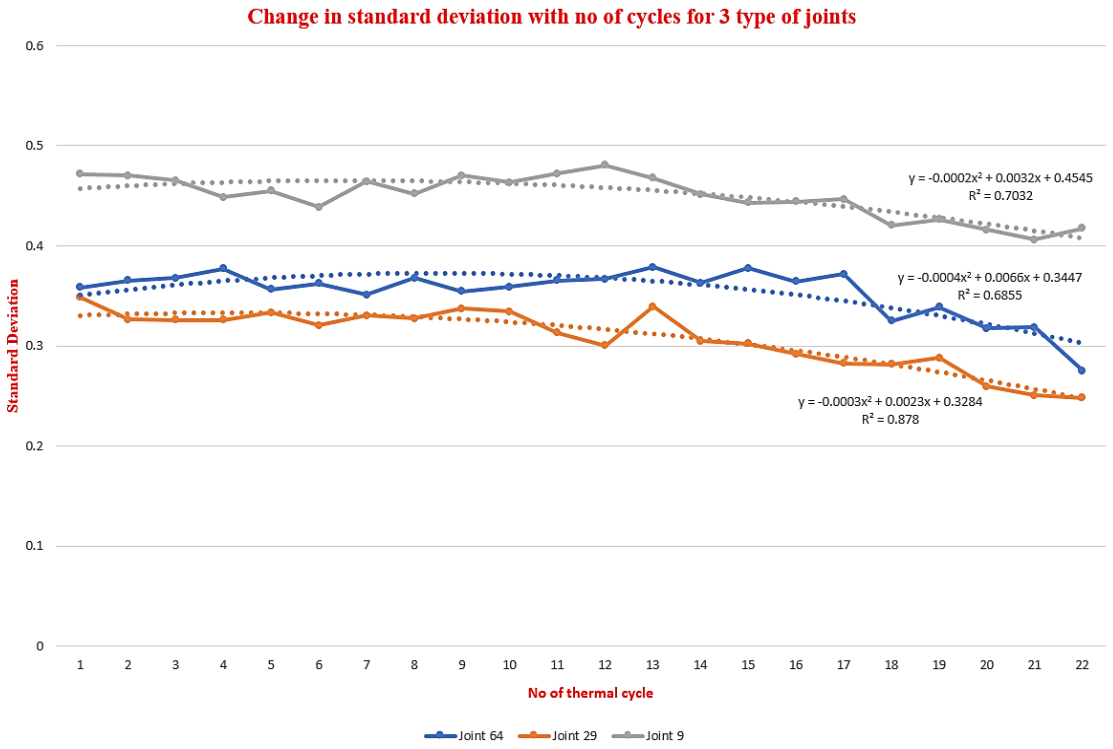
Mathematically this is represented in the form of an equation 6-16 as follows,

$$F(x, y) = \sqrt{\frac{1}{mn-1}} \sum_{(r,c)\epsilon w} \left(g(r,c) - \frac{1}{mn-1} \sum_{(r,c)} g(r,c) \right) 2$$

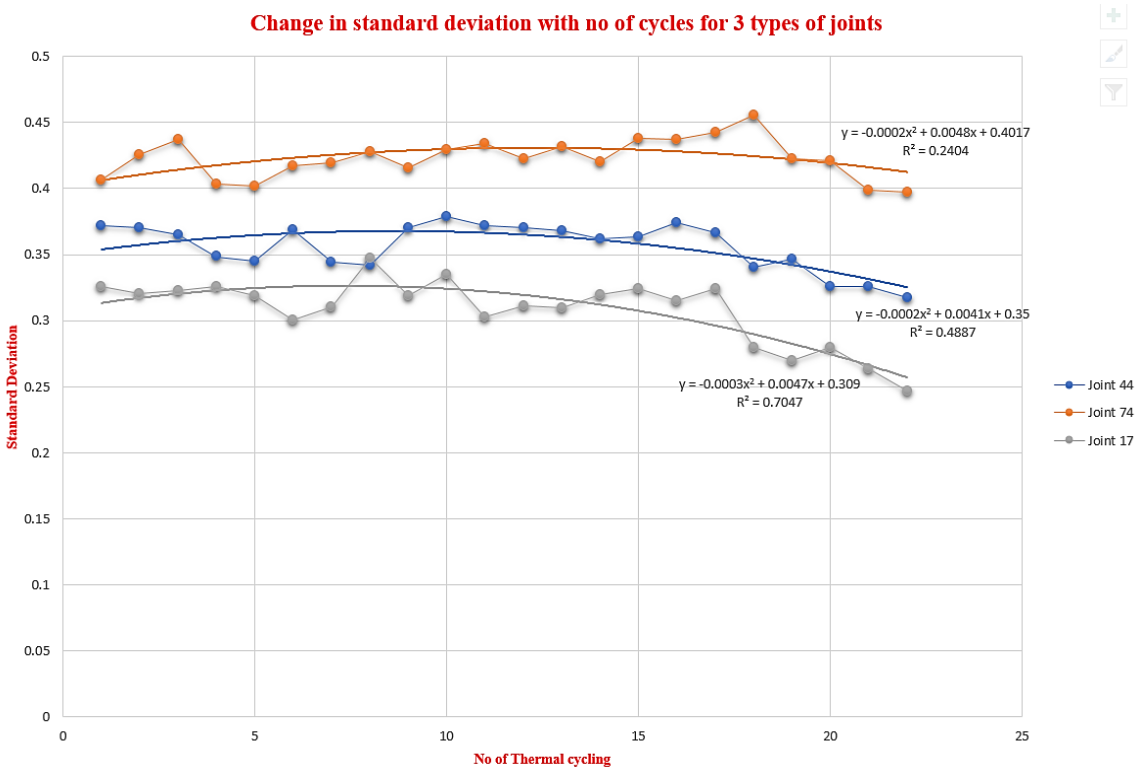
Where f(x, y) is the restored image, 'g' is the normal image, 'r' and 'c' are the row amd column coordinates respectively and 'within a window 'W' of size 'm×n' where the operation takes place (Vijay Kumar et al 2012). However, using SD values and the intensity values obtained in this work, the results to obtain the deformation in solder joints becomes much easier. Standard deviation could be considered as an important benchmark to identify the deviation of each solder joint from another. The correlation of the results is then compared with the TC to determine the quality of those selected solder joints.

From the analysis, a large SD of the acquired images would simply mean that the sample contains images with different variation, which enables us to study the relationship with greater precision. Figure 6-26, the graphical results depicted that there are more increases in variablity in the healthy solder joints than there are for the defective joints. However, based on the observation from Figure 6-26, that identified different types of joints, statistical analysis was done in the depicted results on standard deviation to observe the statistical behaviour with an increase in thermal cycling.

Analysed results of SD on BD09 of U46 Flip chps , 0.8mm substrate thickness is depicted in Figure 6-26 below.The change in variability in or dispersion of, analysis of this particular flips chip during thermal cycling test, is quite different form the others because of some factor that may affect the performance of solder joints on that flip chip, Some of the factors are i) the position of the U46 flip chips on the test sample, ii) the extend of thermal expansion coefficeint mismatch on the flip chips during the ATC test, iii) the thermal profile range,(Heating and the cooling rate involve in the thermal test, iv) solder joints geomtry on the flip chip, v) the level of compliancy of the flip chip assembly.



(a)



(b)

Figure 6-26: Variation in standard deviation of joint number a) 29, 9, 64 and b) 17, 44 and 74 of U46 Flip chip, 0.8mm board at different TC test.

6.7.1 Findings

Using the designed test boards has enabled to carried out an investigation in which the standard deviation was used to analyze and study the failure rate of those joints .Conceptually, it is important to observe that as the number of cycles are increased the solder joint irregularity continues, and the width of the interval decreases, identifying a change in variation of standard deviation. The graphical graph of an SD distribution approaches an increase in irregularity of the image. In this study, a novel feature representation formed with statistics using standard deviation of Gaussian method to monitor the performance of solder joint during TC test has been covered and proposed. .

Accordingly, the standard deviation is calculated for constructing the feature representation which greatly helps in analysing the feature data while not leading to heavy information losses. In addition, the standard deviation used in this performance study

could be described as a descriptive method that helps to indicate the variability in the acquired solder joints images on both 0.8mm and 1.6mm test samples.

6.8 Summary

In this chapter, the ability to accurately detect the anomalies and failures in solder joints during environmental exposure is the key factor in assessing the reliability or performance of the solder joint. Three failure criteria were compared in solder joints' reliability life estimation under thermal cycling test. These failure criteria include a failure criterion based on the area plots, form factor plots, and standard deviation chart. Results from this research study shows that those failure criteria have variation in the cycles to failure for constant temperature cycling ranges. This is because as the size or area of the solder joints increases, the crack length increases and the time for crack propagation increases. However, the analysis results from this study revealed that solder joints' stability is sensitive to board thickness. Evidence has shown that the solder joints on the 0.8mm HASL board have the lowest levels of reliability. On the other hand, the solder joints on 1.6mm HASL have better levels of reliability. This indicates that there is a statistically significant difference in reliability life among solder joints for -40 to +85°C thermal cycling range data on the flip chip components. However, in this study, constant temperature profiles are applied on different circuit board assemblies on the reference geometry of the solder joint to study the effects of ramp rate, dwell time and temperature range on the region of interest shapes. It is found that the stress level of solder joint during the thermal cycle test increases at longer dwell time. This reflects the accumulation of creep damage with time on the ROI shapes.

7 Analysis and Discussion

The basic aim of this study was to estimate and monitor the failure rates of the reliability of solder joints under thermal cycling test using a non-destructive technique (NDT) called acoustic micro imaging (AMI). Geometrical feature extraction methods like area and form factor were used to study and analyse the failure rate and the effect of substrate thickness on the reliability of solder joints. It is of note that these research studies have been carried out on two different boards of thicknesses of 0.8 mm HASL and 1.6 mm HASL without under fill. It can be observed from chapter 5 that the solder joint life decreases as the board thickness decreases. Also, the flip chips components on 1.6mm board show better performance, which is because the thicker board absorb less heat, hence reducing the stress level of solder joints on the flip chips component. However, in this chapter, analysis of variance (ANOVA) was used to analyse solder joint defect on the characteristic life of flip chip assemblies. This section includes the analysis for the failure detection and failure criteria comparison in previous chapters.

Analysis of variance also helps to determine the significant factors which affect the geometrical reliability life of the solder joints under the flip chips for both test samples with the same temperature cycling range. The geometrical feature extraction parameters such as the area, the form factor were used in the ANOVA. This is because the variation in the area and the form factor signifies the defect occurrence cycles during the validation test, which provides a better way to estimate the performance of the solder joint during mission life, this is well depicted in chapter 6.

7.1 Anova Hypothesis in this research study

The percentage contribution of an individual parameter cannot be determined by the simple analysis but can be achieved through ANOVA. This refers to the application of a statistical method, which separates the total variability of the responses into contributions from each parameter (Rosa, 2018). The percentage contribution of an individual parameter is defined as the pure sum of the squared deviation of each factor divided by the total sum of the squared deviations. This can be used to evaluate the importance of various parameters on the response acquired during the validation test.

The ANOVA tested the following hypotheses for the reliability life of 0.8mm and 1.6mm HASL board, using the thermal profile of -40 to +85 °C. Hence, to prepare for the ANOVA test, the selected solder joints were divided in two groups based on their distance to neutral points. The mean of the acquired data was used as reference to get the average and the variance. The solder joints (JT) with score less or equal to the mean were put in a group and assume be a good joints and the remaining were put in another group. After dividing solder joints into two groups, a two-way ANOVA was conducted to examine the difference between the mean of the solder joints under two different PCB thickness. A *p* value of less than .05 was required for significance. The results table shown in Appendices C, which can be found in the storage device at the back of this thesis, contains the number of components for estimation of the solder joint characteristic life using the area and the form factor data. The ANOVA used in this research study depicted whether each performance study investigated the individual behaviour of solder joints on the flip chip packages whilst considering the hypothesis that reliability of the test sample is influenced by placement location on the PCB floor plan layout, PCB substrate thickness, and physical constraints placed on the PCB during the validation test.

Table 7-1 shows that the package construction was a significant factor in the reliability of solder joints on U23 flip chips of 0.8mm HASL board.

Table 7-1: (a) and (b) ANOVA Table for area characteristic life of joint number 95 and 107 (-40 to 85°C)

Groups	*Count*	*Sum*	*Average*	*Variance*
JT95	29	14244	491.1724138	26792.14778
JT107	29	16705.2	576.0413793	31629.3668

(a)

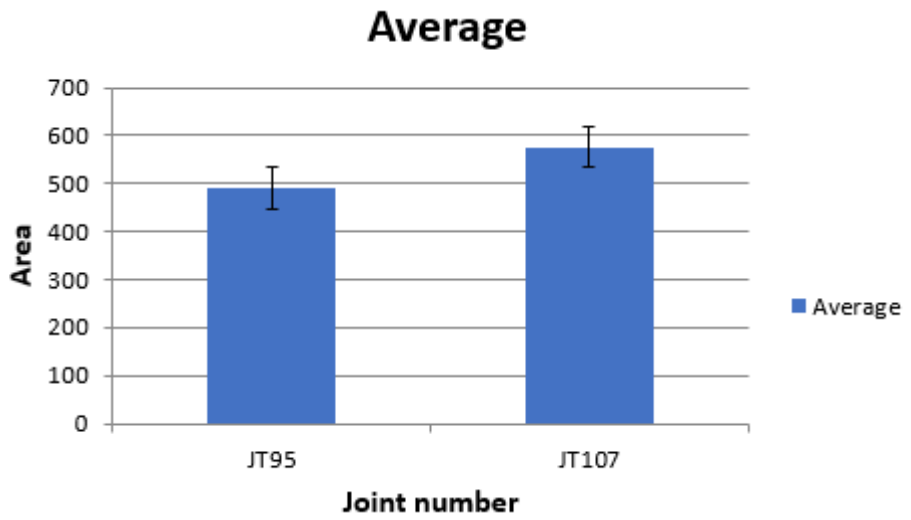
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	0.064036204	1	0.064036204	5.704547369	0.020317107	4.012973319
Within Groups	0.628626112	56	0.011225466			
Total	0.692662316	57				

(b)

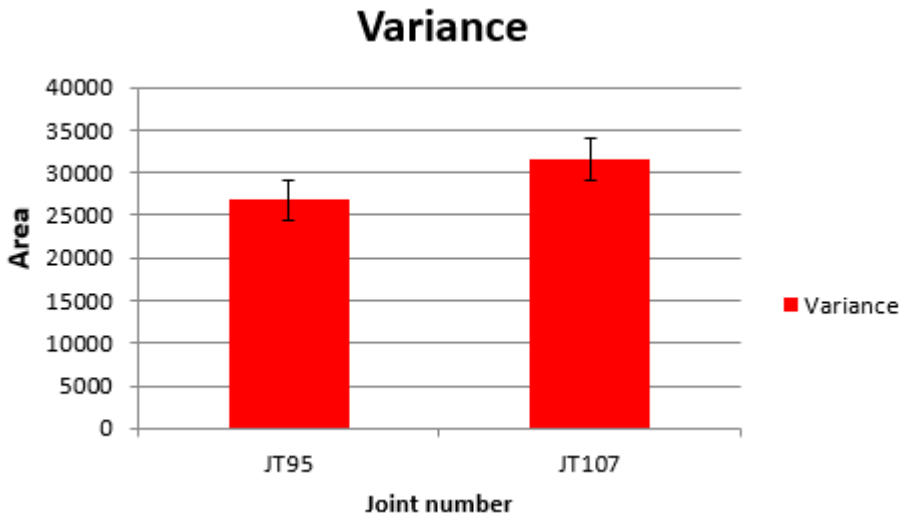
Parameters definitions: where N**:** Number of Samples, SS: Sum of Squares which measures the variation from the mean, DF**:** Degree of Freedom this refer to terms in the sum of squares =N-1, MS: Mean Square which is the sum of squares (SS) divided by the number of degrees of freedom. F is the variance ratio which equals the mean sum of squares (MS) divided by the means square error, and p-value: Probability value which is used to determine if the results are statically significant (Minitab, 2014).

Figure 7-1 shows that PCB thickness has a statistically significant effect on the characteristic life of solder joints. Figure 7-1 graphically shows the average and variance characteristic life plot for the joint 95 and 107 on U23 flip chip of 0.8mm HASL board. From the calculation of the Average, it shows that the area increases more in Joints 107 more than Joint 95 as the thermal cycling increases.

From the calculation of the Variance, it shows that the rate of increase in area of Joint 107 is higher than Joint 95. Nevertheless, the test of significance is performed by comparing the calculated F-ratio with the standard F-table. F-value in table 7-1 is greater than the F-critical value for the alpha level selected is 0.005(Minitab, 2014). Hence, the p-value is very low. Therefore, we have evidence that each joint has different significant degradation effects and it increases along the joints. The results in Figure 7-1 of the analysis also show a significant change in the trend of the failure in solder joints.



(a)



(b)

Figure 7-1: Anova analysis of the average and variance of joint number 95 and 107 on U23 flip chip on 0.8mm board.

Table 7-2 shows the average and variance characteristic life plot for the joint 9, 29 and 64 on U23 flip chip of 0.8mm HASL board. Which also shows that the PCB thickness has a statistical significant effect on the solder joint life at -40 to 85 °C temperature cycling range.

Table 7-2: (a) and (b) ANOVA Tables for area characteristic life of joint number 95 and 107 (-40 to 85°C)

Groups	*Count*	*Sum*	*Average*	*Variance*
JT9	29	9324	321.5172414	11757.18719
JT29	29	14468	498.8965517	12594.4532
JT64	29	16033	552.862069	23069.26601

(a)

ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	849662.5517	2	424831.2759	26.87620133	9.49652E-10	3.105156608
Within Groups	1327785.379	84	15806.9688			
Total	2177447.931	86				

(b)

Figure 7-2 depicted the average and variance characteristic life plot for the joint 29, 9 and 64 on U23 flip chip of 0.8mm HASL board. From the calculation of the Average, it shows a gradual degradation increase from Joints 9, 29 and 64 as the area increases from one joint to another. From the calculation of the Variance, it shows that the rate increase in area is higher in Joint 64 and lowest in Joint 9.

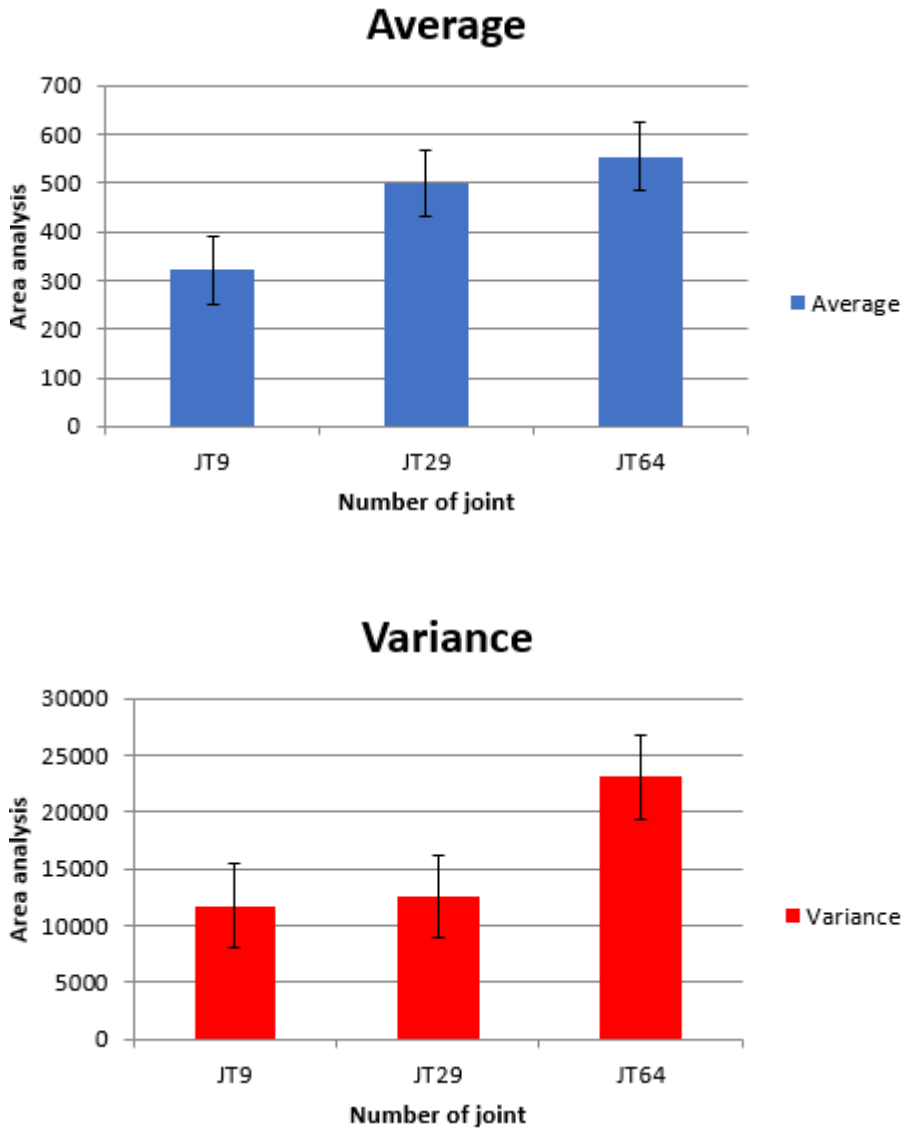


Figure 7-2: Average and variance of joint number 29,9 and 64 for 0.8mm HASL board.

7.1.1 ANOVA Results: Form Factor Characteristic Life using -40°C to +85 °C

Reliability life for different solder joints at the same temperature cycling range was examined. At -40 to +85°C temperature cycling range, form factors were significant features which differentiate p-values of solder joints respectively. The form factor analysis of multiple comparisons shown in Table 7-3 indicates that the characteristic life for 0.8 mm HASL board is statistically significantly different from another. That allowed us to estimate the influence of PCB thickness and interactions between them on solder joint life.

Table 7-3: (a) and (b) shows the characteristics life for 0.8mm HASL board for joint 9, 29 and 64.

Groups	*Count*	*Sum*	*Average*	*Variance*
JT9	29	19.5758	0.675027586	0.012644172
JT29	29	16.5702	0.571386207	0.007525096
JT64	29	14.4396	0.497917241	0.001205909

(a)

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	0.45923722	2	0.22961861	32.22690768	4.10103E-11	3.105156608
Within Groups	0.598504934	84	0.007125059			
Total	1.057742154	86				

(b)

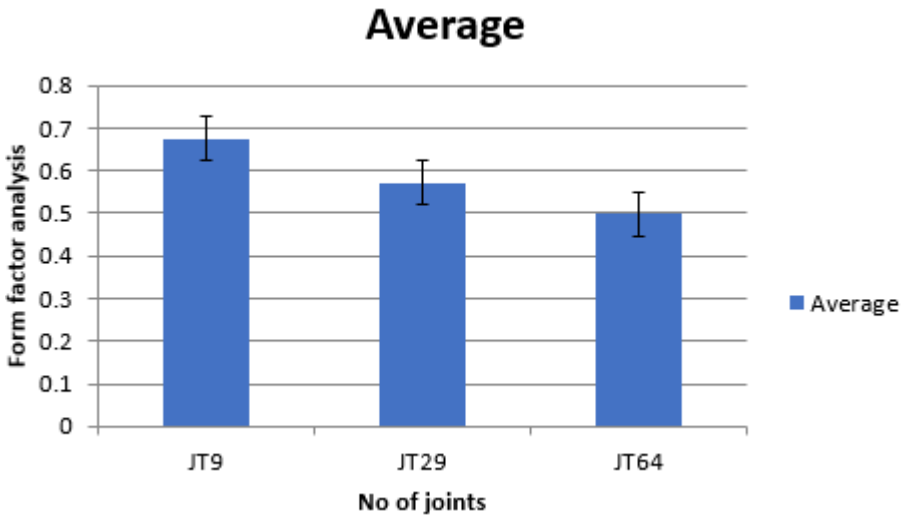


Figure 7-3: Anova average of joint number 29, 9 and 64 for 0.8mm HASL board based on form factor.

From the calculation of the average in Figure 7-3, shows that the form factor from joints 9, 29 and 64 is decreasing. It also shows that the rate increase in area is higher in joint 64 and lowest in joint 9. Hence, p-value in table 7-3 is very low because the F-value is greater than the F-critical value for the alpha level selected is 0.005, therefore, we have evidence that each joint has different degradation effects and affects the shape of the joints.

7.1.2: ANOVA Results for 1.6mm HASL board on U23 flip chip: Area Characteristic Life using -40°C to +85 °C thermal profile.

The area analysis of multiple comparisons shown in Table 14 indicates that the characteristic life for 0.8 mm board is statistically significantly different from that for 1.6mm. In addition, the characteristic life for 1.6mm board is statistically significantly longer than that for other pitches.

Table 7-4: (a) and (b) ANOVA tables for area characteristic life of joint number 95 and 107 of U23 flip chips -40 to 85°C thermal profile

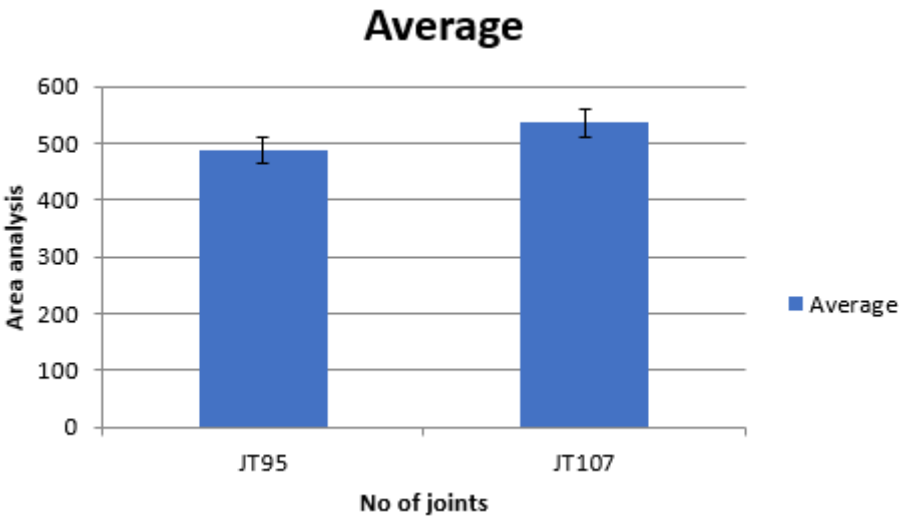
Groups	*Count*	*Sum*	*Average*	*Variance*
JT95	31	15112	487.483871	39934.32473
JT107	31	16612.7	535.8935484	50063.65729

(a)

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	36324.20145	1	36324.20145	0.807222576	0.372534111	4.001191306
Within Groups	2699939.461	60	44998.99101			
Total	2736263.662	61				

(b)

The Anova area analysis plot for U23 flip chip in Figure 7-4 shows that the characteristic life for 1.6 mm HASL board is more preferable in terms of reliability compared to 0.8mm HASL board. In addition, the characteristic life for 1.6mm board is statistically significantly longer than that for other boards. From the calculation of the average, it shows that the area is neither increasing nor decreasing in any order for both joints. From the calculation of the variance, it shows that the rate of change in area is not dependent on the joint positions.



(a)

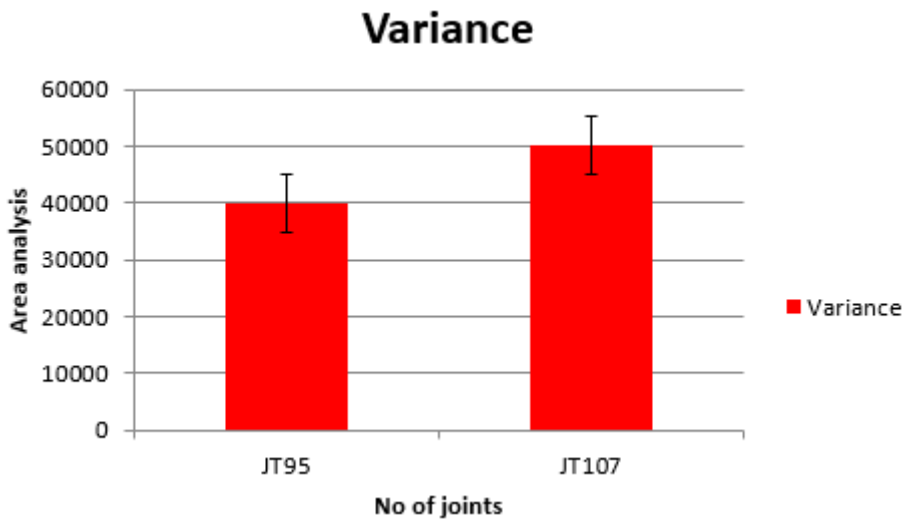


Figure 7-4: (a) and (b) depicted the Anova analysis of the average and variance of joint number 95 and 107 on U23 flip chip on 1.6mm board

However, Table 7-5 a and b shows the average and variance characteristic life plot for the joint 9, 29 and 64 on U23 flip chip of 1.6mm HASL board. Which also shows that the area array package construction has a statisticallly significant effect on the area analysis for the -40 to 85 °C temperature cycling range.

Table 7-5: (a) and (b) ANOVA tables for area characteristic life of joint number 9, 29 and 64 of U23 flip chips using -40 to 85°C thermal profile on 1.6mm board.

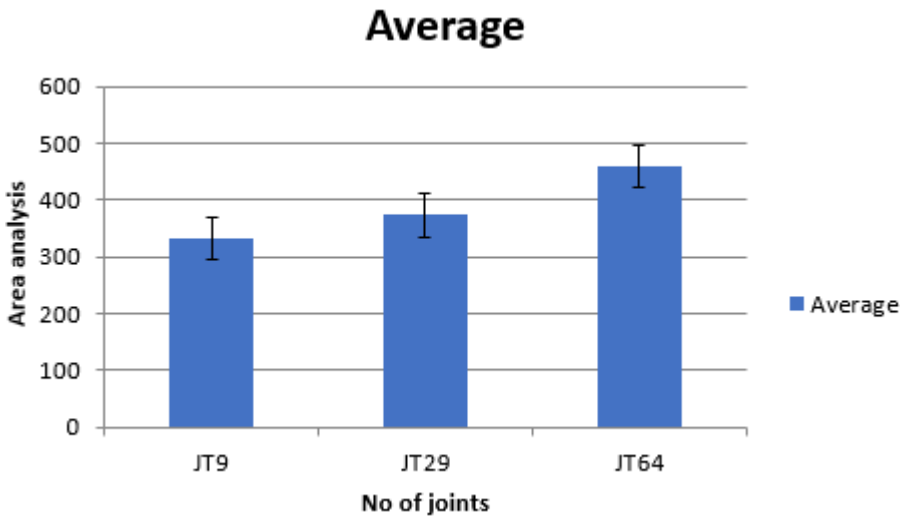
Groups	*Count*	*Sum*	*Average*	*Variance*
JT9	31	10326	333.0967742	9438.823656
JT29	31	11572	373.2903226	18729.74624
JT64	31	14269	460.2903226	26095.87957

(a)

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	262081.4409	2	131040.7204	7.244561867	0.001209801	3.097698035
Within Groups	1627933.484	90	18088.14982			
Total	1890014.925	92				

(b)

Figure 7-5 shows that the thermal cycling test has a statistically significant effect on the characteristic life of solder joints.From the calculation of the average in Figure 7-5(a), it shows that the average area of all cycles in joint 64 is higher and lowest in Joint 9. From the calculation of the variance in figure 7-5(b), it shows that the rate of change in area is dependent on the joint positions throughout the cycles.



(a)

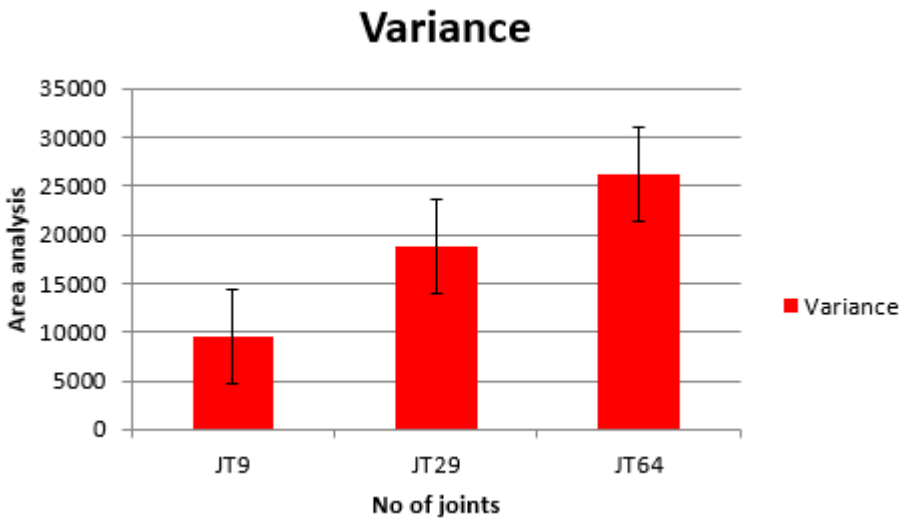


Figure 7-5: Average and variance of joint number 29, 9 and 64 of U23 flip chip of 1.6mm HASL board.

7.2 ANOVA results using two factor with replication 0.8mm and 1.6mm HASL Board

In this study, ANOVA for solder joints on different test samples was conducted as well. The effects of the thermal cycling on solder joint life are summarized in Table 7-6. Table 7-6 shows the estimated coefficients of solder joints 95 and 107 and the associated standard error on 0.8mm and 1.6mm boards. In order to make the ANOVA analysis valid in this study, the square root transformation is necessary. The standard error is used to estimate the standard deviation for that term in this study. A probability for the p-value below 5% indicates that term is a significant effect. Based on both the standard error and the probability for the p-value, it is intuitive that the board thickness and components population on the printed circuit board has significant influence on the fatigue life of solder joints, which is consistent with the ANOVA results.

The ANOVA table 7-6 show that the component size has a statistically significant effect on the solder joints' life under TC test. It shows that the shear stress for SnPb (Sn=52.9%, Pb=45.9%) solder joints is higher in thinner board 0.8mm for the same component size compared to thicker board 1.6mm.

Table 7-6: (a) and (b) ANOVA tables for area characteristic life of joint number 95 and 107 of U23 flip chips using -40 to 85°C thermal profile on both 0.8mm and 1.6mm.

SUMMARY	JT95	JT107	Total
Board nine(0.8mm)			
Count	29	29	58
Sum	14244	16705.2	30949.2
Average	491.1724	576.0414	533.6069
Variance	26792.15	31629.37	30530.56
Standard Error	30.39518	33.02526	
Board Ten(1.6mm)			
Count	29	29	58
Sum	13546	14838.7	28384.7
Average	467.1034	511.6793	489.3914
Variance	36118.45	44226.95	39973.39
Standard Error	35.29113	39.05211	

(a)

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Sample	56695.35	1	56695.35	1.634261	0.020376	3.925834
Columns	121480.7	1	121480.7	3.50172	0.043915	3.925834
Interaction	11770.62	1	11770.62	0.339292	0.056141	3.925834
Within	3885474	112	34691.73			
Total	4075420	115				

(b)

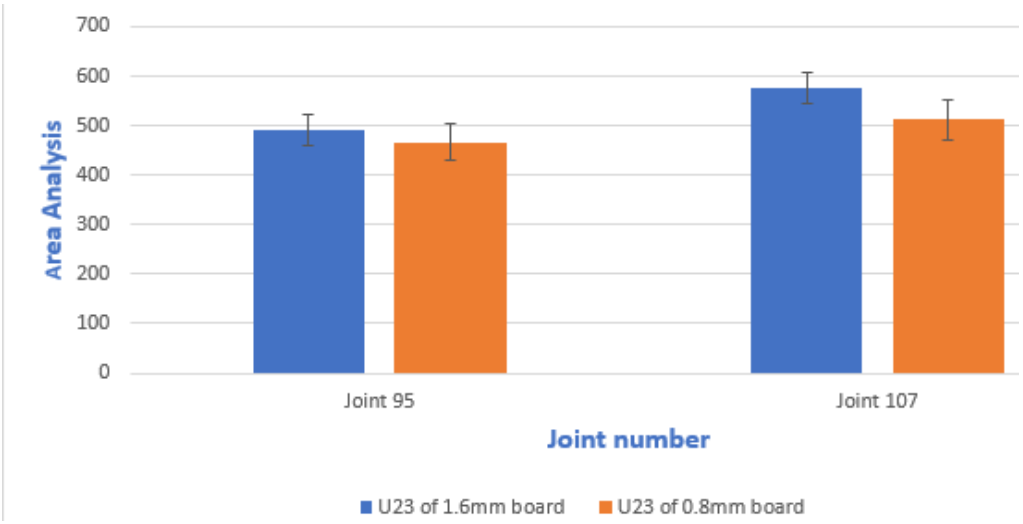


Figure 7-6: Graphs showing joint number 95 and 107of U23 flip chip for both 0.8mm and 1.6mm HASL board.

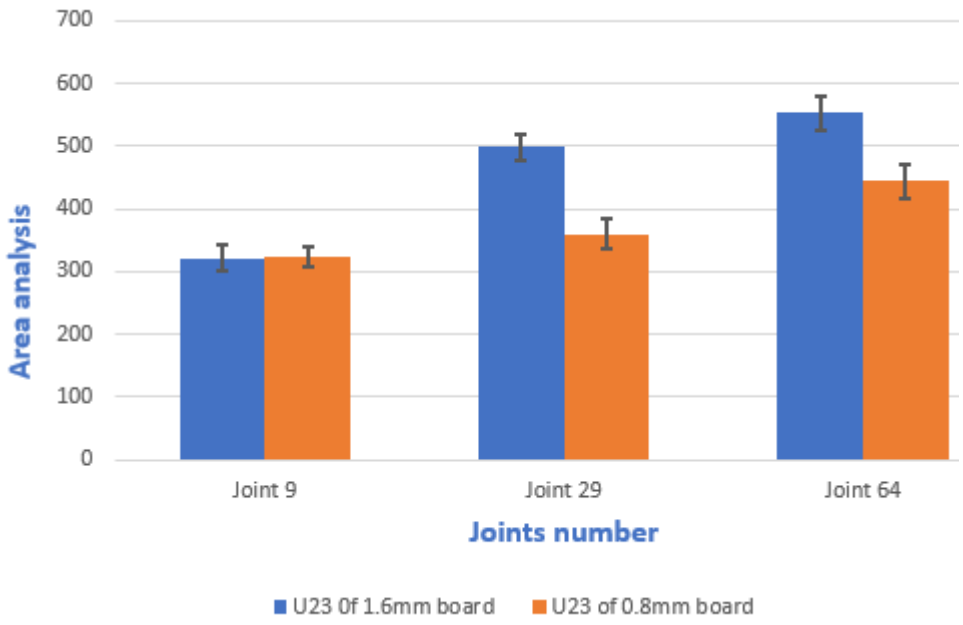


Figure 7-7: Graphs showing joint number 9, 29 and 64 of U23 flip chip for both 0.8mm and 1.6mm HASL board

7.2 Chapter Summary

The purpose of this study was to examine a statistical approach for feature selection in life monitoring of solder joints under thermal cycling tests. Cycles-to-failure for the 0.8mm and 1.6mm board validation data was determined using Analysis of variance (ANOVA). ANOVA was used to see if PCB layout had a statistically significant effect on the characteristic life and slope of the flip chip assemblies. The sensitivity of this kind of method was then compared with the selected solder joints in chapter 6. Using the mean of the acquired data as reference, the selected solder joints was divided into various groups to classify and check the statistical significant relationship exist between the solder joint on two printed circuit boards (PCBs). The ANOVA technique was computed using a two-way ANOVA to analyse the acquired data. The ANOVA was significant, the effect size was high on those solder joints, allowing to rejecting the null hypothesis, and indicating that there is a statistically significant relationship with strong effect size between the solder joints on 0.8mm and 1.6mm HASL board. Likewise, the analysis test indicated that PCB thickness affects the solder joint interconnect reliability. These results support the conclusion that there is a statistically significant and strong relationship between solder joints under thermal cycling test and the PCB thickness.

8 Conclusion

The achievement of the research aims has enabled the development of a nondestructive methodology called acoustic micro imaging to evaluate the reliability of solder joints under thermal cycling test. The investigation of the solder joints on 0.8mm and 1.6mm HASL circuit board assemblies was considered to be the first time the Gen6™ C-Mode Scanning Acoustic Microscope was used to monitor and analyze the reliability of solder joints under thermal cycling tests. The research developed a concept in which the validation experimental work and the feature extraction method, characterized the reliability study of solder joints using the geometrical and time domain features extraction method. This allowed repeatability and reproducibility of study methods of analysing defect in solder joints of area array packaging. In this research, auto-comparison segmentation analysis method was designed and developed to effectively segment, and identify solder joint defects on the packages.

The main contribution made in this research study are as follows:

1) An attempt was made for the first time to bring in medical image analysis method that was used to detect sickle blood cells in blood samples. This method was adopted in this research, to present a novel method that determine and evaluate the variations in the region of interest shapes in reliability study of solder joints under thermal cycling test. Based on the observations, it is noteworthy to know that the variations in size of the region of interest may have a significant impact on the reliability of solder joints.
2) A new relationship between the solder joints was designed, through which the size of area of solder joints under thermal cycling test can be measured. However, the results has a good relationship between the acquired image data and solder joint area size under ATC test, which has not been fully studied before in AMI inspection.
3) A new image segmentation and feature extraction method was designed and implemented in this research work to study the performance of solder joints under thermal cycling test. This method was used to extract image features such as mean intensity, the AMI cycle to failure of solder joints, the structural similarity model, histogram differences of the region of interest. Hence, through data analysis the 3D segmentation of solder joints was designed.

4) In this research study, a new less aggressive profile of -40ºC to +85ºC was used, this successfully led to a slower failure process, which enabled finer tracking of crack propagation in solder joints under thermal cycling test. However, this also facilitated the development of an image feature based joint fatigue degradation model for through-life monitoring of crack initiation and propagation.

5) The successful development of the non-destructive methodology significantly improved the flexibility and robustness of the inspection system to monitor solder joints under environmental exposure. A comprehensive comparison between solder joints on different substrate thickness evaluation methods was presented in this research, in which the reliability of solder joints was assessed using 0.8mm and 1.6mm failure criterion. It is depicted that the substrate thickness had a statistically significant effect on the area and form factor characteristic life of solder joints at the same thermal cycling range, with 0.8mm HASL packages having the shortest reliability characteristic life. The test results obtained in chapter 5 and 6 from this research study could provide some guidance on how to estimate the effect of TC on solder joints.

6) The research has successfully analysed the defects in solder joints by using geometrical feature extraction like area and form factor. This has demonstrated better stability in measuring the solder joints' defects, and how the crack propagated in solder joints under thermal cycling tests. Further analysis on those solder joints was done using analysis of variance (ANOVA) techniques that demonstrate how the PCB thickness affects the failure rate of solder joints. This illustrated that the defects on solder joints during the thermal cycling test are related to component populations on the printed circuit board.

8.1 Recommendation for Future Work

In order to improve the current monitoring inspection system and expand the application of ATC to monitor the performance of solder joint, there is tremendous scope for pursuing further research study. Some of the potential directions for future research are presented in this section

1) Leaded solders in AAP have been the most used materials because of their great properties for interconnecting the flip chips component, but due to environmental legislation, lead free solders have been developed. The lead free solders are an initiative to help the environment. However, with respect to conducting performance study analysis on AAP, further study must be carried out on lead free test samples of the same flip chip components to emphasise the effect of using the sample thermal profile and the same parameters used for the validation inspection.

2) The use of different parameters both on validation test and inspection techniques in this performance study could have an effect on the analysis. In respect to this, further analysis should be conducted to understand the effect of different parameters on the test samples. For example to conduct an inspection on the solder joints at different AMI resolution, including 3D analysis from VRM data, to compute the sensitivity to performance changes.

3) Expansion of application scope, thus this thesis has investigated solder performance under thermal cycling test, which is the most common source from testing fatigue on solder joints. Hence, combining vibration and thermal cycling tests could give more precise results for products working under those environments, since, dynamic deflections of materials on area array packaging caused by vibration can result in huge problems and malfunctions of solder joints on the flip chips.

Appendices 1

Appendix 1:ATC preliminary test data for both 0.8mm and 1.6mm……USB drive attached to the inside back cover page

Appendix 2 AMI preliminary scans on both test samples ...……USB drive attached to the inside back cover page

Appendix 3: A full data set of the AMI, X-ray images undertaken in this performance study. Test boards configurations and assembly information are also contained in this USB. …….……USB drive attached to the inside back cover page

Appendix 4: MATLAB programs used in the image processing, feature extraction……USB drive attached to the inside back cover page

Appendix 5: Graphical Results of all ATC test during the study ...……USB drive attached to the inside back cover page

Appendices 2: Publications

1) Initial Investigations into Through-Life Monitoring of Solder Joints

Adeniyi, O.A, Braden, D.R., Zhang, G.M. and Harvey, D.M. 2016

(Best Oral Presentation Award)

Liverpool John Moores University, Faculty Research Week, FET PGR

Abstract: In this study, solder joints were monitored using ultrasonic transducers. It is well documented that solder interconnections are the weakest link in terms of a circuit board assemblies (CBA) reliability. This is due in part to the coefficient of thermal expansion mismatch in materials used in the construction of components found on CBA when exposed to thermal cyclic environmental conditions, which in turn lead to fatigue failures. This paper presents a method to monitor solder joints in area array packaging using non-destructive techniques. Test boards with organic substrate thickness of 0.8mm and 1.6mm, containing six flip-chips and eight BGA chips were been subjected to an accelerated thermal cycling test (ATC) that ramps between 125°C and -40°C. Test boards were been monitored at regular intervals by Acoustic Micro Imaging. Experimental work to show difference image qualities for transducers with different frequencies were been performed.

2) Water Temperature Influences on Ultrasound Inspection of Solder Joints

Adeniyi, O.A, Braden, D.R., Zhang, G.M. and Harvey, D.M. 2017

Liverpool John Moores University, Faculty Research Week, FET PGR

Abstract: In this study, solder joints were been monitored using Acoustic Micro Imaging (AMI) for inspecting effects of a change in a particular parameter on the solder joints. This paper presents a method to monitor solder joints using water temperature as the major parameter. The test boards with organic substrate thickness of 0.8mm and 1.6mm, containing 6 flip-chip packages and 8 BGA chips

were subjected to Accelerated Thermal Cycling Test (ATC) with temperatures varying between -40 and 125°C. Test boards were been taken out at 4cycles and monitored at regular spaced intervals with AMI. Experiments to show the difference in image qualities for 230MHz transducers were also been performed

3) **Non-destructive Evaluation and Life Monitoring of Solder Joints in Area Array Packaging**

Adeniyi A. Olumide, Kangkana Baishya, Guang-Ming Zhang, Derek R. Braden, David M. Harvey

Electronic System-Integration Technology Conference (ESTC), Germany, 2018.

Abstract*:* Determining the lifetime of solder joints on area array packaging through non-destructive evaluation subjected to thermomechanical loads is crucial for reliability testing of electronic devices. Circuit board assemblies (CBA) are expose to cyclic changes in temperature. The rate of change, exposure time and thermal excursion limits are dependent upon product application and usage known as 'Mission Life'. The purpose of this study is to evaluate the application of an acoustic micro-imaging (AMI) inspection technique, in monitoring solder joints through lifetime performance. Test boards with various area array packages, different surface finish configurations and substrate thickness were subjected to an accelerated thermal cycling test (ATC). The test profile used was -40°C to +85°C with 30 minutes dwell. AMI scanning was performed every 4cycles over a total period of 220cycles, in order to obtain enough adequate failure data at high stress to accurately project (extrapolate) what the cumulative distribution function (CDF) at use will be. The cracks on the solder joints was determined by using statistical analysis to observe the behavior of the joints at the region of interest (ROI) with increase in thermal cycling. The differences in the plot patterns also confirms the variations of frequency intensity levels for different thermal cycles

4) **Non-destructive and Life Monitoring of Solder Joint under Thermal Cycling Conditions**

Adeniyi, O.A, Braden, D.R., Zhang, G.M. and Harvey, D.M. 2018
Liverpool John Moores University, Faculty Research Week, FET PGR

Abstract: The purpose of this study is to evaluate the application of an acoustic micro-imaging (AMI) inspection technique, in monitoring solder joints through lifetime performance. Test boards with various area array packages, different surface finish configurations and substrate thickness were subjected to an accelerated thermal cycling test (ATC).In order to obtain enough adequate failure data at high stress to accurately project (extrapolate) what the cumulative distribution function (CDF) at use will be.

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