# Bidirectional Hybrid HVDC CB with a single HV Valve

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**Abstract – This paper examines two new bidirectional hybrid dc circuit breaker topologies for application in meshed dc grids. The goal is to retain performance of hybrid DC CB with bidirectional current interruption, while reducing semiconductor count, DC CB size and weight. The fault current is routed to the unidirectional internal valve using multiple additional ultrafast disconnectors. Operation of both topologies is studied using a *320 kV, 16 kA* simulation model, as well as demonstrated on a *900 V, 500 A* lab prototype. The control systems are presented and discussed in detail. The low-voltage hardware prototypes verify performance of several new technical and operating solutions in laboratory conditions. A comparison is made with the existing DC CB topologies and performance and reliability compromises of each topology are assessed. The conclusion is that it might be possible to halve the DC CB semiconductor count while retaining same *2 ms* opening speed and bidirectional operation.**

***Index Terms*-- DC meshed grids, HVDC protection, HCB, fault current limiting.**

## I. Introduction

Substantial recent interest in developing high voltage (HV) DC grids has resulted in research and technology advances of the HVDC circuit breaker (CB) technology [1]-[8]. Different DC CB technologies (i.e. solid state, mechanical, and hybrid) have been developed and high-voltage prototypes demonstrated in the past few years [2]-[8]. The mechanical breaker based on active current injection [2]-[4] benefits from low cost and losses but the opening time is fairly long, in the range of *5-8 ms*, while recent demonstrations with VSC assisted mechanical DC CB demonstrated *10 kA* interruption in *3 ms* [5]. Solid-state breaker [2] on the other hand benefits from very short opening time but has excessive conduction losses, and therefore this topology is not considered attractive for HVDC applications.

The hybrid IGBT-based DC CB (HCB) offers benefits of the above two technologies [8]-[9]. Low-loss operation in closed state is achieved using mechanical branch to conduct load current while a semiconductor valve provides fast current breaking capability. The main valve is a critical HCB component, and it is similar to one of the 6 valves in a typical VSC HVDC converter station [10]. If bidirectional current interruption is required, then two main valves are needed.

In all publications on hybrid DC CB [8]-[9], bidirectional device is assumed, however it is clear that a unidirectional version is feasible and will be available as a commercial product. The performance requirements for each project will specify if unidirectional or bidirectional HCB is needed.

Reference [11] presents slightly different HCB based on full-bridge cells in the main valve, which has bidirectional interruption capability. Unidirectional version could be developed using less-expensive half-bridge cells.

Reference [12] recognizes that there is potentially significant cost saving if a unidirectional main valve is used. It proposes a new bidirectional HCB where the main branch consists of a single HV IGBT valve and 4 HV diode valves under the assumption that diode valve is considerably less expensive and has better reliability than IGBT valve. Nevertheless this HCB requires 4 diode valves rated for line voltage which will have substantial size and weight despite its presumed lower cost.

The high-cost (bidirectional) main breaker branch of HCB can be shared between two HCBs on two nearby lines in a DC substation as it is analyzed in [13].

Driven by the potential for significant HCB simplification, this paper examines further solutions for a bidirectional hybrid DC CB. The primary goal is to reduce semiconductor count, but also to analyse performance and reliability compromises required with each topology. The findings will be illustrated using PSCAD modeling, but also confirmed on a *900 V, 500 A* laboratory DC CB hardware demonstrator.

## II. Application for bidirectional HCB

### A. *Unidirectional DC CB*

Fig. 1 shows schematic for a unidirectional hybrid DC CB. It includes a unidirectional load commutation switch (LCS) and unidirectional main valve, while all other components are identical as in bidirectional DC CB [9]. The main valve consists of multiple cells which can be individually controlled. The inductor $L_p$ represents parasitic inductance.

Operating principle and control of this DC CB topology is given in [9],[14]. Only a summary is given here. Opening process begins by turning LCS off which commutates current into the main branch. When auxiliary branch current reaches zero, ultrafast disconnector (UFD) $S_1$ begins opening. It fully opens in *2ms*, facilitating HV insulation for the LCS. At this stage $T_2$ turns off transferring current into the energy absorption branch. Once the current through the inductor falls below the residual current limit, residual current breaker (RCB) $S_2$ opens and fully isolates the breaker.

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Unidirectional DC CB may suffice in many applications and potential applications are studied in [15]. As an illustration, Fig. 2 shows a 4-terminal (5-node) DC grid which employs 4 unidirectional DC CBs. As an example, DC CB5_3 would be required to operate only for the shown fault (on cable 53). There is no benefit in having bidirectional operation, not even for back-up protection since AC CBs on each radial line act as back-up protection.

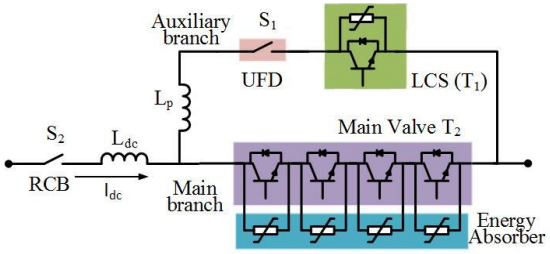


Fig. 1. Unidirectional HVDC CB

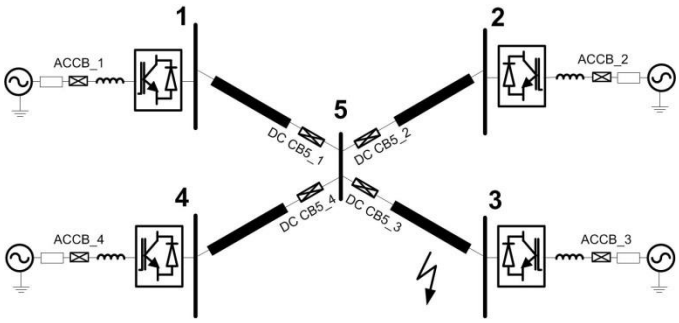


Fig. 2. Radial DC grid with 4 unidirectional HVDC CBs

## B. *Bidirectional DC CB*

A bidirectional HCB will have two main valves as described in [9] and for completeness illustrated in Fig. 3. This topology is very similar to unidirectional topology shown in Fig. 1, the only difference being that both the LCS and main branch are implemented in bidirectional configuration with two valves, doubling the count of semiconductors.

Fig. 4 shows a 4-terminal (6-node) DC grid with a single bidirectional DC CB. In this case the grid has two protection zones (as indicated), and DC CB6_5 would be required to operate for a fault on any location in this DC grid.

However, in most applications in complex DC grids, assuming fully or partially selective protection, primary protection function will be achieved with unidirectional DC CBs. The back-up protection and bus-bar protection, if these are required, will demand bidirectional breaking function of some installed DC CBs.

In the open and closed states, system-level performance of the unidirectional and bidirectional DC CB types is essentially the same as they block or conduct current in both directions. Bidirectional current blocking of open HCB is achieved by having RCB open. Meanwhile, antiparallel diodes in the LCS ensure that current can flow in both directions through the auxiliary branch when the breaker is closed.

The main difference between the two topologies is the inability of a unidirectional HCB to open under current in both directions. As shown in Fig. 1, IGBTs of both LCS and $T_2$ carry the current in only one direction while antiparallel diodes carry it in the other.

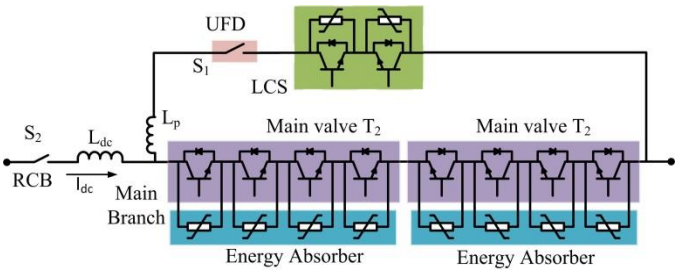


Fig. 3. Bidirectional HVDC CB with 2 main valves (topology 1)

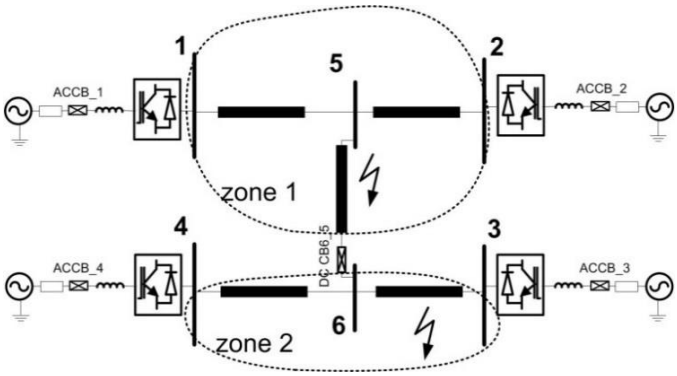


Fig. 4. DC grid with a bidirectional HVDC CB

In order to break current in both directions, both the auxiliary and main branch need to have bidirectional blocking capability. Since LCS is typically implemented as a 3x3 matrix of IGBT modules [16] and thus constitutes a very small portion of the total DC CB cost, bidirectional blocking capability of the auxiliary branch is achieved by simply adding another LCS facing the opposite direction. With this arrangement, operating time and control of the auxiliary branch remain unaffected, however, conduction losses are increased compared to unidirectional topology.

On the other hand, achieving bidirectional blocking capability of the main branch requires two main valves which leads to higher cost, size and weight compared to unidirectional solution. The HCB with two main valves as shown in Fig. 3, will be labelled topology 1. Two new topologies will be investigated:

1. Unidirectional main valve with 2 UFDs (topology 2)
2. Unidirectional main valve with 4 UFDs and 4 LV switches (topology 3).

# III. Unidirectional Main Valve with 2 UFDs

## A. *Topology description*

Fig. 5 shows bidirectional HCB with a single main valve and 2 double-throw UFDs. The bidirectional breaking capability is achieved using double-throw UFDs $S_3$ and $S_4$ to route the current in the positive direction through $T_2$ regardless of the line current direction. $S_3$ and $S_4$ are controlled simultaneously and have two positions, 0 and 1. If DC current $I_{dc}$ is positive then position 1 directs current $I_{T2}$ in positive direction through T2. If $I_{dc}$ is negative, then position 0 directs current $I_{T2}$ in positive direction through $T_2$. The justification for this topology is that cost of two UFDs (mechanical devices) is expected to be favorable compared to cost of a full main valve $T_2$. The UFDs

$S_3$ and $S_4$ are similar to $S_1$, and are assumed to operate in *2ms* [17], except that double throw contacts are employed.

A schematic of double-throw UFD is shown in Fig. 6. The switch topology is similar to a conventional single-throw UFD, which has Thomson coils (TCs) to move actuator disks in both directions [17]. Similarly as single throw UFD, the double-throw UFD has two positions. The difference is only in the contact assembly, since one of the rods has two sets of contacts attached to it, also known as throws.

There have been no reports of double-throw UFDs being manufactured for HV applications. However, given the similarities with single-throw UFDs which have been built and tested at high voltage [8],[11],[17], it is unlikely that any major obstacles would be encountered in making these devices.

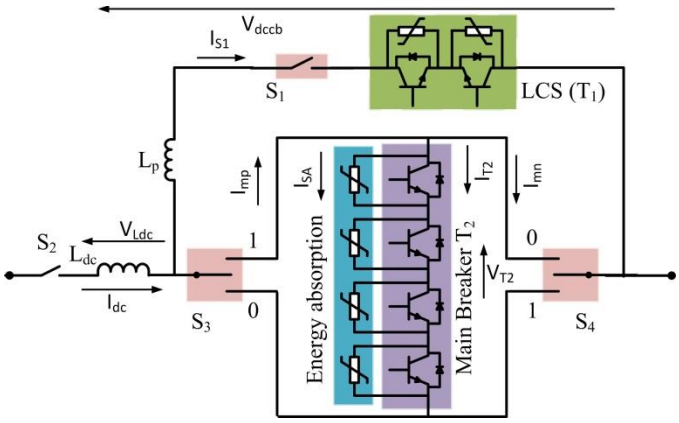


Fig. 5. Bidirectional HVDC CB with single main valve and 2 UFDs (topology 2)

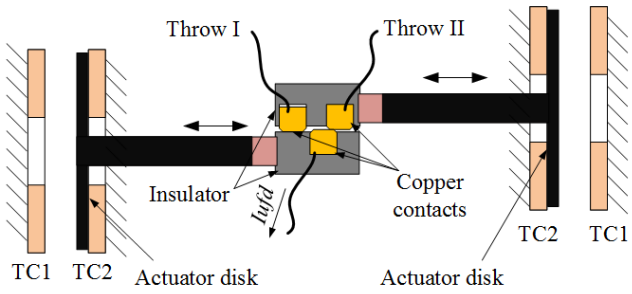


Fig. 6. Single pole, double-throw UFD schematic

## B. *Control logic*

Control system for this topology is shown in Fig. 7. The control signals for mechanical switches are named $S_1 \ldots S_4$ while feedback (status) signals are named $S_{1s} \ldots S_{4s}$ (open - 0, closed - 1). Control signals of semiconductor switches, as well as current measurements, are show in Fig. 5.

The protection relay will normally be sending one signal to HCB [14], denoted as $K_{grid}$ in Fig. 7. The block "directional logic" uses current, voltage and switch position measurements (switch positions $S_{3s}$ and $S_{4s}$, line current $I_{dc}$, inductor voltage $V_{Ldc}$ and voltage across the whole HCB $V_{DCCB}$) to determine if DC CB is oriented in the expected direction of current in either opening or closing. This directional HCB logic can be implemented either in relay or in the HCB itself. Not all measurements need to be internal to the breaker. $V_{Ldc}$ is only used to determine the sign of $I_{dc}$ differential which can also be

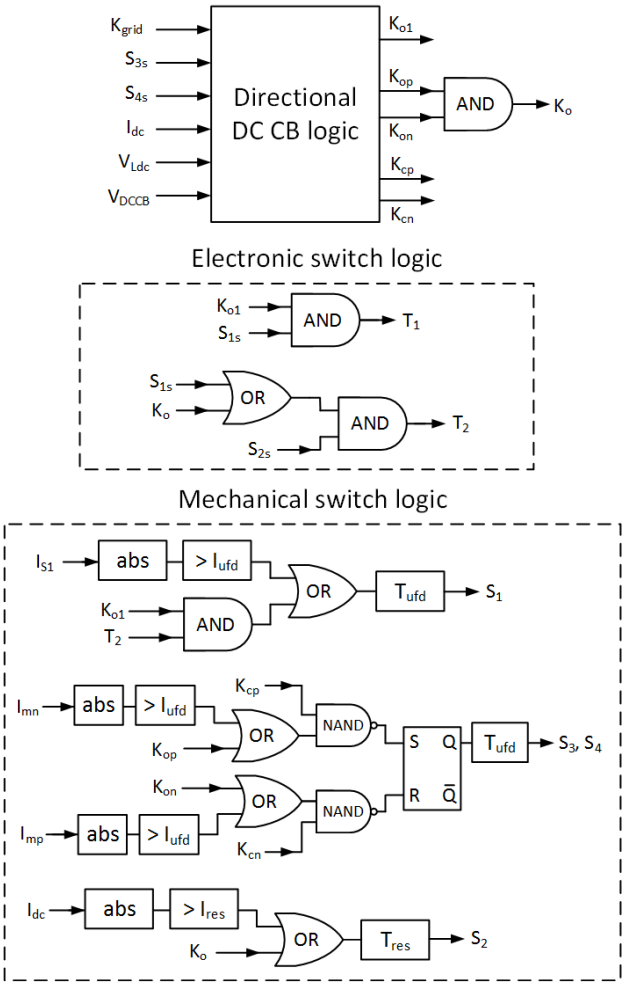


Fig. 7. Control logic of bidirectional HCB with single $T_2$ and 2 UFDs

obtained directly from $I_{dc}$ measurements. The sign of $V_{DCCB}$ is used to determine the closing direction of the breaker and this measurement can be obtained as a difference between cable and DC bus voltage. Once the direction is determined, internal opening ($K_{o1}$,$K_{op}$,$K_{on}$) and closing ($K_{cp}$,$K_{cn}$) signals are generated. The opening sequence is as follows:

1. $K_{grid}$ is set to zero which initiates HCB opening.
2. Directional logic determines the opening direction. Setting $K_{op}$ or $K_{on}$ to 0 initiates opening in the positive or negative direction respectively.
3. If the sign of $I_{dc}$ corresponds to the sign of $V_{Ldc}$ (indicates current differential) and $S_3$ and $S_4$ are aligned in the desired opening direction, $K_{o1}$ is set to 1 which opens $T_1$. This logic ensures that the current will not change direction if commutated into $T_2$, as well as that $S_3$ and $S_4$ have finished moving.
4. If sign of $I_{dc}$ differs from the sign of $V_{Ldc}$, opening of $T_1$ is delayed, since this indicates that current will change direction. When current crosses zero, the opening process continues normally.
5. If $S_3$ and $S_4$ are not oriented in the direction of (fault) current, a command is issued to change the position. The position change of $S_3$ and $S_4$ takes *2 ms* ($T_{ufd}$).
6. Once the opening criteria for the auxiliary branch are satisfied, $T_1$ is turned off and current commutates into the main branch. When current through $S_1$ falls below its

chopping capability $I_{ufd}$ (assumed as 1 A [17]) $S_1$ opening command is given and it opens in *2 ms*.

$T_2$ turns off as soon as confirmation is received that $S_1$ is open. Current commutates into the energy absorption branch which isolates the fault.

7. $S_2$ opens when the residual current falls below the limit $I_{res}$ (assumed as *10 A*). This step takes around *30 ms* ($T_{res}$).

The closing sequence is:

1. $K_{grid}$ is set to 1 which initiates the closing sequence. Closing direction is determined from the sign of $V_{DC\,CB}$.
2. $S_3$ and $S_4$ are directed to the corresponding position by setting $K_{cp}$ or $K_{cn}$ to 0.
3. Closing command is sent to $S_2$ which closes in *30 ms*.
4. Upon receiving confirmation that $S_2$ is closed, $T_2$ turns on at which point DC CB starts conducting.
5. Closing of main valve initiates *2 ms* closing of $S_1$.
6. Upon receiving confirmation that $S_1$ is closed, $T_1$ turns on and current commutates into the auxiliary branch.

The total opening time of this topology is either *2* or *4 ms*, depending on the initial orientation of $S_3$ and $S_4$ with respect to the fault current direction. Faster opening is achieved if the two are aligned since $S_3$ and $S_4$ do not operate. $S_3$ and $S_4$ do not carry any current in closed state and can be manipulated. This can be used to an advantage by maintaining $S_3$ and $S_4$ orientation in the direction with higher probability of fault occurrence, such as towards the cable rather than a DC bus. Nevertheless, $L_{dc}$ needs to be dimensioned for the worst-case scenario (*4 ms* opening) which implies a twofold increase in installed series inductance compared to topology 1.

### C. *Simulation results*

PSCAD Simulation results for a *320 kV, 16 kA* HCB with 2 UFDs are shown in Fig. 8. Main breaker parameters are given in Table II in the appendix. Fault is applied at *0.3 s* in the negative direction (to study worst case) while trip order is given when line current exceeds *8 kA*. $S_3$ and $S_4$ are initially in position 0 which requires change in orientation and results in *4 ms* breaker opening time. The results verify opening sequence described in section III. A. Fig. 8 (c) shows that load current $I_{dc}<0$, but current in the main branch $I_{T2}>0$. Voltage spike appearing across $T_1$ is caused by parasitic inductance $L_p$ as analyzed in [16] and is limited by the $T_1$ surge arrester. Fig. 8 (e) shows that all three UFDs block the same voltage (voltages across $S_3$ and $S_4$ are given for the positive throw).

### D. *Laboratory hardware demonstration*

Experimental verification of topology 2 has been carried out using *900 V, 500 A* DC CB test circuit and HCB prototype, described in [18]. The main breaker parameters are given in Table III in the appendix. The low-voltage disconnector $S_1$ is described in some detail in [19], and two similar double throw UFDs $S_3$ and $S_4$ are fabricated as shown in Fig. 9.

Fig. 10 shows the component testing results for a single-pole double-throw UFD. The Thomson coil current shows approximately *2900A* peak, which is required for fast opening. Both throws are energized with a low voltage of *2 V* through *4* Ω resistors giving around *0.5 A* in conducting state, which is the current level that UFD can interrupt. The two signals represent voltage measured across the resistors on each position of the UFD. It is seen that total operating time is around *2 ms*. Because of lateral contact overlap, UFD remains a closed circuit for approximately *0.4 ms* after the pulse is given, and it starts arcing *0.4 ms* before the final closed state.

Current breaking operation of the topology 2 HCB prototype is demonstrated in Fig. 11. $S_3$ and $S_4$ are initially oriented in the opposite direction from the fault to simulate worst-case scenario. Because of negative current, $T_1$ conducts for the first *2 ms* while $S_3$ and $S_4$ reconfigure positions. After $S_3$ and $S_4$ change position, $T_1$ turns off and current commutates into the main branch. It takes additional *2 ms* for $S_1$ to open. The total time for voltage to recover is *4 ms*, and then it takes additional *4 ms* for current to reduce to zero.

The applied DC voltage is *900V*, while peak voltage stress on switches is limited to *1500V* by the energy absorbers. The authors have obtained these encouraging results on low-voltage prototypes only, and further tests at higher voltages and currents would be required as the next development step.

## IV. Unidirectional Main Valve with 4 UFDs and 4 LV Switches

### A. *Topology description*

Fig. 12. shows bidirectional HCB topology where main branch consists of a single $T_2$ valve, *4* UFDs and *4* LV (low

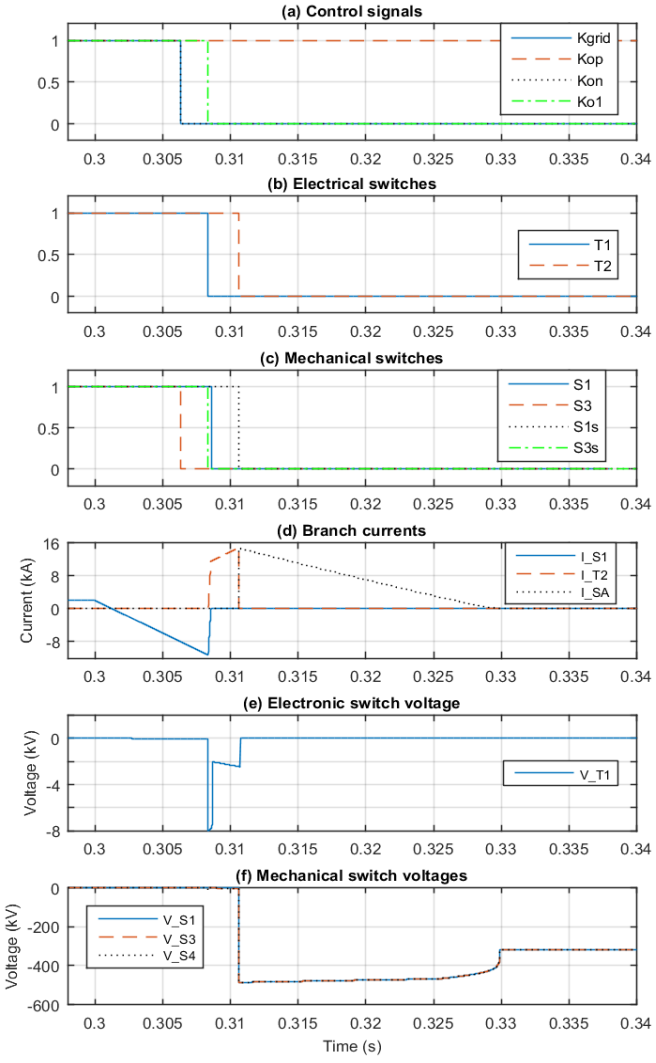


Fig. 8. Opening of DC CB topology 2 under negative fault current

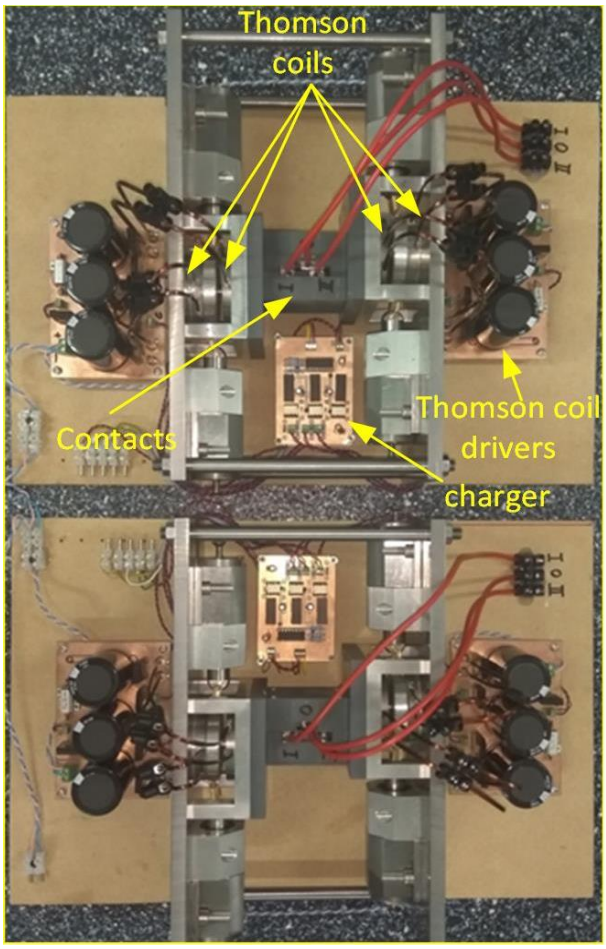


Fig. 9. Two single-pole double throw UFDs.

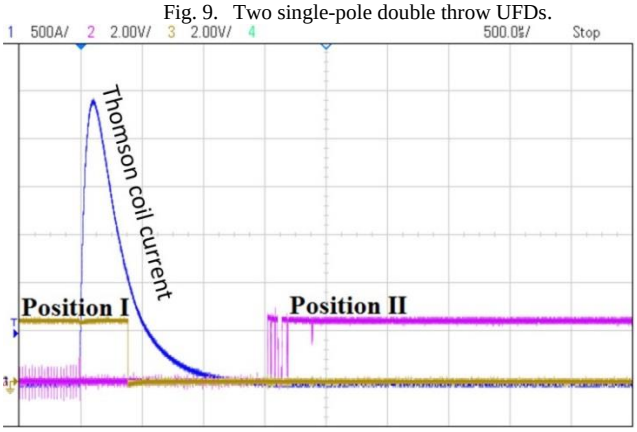


Fig. 10. Testing of single-pole double throw UFD. Current: 500A per division. Position I and II: 2V per division.

voltage) switches (diodes). LV switches are oriented in pairs ($D_{p1}$-$D_{p2}$ and $D_{n1}$-$D_{n2}$) and used to route the current through the main branch. The arresters across diodes are placed to eliminate voltage spikes at switching, similarly as with LCS, and have no energy absorption requirement. If load current is positive, diodes $D_{p1}$ and $D_{p2}$ direct current through $T_2$ in the positive direction. If load current is negative, $D_{n1}$ and $D_{n2}$
direct current through $T_2$ in the positive direction. Once the current direction is established, UFDs of non-conducting LV switches open to provide HV insulation before $T_2$ turns off. Diodes take full current stress (no voltage blocking) while UFDs take full voltage stress (no current interruption). This

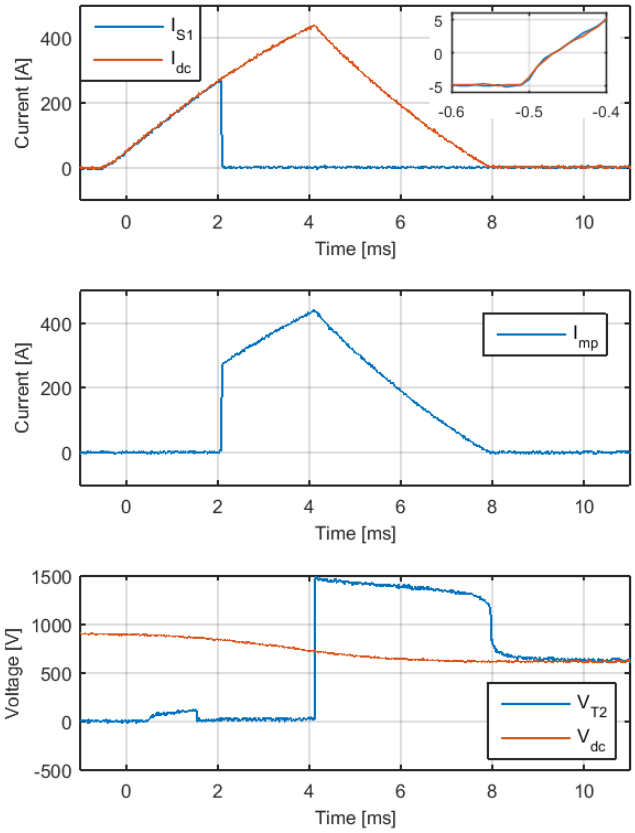


Fig. 11. Experimental test response of topology 2.

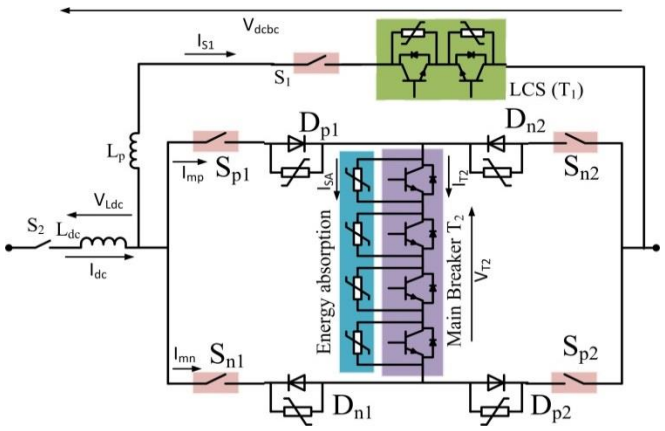


Fig. 12. Bidirectional HVDC CB with a single main valve, 4 UFDs and 4 LV switches (topology 3).

arrangement will have substantially lower semiconductor count compared with 4 HV-rated diode valves in [12].

A major advantage of this approach, compared with topology 2, is that UFDs in the main branch operate simultaneously with the auxiliary branch UFD $S_1$ so the total opening time remains *2ms* (same as for topology 1).

### B. *Control logic*

The control system is shown in Fig. 13. Since all four UFDs in the main branch are closed in normal (closed) operation, current is redirected using diodes and directional logic is simpler than with topology 2. The opening sequence is:

1. $K_{grid}$ is set to zero which instructs HCBB to open. Opening direction is determined from the sign of $V_{Ldc}$. Once the sign

of $I_{dc}$ becomes equal to the sign of $V_{Ldc}$, opening sequence is initiated by setting $K_{op}$ or $K_{on}$ to 0.
2. As $T_1$ turns off, current commutates into the main branch. When current through UFD falls below their breaking capability $I_{ufd}$, opening command is given to $S_1$ and 2 of UFDs in the main branch. $S_1$ opens simultaneously with $S_p$ or $S_n$ pair so the whole process takes only *2 ms*.
3. $T_2$ turns off as soon as confirmation is received that $S_1$ and $S_p$ or $S_n$ are fully open. Current commutates into the energy absorption branch which isolates the fault.
4. $S_2$ opens when line current falls below the limit $I_{res}$.
5. The remaining main branch UFDs open when their current falls below $I_{ufd.}$

The closing sequence of topology 3 is:

1. $K_{grid}$ is set to 1. Depending on the sign of $V_{DC\ CB}$, current direction is determined and corresponding signals $K_{cp}$ or $K_{cn}$ are set to 0.
2. Closing command is sent to $S_2$ which closes in 30 ms.
3. Upon receiving confirmation that $S_2$ is closed, closing signal is sent to either $S_p$ or $S_n$ pair depending on the closing direction.
4. When either UFD pair closes $T_2$ turns on. HCB starts conducting at this point.
5. Closing of main valve triggers simultaneous closing of $S_1$ and the remaining $S_p$ or $S_n$ pair. This takes 2 ms.
6. Upon receiving confirmation that $S_1$ is closed, $T_1$ turns on and current commutates into the auxiliary branch.

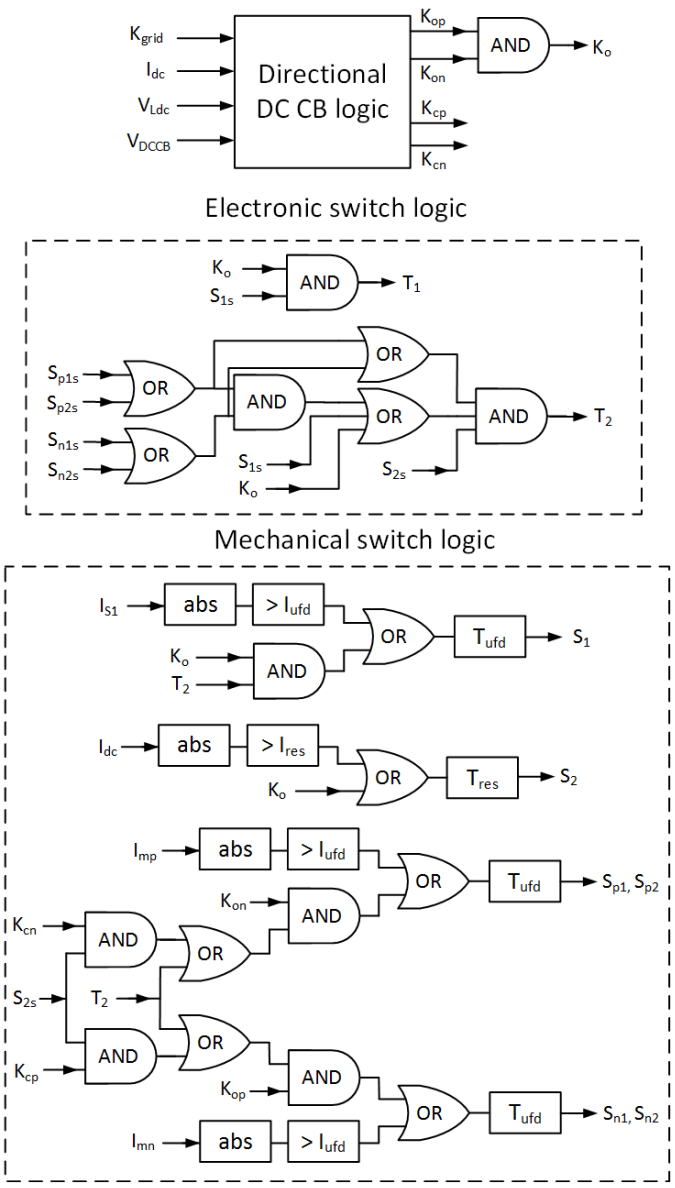


Fig. 13. Control logic for bidirectional HVDC CB with single T2, 4 UFDs and 4 LV switches.

The total opening time for topology 3 is *2 ms* irrespective of fault direction which is a significant improvement compared to topology 2. Since opening time does not differ from topology 1, $L_{dc}$ size remains the same. As visible from Fig. 12, the energy absorption branch can be fully isolated using four main branch UFDs. Depending on the V-I characteristic of the main surge arrester, $S_2$ could be omitted from this topology if arrester leakage current is below UFD chopping current $I_{ufd.}$

On the downside, this topology requires 5 UFDs, and each of the 4 additional UFDs will have 2 bushings which increases space requirement. However, size and weight have not been analyzed in any depth in this article.

### C. *Stresses on diodes*

Diodes are crucial new components in this topology, and their stresses will determine cost-effectiveness of this topology. The diodes conduct while $T_2$ conducts but also while energy absorber conducts. The peak current stress is same as for $T_2$, i.e. peak interrupting current (*16kA* for the test system). They do not take load current. The diodes therefore conduct for *10ms-20ms* at most and their thermal stress is larger than on $T_2$. The simplest thermal management would be to install multiple parallel diodes to avoid forced cooling.

The peak voltage stress happens at the instant when current is commutated from the auxiliary branch to the main branch. The two diodes that do not conduct will experience reverse voltage equal to the voltage drop across $T_2$ at the commutation. The calculation of voltage stress on LCS is presented in detail in [16], and a similar procedure can be used. However, parasitic inductances $L_p$ and others have no impact since diodes do not have fast turn off, and the expected peak voltage stress for *320kV* HCB is *2-3kV*.

The operating instant when $T_2$ turns off should be carefully analyzed since the peak current is commutated from $T_2$ to the energy absorber (with substantially higher voltage), while diodes should continue to conduct. This is very unusual operating condition for diodes, and the diode current should remain higher than the holding current (in tens of Ampere). In case when HCB is interrupting very low current, diode current may drop below holding current and diodes may turn off before UFD opens. The arresters across diodes ensures that in such case any voltage spike will not destroy diodes.

### D. *Simulation results*

The opening process of a *320 kV, 16 kA* topology 3 HCB is shown in Fig. 14, using identical test as for topology 2.

Main breaker parameters are given in Table II in the appendix. Simulation results show that DC CB opens in *2 ms* irrespective of fault current direction. It is seen that the voltage across diodes remains low.

Closing process in the positive direction is shown in Fig. 15. Control signals are not shown since the closing command ($K_{grid}$=1) is given at 0.4 s (outside of the time range). Line current commutation into and from the main branch is smooth and no overvoltages appear across LV switches.

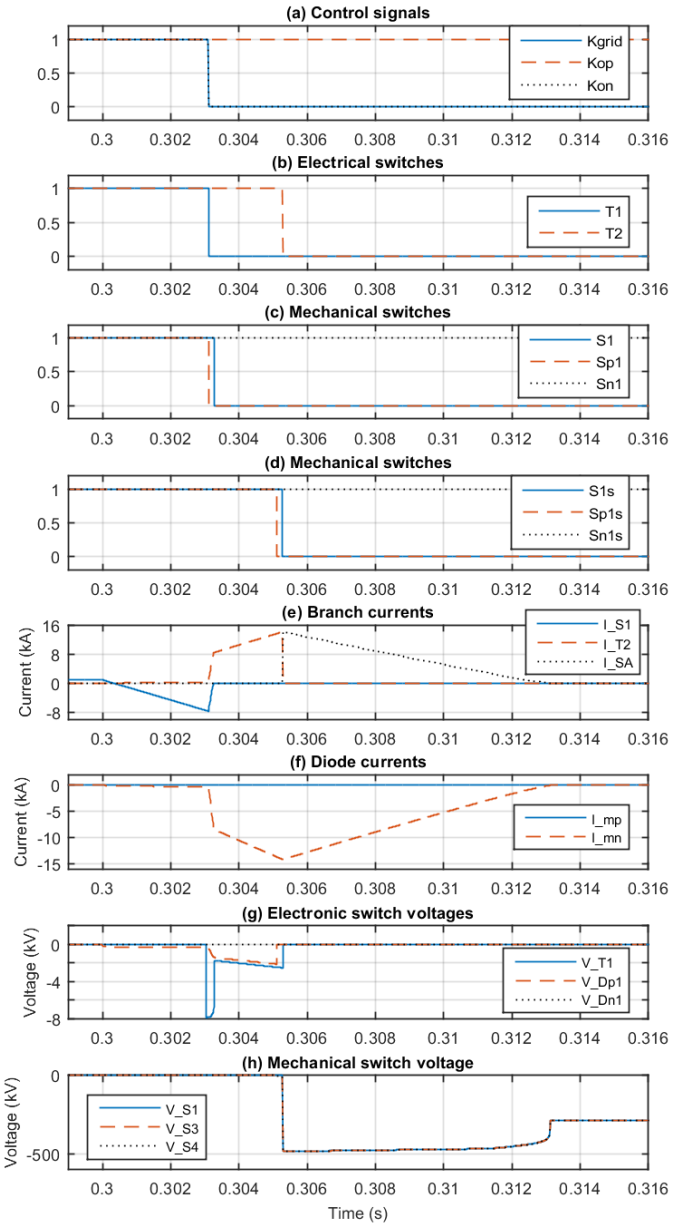


Fig. 14. Opening of topology 3 under negative fault current

## E. *Laboratory demonstration*

A photograph of 4 diodes (ON Semi RURG8060, *600V, 80A*) with their arresters is shown in Fig. 16. Low voltage (*130V, EPCOS B72240B0750K001*) arresters are used to confirm that proposed DC CB operates well with low diode voltage stress.

The test response of hardware HCB topology 3 is shown in Fig. 17. All parameters are given in Table III in the appendix.

Since current measurements are performed using a combination of AC and DC probes, the curves do not perfectly overlap. The additional diode resistance also causes some difference compared with the other topologies. Nevertheless, test results demonstrate that the opening time is identical to the bidirectional HCB with two main valves. Voltage measurements across UFDs confirm they are fully open when the main valve turns off.

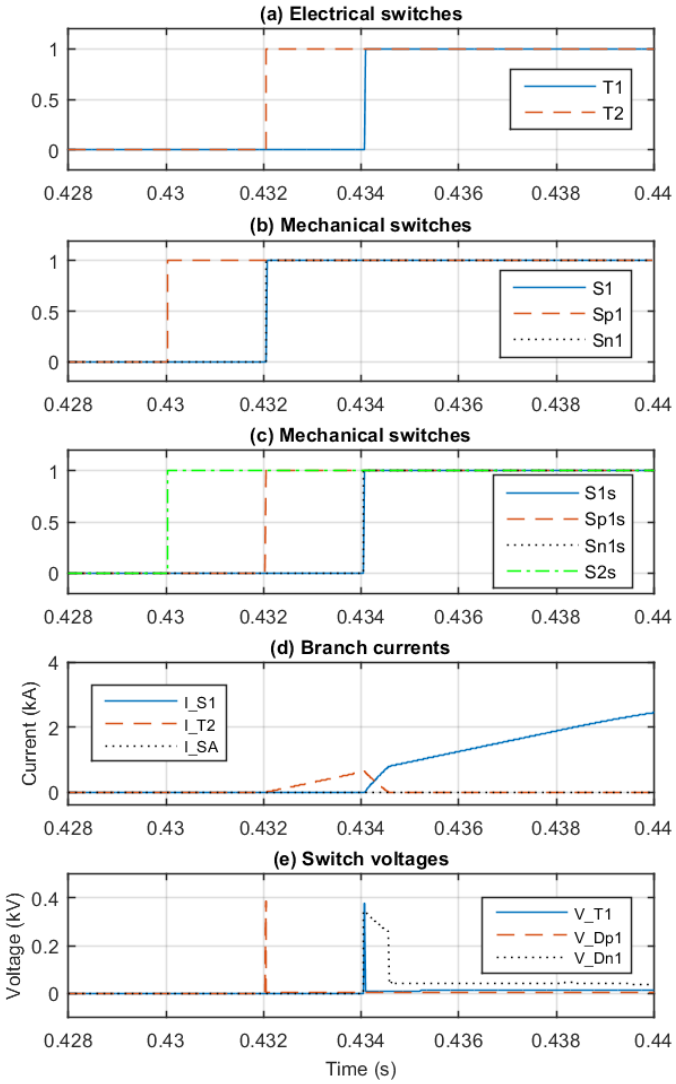


Fig. 15. Simulation of closing sequence of topology 3

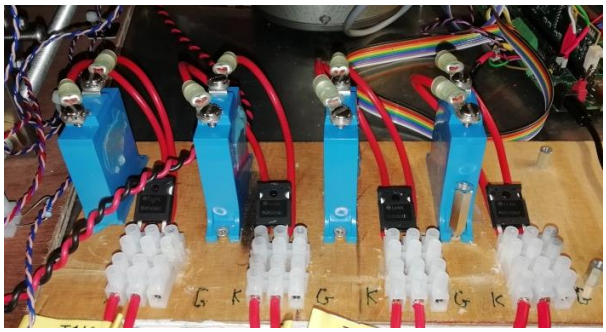

Fig. 16. 4 ON Semi diodes and arresters in topology 3

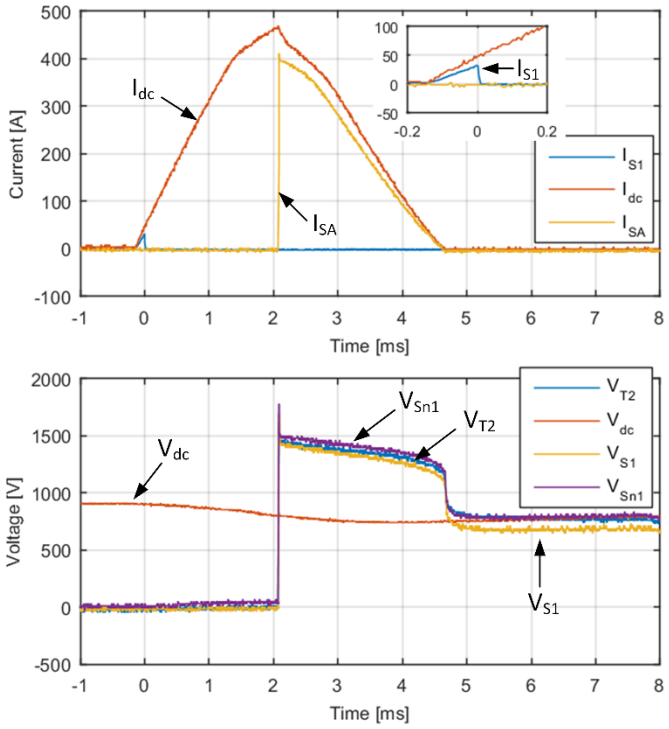


Fig. 17. Experimental test response of topology 3

## V. Comparison of Topologies

Comparison between the three bidirectional HCB topologies is given in Table I. Topology 2 is the most cost-effective with the lowest number of components (electrical and mechanical). However, since opening time may be twice as long compared to the other two topologies (depending on current direction), it requires double the series inductance (to ensure adequate peak current) which also implies double the energy rating of energy absorbers. Also, this topology demands development of new device, double-throw UFD. This topology is nevertheless substantially more cost-efficient than topology 1 because of the lower number of semiconductors.

Topology 3 is the most attractive topology, offering identical system-level performance as topology 1 at half the number of semiconductors. Since topology 2 requires over-dimensioning of DC inductor and surge arresters, topology 3 would likely have the lowest overall cost.

Considering of immaturity of HCB technology, it is reasonable to expect higher UFD failure rate compared to electronic switches. Moreover, modular design of the HV valve and LCS makes them tolerant to single component failure whereas the same does not apply for UFDs. Topology 1 can therefore be considered the most reliable since it contains the least amount of critical components (only a single UFD).

With topologies 2 and 3, HCB might still operate if one (or in some cases even two) main branch UFDs malfunction, however, it can do so in only one direction.

Table I Comparison of bidirectional HVDC CB.

| | Two $T_2$ valves | 2 UFDs | 4 UFDs, 2 thyristors |
|---|---|---|---|
| Operating time | 2 ms | 2-4 ms | 2 ms |
| HV valve | 2 | 1 | 1 |
| LCS | Bidirectional | Bidirectional | Bidirectional |
| UFDs | 1 | 3 | 5 |
| Diodes | 0 | 0 | 4 |
| Inductor | 100 mH | 200 mH | 100 mH |

## VI. Conclusion

Three bidirectional HCB topologies are analyzed in this paper. Topology 1 uses two HV valves which substantially increases semiconductor count, size and weight compared to a unidirectional HCB. The newly proposed bidirectional topology 2 uses only a single HV valve with two double-throw UFDs. However, it is concluded that the opening time in the worst-case scenario is doubled. The proposed topology 3 uses a unidirectional IGBT valve with additionally 4 UFDs and 4 diodes. This topology offers the same system-level performance as topology 1 but with half the number of semiconductors. On the other hand, increased number of mechanical components makes topologies 2 and 3 less reliable than topology 1. The experimental results on *900V 500A* DC CBs have confirmed theoretical findings.

## VII. Appendix. 320kV, and 900V test systems

Table II Parameters of the 320kV, 16kA HCB.

| SL.NO. | PARAMETER | VALUE |
|---|---|---|
| 1 | Voltage rating | 320 kV |
| 2 | Current rating | 2 kA |
| 3 | Maximum Breaking current | 16 kA |
| 4 | UFD operation time | 2 ms |
| 5 | Limiting inductor $L_{dc}$ (topology 2) | 200 mH |
| 6 | Limiting inductor $L_{dc}$ (topology 3) | 100 mH |
| 7 | Parasitic inductance $L_p$ | 0.2 mH |

Table III Parameters of the 900V, 500A HCB.

| SL.NO. | PARAMETER | VALUE |
|---|---|---|
| 1 | Voltage rating | 900 V |
| 2 | Current rating | 30 A |
| 3 | Maximum Breaking current | 500 A |
| 4 | UFD operation time | 2 ms |
| 5 | Limiting inductor $L_{dc}$ (topology 2) | 7 mH |
| 6 | Limiting inductor $L_{dc}$ (topology 3) | 3.5 mH |

## VIII. Acknowledgment

The authors are thankful to Mr R. Osborne for help with the experimental studies.

## IX. References

[1] D Jovcic and K Ahmed "High Voltage Direct Current Transmission: Converters Systems and DC Grids", Wiley, 2015.

[2] CIGRE joined WG A3 and B4.34 "Technical Requirements and Specifications of State of the art HVDC Switching Equipment" CIGRE brochure 683, April 2017.

[3] K. Tahata, S. Oukaili, K. Kamei, et al., "HVDC circuit breakers for HVDC grid applications," Proc. IET ACDC 2015 conference, Birmingham, UK, pp. 1-9, Feb 2015.

[4] T. Eriksson, M. Backman, S. Halen, A low loss mechanical HVDC breaker for HVDC grid applications, B4-303, CIGRE 2014, Paris.

[5] L Ängquist at all, "Design and test of VSC assisted resonant current (VARC) DC circuit breaker" 15th IET International Conference on AC and DC Power Transmission (ACDC 2019), Coventry, UK, Feb. 2019.

[6] W. Grieshaber, J. Dupraz, D. Penache, et al., “Development and Test of a 120kV direct current circuit breaker,” Proc. CIGRÉ Session, Paris, France, pp. 1-11, Aug 2014.

[7] A. Shukla and G. Demetriades, “A survey on hybrid circuit-breaker topologies,” IEEE Trans. Power Del., 30, (2), pp. 627-641, 2015.

[8] R.Derakhshanfar et al, “Hybrid HVDC breaker – A solution for future HVDC system” CIGRE paris 2014, B4-304.

[9] Häfner, J., Jacobson, B.: ‘Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids’. Proc. CIGRE 2011 Bologna Symp., Bologna, Italy, Sep 2012, pp. 1-7

[10] CIGRE WG B4.52 “Feasibility of HVDC grids” *CIGRE technical brochure 533, Paris, April 2013*

[11] G.F. Tang, X. G. Wei, W.D. Zhou, S. Zhang, C. Gao, Z.Y. He, J. C. Zheng “Research and Development of a Full-bridge Cascaded Hybrid HVDC Breaker for VSC-HVDC Applications”, A3-117, CIGRE Paris 2016

[12] B. Yang, D. Cao, W. Shi, W. Lv, W. Wang, B. Liu, “A novel commutation-based hybrid HVDC circuit breaker”, CIGRE B4 colloquium, Winnipeg, October 2017.

[13] Chuanyue Li, Jun Liang, and Sheng Wang, “Interlink Hybrid DC Circuit Breaker”, IEEE Transactions on industrial electronics, vol. 65, no. 11, November 2018.

[14] W. Lin, D. Jovcic, S. Nguefeu and H. Saad, “Modelling of High Power Hybrid DC Circuit Breaker for Grid Level Studies,” IET Power Electronics, Vol. 9, issue 2, February 2016, pp 237-246

[15] A. Jehle, D. Peftitsis, and J. Biela, “Unidirectional hybrid circuit breaker topologies for multi-line nodes in HVDC grids,” in Proc. 18th Eur. Conf. Power Electron. Appl., Karlsruhe, Germany, 2016,pp. 1–10

[16] Hassanpoor, A., Häfner, J., Jacobson, B.: ‘Technical assessment of load commutation switch in hybrid HVDC breaker’, IEEE Transactions on Power Electronics, 2015, 30, (1), pp. 5393-5400

[17] P. Skarby and U. Steiger, “An Ultra-fast Disconnecting Switch for a Hybrid HVDC Breaker– a technical breakthrough”, Proc. CIGRÉ Session, Alberta, Canada, pp. 1-9, Sep 2013

[18] M Hedayati and D. Jovcic “Reducing peak current and energy dissipation in hybrid HVDC CBs using Disconnector voltage control” IEEE Transactions on Power Delivery, Vol 33, isue 4, pp 2030-2038.

[19] M. Hedayati, D. Jovcic “Low Voltage Prototype Design, Fabrication and Testing of Ultra-Fast Disconnector (UFD) for Hybrid DC CB” CIGRE B4 colloquium, Winnipeg October 2017

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