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# Steep Slope Field-Effect Transistors With B–Te-Based Ovonic Threshold Switch Device

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**ABSTRACT** In this letter, a new ovonic threshold switch (OTS) device based on simple binary Boron–Tellurium (B–Te) film is developed and implemented in series with the source region of a transistor. The newly developed B–Te-based device shows excellent characteristics such as low operating voltage, low leakage current, abrupt turn-on/off slope, fast switching speed, high endurance, and high thermal stability. Due to the great properties of the B–Te OTS device, the implemented transistor exhibits subthreshold swing less than 10 mV/dec and high on/off current ratio greater than  $10^5$ . Moreover, we present a direction of implementing an ideal transistor based on simulation results explaining the effect of off-state resistances and threshold voltages of the OTS devices on the  $I_{DS}$ - $V_{GS}$  characteristics of the implemented transistor.

**INDEX TERMS** Threshold switching, field-effect transistor, steep slope, subthreshold slope, ovonic threshold switch.

## I. INTRODUCTION

To achieve an ultra-low power FET, a transistor with extremely steep subthreshold swing (SS) less than 10 mV/dec, low leakage current and low operating bias must be developed. However, the fundamental limitation of the SS in a conventional MOSFET is 60 mV/dec at room temperature by Boltzmann's theory which acts as a huge barrier for lowering the operation voltages [1], [2]. To overcome this barrier, a concept of hyper-FET based on insulator-to-metal transition (IMT) material ( $\text{VO}_2$ ) was reported which showed enhanced SS less than 8 mV/dec. However, hyper-FET has difficulties in achieving low leakage current and low operating bias condition which come from the electrical characteristics of the  $\text{VO}_2$  [3]. To solve these problems, many groups have proposed replacing the  $\text{VO}_2$  with an electrochemical metallization (ECM) type threshold switching (TS) device with an extremely high off-state resistance [4]–[6], but this type of device also has problems such as the voltage-time dilemma and the slow turn-off speed which hinder its practical application as a transistor [7], [8].

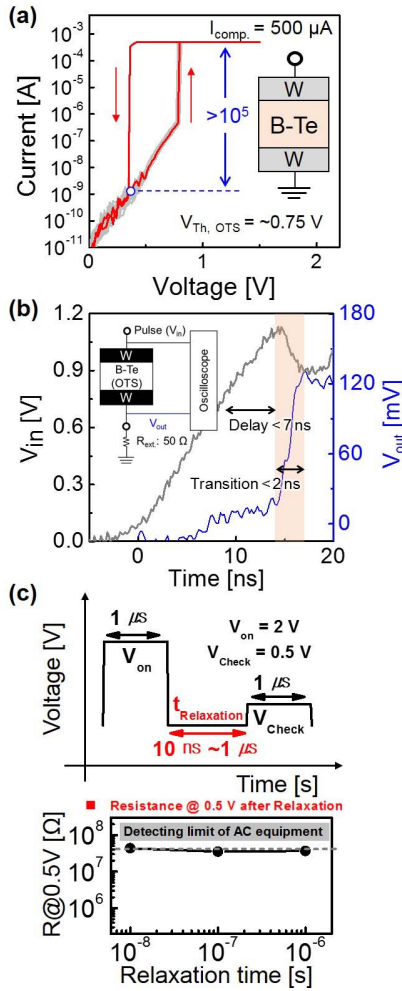
Recently, Ovonic Threshold Switch (OTS) devices which exhibit fast switching speed and low leakage current have attracted much attention as devices that can replace the other

TS devices [9]–[13]. However, these devices cannot be used to implement a steep slope transistor due to their material complexity, high operating voltage, and low thermal stability issues.

In this letter, we first demonstrate a Boron-Tellurium (B-Te) based binary OTS device [14] with excellent characteristics such as low operating voltage, low leakage current, sharp switching slope, fast switching speed, high endurance, and high thermal stability. Subsequently, we present a steep slope field-effect transistor (FET) using the newly developed OTS device instead of the  $\text{VO}_2$  device in the concept of hyper-FET. Thanks to the great properties of the B-Te based OTS devices, the newly implemented transistor shows subthreshold slope (SS) less than 10 mV/dec and high on/off current ratio greater than  $10^5$ . In addition, a direction to achieve an ideal transistor is provided based on simulation results demonstrating the effect of off-state resistances and threshold voltages of the OTS devices on the  $I_{DS}$ - $V_{GS}$  characteristics of the implemented transistor.

## II. EXPERIMENTS

A newly developed TS device is connected in series with the source side of a transistor, whose gate length is 0.5  $\mu\text{m}$ . For

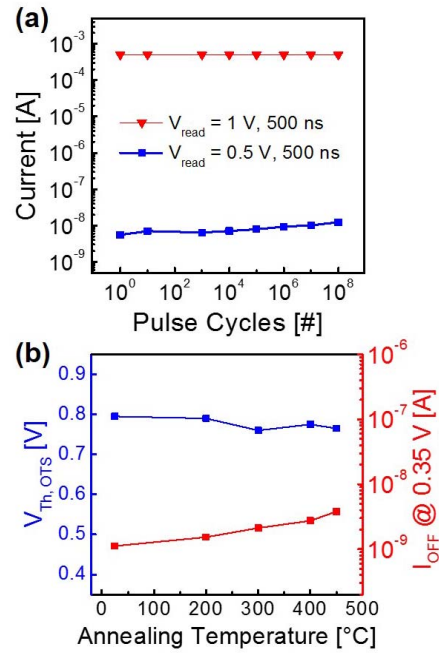


**FIGURE 1.** (a) DC I-V characteristics of W/B-Te/W device showing high on/off current ratio. (b) Turn-on and (c) turn-off transition time of the device faster than 10 ns measured using oscilloscope.

the TS device, we fabricated a W/B-Te/W stacked structure of device using a flat W wafer patterned with cell size of  $(30 \text{ nm})^2$ . For the TS layer, a 12-nm-thick Te-rich boron telluride film ( $B_{0.25}\text{-Te}_{0.75}$ ) was deposited on the prepared wafer by adopting a co-sputtering process using Boron and Tellurium targets. The top W electrode was deposited on the B-Te film by a sputtering process using a tungsten target.

### III. RESULTS AND DISCUSSION

Fig. 1 shows the electrical properties of our new B-Te based OTS device. Fig. 1 (a) illustrates the DC current-voltage (I-V) characteristics of the B-Te based OTS device which exhibits stable threshold switching behaviors at a current compliance of  $500 \mu A$ . The device is initially in high resistance state (OFF-state) which suppresses its leakage current flow at low electric field effectively. However, when an external voltage larger than a specific voltage value called threshold voltage ( $V_{Th, OTS}$ ) is applied on the top W electrode, the OTS phenomenon [15], [16] is triggered in the B-Te switching layer and thus the abrupt current transition

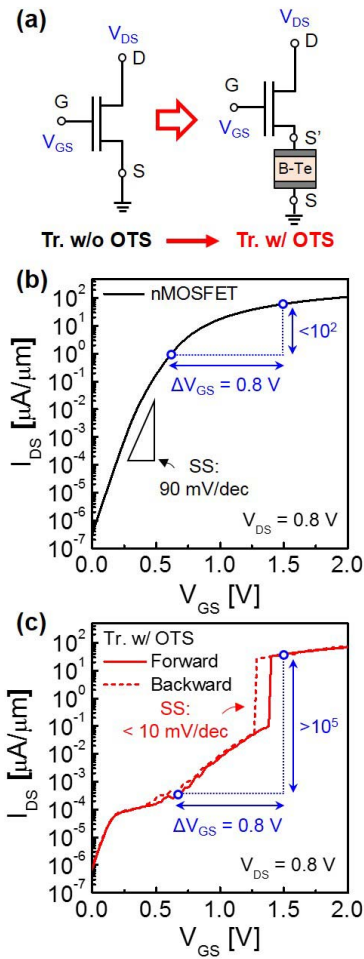


**FIGURE 2.** Reliability test results of the B-Te based OTS device showing (a) high AC endurance up to  $10^8$  cycles and (b) high thermal stability up to  $450^{\circ}C$ .

occurs. By this transition, the resistance of the device suddenly drops by several orders of magnitude. This low resistance state (ON-state), however, is no longer retained when the applied voltage is reduced to a low level and returns to the initial high resistance state. The on-state to off-state current ratio ( $I_{ON}/I_{OFF}$ ) of the B-Te based device resulting from this OTS phenomenon is about  $10^5$  as shown in the figure. Figs. 1(b) and (c) provide information about turn-on/off transition speed of the device measured using oscilloscope. Both of the turn-on/off transition speeds are measured to be faster than 10 ns. This fast switching behavior is due to the electronic nature of the OTS transition that does not involve atomic rearrangements or structural changes [17], [18].

Fig. 2 provides information about the stability of the device under electrical and thermal stresses. The endurance test result shown in Fig. 2 (b) demonstrates the ability of the device to endure  $10^8$  AC cycles with 500 ns program and read speeds without significant degradation. The high stability of the device which exhibits no significant degradation in electrical properties even after the annealing process of  $450^{\circ}C/30$  min is shown in Fig. 2 (c).

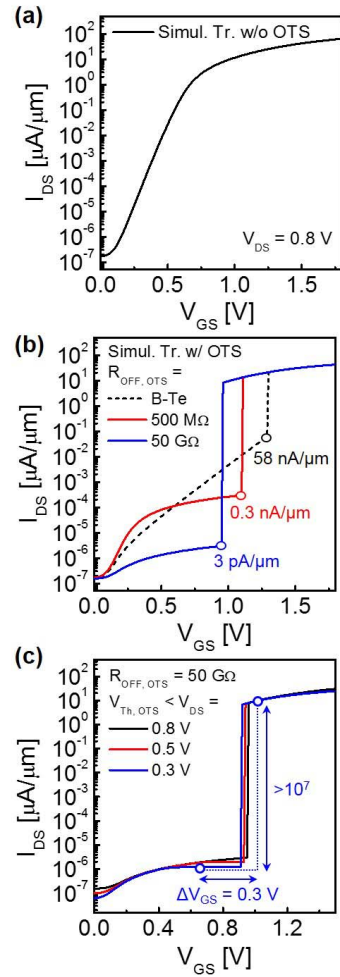
The newly developed B-Te based OTS device is implemented in series with the source region of a normal nMOSFET with gate length and width of  $0.5 \mu m$  and  $5 \mu m$ , respectively, in order to reduce the SS of the transistor. Fig. 3 (a) shows simplified schematics of the transistors without/with the B-Te based OTS device. The drain current versus gate voltage ( $I_{DS}-V_{GS}$ ) characteristics for a transistor without the OTS device and with the OTS device are shown in Fig. 3(b) and (c), respectively. A fixed drain voltage of  $0.8$  V



**FIGURE 3.** (a) Simplified schematics of transistors without/with the B-Te based OTS device.  $I_{DS}$ - $V_{GS}$  characteristics of a transistor (b) without the B-Te based OTS device and (c) with the device. Steep SS of 10 mV/dec and high on/off current ratio of  $10^5$  were confirmed in the implemented transistor.

larger than  $V_{Th,OTS}$  (0.75 V) is applied during the  $I_{DS}$ - $V_{GS}$  sweep. The transistor without the OTS device exhibits normal nMOSFET operation with SS of 90 mV/dec. On the other hand, the transistor with the OTS device show SS less than 10 mV/dec and high  $I_{ON}/I_{OFF}$  greater than  $10^5$  at low supply voltage condition ( $V_{DD} = 0.8$  V) due to the abrupt transition and low leakage current properties of the OTS device. Compared to the conventional transistor which shows  $I_{ON}/I_{OFF}$  less than  $10^2$  under the same  $I_{ON}$  and supply voltage conditions, our new transistor exhibits leakage current reduced by three orders of magnitude.

Despite significant improvements achieved by using our new B-Te based OTS device, the leakage current and the applied drain voltage of the implemented transistor should be reduced to sub-pA/ $\mu$ m and below 0.3 V respectively for ultra-low power applications [19]. To achieve extremely low leakage current, the off-state resistance of the OTS device ( $R_{OFF,OTS}$ ) must be significantly increased. We evaluate the  $R_{OFF,OTS}$  requirements to realize a transistor



**FIGURE 4.** Simulated  $I_{DS}$ - $V_{GS}$  characteristics of a transistor (a) without any external device and (b) with OTS devices having different off-state resistances. Extremely high on/off current ratio greater than  $10^7$  was confirmed for transistor with OTS device having  $R_{OFF,OTS}$  of 50 G $\Omega$  and  $V_{Th,OTS}$  less than 0.3 V at near-threshold operation condition.

with a sub-pA/ $\mu$ m leakage current through simulations performed using a program that calculates current-voltage characteristics of various transistors. Fig. 4 (a) shows a simulated  $I_{DS}$ - $V_{GS}$  characteristic of a normal transistor with SS of 90 mV/dec. Based on this transistor, we simulate  $I_{DS}$ - $V_{GS}$  characteristics of transistors with OTS devices having different off-state resistances connected to the source side, as shown in Fig. 4(b). According to our simulation result,  $R_{OFF,OTS}$  larger than 50 G $\Omega$  ensures the transistor leakage current of sub-pA/ $\mu$ m at any operating bias condition. In addition, to reduce the applied drain voltage, the  $V_{Th,OTS}$  should be lowered as shown in Fig. 4 (c) because a  $V_{DS}$  smaller than  $V_{Th,OTS}$  cannot provide enough voltage to turn-on the OTS device by voltage division. As described in the figure, the low power transistor with the OTS device having  $R_{OFF,OTS}$  of 50 G $\Omega$  and  $V_{Th,OTS}$  slightly less than 0.3 V can exhibit extremely high  $I_{ON}/I_{OFF}$  greater than  $10^7$  even at the near-threshold operation condition ( $V_{DD} < 0.3$  V).

#### IV. CONCLUSION

We have developed a B-Te based OTS device and implemented it to a normal MOSFET to reduce its SS for low power applications. The B-Te based OTS device exhibited excellent properties such as low leakage current, abrupt turn-on/off slope, fast switching speed, high endurance, and high thermal stability. These great properties enabled the implemented transistor to have a steep SS of 10 mV/dec and high  $I_{ON}/I_{OFF}$  ratio greater than  $10^5$ . In addition, we confirmed through simulations that a direction to achieve an ideal low power transistor in this concept is to develop OTS devices with  $R_{OFF}$  greater than 50 G $\Omega$  and  $V_{Th}$  lower than 0.3 V.

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