Power mezzanine PDB-LTM: Status of the boards production

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LAr March 2019 (March 5, 2019)

Production Plane

Pre-production → 8 boards

Lot 1→ 10 boards

Lot 2 → 40 boards

Lot 3 → 50 boards

Lot 4 → 50 boards

Total: 158 boards

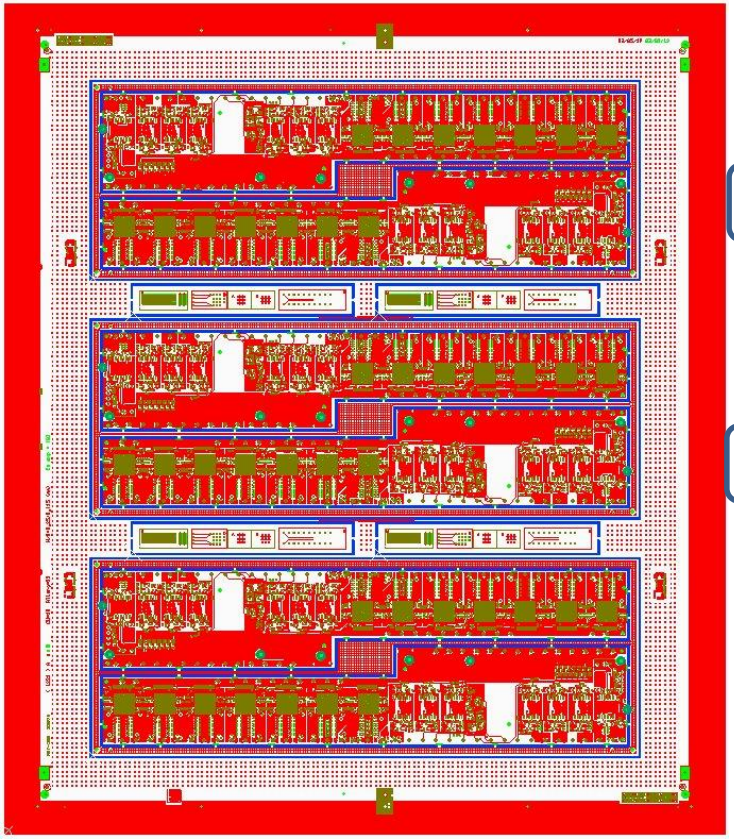
Components have been purchased for full production

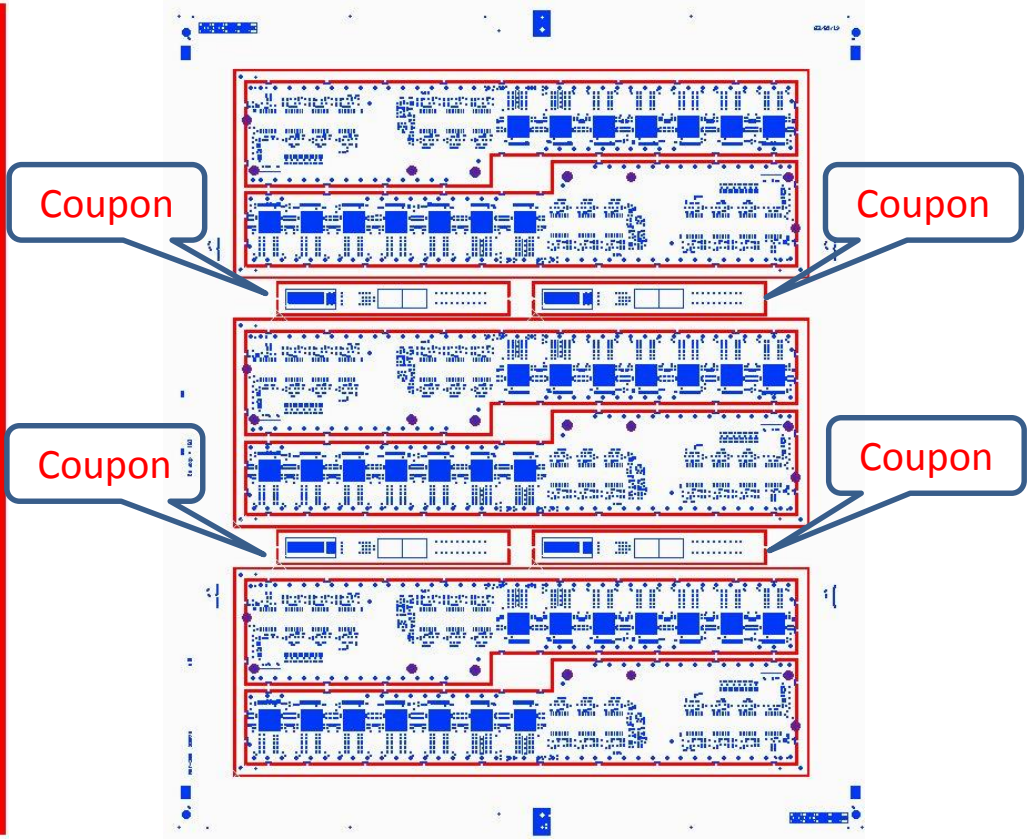
PCB for lots 1-4 will be manufactured in a single lot (IPC Class 2).

The boards will be assembled and inspected according to IPC610 class 3.

Pre-production slot (Feb 2019)

2 panel (12 PCB, 8 populated, 2+2 for manufacturer QA and destructive tests – no more PCB available)



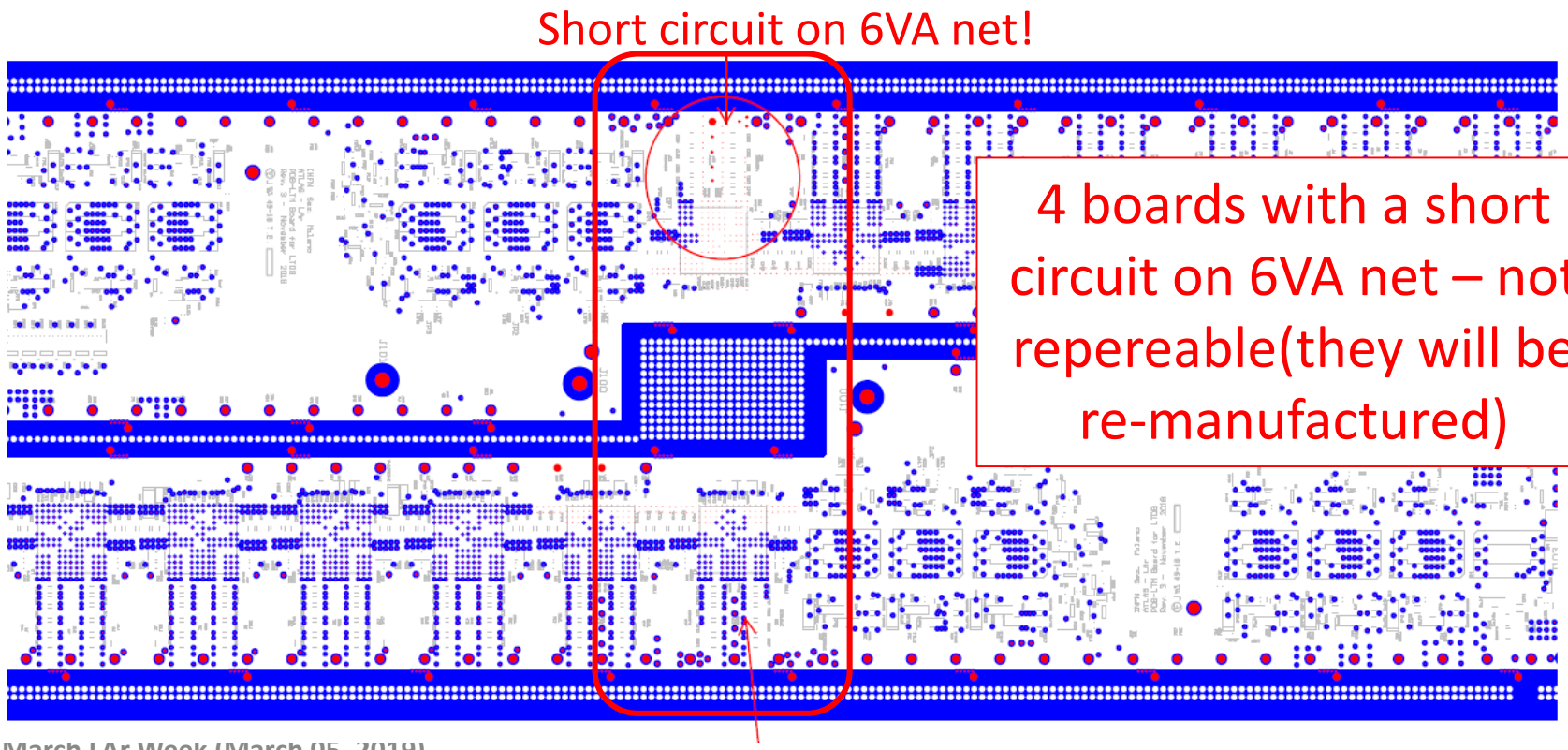


Subset of the panel

The upper board has been realized in the wrong way!

The upper board is a «rotated» copy of the lower (original) board

During the “panelization”, the pads that create the insulation (antipad) from all the holes not connected to the 6VA plane have been accidentally removed

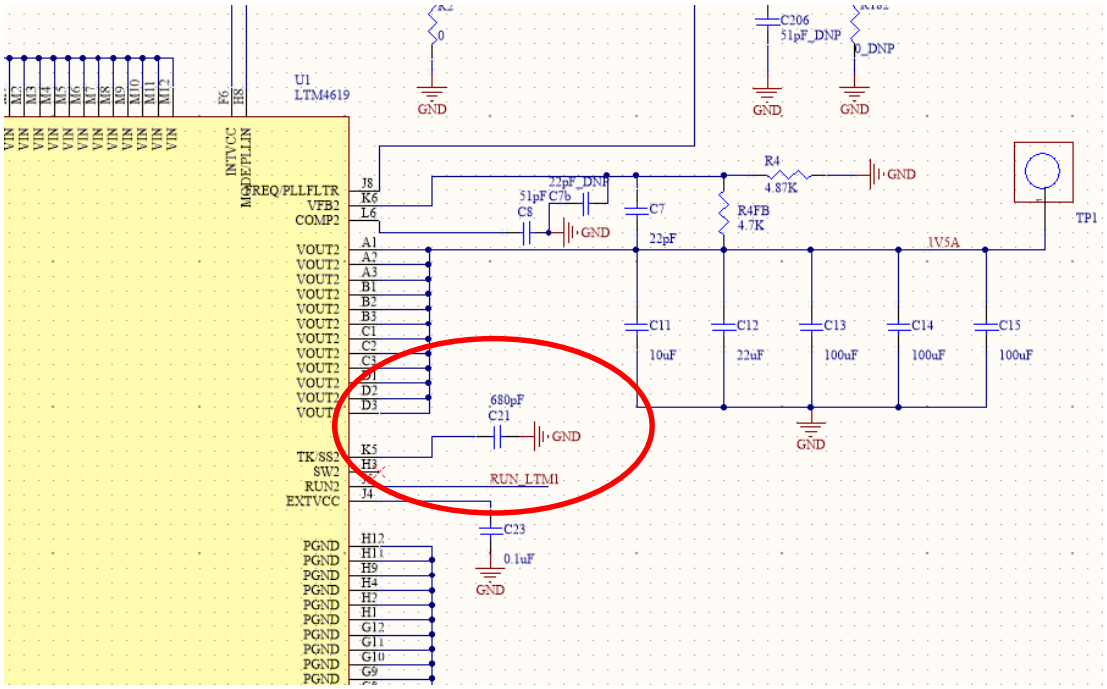


Issue of the 1v5 net

Capacitor C21 for LTM1 (and C67 for LTM3) should have been changed from 0.1 µF to 680 pF in this release of the PDB-LTM.

WHY: to have a more rapid soft start

Reason: this new value was not updated in the BOM



The circuit with the new capacitor operates correctly in Milan but does not operate correctly at BNL.

Tests are ongoing to understand why such a different behavior in the two set-up

$T_{soft\text{-}start}$ evaluation

$T_{soft\text{-}start}$ is obtained by the following equation:

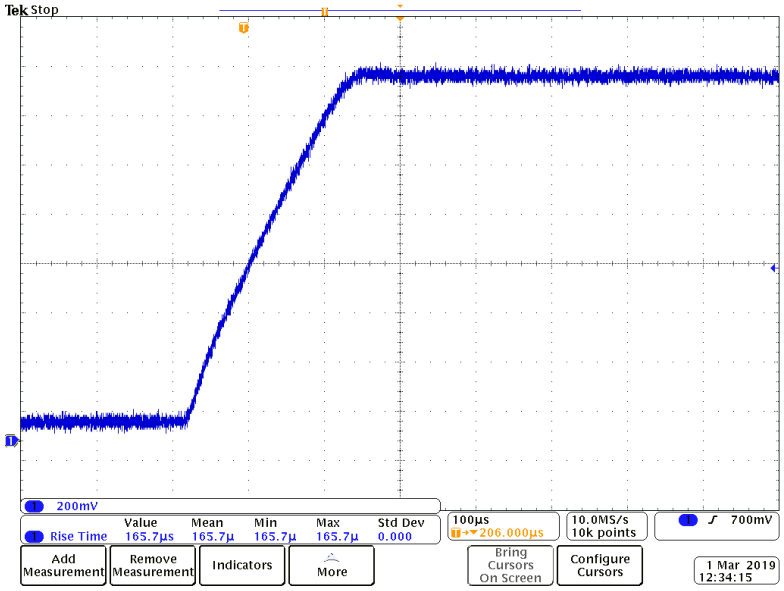
$$t_{SOFT\text{-}START} = \frac{0.8V \bullet C_{SS}}{1.3\mu A}$$

C	$T_{soft\text{-}start\ calculate}$	$T_{soft\text{-}start\ measured}$	Notes
470 pF	~ 0.289 ms	~ 0.240 ms (BNL*)	see slide 9
680 pF	~ 0.418 ms	~ 0.300 ms (Milan*)	see slide 13
0.1 µF	~ 61 ms	~ 55 ms (Milan) ~ 40 ms (BNL*)	see slide 10

* E-mail Hao 2019-03-01.

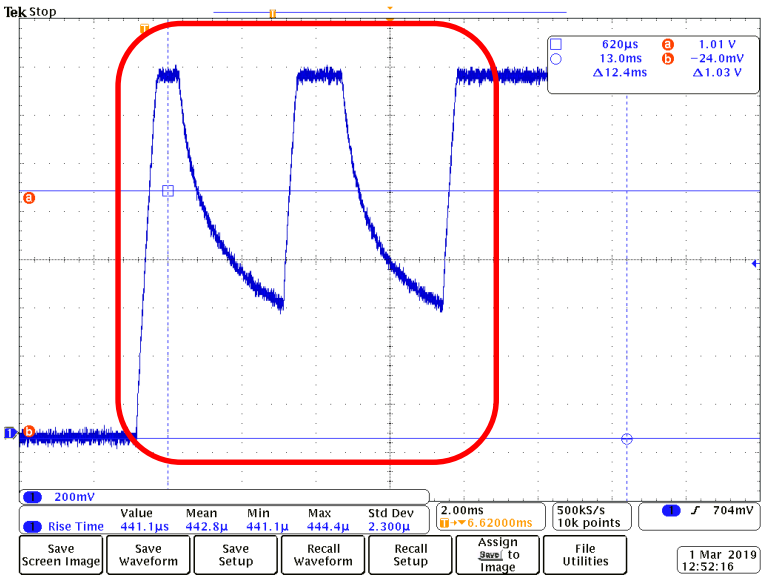
Test at BNL (by Hao)

Proper operation of the LTM 1



PDB LTM #7 LTM 1, C = 470 pF,
Net Name= 1V5A,

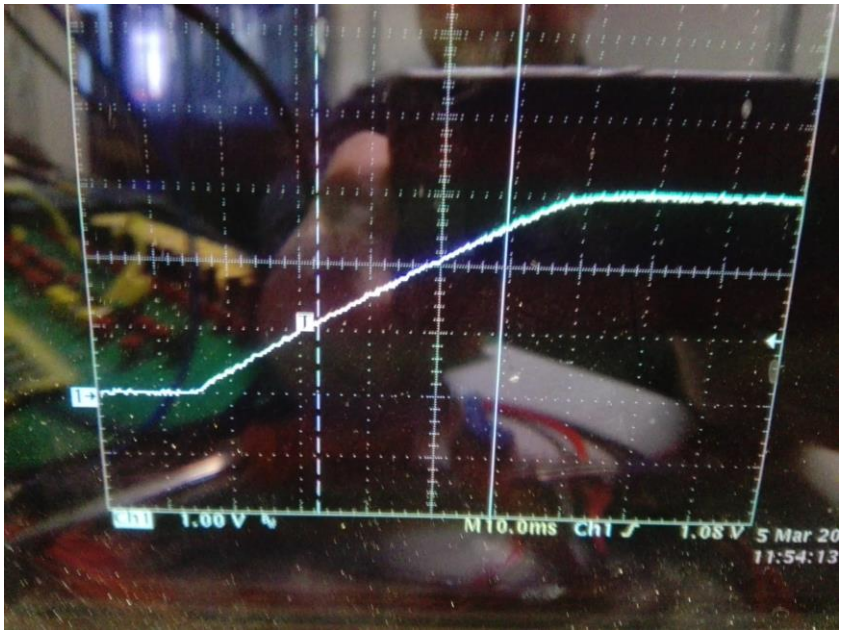
Repetitive shutdown during the soft start up of the LTM 3



PDB LTM #7 LTM 3, C = 470 pF,
Net Name= 1V5B

Scopes from Hao, thank you.

Test at Milano (by Stefano) – 1 of 4



Test obtained on LTM 1 with the old value of C21 (0.1 µF)

Time to ramp up about ~ 55 ms (0 – 100%).

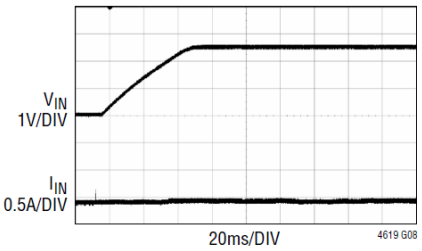
Output voltage work properly

Warning. External differential probe with gain has been used: V/div shown is not correct.

The experimental ramp up time is in compliance with the charts from manufacturer (please note that charts are obtained for different value of input voltage and output voltage, @0A and4 A of load current, resistive load).

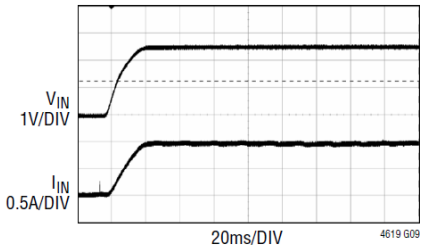
From chart: about 25 – 60 ms

Start-Up, I_{OUT} = 0A



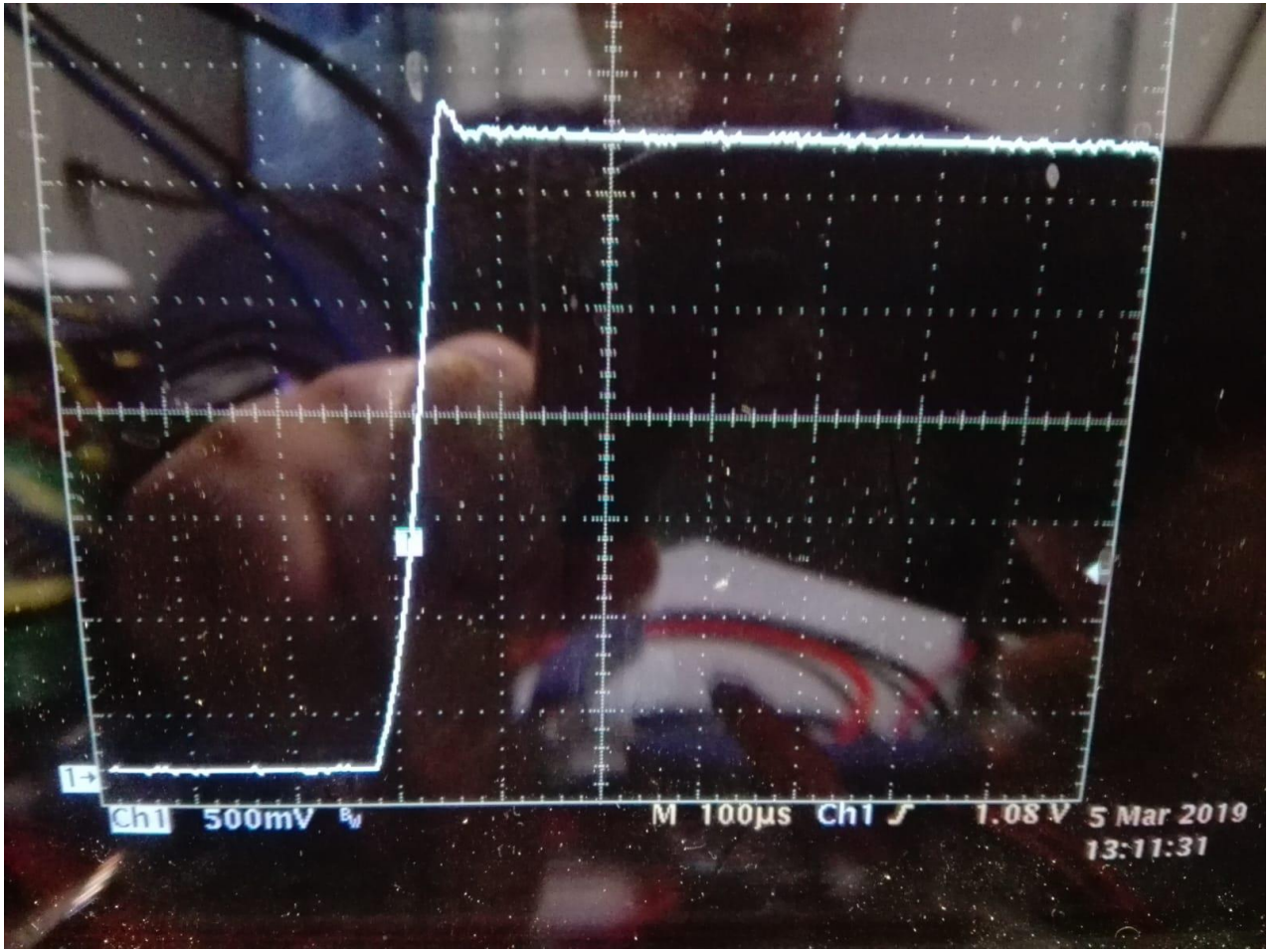
V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0A
C_{OUT} = 2× 22µF 10V
AND 1× 100µF 6.3V CERAMIC CAPs
$C_{SOFTSTART}$ = 0.1µF
USE RUN PIN TO CONTROL START-UP

Start-Up, I_{OUT} = 4A



V_{IN} = 12V, V_{OUT} = 2.5V,
I_{OUT} = 4A RESISTIVE LOAD
C_{OUT} = 2× 22µF 10V,
AND 1× 100µF 6.3V CERAMIC CAPs
$C_{SOFTSTART}$ = 0.1µF
USE RUN PIN TO CONTROL START-UP

Test at Milano (by Stefano) – 2 of 4



Test obtained on LTM 1 without C21.

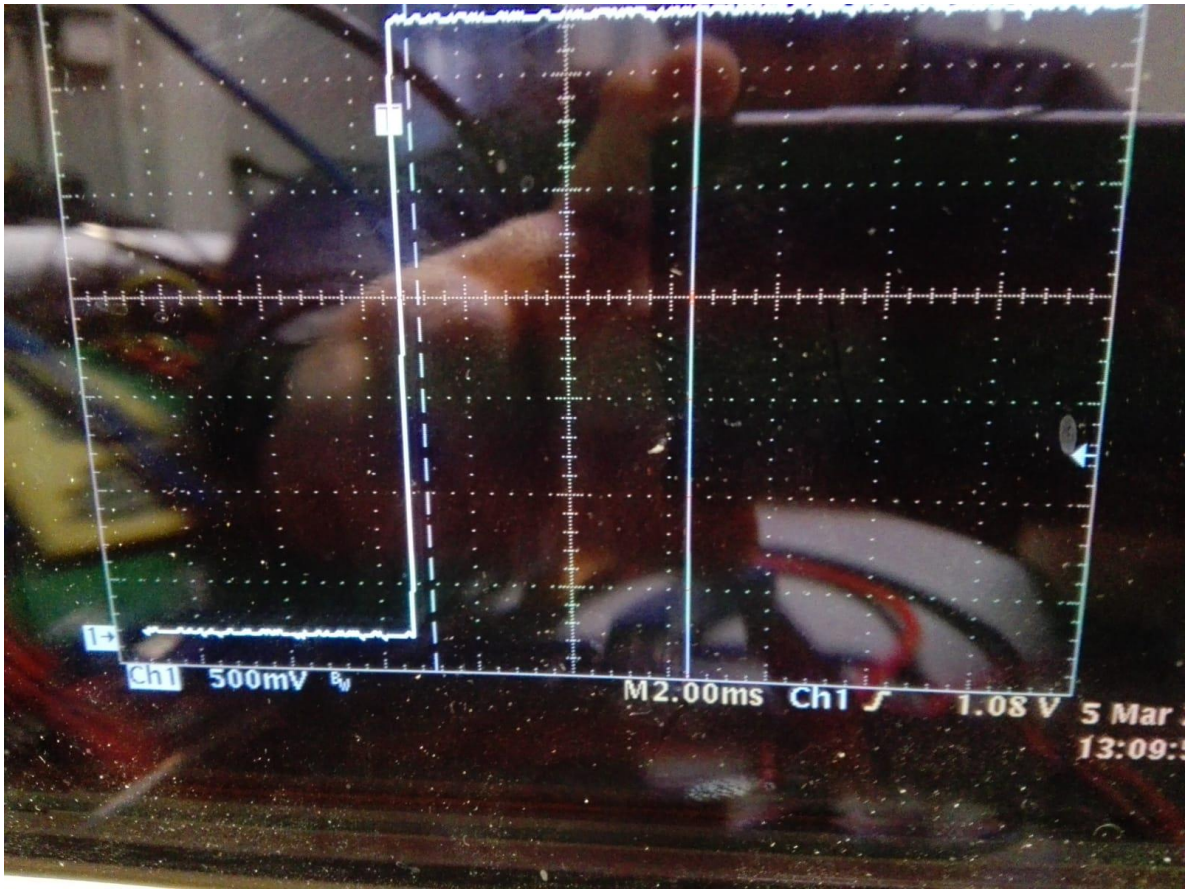
Time to ramp up about 100 µs.

Output voltage work properly (but there is presence of a little overshot)

No oscillation and no “turn off – turn on” cycles.

Warning. External differential probe with gain has been used: V/div shown is not correct.

Test at Milano (by Stefano) – 3 of 4



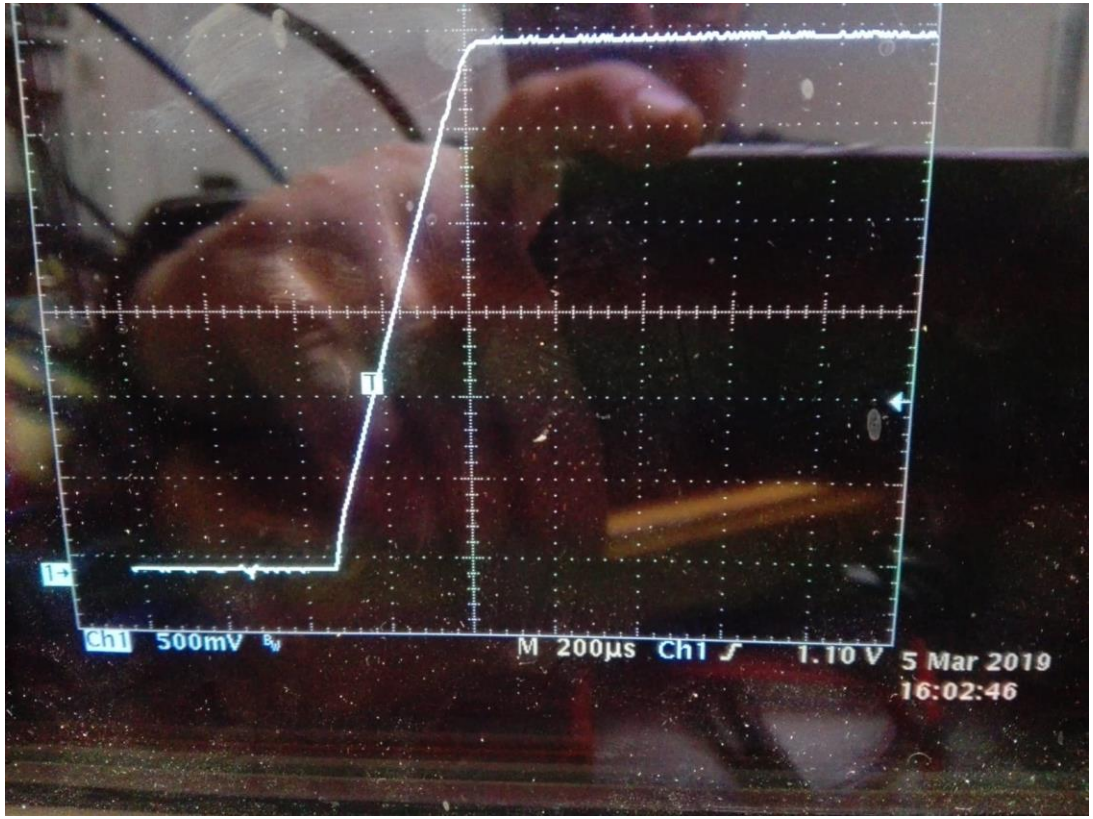
Test obtained on LTM 3 without C67.

Time to ramp up about 100 µs.

Output voltage work properly (scale s/div is different to highlight the long-term behaviour, the little overshot is not more visible)

No oscillation and no “turn off– turn on” cycles.

Test at Milano (by Stefano) – 4 of 4



Test obtained on LTM 1 with C21 = 680 pF as required.

Time to ramp up about 300 µs.

Output voltage work properly

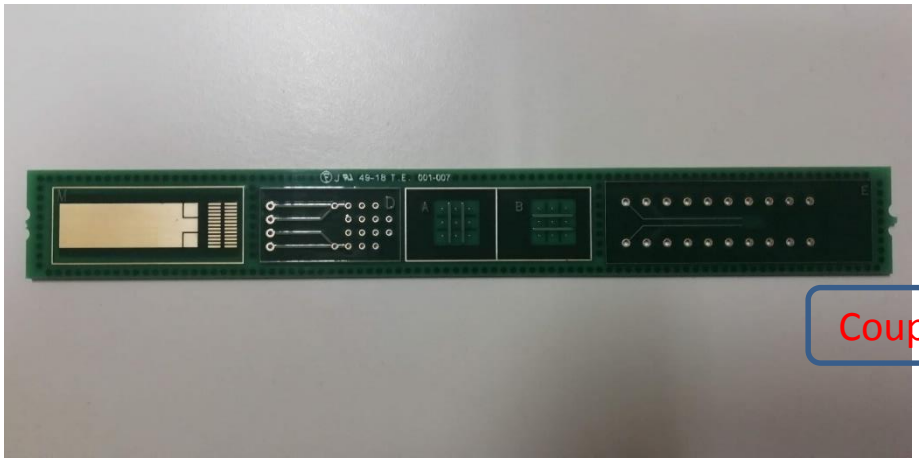
No oscillation and no “turn off – turn on” cycles.

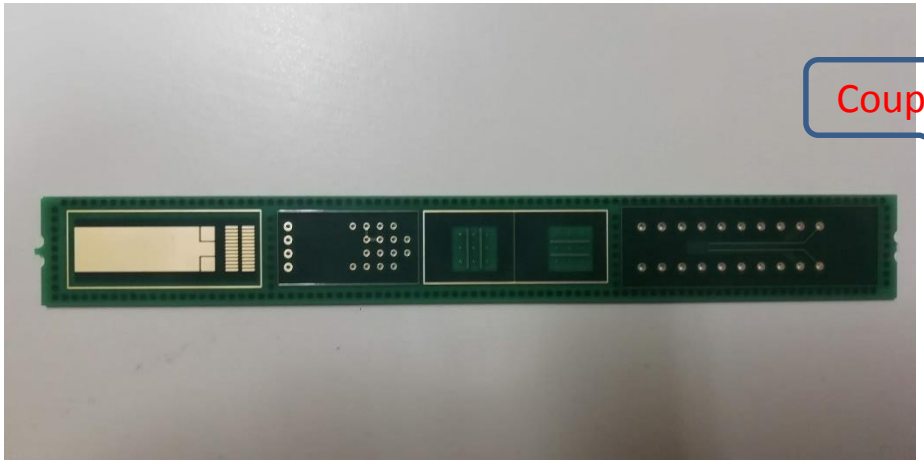
Warning. External differential probe with gain has been used: V/div shown is not correct.

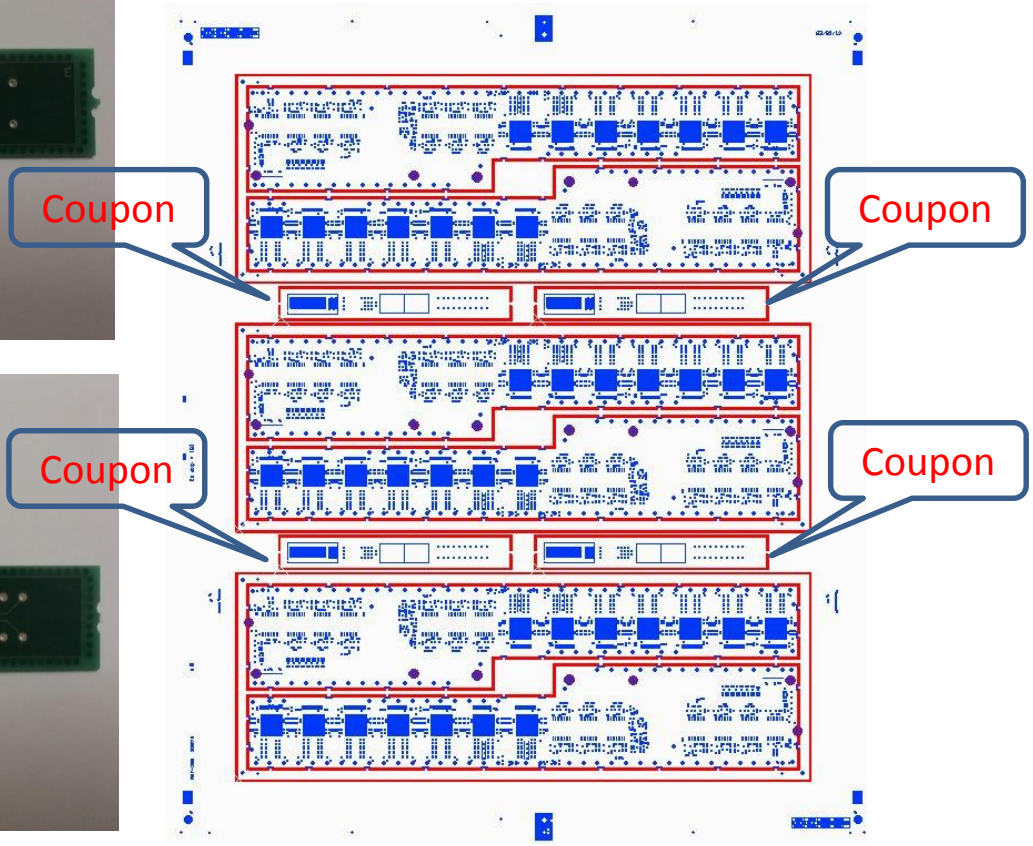
MORE TEST ARE ONGOING …….

The end

The first lot







The boards

A second problem is due to errors in “ populating” the board.

Some components, labelled as «DNP (Do Not Mount) were mounted by the assembler

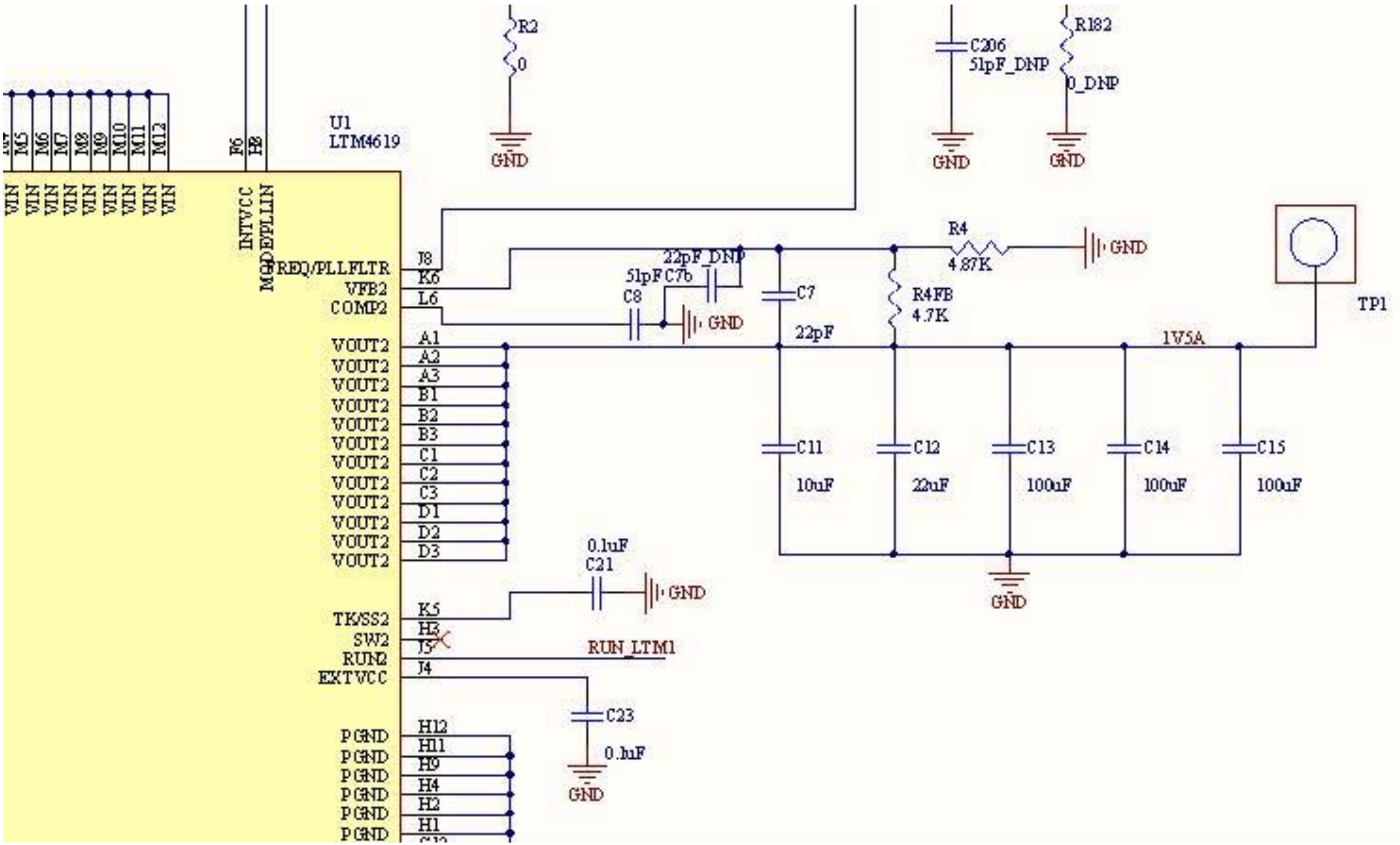
Please note that the manufacturer is the same of all previous versions! …… he did not read instruction??

We had to remove all not-wanted components.

Almost Solved!

Only one problem is still present on the boards.

See the next slide



U1
LTM4619
R2
0
GND
C206
51pF_DNP
R182
0_DNP
R4
4.87K
TP1
FREQ/PLLFLTR
VFB2
COMP2
22pF_DNP
51pF C7b
C8
C7
22pF
R4FB
4.7K
1V5A
VOUT2
C11
10uF
C12
22uF
C13
100uF
C14
100uF
C15
100uF
0.1uF
C21
TK/SS2
SW2
RUN2
EXTVCC
RUN_LTM1
C23
0.1uF
PGND
INTVCC
MODE/PLLIN
VIN