



## PDB issues and Production Plan

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### Introduction



8 PDB pre-production boards (version 3) received in Milano end of February Differences between version 3 and previous version (version 2):

- 1. Different values of some resistors in order to optimize a few output voltages as requested by Hao after some tests of PDB v2 in the LTDB
- 2. Some geometrical changes implemented in the frame

### Of the 8 pre-production PDBS:

- 4 boards were not useable because of a mistake made by the manufacturer (problem understood

   see March Lar week presentation
  - https://indico.cern.ch/event/800559/contributions/3339352/attachments/1806520/2948521/PDB-LTM 2019-03-05.pdf
- 4 boards were successfully tested in Milano and 3 of them were sent to BNL

During the tests in BNL, a start up sequence not correct in some situation was observed. The problem could not be reproduced in Milano with the other v3 board. Moreover the problem was not observed with v2 boards (neither in Milano nor in BNL)

Investigation on this issue started and the problem was traced to dependencies on the LVPS used in the tests. Milano had used always the same LVPS in the tests, BNL used not only the Wiener LVPS but also other devices (Vicor and Keysight).

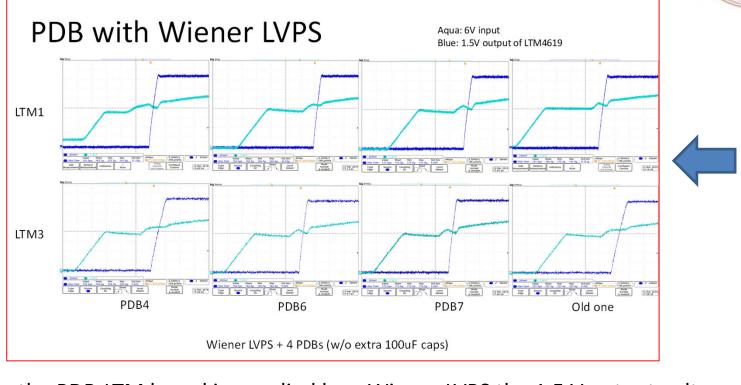
Moreover the input capacitors of the LTDB were changed to be compatible with 48 V input voltage for Phase II:

to be compatible with the footprint in the LTDB layout the capacitance was slightly reduced



# PDB-LTM with Wiener LVPS



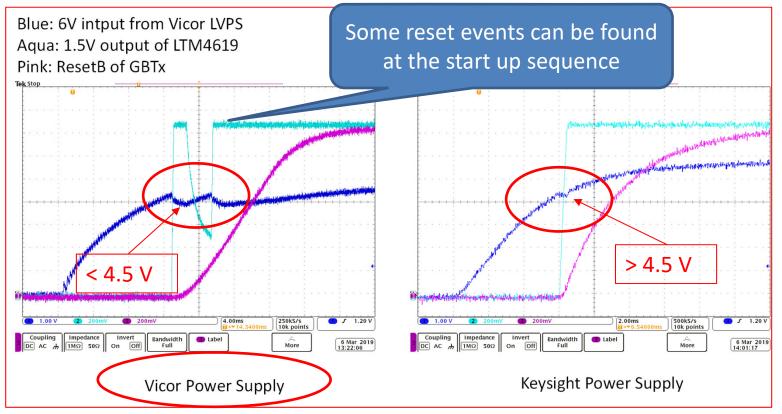


- Slide presented by Hao (PDB\_Test\_0316.v1.pptx) When the PDB-LTM board is supplied by a Wiener LVPS the 1.5 V output voltage ramp up (blue) shows the correct behavior
- The output voltages from LTM 1 and 3 are the ones where the power on ramp-up must be fast: this is necessary to get proper timing for power on reset of GBTx chips (details has been presented in a previous FE WG meeting)

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# INFN... but when Vicor and Keysight LVPS have been used...





Slide presented by Hao (PDB\_Test\_0316.v1.pptx)

- One or more short reset events of the LTM device can be observed (in particular with VICOR LVPS).
- This is mainly due to the behavior of the output voltage of the LVPS (which is the input voltage of the LTM).
- This is well clear when the LTM starts (see the red circles on the figures).
- The output voltage of the power supply tends to decrease just enough so that in some situations it falls below the minimum operating value of the LTM devices (4.5 V).



# Proposed solutions



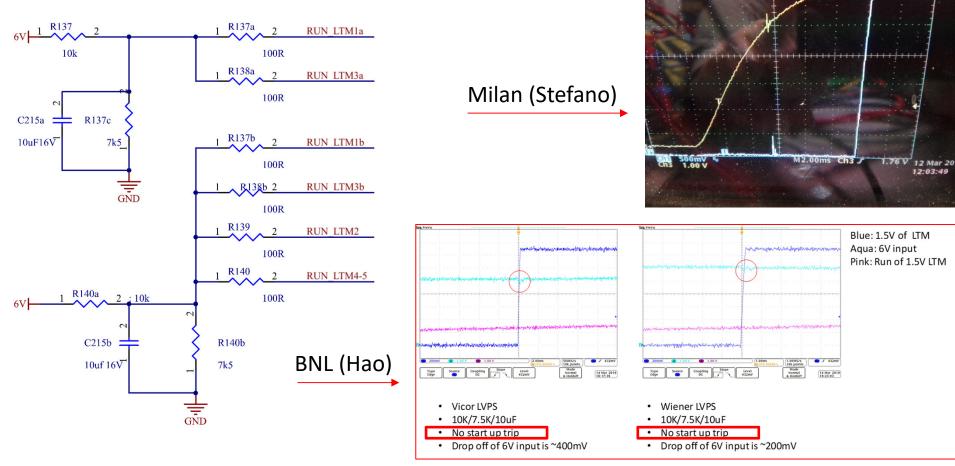
- To avoid this dependency from the LVPS, cables, etc... different solutions have been discussed.
- In the end it was decided to implement the following modification to the PDB:
  - delay the switching ON of the LTM device when the LVPS device has reached a value of its output voltage (>> 4.5 V) such as to prevent the switching OFF of the LTM device
- This soft start circuit modification is strictly necessary only for the 2 output voltages from LTM 1 and 3 but, in order to have the best flexibility, the new circuit has been implemented for all the LTM devices.



# Proposed solution



- Solution successfully tested on PDB v3 both in Milano and at BNL
- Change implemented in PDB v4





### **Production Plan**



- Gerber files of PDB with new layout (v4) were sent to manufacturer (ARTEL) on 22/3. During last week there were a few iteration with the manufacturer that asked some changes in the layout in order to improve the solderability in a few points.
- Production of 8 boards has started
- We expect to receive back 8 PDBs in Milano by 10/05
- We need one week to test in Milano and then we can ship them to BNL
- If after the tests, we give the manufacturer green light for full production we should start receiving production PDBs in Milano by 5/7
- By end of July we think we can receive, test in Milano and ship to BNL about 70 units total