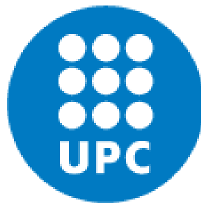

UNIVERSITAT POLITÈCNICA DE CATALUNYA
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Interdigitated Back Contacts Solar Cell Based on Thin Crystalline Silicon Substrates

Thesis submitted in partial fulfillment of the requirement for the PhD Degree issued by the Universitat Politecnica de Catalunya (UPC), in its Electronic Engineering Program

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September 2018

Electronic Engineering Department

Acknowledgement

The first and foremost gratitude goes to my supervisor Dr. Isidro Martín Garcia. From the first day of entering the PhD program he has been instantly helping and supporting me. His knowledge and patience always guide and encourage me. No matter when, I always can get help from him to solve the problems I encountered during the study. He has done everything a supervisor can do for his student. It is my great pleasure to work with him.

I would like to give my great appreciation to Prof. Ramón Alcubilla and my co-supervisor Dr. Moisés Garín. Ramón is always ready to hear my progress on study and inspire me with many ideas, and it is his trust makes it possible that I won the scholarship. Without the guidance and ideas from Moisés, the first obtained experimental results of my PhD study cannot come out, which gives me a lot of confidence.

I also would like to thank Dr. Pablo Ortega for giving me valuable suggestions on laboratory work. Deepest thanks to Dr. Gema López, who taught me the most on laboratory work. The experience she shared with me makes me a skilled experimenter from a green hand. To Trifon Trifonov and Arnau for the professional skill on taking SEM images and teaching. Special thank goes to lab technicians Miguel and Xavi, who help me a lot on daily work. Thank you Miguel for the concern and great help for me. I will never forget the moments we pass together in the laboratory with Gema, Eric, Gerard, Guillermo, David Cardador, Rasha, etc. I am also thankful to Luis Enrique from ICFO for the assistance on RIE and ALD. Thanks to other professors from the group, Sandra, Cristobal and Kim, for your help and support.

Next, I would like to thank all friends from the PhD office, David Cavalheiro, Mohamed Saad, Martín, Teresa, Lukasz, Chenna, Sergi, Bremnen, Santi, etc., for the precious café/beer time and talks we had together. Thank all the friends that I got to know in UPC, especially H. Yang, B. Ye, M. Zhang, and J, Lei, for years of support and friendship.

I would like to say thank you to my parents, it is your understanding and unconditional love that keep me optimistic and growing up. I cannot make it today without your support and

encouragement. Finally, I would express my sincere thankfulness to my wife, Wenfei, for your support and love all these years, from the moment that we listened the song together.

Abstract

This thesis contributes to the fabrication technology of c-Si solar cells on thin substrates based on Interdigitated Back-Contacted (IBC) structures. The potential of this structure to obtain high efficiencies is well-known. However, important challenges should be addressed to adapt it to thin c-Si substrates, such as the manufacturing of the thin c-Si substrate itself, light absorption enhancement, device structure design, surface passivation, etc. Focused on these challenges, experiments and simulations have been carried out, including innovative thin c-Si substrate fabrication method *Millefeuille* process, novel IBC solar cell structures combining laser doping and silicon heterojunction technologies and thin IBC solar cell performance prediction through simulation. Finally, a 30 μm thick c-Si solar cell is fabricated by thinning down a finished device applying a silicon etching technique that combines dry and wet etching.

Considering the *Millefeuille* process, based on the technological know-how the impact of both modulated profile and periodicity of silicon pores on the generated thin layer quality is explored and the results are visualized by SEM images. Furthermore, the solid-void transformation evolution during the high temperature annealing reveals the pore status at 35, 60 and 90 minutes, allowing a deeper understanding of the practical silicon atomic surface diffusion and the shape evolution.

In order to find a viable and promising device structure that can be used in case of thin silicon substrates, a hybrid p-type solar cell structure is reported. In this case, emitter is based on silicon heterojunction technology while the base contacts are created by laser processing Al_2O_3/SiC_x films. Special attention of the compatibility of both technologies has been paid in the proposed fabrication process including emitter region re-passivation and contact metallization. This work provides a new approach for achieving low-temperature high efficiency c-Si solar cells, as well as a novel pathway compatible to the fabrication of IBC devices based on thin c-Si substrate.

In parallel with experimental progress, the simulation on thin c-Si IBC solar cell is carried out for performance study and prediction involving two typical rear surface doping structures: fully- and locally-doped. Simulation results of fully-doped structure reveal an efficiency potential of 16-17 % for thin c-Si IBC solar cell based on substrates of 10-15 μm without changing the

technology developed for thick ones. Regarding the locally-doped structure, its performance is less tolerant to the degradation of front surface passivation. Additionally, a strong reduction of short-circuit current related to stronger requirements in the effective diffusion length is also deduced. Finally, a reduction of saturation current density, probably related to a change in the distribution of current that flow parallel to the rear surface, is also observed when the device is slimmed down. Next, a thin IBC c-Si solar cell efficiency potential is explored through rear contacts pitch study and the highest conversion efficiency is expected when contact pitches are minimum in the range of study.

Finally, efforts are paid to get a thin c-Si solar cell through thinning down an already finished device of thick substrate. A silicon etching process based on RIE and wet chemical etching is proposed. Different experiments demonstrate that the front surface can be successfully repassivated after etching process. Additionally, random pyramids are created on that surface and the optical response of thin c-Si substrates is measured revealing a potential photogenerated current in the range of 40 mA/cm2 for 30 μm-thick substrates. Applying all these techniques to a final device, a 12.1 % efficiency is achieved and the front surface recombination velocity is deduced to be 1500 cm/s by comparing EQE with simulation results.

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Chapter I

Introduction

In this chapter, an introduction of the thesis is given including several aspects: the current status of photovoltaics solar energy especially for devices based on crystalline silicon material; the challenges for thin crystalline silicon solar cell fabrication and the Interdigitated Back Contacts structure design; a brief review of the state of the art of these devices and the related theoretical and technical background. Based on the provided information in this chapter, the main line of study as well as the objectives of the thesis are clarified and targeted.

I. 1 Current status of photovoltaics solar energy and thesis motivation

Electricity as a form of energy is essential for all sectors of the modern society. A clean, cheap and renewable electricity generation process has been identified as a one of the main conundrums of the last decades.

Photovoltaic (PV) solar energy is considered as one of the promising, sustainable and environment-friendly energy resource that could help in this way. Since the first effective solar cell was fabricated in Bell's Laboratory in 1954 [1, 2], a great effort has been devoted to develop more efficient and cost-competitive devices. As a result, PV solar energy for terrestrial application has exponentially grown playing a more and more significant role. The PV installation status by the end of 2017 is shown in the Fig. I. 1. The accumulative installation of PV modules are more than 400 GW around the world and the photovoltaics is a fast growing market as it is demonstrated by the Compound Annual Growth Rate (CAGR) of PV installations that was 40% between 2010 to 2016 [3].

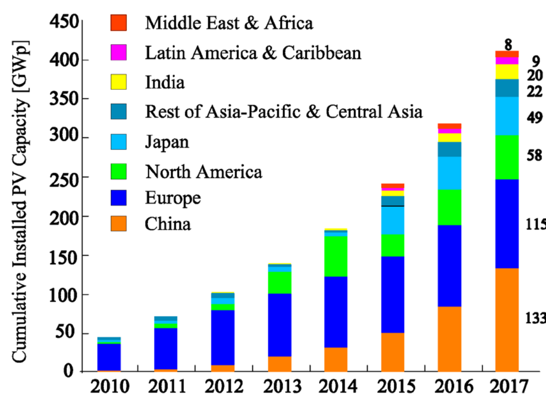

Fig. I. 1 Global cumulative PV installation until 2017 [3]

Among all kinds of technology or material utilized for PV device production, crystalline silicon has been the dominant one in photovoltaic market in the last decades when the PV market has followed an explosive growth, competing against other PV technologies as Thin Film and multi-junction solar cell based concentrated photovoltaics. As it is shown in Fig. I. 2, Si-wafer based PV technology accounted for about 94% of the total production in 2016. The share of multi-

crystalline technology is now about 70% of total production, leading to the market share of all thin film technologies amounted to about 6% of the total annual production in 2016 [3].

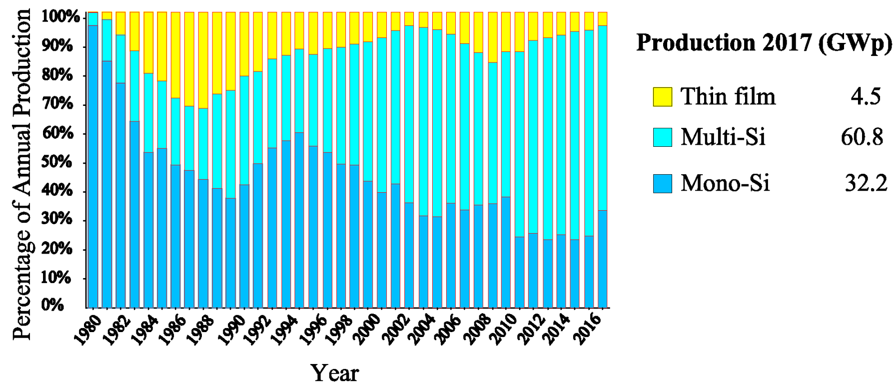

Fig. I. 2 Evolution of market share of different technologies for PV production [3]

Regarding the energy conversion efficiency, the record lab cell efficiency is 26.7% for mono-crystalline [4] and 22.3% for multi-crystalline [5] silicon wafer-based technology. The former is very close to the theoretical limit of 29.4 % [6] assuming perfect optics and surface properties and only intrinsic recombination properties in the c-Si bulk. Consequently, the dominant position of c-Si technology could not be based on further increase in conversion efficiency but on a constant cost-reduction strategy applied throughout all the value chain. One of the trends is the reduction of the substrate thickness, since c-Si wafer accounts for 40% of today's cell cost [7] and most of the incident photons are absorbed in the first microns beneath the surface. Substrate thickness has been systematically reduced in the last years to the current 150-160 μm and it is foreseen that wafer thickness could be reduced even further to 120 μm and the module technology in the future will be able to use wafers as thin as 100 μm [7]. These data demonstrate that c-Si solar cell manufacturers are paying big efforts in reducing device thickness applying expected improvements of current technology. However, novel approaches could lead to further thickness reduction leading to a further cost-saving. Currently, many research groups are focused on envisaging the fabrication technology and solar cell structure needed for devices well below 100 μm while keeping high efficiency (a detailed state of the art review of thin c-Si solar cell is reported in chapter II).

This thesis aims at contributing to the technology needed to fabricate c-Si solar cells on thin substrates based on Interdigitated Back-Contacted (IBC) structure. A sketch of this type of structure is shown in the next Fig. I. 3. As it can be seen, all the contacts are located at the rear side of the cell keeping the front surface without any shadowing from the metal grid. The potential of this structure to obtain high efficiencies is demonstrated by the fact that it is the one used in the last world record efficiency solar cells [4, 8-9]. However, important challenges should be addressed to adapt it to thin c-Si substrates as described in the next subsection.

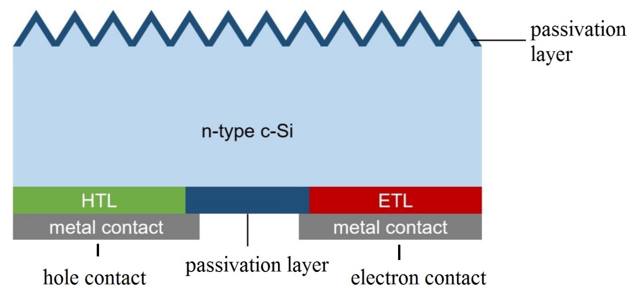

Fig. I. 3 A sketch of Interdigitated Back-Contacted (IBC) structure

Before going into the details, the word “thin” applied to c-Si substrates should be defined as it is a key word of this work and will frequently appear through the thesis. Typically, Si wafers below 150 μm are labeled as “thin”. Recently, due to the interest by the industry in reducing substrate thickness and the introduction of new promising techniques to produce thinner kerfless wafers, there is an increasing tendency to term substrates with thickness in the range 1-20μm as “ultrathin”, however it is usually used in a certain context to differentiate them from the traditional thin wafers. Since there is still no standard for thickness categories of c-Si wafer and each fabricated “thin” c-Si solar cell could have a different thickness, the thickness of the c-Si substrates will be specified besides the term “thin”. In this work, generally a thickness in the range of 10 to 50 μm is referred as thin through the whole text, except for the literature review presented in next chapter in which the term “ultrathin” is used for consistence with the authors.

I. 2 Challenges for thin c-Si solar cell based on IBC structures

A first challenge is the manufacturing of the thin c-Si substrate itself. In order to keep the cost-reduction strategy, a cost-competitive technique to obtain the c-Si substrate should be found. Nowadays, several techniques have been proposed and a review of them will be included in chapter II. As a first approach, massive Si etching from c-Si thick substrates to get thin wafers has little attraction from industrial solar cell production due to its cost. The most promising solutions involve standalone thin c-Si substrates extracted from thick c-Si, for example through substrate cleavage. However, there is not a well-established technology that could be considered as a standard solution to this challenge yet.

Regarding solar cell processing based on thin Si substrate, the maintenance of relatively high efficiency is required in order to realize the cost-saving strategy. For fulfilling this objective, the very first consideration is the optical performance of the cell. Light absorption plays a major role on device efficiency due to the weakening of the long wavelength sun light absorption when the c-Si substrate absorber is thinner. The light absorption coefficients of intrinsic silicon [10], are shown in Fig. I. 4.

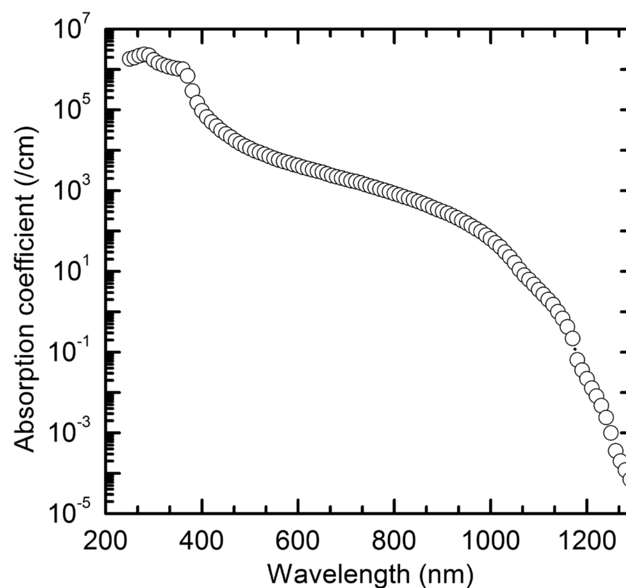

Fig. I. 4 Absorption coefficient of Silicon [10]

As it can be seen, absorption coefficient is reduced for increasing wavelengths. Following Beer-Lambert law, light absorption shows an exponential decay with a characteristic length equals to the inverse of the absorption coefficient, i.e. absorption length. Then, at the absorption length the substrate has absorbed a factor of $1\text{-}e^{-1} \approx 64$ % of the incident light. For example, the data point at the 1000 nm shows an absorption coefficient of 64 cm^{-1}, hence the absorption depth is 155 µm meaning that the 155 µm-thick intrinsic silicon material would show an optical loss of 36 % when only one pass of the light through it is considered. Notice that 155 µm is a thickness which is currently used in commercial devices meaning that optical losses due to low absorption of IR photons occur. Fortunately, very low sun irradiance is located beyond 1000 nm when the standard spectrum for terrestrial application is considered (AM1.5g spectrum). These optical losses would dramatically increase when thin substrates are involved. Not only the optical loss would start for shorter wavelengths, but the sun irradiance is much intense for wavelengths closer to the visible range resulting in a critical loss. As a consequence, a strategy for light trapping, i.e. increase the optical path of the light inside the substrate, must be considered for thin devices.

Conventionally, c-Si surface roughness for light anti-reflection is realized by pyramids texturing and it has been broadly used for laboratory and commercial PV cells due to its effective light absorption enhancement. This kind of surface morphological deformation is achieved at the expense of the c-Si material etching, while the etched Si thickness could be as deep as about 20 µm. This approach is appropriate for c-Si solar cells that are based on conventional Si wafer as the etched thickness is not significant for the wafer mechanical properties and the subsequent processing steps. However, in case of thin c-Si material, it does not seem a feasible solution. As a consequence, an experimentally viable pathway should be determined for effectively improving the thin c-Si light absorptance. It should be mentioned that along this work, despite some efforts have been paid to improve optical properties of thin c-Si solar cells (see reference [11]), this challenge has not been addressed in depth due to time limitations.

Besides the light absorption management task for thin c-Si solar cell, device structure design is essential for approaching high efficiency. Historically, double side contacted c-Si solar cells have been considered as reference structure [12]. In such devices, the electron contact is on one surface while the hole contact is located on the opposite one. As it was mentioned before, the rear

contacts structure has the advantage that no metal grid is on the front side avoiding the shadow loss; secondly, the electron and hole contacts are all arranged at the rear surface hence the contacts area can be tailored approaching the optimum design without worrying about the trade-off between the contacts series resistance and the front metal finger reflectance. Furthermore, this structure facilitates the cell stringing and wafer interconnection for module fabrication.

For thin c-Si substrates, the IBC structure shows further advantages. Since all contacts are at the rear side, the front surface requirements are relaxed to just a good surface passivation allowing a more flexible application of light trapping techniques. Additionally, IBC structure will potentially facilitate cell processing and assembling, in particular for very thin fragile c-Si substrates. This type of substrates can be transferred to a transparent panel (e.g. glass or silicone, also used for cell encapsulation) leaving the rear surface accessible for contact definition. Some devices using this structure on thin c-Si substrates have been reported in the literature leading to efficiencies of 18.9 % and 13.7 % on 45 and 10 μm-thick solar cells, respectively [13, 14]. Although an optimum device structure for thin devices has not been established, IBC structure is considered as a promising candidate for high efficiency thin c-Si solar cell.

Classically speaking, base and emitter formation is one of the critical step of the c-Si solar cell processing, during which, the definition of p-n junction region is realized. The emitter formation based on dopant thermal diffusion has dominated the solar cell fabrication for a long time in both laboratory and industrial areas. The technology is quite established and the relevant parameters such as the dopant concentration profile as a function of time and temperature can be accessed by mature numerical simulation. However, the high temperature thermal diffusion is a power and time consuming procedure and, more importantly, its application to thin c-Si substrates is not straightforward due to their different mechanical and thermal properties. Thus this step must be adapted to be feasible for thin substrates or even replaced by other more convenient low temperature approaches.

As in case of thick Si wafer, a good surface passivation is an essential quality indicator to assure the final PV device performance. Due to mono-crystalline silicon material properties, recombination at the surfaces dominates recombination mechanisms which is even more

significant for thin c-Si substrates. Special attention must be paid to this task adapting the conventional technologies, typically consisting of dielectric deposition, to the requirements of thin substrates.

As a conclusion, back contacted structure is a viable and promising design for high efficiency thin c-Si solar cells that would potentially facilitate the solar cell optical and electrical processing

I. 3 Thesis outline

This thesis addresses part of the challenges described above. In particular, chapter III reports on the improvements applied to a technology called "*millefeuille*" which lead to multiple thin c-Si substrates from a single wafer. This technology, based on the application of macroporous silicon with modulated width, has been developed in our research group. The chapter deals with the impact of porous periodicity and profile to the quality of the c-Si layers. In chapter IV, a fabrication process combining laser doping and heterojunction technology is explained. These devices have homojunction base contacts while emitter contacts are based on silicon heterojunction resulting in hybrid devices. Both technologies are low temperature and potentially compatible to thin c-Si substrates. A fabrication process combining both technologies is proposed and its potential is demonstrated by applying it on conventional c-Si substrates. Chapter V is focused on the effect of substrate thickness and front surface recombination velocity on c-Si IBC solar cells. This work is done through 3D simulations where a rear surface configuration mimicking high efficiency devices is defined as a reference. Then, substrate thickness is reduced from 280 to 10 µm with interesting effects on carrier collection and cell efficiency. In chapter VI, a 30 µm-thick solar cell is fabricated with relevant efficiency. In order to minimize handling problems, we start from a thick c-Si substrate where the rear surface is processed using conventional technologies. Then, the substrate is mechanically and chemically thinned down to be finally textured and repassivated. The obtained results are validated through 3D simulations. Finally, chapter VII shows the conclusions and future work related to this thesis.

Before going into all these results, next chapter describes the background on which the work is based. It includes a theoretical and technical background as well as a detailed state of the art of thin c-Si solar cells.

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Chapter II

Fundamental Background

In the first part of this chapter, the state of the art of thin c-Si solar cell fabrication and development is presented. This part covers several challenges for achieving efficient thin c-Si solar cell, namely, thin c-Si substrate fabrication method, passivation strategy, device structure design and light absorption enhancement. Representative reports from literature relating to these topics are selected and introduced briefly.

In the second part of the chapter, a brief introduction of solar cell basic theory and a description of technical background are presented, giving a general understanding of c-Si solar cell fundamentals and the experimental equipment used.

II. 1 State of the art

The research on silicon photovoltaics has a long history and fruitful results. However, the thickness of silicon substrates is normally in the range of 150 and 300 µm which is limited by the silicon wafer sawing technique. The study on thin silicon substrate based solar cells is attracting attention due to the cost-saving expectation and the emerging silicon wafer thinning technologies, and it involves various study fields, including the thin silicon wafer fabrication method, the improvement of light absorption on thinned absorber, the feasibility of different surface passivation strategies and recombination mechanisms, etc. In fact, a complete revision of all crystalline solar cell related components is required.

A recent published silicon solar cell efficiency table [1] is presented in Table II. 1. It can be seen that competitive efficiency has been obtained although a substantial reduction of substrate thickness. An efficiency higher than 20 % is reported for a silicon substrate as thin as 35 µm [2]. Moreover, a more than significant 10 % of efficiency is obtained with only 2 µm thick substrate [3].

Table II. 1 Efficiency records of silicon solar cell, cited from Green 2018

Classification	Efficiency (%)	Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor (%)	Description
Silicon						
Si (crystalline cell)	26.7 ± 0.5	79.0	0.738	42.65	84.9	Kaneka,n-type rear IBC
Si(multicrystalline cell)	22.3 ± 0.4	3.923	0.6742	41.08	80.5	FhG-ISE,n-type
Si(thin transfer submodule)	21.2 ± 0.4	239.7	0.687	38.50	80.3	Solexel (35 µm thick)
Si (thin film minimodule)	10.5 ± 0.3	94.0	0.492	29.7	72.1	CSG solar(<2 µm on glass)

Research on this topic has two main challenges: on one hand, a fabrication technique for thin high quality c-Si substrate at low cost is not established; and on the other hand, the device processing as a whole is more difficult considering the fragile and even flexible features of thinned c-Si substrates. Thus, an adapted fabrication procedures should be considered combining thin substrate fabrication and device processing. In order to have a general understanding of the present progress about thin crystalline Si film based solar cells, a review based on a series of representative articles are presented, the review presented below is divided into several topics: the thin c-Si

obtaining method, passivation strategy, structure design of solar cell and light absorption enhancement.

II. 1. 1 Thin c-Si substrate fabrication method

In the next part, several thin c-Si substrate fabrication methods are introduced, namely, silicon etching on Si and SOI (Silicon on insulator) wafer, porous silicon (PSI) layer transfer, c-Si films exfoliation, liquid phase silicon crystallization, and silicon *Millefeuille* process

(a) Bulk silicon thinning from thick wafer

As a first approach, the fabrication of the thin film by thinning the original thick silicon wafer based on chemical wet etching is reported [4-6]. Typically, a 300-400 μm thickness float-zone (FZ) wafer is etched by chemical etching to the desired thickness. The thickness of the etched thin films are characterized by the transmittance of a white light source from backside as well as by SEM. A 50 μm thin wafer fabricated by mechanical grinding and wet chemical etching is also reported in [6]. This wafer thinning strategy is shown in the Fig. II. 1 schematically. As can be seen, the fabrication of solar cell device is either arranged before substrate thinning or after that.

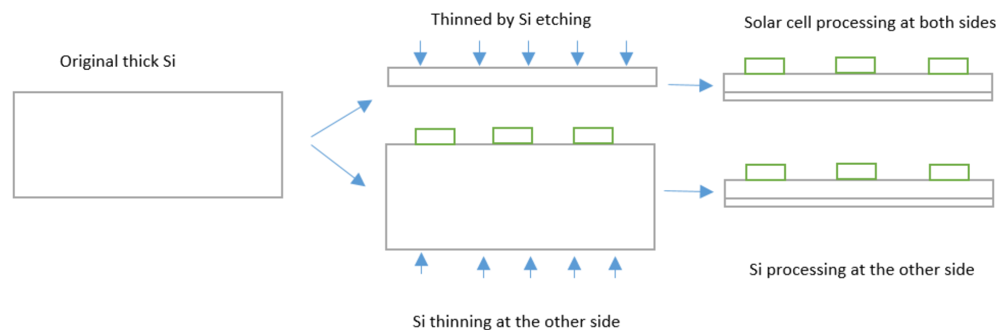

Fig. II. 1 schematic diagram of thin c-Si solar cell fabrication based on normal Si wafer

S. Jeong *et al.* [7] employed a SOI (Silicon on insulator) silicon wafer for obtaining the thin Si layer. After processing the exposed surface with thermal oxidation, n^+/p^+ regions patterning and diffusion, the back side of the SOI wafer is patterned and etched by reactive ion etching (RIE) method. Then the buried oxide layer is exposed and removed by wet chemical etching for

following treatment. Hence, a 10 μm Si substrate is obtained from SOI wafer. The schematic diagram can be seen in the Fig. II. 2.

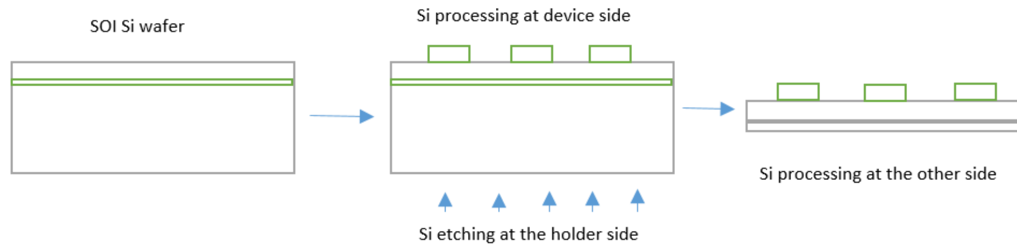

Fig. II. 2 Schematic diagram of thin c-Si solar cell fabrication based on SOI wafer

(b) Porous silicon thin layer transfer

A more efficient and promising method for fabricating thin crystalline silicon wafer-sized film is porous silicon (PSI) layer transfer, referencing several reported layer transferring methods [8-11]. Several researchers have chosen this method rather than etching normal Si wafer, since massive Si etching to get thin wafer has little attraction towards industrial solar cell production due to its costs. Rather than the chemical Si etching, PSI layer transfer method can generate thin Si film by separating the epitaxial-grown Si layer along the preformed porous layer based on a recyclable Si substrate. This technology is regarded having a future because except the front surface treatment, all the solar cell processing like back surface passivation, back contacts and back surface field (BSF) formation, etc., can be realized before layer transferring simply by following existed conventional processing sequences. It has a great interest in laboratory study and industrial area for the compatibility with the equipment which are prepared for normal silicon wafers based solar cell fabrication. For example, F. Haase *et al.* [12] employ Porous Silicon layer transfer method to fabricate back junction, back contact thin c-Si solar cell before detach it from the parent substrate. Another possibility to process thin substrates is to attach them to a steel layer. This layer is utilized for supporting the transferred epitaxial Si layer from a porous silicon donor substrate while the steel works as back contact [13, 14].

(c) Crystalline silicon films exfoliation

The idea is to exfoliate thin c-Si films from a thick substrate by weakening a crystalline plane at a certain depth inside the substrate. Then, the c-Si between the front surface and the corresponding depth is exfoliated. One possibility is to use proton ion implantation to make the crystal more fragile [15].

The energy of the ion implantation determines the penetration depth of the protons and therefore the thickness of the silicon film. It is also possible to exfoliate the sheet without having weakened any crystalline plane previously. This type of technique is based on the separation of the film by thermal stress. It is realized by exfoliating a material that is contacted on the silicon surface and its coefficient of thermal expansion is very different from that of silicon (different materials have been tested such as metals [16, 17] or polymers [18, 19]). Then the temperature is abruptly modified, giving rise to a thermal stress that breaks off the silicon film. Recently, this type of technique has been combined with the two methods previously presented for marking the exfoliation plane: the porous silicon [20] and the proton implantation [21]. In addition, the deposit of a thick layer of aluminum has been reported as a material to facilitate exfoliation and which in turn can be used as a back contact in the solar cell [22]. In this case the fragilized plane is marked by the formation of a notch with a laser beam. In the Fig. II. 3 a diagram of this technique can be seen.

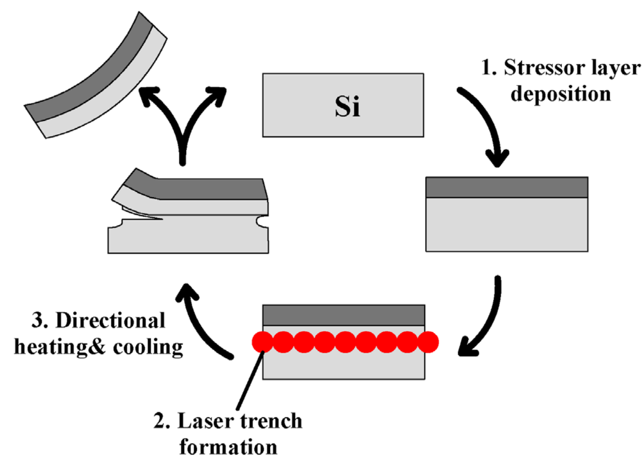

Fig. II. 3 Diagram of crystalline silicon films exfoliation [22]

(d) Liquid phase crystallized silicon layers:

In this case the thin silicon substrate is achieved by evaporation of silicon on a glass and its subsequent recrystallization. A schematic figure of this technique is presented in Fig. II. 4 [23]. To reduce the costs of the deposit, it is done by evaporating silicon at a very high rate, giving rise to an amorphous layer of low quality. The recrystallization can be carried out by means of an electron beam [24] or a laser beam in the infrared [25]. To cover a large area, the recrystallization is done in several passes of the adjacent beam giving rise to a polycrystalline silicon, i.e., with different orientations in the same substrate. Thus, the quality of the obtained material is much lower than for the other technologies discussed. However, diffusion lengths of minority carriers longer than the usual thicknesses of 10-20 μm have been achieved, making their use for solar cells as demonstrated by [26].

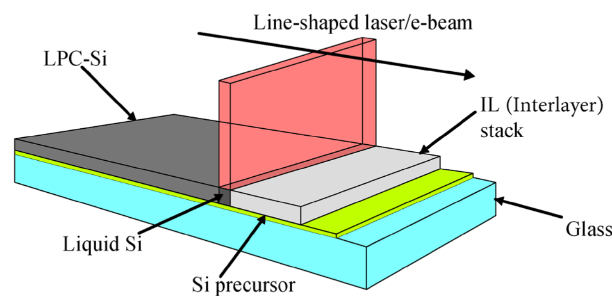

Fig. II. 4 Schematic figure of liquid-phase silicon films crystallization [23]

(e) Millefeuille process

Millefeuille process is another kind of thin layer transfer method allowing multiple silicon thin layers fabrication by single step from a single crystalline n-type silicon wafer. This method was invented by the researchers from Micro and Nano Technology group (MNT) of UPC [27]. The schematic fabrication procedure is revealed in the Fig. II. 5 and the main steps are silicon porosification and high temperature annealing, leading to the multilayer generation. As can be seen from the SEM image, silicon thin layers with smooth surfaces are completely separated. Based on the technological know-how of the *Millefeuille* process, a further study of silicon pores on generated thin layer quality is carried out and reported in detail in next chapter. This process

provides a viable path for economic fabrication on thin free-standing silicon substrate for photovoltaics applications.

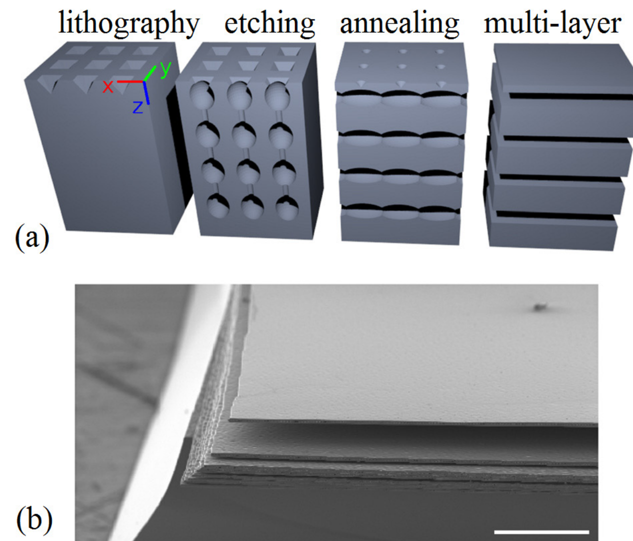

Fig. II. 5 Silicon "*millefeuille*" fabrication process: (a) Schematic view of the four stages of c-Si multiple layers formation: lithography, electrochemical etching, annealing, and thin layer formation. (b) SEM image of a final "*millefeuille*" structure standing on the silicon wafer. Scale bar is 100 µm [27]

II. 1. 2 Passivation strategy

Currently, the passivation with regard to the thin c-Si solar cell generally follows the conventional thick c-Si solar cell mechanism which is typically based on dielectric layers. For example, PECVD deposition of Silicon oxynitride (SiON) and silicon nitride (SiN_x) are also widely used for Si surface passivation [13, 14]. These two kinds of passivation layers also serve as antireflection layer for entering more incident light from the front side of ultra-thin c-Si solar cell. Aluminum oxide (AlO_x) is another promising passivation candidate material, which is used as front surface passivation after the PSI layer is detached from the donor thick wafer [12].

Interestingly, the requirements for c-Si material quality are relaxed due to the increase if surface-to-volume ratio when c-Si substrates are thinned down. For example, in the work of S. Jeong *et al.* [7], passivation is based on thermal oxidation. However, a deep analysis is conducted revealing the correlation among the thickness of solar cell, the efficiency of solar cell and the

surface recombination velocity. It is reported that if the surface recombination velocity is 20 cm/s, the 10 μm thick device showed efficiency maintained at around 20% although the lifetime decreased significantly, from 10 ms to 10 μs. In contrast, the efficiency of the 200 μm thick device with a similar decrease in effective lifetime would be changed significantly, from 21.8% to 6.5%. The conclusion is that a well passivated ultra-thin c-Si solar cell can keep efficiency even when the quality of the material is low.

II. 1. 3 Solar cell structure design

Generally, the c-Si solar cell structure varies from each other due to the different arrangement of the electrical contacts. Electron and hole contacts can either be arranged at both side of the cell, or gathered at only one side, while the contacts can either be full-area coverage or line- or point-like being determined by the emitter and base region of the cell. Hence, the c-Si solar cell structure design can be considered as the arrangement of the locations where electron and hole extraction occur, while an optimum structure promotes the free carrier generation and extraction before recombination.

Typically, substrates based on a chemical-etched Si layer from a normal thick Si wafer are preferred for double-side contacted structures [4-5]. However, PSI transferred thin Si can also be used in this type of design [13, 14]. It should be noticed that the emitter region in case of PSI transferred layer is at the rear surface as a consequence of the Si epitaxial growth.

Taking advantage of SOI wafer, an interdigitated back contact (IBC) solar cell [7] is presented in Fig. II. 6. This kind of structure can eliminate the front surface contacts shadow loss, more importantly, it facilitates contact formation on the exposed surface while the other surface is not accessible. IBC structure can be also found in LPC substrates with relevant efficiencies [26]. In this case, electron and hole contacts are based on silicon heterojunction technology, as shown in Fig. II. 7.

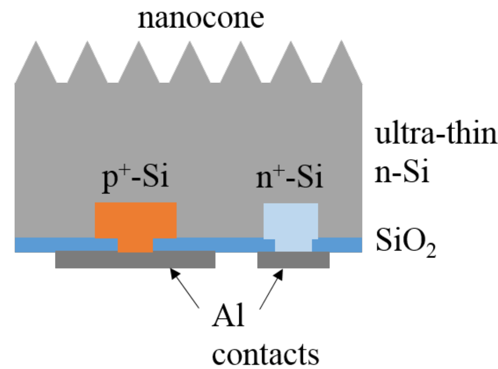

Fig. II. 6 Schematic solar cell structure IBC nanocone [7].

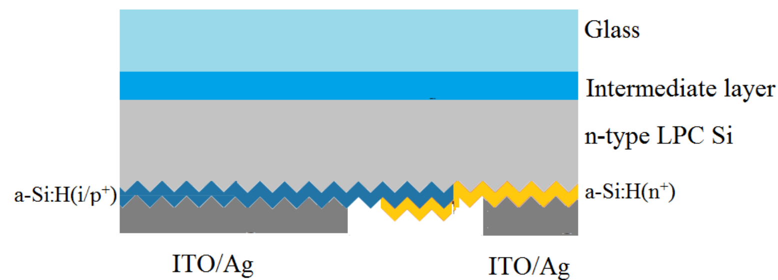

Fig. II. 7 IBC structure in LPC substrates with heterojunction technology [26]

II. 1. 4 Light absorption enhancement

Light absorption enhancement is considered as an indispensable part involved in ultra-thin c-Si processing for high energy conversion efficiency, which has been reported by many researchers in this area. More effective and advanced absorption enhancement mechanism is primarily required in terms of ultra-thin c-Si solar cell, as the thinner the bulk material is, the more photons being transmitted through the c-Si before generating electron-hole pair due to the relatively low Si absorption coefficient. Besides, the conventional light trapping pattern, like texturing, may not be incorporated easily to ultra-thin Si film.

In order to improve optical absorption in thin c-Si substrates, two problems must be addressed. On the one hand, front reflectance should be reduced as much as possible, similarly than for conventional thick solar cells. This objective could be fulfilled by defining patterns on the front

surface bigger than the involved light wavelength, i.e. in the range of some microns, in order to increase the opportunities for a photon to be transmitted into the c-Si substrate. For example, shallow c-Si texturization is reported in [12-14]. Another possibility is to create a soft refractive index transition between the air and the absorber like in the case of black silicon [28]. In this case, c-Si front surface is nanotextured resulting in a porous material that could perfectly adapt the transition between both media.

On the other hand, optical path of photons that reach rear surface should be enlarged. This effect needs a good rear internal reflection together with a randomization of the angle of reflection. By this strategy, photons impinge front surface at an angle out of the scape cone resulting in light confinement. It has been demonstrated that optical path can be increased up to $4n^2$ times [29], where n is the refractive index of the absorber. This light scattering can be done by patterning front, rear or both surfaces.

With these objectives in mind, many different approaches have been proposed in the literature. Among them, one can find nanopyramids [30], nanocones [31], plasmonic scatterers [32] and MIE resonators [33] with good results. For example, reference [34] reports that a 10 μm thick c-Si slice absorbs as much as a conventional 300 μm thick wafer when nano inverted pyramids are introduced. All these alternatives show surface structures in the range of 1 μm or lower. In order to correctly simulate them, the finite difference time domain (FDTD) method should be used [31].

II. 1. 5 Information summary table

In order to have a straightforward vision of the state of the art, several solar cell related parameters are summarized in the Table II. 2 below.

Table II. 2 Summary of the technical parameters of selected thin c-Si solar cells from literature

References	[4]	[5]	[7]	[13]	[14]	[12]	[26]
Efficiency	21.50%	6%-7%	13.70%	16.80%	15.10%	18.90%	14.2%
Thickness	47μm	10 to sub-2μm	10μm	18 μm	20 μm	45 μm	13 μm
Substrate obtaining method	chemical etching	KOH wet etching	RIE etching of SOI	PSI	PSI	PSI	LPC
Structure	PERL	both side contacts	nanocone-IBC	PERL	PERL	BC BJ cell	IBC-SHJ
Passivation strategy	oxide silicon layer	aluminum oxide	Silicon oxide	silicon oxide at the back surface. 75nm SiON at front surface	SiO_2 at back surface; SiN_x at front surface	SiO_2 at lower surface and AlO_x at the front surface	SiO_xN_y(ON(ON)) interlayer at front and a-Si:H at rear with BSF at emitter
Contacts	metal	Cr and Ag	Al	Al+Steel at rear selective n+laser doping followed by Ni/Cu plating at front	Al+Steel at rear selective n+laser doping followed by Ni/Cu plating at front	Al	ITO/Ag
Light trappingat front surface	inverted pyramids	nanocone	nanocone	shallow texturing	shallow texturing	KOH texturing	Anti-reflection foil
Rear surface configuration	electro-statically induced n-type layer	nanocone	IBC (metal Al)	point Al contact	point Al contact	IBC (metal Al)	Rear surface texturing

II. 2 Theoretical and technical background

II. 2. 1 Brief fundamental physics of c-Si solar cells

Generally, solar cell can be regarded as a sunlight-electricity converter that consists of three essential parts, namely, the light absorber, electron collector and hole collector no matter what kind of material it is based on. When the solar cell is placed under the sun, photons reach into the absorber and the electron and hole carriers are generated. Then these carriers gather at their collector regions respectively simultaneously creating a current in the circuit outside the device

and a potential difference between both contacts. Once the device is contacted and circuited with any electronic load, the light can be exploited in form of electricity.

Silicon is a material candidate for the application of light-electricity conversion due to its sunlight-wavelength-suited bandgap, which is 1.12 eV, i.e., photons with energy superior 1.12 eV can give their energy to generate electron-hole pairs. However, neither all the photon with energy higher than the absorber's bandgap can have the opportunity to excite an electron, nor all the generated carriers can be extracted from the solar cell. These facts are two main challenges limiting the energy conversion efficiency of solar cell. More precisely, the former is the light absorption and the latter is the recombination. The thermodynamic energy conversion limit was calculated by Shockley and Quisser [35] to be 29.4% under AM1.5G spectrum condition involving only the intrinsic recombination of silicon.

In the framework of this thesis, crystalline silicon bulk material is the light absorber. Thanks to the relatively longer carrier diffusion length of single-crystalline silicon than multi-crystalline and amorphous material, the light generated electrons and holes can be transported within the bulk material with negligible recombination. How to effectively attract and restrain these carriers to their own collector is actually the core challenge for realizing the function of light-electricity conversion. Doping of n and p type dopant material on different regions of silicon material, as a conventional fabrication method, is a viable path for achieving the separation of carriers. As a by-product, p/n junction is formed. Due to the thermodynamic energy level difference of electron-rich n region and hole-rich p region, the privilege for either electron or hole transport presents. Alternatively, carrier selective layer deposition is employed to achieve the similar function as the p/n doping, for which, the layers that are formed by material favoring the conduction of electron and hole are respectively deposited at each region on the surface of silicon, i.e., electron transport layer (ETL) and hole transport layer (HTL).

(a) Electrical performance under illumination: the IV curve and PV parameters

The question of how much energy can be converted from sunlight to electricity through solar cell is significant. To measure it, a device is characterized by sweeping a range of applied voltage under an illumination that could be sunlight or, more conveniently, the solar simulator in

laboratory. Solar cell is made from a semiconductor material and the electrical performance under dark condition of a solar cell is an analogue to a conventional diode. When a solar cell is illuminated, a photogenerated current (J_{ph}) is added to the equivalent diode circuit. The equivalent circuit is schematized in the Fig. II. 8.

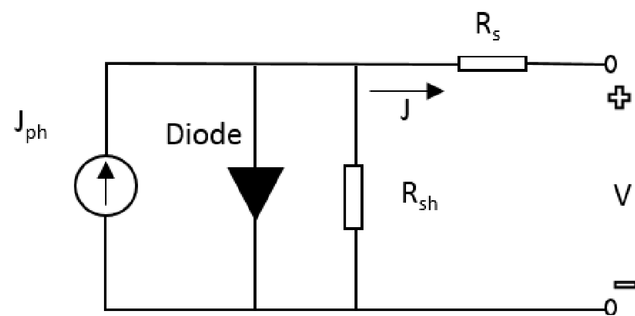

Fig. II. 8 Equivalent circuit of photovoltaic device

The electrical mode presented above includes the series and shunt resistance influences that can alter the solar cell device performance. Along with the increase of series resistance R_s, that could be induced by contact resistance, emitter and base resistance, metal contact ohmic losses, etc., the converted current by solar cell photogeneration is suffered more dissipation and the terminal voltage drops, leading to a lower efficiency. Shunt resistance is set to describe the bypassed current instead of being extracted and used. A very resistive shunt is preferable and a low shunt can degrade the solar cell performance by declining the current at terminal.

In order to describe the electrical performance of a solar cell quantitatively, a mathematical expression is given (II. 1)

$$J(V) = J_{ph} - J_0 \left[exp\left(\frac{e(V - J \cdot r_s)}{nkT}\right) - 1 \right] - \frac{V - J \cdot r_s}{r_{sh}} \qquad \text{(II. 1)}$$

in which, J and V are terminal current density and voltage, J_{ph} is solar cell photocurrent density, r_s and r_{sh} is the normalized series and shunt resistances, e is electron charge, n is the ideality factor that express the relation between current and recombination mechanism (for example, n=1 when recombination takes place at the quasi-neutral regions while n≈2 when it occurs at space charge regions, thus n is normally between 1 and 2), k and T are Boltzmann constant and temperature in Kelvin respectively. J_0 is a kind of coefficient describing the recombination

current density usually named as reverse saturation current density. A higher J_0 implies a stronger recombination that occurs either in space charge region or quasi neutral regions. Based on the expression equation, a J_0 increase leads to a reduction of V_{oc} which should be prevented.

By sweeping the voltage from zero to beyond V_{oc}, a series of current-voltage data pair is obtained. A typical *J-V* curve of a solar cell is shown in Fig. II. 9.

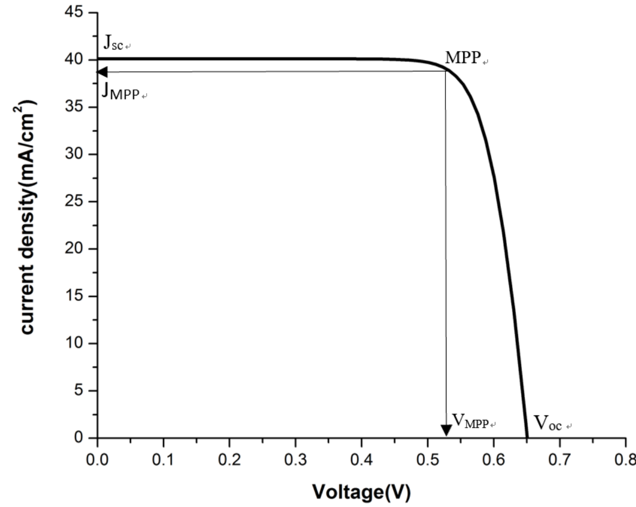

Fig. II. 9 Typical current-voltage curve of solar cell under illumination

As presented in the Fig. II. 9, the efficiency of the solar cell is derived from the ratio between the maximal producible power and the incident solar energy (0.1 W/cm^2 under standard 1 sun condition). The current density and voltage where locates the maximal power point (MPP) are J_{MPP} and V_{MPP}, and the maximal power is the product of both values. Fill factor (*FF*) is a parameter defined as the ratio of maximal power and the product of V_{oc} and J_{sc}. Thus the efficiency can be expressed as (II. 2):

$$\eta = \frac{P_{MPP}}{P_{in}} = \frac{J_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \tag{II. 2}$$

(b) Internal and external quantum efficiency

The current voltage curve is an essential expression of the energy conversion capacity of the device as a whole. However, the performance response of the device on distinct incident light

spectral condition is hard to know with merely J_{sc}, V_{oc} and FF values and the in-field measurement is not always feasible. The measurement on quantum efficiency, or spectral response especially for solar cells, allows estimating the device current output under different spectrum.

Neither all the sunlight can be absorbed by the solar cell absorber, nor all the photogenerated carrier can be extracted and exploited. To each wavelength of light, the ratio between extracted carriers and the incident photons is defined as the external quantum efficiency (*EQE*) for this wavelength of light. This parameter accounts for the optical loss and the photogenerated carriers' recombination before extraction. The optical loss involves any photon that is not absorbed by the absorber material, while the carrier recombination occurs after the photon absorption and carrier separation. Excluding the optical loss, the quantum efficiency is concreted as internal quantum efficiency (*IQE*).

Once the external quantum efficiency is available, the current output under a certain spectrum of light is accessible by integrating *EQE* multiplied by the corresponding incident spectrum for the wavelength range of interest. Similarly, Spectral response is a parameter for a direct calculation from irradiance to the spectrally-resolved current which is also widely used.

(c) Carrier lifetime and surface recombination velocity

As mentioned previously, the internal quantum efficiency describes the capacity of carrier extraction after photogeneration and thus a high *IQE* implies a low recombination. The *IQE* largely depends on carrier lifetime, in other words, the carrier which has a longer lifetime has more probability to be extracted leading to a higher internal quantum efficiency. The pursuing for a high carrier lifetime is one of the most important task during the device design and fabrication, thus the recombination mechanism of carriers should be clarified at first.

Generally, recombination processes can be divided in two types, which are radiative and non-radiative respectively. In case of radiative process, the transition of electron between valence and conduction bands involves the emission of energy in form of photon. On the contrary, there is no emitted photon involved in case of non-radiative process and the energy can be transferred to a third electron or hole carrier, such as Auger recombination, or to the crystal lattice. The latter needs

the presence of a foreign atom or crystal defect that leads to an energy level within the band gap which carriers may occupy. Through this energy trap, recombination of carriers can occur, and it is referred as Shockley-Read-Hall (SRH) generation-recombination.

Therefore, the generation-recombination mechanism of carriers is categorized into radiative, Auger and Shockley-Read-Hall generation-recombination. Therefore, the bulk lifetime is calculated by equation (II. 3):

$$U = \frac{\Delta n}{\tau_{rad}} + \frac{\Delta n}{\tau_{Aug}} + \frac{\Delta n}{\tau_{SRH}} = \frac{\Delta n}{\tau_{bulk}} \quad (II.3)$$

Where Δn is the excess carrier density generated by the light. Since this carrier density is composed by electron-hole pairs $\Delta n=\Delta p$. Assuming a constant Δn along the bulk, the total carrier lifetime is attributed to these three aspects, and the calculation is expressed in equation (II. 4).

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \quad (II.4)$$

Regarding c-Si surface, its recombination rate could be significant since the continuity of the crystal lattices vanishes, and dangling bonds, i.e. defects states, appear due to the partially bonded silicon atoms. Actually, recombination at surfaces follows the SRH mechanism as explained previously, and the net recombination rate is given by adding a parameter called recombination velocity (S).

$$U_{surface} = S \cdot \Delta n_{surface} \quad (II.5)$$

However, the Δn at surfaces can be found much different to the Δn of the bulk, thus an effective surface recombination velocity is appreciated.

$$U_{surface} = S_{eff} \cdot \Delta n \quad (II.6)$$

Obviously, the containment of SRH recombination at silicon surfaces is viable either by reducing the density of defects states or unbalancing carrier concentrations at the surface high recombining areas.

Finally, the total carrier lifetime can be regarded including surfaces lifetime and bulk lifetime. The total carrier lifetime can be measured experimentally leading to the effective minority carrier lifetime (τ_{eff}), and the expression is given (II. 7)

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{eff,front}}{W} + \frac{S_{eff,rear}}{W} \tag{II. 7}$$

in which, W is the thickness of the sample.

II. 2. 2 Fabrication and characterization techniques

In this section, a brief description of the most relevant equipment for fabrication and characterization of the solar cells is reported. Apart from them, there are some other basic laboratory equipment, such as thermal and e-beam evaporator for metallization, RF sputtering, mask aligner and chemical bench, etc., that were frequently used but not described in detail in this document.

(a) Thermal Atomic Layer Deposition, ALD:

The atomic layer deposition (ALD) system in laboratory is the Savannah from Cambridge Nanotech Company. The ALD reaction is actually two sequential non-overlapping precursor-surface reactions that are realized by exposing the sample surface to each type of precursor, then the high quality thin film material is grown by a number of cycles. This deposition technique was exclusively used for aluminum oxide (Al_2O_3) deposition onto c-Si surface. To deposit this layer, the precursors are trimethylaluminum ([$Al(CH_3)_3$], TMA) and H_2O respectively.

The sample is firstly cleaned by a standard RCA process Then the first reaction of an ALD cycle begin with TMA exposure to the sample surface and the gas-solid reaction is self-limited once all the reactive sites on the sample surface is consumed. Next, a gas purge step of nitrogen is carried out to remove the non-reacted TMA and the reaction product CH_4, and at this moment the sample surface is terminated by Al-$(CH_3)_2$. Then a pulse of another precursor H_2O is followed reacting with the dangling methyl groups creating the Al-O-H, and a purge of N_2 is provided for

chamber evacuation, thus a full ALD cycle is finished. By repeating 480 ALD cycles, a 50 nm-thick of aluminum oxide layer is deposited. The deposition condition is shown in the Table II. 3.

Table II. 3 Precursors parameters and deposition conditions for ALD

	Temperature in chamber	Precursors (pulse time)	N_2 purge flow (duration)	Growth per cycle (GPC, Ångström)
Al_2O_3	200 °C	TMA (0.05 sec) H_2O (0.015 sec)	20 sccm (5 sec)	1.1 Å

(b) Plasma enhanced chemical vapor deposition (PECVD):

Plasma enhanced chemical vapor deposition belongs to chemical vapor deposition techniques, which are focused on thin films deposition from vapor phase to solid state on substrate. Process gas is decomposed aided/enhanced by a plasma created by radio-frequency (13.56 MHz) discharge between two flat and parallel electrodes.

In this work, RF PECVD from *Elettrorava* was used to deposit diverse types of thin films, such as amorphous silicon (a-Si:H), phosphorous doped amorphous silicon and silicon carbide (SiC_x). The precursor gases parameters and the deposition conditions are summarized in the Table II. 4 below:

Table II. 4 Precursors parameters and deposition conditions for PECVD

	Temperature(display)	Pressure(mbar)	Potential power (W)	Precursors (sccm)
a-Si:H layer	300 °C (500°C)	0.5	6	SiH_4(36)CH_4(12)
N type a-Si:H layer	300 °C (500°C)	0.5	6	SiH_4(36)PH_3(4)
SiC_x	300 °C (500°C)	1	18	SiH_4(1.2)CH_4(60)

This equipment mainly consists of two chambers, which are load-lock chamber and reaction chamber. After moving the sample into the reaction chamber, precursors gases mixture are introduced though Mass Flow Controller and pumped out continuously for maintaining a constant pressure. Once the plasma is ignited by a RF generator between the upper and lower electrodes, the gas mixture is decomposed in species reacting between them and on the sample surface depositing the film.

II. 3 Solar cell characterization equipment

II. 3. 1 Carrier lifetime measurement

The lifetime performance study of photogenerated minority carriers is valuable for device quality control, i.e., a high carrier lifetime output represents a low recombination within the sample volume (including bulk and surfaces) and it is critical for approaching high efficient solar cell.

The instrument used for photogenerated carrier lifetime measurement is Sinton WCT-120 which is commercialized by Sinton Consulting [36]. Two main parameters that are captured during the measurement which are the photoconductance $\Delta\sigma$ and the light intensity. The photoconductance $\Delta\sigma$ is measured contactlessly by inductive coupling for determining the excess carrier density Δn; while the light intensity is measured by a calibrated solar cell which is located near the sample under test, and the photogeneration rate *G(t)* can be estimated considering the reflection losses of the sample. Then the effective lifetime is calculated (II. 8):

$$\tau_{eff} = \frac{\Delta n}{\left(G(t) - \frac{d\Delta n}{dt}\right)} \qquad (\text{II.} 8)$$

The operation modes of this method can be either quasi-steady-state photoconductance (QSSPC) or photoconductance decay (PCD). In former mode, the light intensity of the illumination varies monotonically with a decay time of about 2.3 milliseconds allowing the balance of both photogeneration and recombination at each moment of time sweeping a range of Δn level (or injection level), while the latter presents a pulse of abrupt illumination (it lasts only about 15 microseconds) and after which the measurement takes place. The QSSPC mode is compatible with a wide range of carrier lifetime performance and the PCD mode is more suitable for relatively long lifetime carrier case.

As mentioned in section, effective lifetime could be related to bulk and surface recombination parameters. In this thesis, high quality Float Zone c-Si material is used as substrates. Then, we can consider only intrinsic mechanisms, i.e. Auger and radiative recombination rates, within the bulk.

Unless otherwise indicated, we use an intrinsic lifetime (τ_{int}) modeled as reported in reference [37] as bulk lifetime. Then, for samples symmetrically covered with passivating layers, we can get their corresponding effective surface recombination velocity (S_{eff}) using the following equation (II. 9):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{int}} + 2\frac{S_{eff}}{W} \qquad \text{(II. 9)}$$

II. 3. 2 External quantum efficiency

The measurement for external quantum efficiency is realized by using QEX10 Model from PVmeasurement. It consists of xenon lamp source, monochromator, filter and optics systems, providing a stable and monochromatic light. The wavelength for measurement ranges from 300 nm to 1200 nm and the intervals are selected to be 10 nm. The light is modulated at 66 Hz by a mechanical chopper.

Firstly the system is calibrated with a reference photodiode to make the sample measurement accurate. Once the sample under test is well positioned and connected, monochromatic light is applied onto the sample surface with about 1×1 cm^2 area sweeping all the wavelength range. Then the external quantum efficiency at each wavelength is calculated as a ratio between the extracted carrier which is derived from the current density and the incident photons. A bias light generated by a halogen lamp in the range of 0.1-0.2 suns is used to reproduce carrier injection conditions inside the device during EQE measurement. The short circuit current under AM1.5G standard solar irradiance is calculated by *EQE*, (II. 10):

$$Jsc = e \times \int_{300}^{1200} EQE(\lambda) \times AM1.5G(\lambda) \times d\lambda \qquad \text{(II. 10)}$$

II. 3. 3 *J-V* and Suns-V_{oc} measurement

With the calculated J_{sc} value by *EQE* under standard condition, the *J-V* curve under STC can be estimated by adjusting the solar simulator to reach an identical J_{sc} output. Then, J-V curve is

measured using Keithley 2601B SYSTEM SourceMeter. Based on the *J-V* curve, the V_{oc} and *FF* value is extracted and thus the device electrical performance is estimated.

On the contrary to *J-V* measurement, the Suns-V_{oc} measurement can give the solar cell performance without series resistance influence. In this setup, light is generated by a flash lamp and only the open-circuit voltage (V_{oc}) of the device is measured while the illumination intensity is monitored by a calibrated cell during each light flash. According to the assumption of linear relationship between light intensity and J_{sc}, measured intensity in suns is converted to current density and the data pair of current density and voltage without ohmic losses impact is obtained (notice that the device is kept always under open-circuit conditions). The Suns-V_{oc} curve has a great value on the qualification of device diode which provides the hint of series resistance impact on solar cell performance, especially on the *FF*.

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Chapter III

Progress in the Millefeuille process: towards high-quality ultrathin c-Si substrates for photovoltaics application

The *Millefeuille* process, initially proposed by MNT group of UPC, aims to fabricate multiple thin monocrystalline silicon layers from a single n-type monocrystalline silicon wafer and in a single technological step. In other words, it aims to multiply a single wafer into multiple thin wafers at once. This chapter discusses the advances obtained in the *Millefeuille* process through optimization of the porous structure. Based on the technological know-how of the *Millefeuille* process, the impact of the exact pore profile on the generated thin layer quality is explored and discussed. In particular, both the in-depth periodicity and the pore shape are studied, and the results are visualized through SEM images.

III. 1 Introduction

As it was presented in the previous chapters, the usage of thinner substrates is expected to be the main feature of crystalline silicon photovoltaics devices fabrication in the near future. This is promoted by the requirement of cost-savings in order to compete with other low-cost photovoltaic technologies. Currently, the main industrial approach to the fabrication of thinner crystalline silicon wafers is using multi-wire saws of smaller diameter. However, due to the lower yield and increased kerf losses, progress in wafer sawing is not believed to go below 80 μm wafer thickness. In spite of that, high-efficient solar cells based on even thinner substrate is still achievable. For instance, 21.2% efficiency has been reported in 35 μm thick silicon solar cell [1]. Thus, there is still margin for wafer thinning and effective cost-saving while maintaining a relatively high efficiency.

Numerous efforts have emerged to overcome the limitations of wafer sawing, enabling the fabrication of thin silicon wafers, below 50 μm, with minimal wafering material losses, as it was reviewed in chapter II. As a brief summary, for example in the Porous silicon (PSI) layer transfer method a thin crystalline silicon layer is grown by epitaxy over a recyclable wafer whose surface has been previously porosified electrochemically. The porous layer acts as seed for the epy-grouth and, at the same time, enables the separation of final thin substrate. This method has been used to fabricate back junction back contact thin c-Si solar cells [2], however the process complexity of this method leads to a low productivity. Another method is to exfoliate thin c-Si films from a thick substrate by weakening a crystalline plane at a certain depth (such as proton implantation [3]) inside the substrate which in turn can be used as a back contact in the solar cell [4]. This method is similar to the “smart cut” [5] which is used for fabricating SOI wafers. Liquid phase crystallized silicon layers is another promising pathway [6], in this case the thin silicon substrate is achieved by evaporation of silicon on a glass and its subsequent recrystallization thus a low quality of obtained layer is expected.

Another route to produce thin silicon is based on the “empty-space-in-silicon” (ESS) method, devised by Mitsushita and Sato [7, 8]. The ESS method consist in, first, creating an ordered array of pores on the surface of crystalline silicon through standard lithography and dry etching

techniques. This structure is then annealed at temperatures above 950 ºC in deoxidizing ambient, usually Ar or H with very low O_2 partial pressures, so that surface diffusion of silicon is activated. Under the action of surface diffusion, pores collapse trapping a bubble behind the surface (See Fig. III. 1). For close-enough packed pores, trapped bubbles contact laterally, collapsing into a spacing layer and resulting in a thin free-standing silicon layer. Since this process occurs in solid phase by surface diffusion, the final layer is made of high-quality monocrystalline silicon. Although The ESS method was initially conceived for developing silicon-on-nothing electronic devices, Depaw *et al.* proposed to use it as a kerf-less wafer slicing method, by pealing-off the free-standing monocrystalline layer, for developing ultra-thin (1 μm thick) solar cells [9, 10].

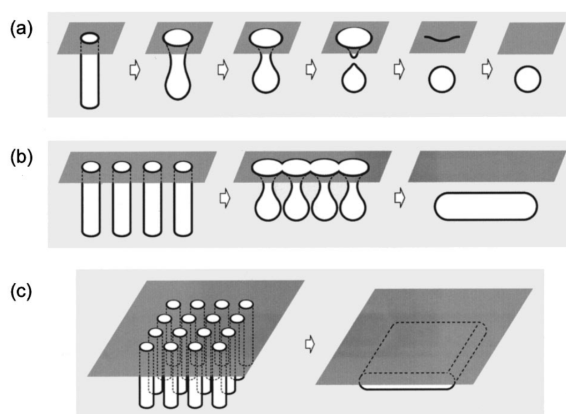

Fig. III. 1 Schematic ESS process. (a) Transformation of a pore into a trapped bubble; (b) Transformation of a line pores into a trapped void; (c) Transformation of a matrix pores into a trapped void. After Empty-space-in-silicon technique for fabricating a silicon-on-nothing structure. [7]

The ESS method creates a single thin layer per process, and further thin layers can be obtained after recycling the substrate, however this imply a polishing step and the repetition of all the process steps. This bottleneck makes this approach expensive and less appealing for photovoltaics application. In order to improve the productivity of thin films from the ESS method, an alternative approach that aims to produce multiple thin monocrystalline layers fabrication in a single step was proposed [11, 12]. In contrast with the ESS method, that uses shallow pores on the surface, here deep pores (hundreds of micrometer depth) are etched electrochemically on the wafer with a particular in-depth pore diameter modulation. During the annealing process, the long pores collapse into a string of bubbles that end forming multiple void planes, resulting in multiple layer

production at one. This process is known as *Silicon Millefeuille* process, in reference to the French pastry, as many free-standing layers can be obtained.

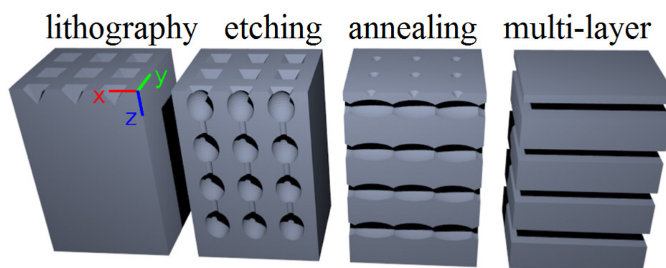

Fig. III. 2 Schematic representation of each experimental step of *Millefeuille* process [11]

The main steps of the *millefeuille* process are shown schematically in Fig. III. 2. As it can be observed, it consists of two main stages: macroporous silicon fabrication with particular in-depth form, and high temperature annealing in hydrogen/argon deoxidizing environment. The silicon macropores formation is made by electrochemical etching and a versatile in-depth porosity formation can be achieved. The annealing step, just as in the ESS method, activates the surface atomic diffusion mechanism, transforming the porous silicon structure into a stack of monocrystalline free-standing layers. One key aspect of the *Millefeuille* process is the in-depth modulation of the pores. The low/high porosity regions created define where the layer/spaces will form. As a result, it defines the number and size of the layers produced. In addition, the exact pore profile created also influences the quality of the final layers as well as the robustness of the process itself. In this chapter, based on the technological know-how of the *Millefeuille* process, the impact of initial pore profiles, i.e., in-depth pore modulation and periodicity, on the property of final generated thin silicon layers is studied.

This chapter is organized as follows. First of all, the experiment-related background theories are briefly introduced involving macroporous silicon fabrication technique and macropores reorganization under high temperature annealing. The detailed experimental method of *Millefeuille* process is described. Next, the impact of initial pore profile, i.e., in-depth pore modulation and periodicity, on the final thin layer property is evaluated. Aiming at high quality thin layer generation for photovoltaics application, three distinct pore profiles candidates are proposed and fabricated. Then, the property of final thin layer is visualized by scanning electron microscope

(SEM) images on the cleaved side for all samples. Finally, the relationship between the voids evolution and annealing time is demonstrated by SEM images employing a square-profile sample.

III. 2 Theoretical background

The *Millefeuille* process is a kind of silicon layer transfer approach allowing multiple thin c-Si layer fabrication from a single n-type single crystalline silicon wafer. It consists of two main consecutive steps, namely, the macroporous silicon formation and the reorganization of the porous structure into a stack of Si layers. The former is realized by electrochemical etching of n-type silicon in hydrofluoric acid (HF) solution and the latter is achieved by surface diffusion through a high-temperature annealing/reorganization in deoxidizing environment. The following sections introduce the fundamental theories of both aspects of the process.

III. 2. 1 Macroporous silicon

Macroporous silicon refers to the formation of ordered arrays of pores in crystalline silicon through anodization in aqueous HF solution and under illumination. The formation of porous silicon through anodic etching was first reported in the 50s by Uhlir and Turner [13, 14]. The porous random structures, with pore sizes that can range from nanometric to micrometric scales, are formed by the anodic dissolution of Si in the HF solution, with the remaining silicon retaining the monocrystalline nature and crystal orientation of the original wafer [15]. It wasn't, however, until the year 1990 that Lehman and Föll reported that ordered macropore patterns could be electrochemically etched by using a pre-structured n-type silicon electrode under back-side illumination [16-18]. The back-side illumination gives rise to the generation of minority carrier holes inside silicon bulk which provides the reactants for the silicon anodic dissolution with HF electrolyte. Based on this model, the porous silicon formation with desired geometry can be realized by adjusting the controllable variables such as illumination intensity, silicon doping level, HF concentration and temperature. It should be mentioned that although there is no single theory to explain the porous silicon process due to its extremely complex nature of chemical reactions and resulting morphology, the knowledge on the phenomenological models still allows us to

control the porous silicon processing with beforehand design, aiming at the *Millefeuille* process. Details of Lehmann's model is described in the following part.

The anodic dissolution of Silicon in HF consumes holes. Macroporous silicon is formed in n-type silicon, therefore, in darkness the availability of holes (the minority carriers) is very small and the electrochemical reaction is stopped. A schematic illustration of the silicon macropores formation process is shown in Fig. III. 3. As it can be observed, holes are provided through back-side illumination, which generates holes that diffuse towards the silicon/electrolyte interface, promoting the reaction there. During the etching, the polarization of the silicon/electrolyte interface leads to the formation of a space-charge-region (SCR) at the silicon surface, indicated in Fig. III. 3 [19]. The electric field associated to the SCR can act as a lens, focusing the arriving holes at the tip of the pores or at the tips of the inverted pyramids at the start. This is a key factor for stable pore growth, as it will be discussed.

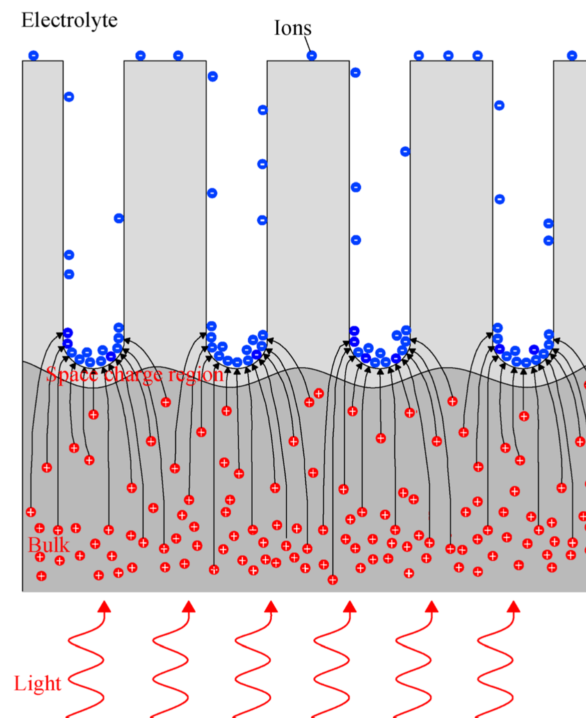

Fig. III. 3 Schematic illustration of the macropore formation in low doped n-type Si [19]

An important parameter of the Lehmann's model is the critical current density J_{ps}, that sets the threshold between pore formation and electropolishing. The current J_{ps} depends on the HF concentration and temperature and can be calculated with the equation (III. 1).

$$J_{ps} = C_{ps}c^{1.5}exp\left(\frac{-E_a}{kT}\right) \tag{III. 1}$$

where C_{ps} is the current density coefficient, c is the HF concentration in percentage by weight, E_a is the activation energy that is the minimum energy required for the dissolution to occur, k stands for Boltzmann constant, and T is absolute temperature in K. The critical current density J_{ps} also depends on the crystal direction, being the biggest for silicon electrodes of <100> orientation.

According to Lehmann's theory, when the applied current density is greater than J_{ps}, diffusion of fluoride ions to the silicon/electrolyte interface is slower than the transport of holes that have been created by back illumination of the wafer. An excessive surface charge of holes builds up and, therefore, the HF molecules that reach any point on the interface will always encounter holes to react. Since convex parts of the silicon electrode are more exposed to the electrolyte, they will dissolve faster, softening the surface of the silicon. On the contrary, when the applied current density J is less than J_{ps}, the minority holes created in the sample with LEDs illumination assistance diffuse to the reaction interface region which are focused at the pore tips due to the hole carrier depletion at the space charge region. Thus, the macropore walls become passivated against dissolution and pores grow in vertical direction. The Fig. III. 3 is an example of the macropore formation when the current density J is below the critical current density J_{ps}.

Fig. III. 4 shows a typical current-voltage characteristic of n-type silicon electrode in aqueous HF solution under different levels of illumination (dashed red lines). The solid red line represents the *I*-*V* curve under strong electrode illumination. For low back side illumination cases, as represented by dashed lines, the reaction is limited by the electrode hole supply instead of the ionic transfer from the electrolyte, and steady pore growth occurs for positive bias, although the applied potential is above the J_{ps} corresponded V_{ps}.

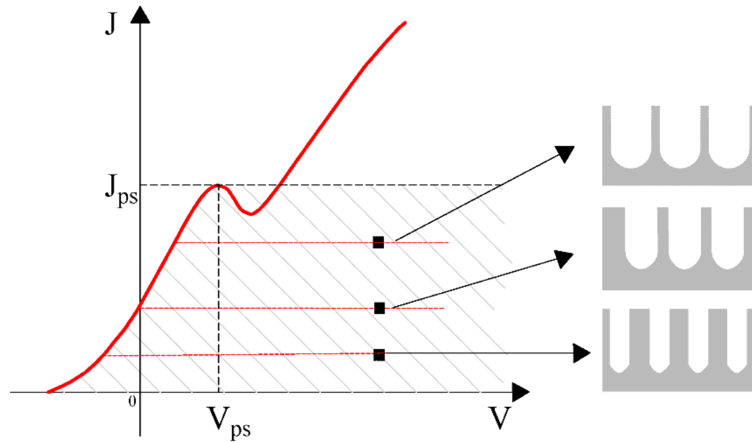

Fig. III. 4 *J-V* characteristic of illuminated n-type silicon electrode in aqueous HF solution. [11]

Lehmann's model takes as assumption that the current density at the pore tips J_{tip} equals, for stable pore growth, the critical value J_{ps}. The ionic transfer from the electrolyte and charge supply from the electrode are, therefore, in steady-state condition at the tips. Due to the lateral passivation of the pores, all charge transfer occurs at the tip of the pores, so the total etching current I equals to the sum of the cross-sectional areas of all pores A_{pores} multiplied by J_{ps}:

$$J_{ps} \cdot A_{pores} = J \cdot A = I \qquad \text{(III. 2)}$$

where A is the initial contact area between the silicon electrode and the electrolyte. The porosity is then calculated as (III. 3):

$$p = \frac{J}{J_{ps}} = \frac{A_{pore}}{A_{cell}} \qquad \text{(III. 3)}$$

in which, p is the porosity of the active area, the A_{pore} is cross-sectional area of the pore, A_{cell} is the cross-sectional area of a unit cell of the pore lattice. If the etching current density J is constant throughout the sample, all pores will be equal in size and dimension, which in turn can be altered by changing the current density by back illumination control. The greater the current, the bigger the pore diameter and vice versa.

The growth rate v of the pores can be calculated through the following equation (III. 4):

$$\nu = \frac{J_{tip}}{nqN_{Si}} \tag{III. 4}$$

in which, J_{tip} is the current density at the pore tip, n is the number of charge carriers per dissolved silicon atom with average number 2.6, q stands for the elementary charge ($1.602\text{x}10^{-19}$ C), and N_{Si} is the atomic density of silicon ($5\text{x}10^{22}$ cm^{-3}).

In summary, by adjusting the applied potential V on n-type silicon electrode in aqueous HF solution and the backside illumination intensity, any of the points in the shaded region representing different pore size in Fig. III. 4 can be obtained. This pore size controllability is the theoretical foundation of the multiple-size pore formation in *Millefeuille* process, allowing to make quantitative and measurable predictions for the resulting pore geometry.

III. 2. 2 Silicon macropore reorganization by annealing

The second step of the *Millefeuille* process is the macroporous silicon reorganization by high-temperature annealing, leading to the formation of solid layers and space layers, even when the temperature is significantly lower than the melting point. The background theory of this experiment can be described as an analogy of the well-known Plateau-Rayleigh instabilities for fluid mechanic, saying that a free falling stream of fluid, initially of a constant radius, is inherently unstable and that will eventually break into a series of droplets with a characteristic spacing between them [20]. In the particular case of high-temperature annealing of c-Si porous structures in deoxidizing environment, such as H_2 and Ar, pores evolve by surface diffusion tending to reduce the surface energy, leading to Rayleigh instabilities and resulting in a series of bubbles beneath the silicon surface. The pores evolution is similar to that of fluid cylinder although the process occurs in solid phase by surface diffusion. In order to generate the separated solid silicon and space layers, the pores must be closely packed, so that the formed bubbles can contact laterally collapsing into a space layer and creating the solid silicon layer on top.

The transformation mechanism leading to surface energy reduction is explained by surface atomic diffusion, which is driven by the gradients in surface curvature k. A flow of atoms from high curvature, where the atoms presents a higher chemical potential, to low curvature regions

appears to reduce such difference. This transformation mechanism is studied by Mullin [21], and a surface diffusion model is proposed.

According to Mullin's model, the atomic diffusion current density J on the surface is given by

$$J = \nu\sigma = \frac{-D_S\gamma\Omega\nu}{k_BT}\nabla_S k \qquad \text{(III. 5)}$$

where ν is the number of atoms per unit area and σ is the rate of atoms diffusion in the surface, D_S is surface self-diffusion coefficient, γ is surface free energy per unit area, Ω is atomic volume, k_B stands for Boltzmann's constant, T is the absolute temperature, and ∇_S indicates surface gradient operator. Thus, the speed of atoms accumulation can be expressed (III. 6):

$$v_n = \Omega\nabla_S \cdot -J = \frac{D_S\gamma\Omega^2\nu}{k_BT}\nabla_S^2 k \qquad \text{(III. 6)}$$

where speed v_n is in the normal direction to the surface and proportional to atomic volume Ω, ∇_S^2 represents de Laplace-Beltrami operator.

Finally, by connecting all the equations, the normal velocity of the evolving surface is obtained, which is known as Mullin's equation [21], as shown below (III. 7-9):

$$v_n = B\nabla_S^2 k \qquad \text{(III. 7)}$$

with

$$B = \frac{D_S\gamma\Omega^2\nu}{k_BT} \qquad \text{(III. 8)}$$

and

$$k = \frac{1}{2}(k_1 + k_2) \qquad \text{(III. 9)}$$

The parameter B in equation (III. 8) is a constant and account for the material and absolute temperature. The surface self-diffusion coefficient D_s, surface free energy per unit area γ, atomic volume Ω, number of atoms per unit area ν and absolute temperature T are measurable. The

gradients in surface curvature k is the mean curvature of the surface, defined as the average of two principal curvatures, k_1 and k_2. Through controlling surface curvature of the macropore, i.e., pore in-depth diameter, distinct pore surface evolution are expected under high temperature annealing.

III. 3 Experimental method:

The experiment starts from a 4-inch, 350 µm-thick Czochralski (CZ) n-type silicon wafer with both sides polished. The crystal orientation of silicon wafer is <100> and the resistivity is 0.5 Ω·cm. A highly doped n^+ layer is firstly ion-implanted on the back surface of the wafer that works simultaneously as transparent contact and as a back surface field for minimizing surface recombination losses. Based on the schematic experimental procedure of *Millefeuille* process shown in Fig. III. 1, the detailed experimental steps are described in the following sections.

III. 3. 1 Surface inverted-pyramids patterning

A brief summary of the photolithography procedure is reported hereby and a schematic sample preparation diagram is shown in Fig. III. 5. In order to etch inverted-pyramids at front surface, an oxide layer is thermally grown as a mask. Simultaneously, the rear contact of n^+ layer is improved since the implanted impurities at rear surface are driven-in during the high temperature oxidation. Next, the thermally grown oxide layer is protected by photoresist mask, and 1×1 µm square array with 2 µm pitch is created through photolithography. Then the oxide layer is patterned by RIE etching. Finally, inverted-pyramids are etched by TMAH at the exposed c-Si surface. These four technological steps are described in detail below.

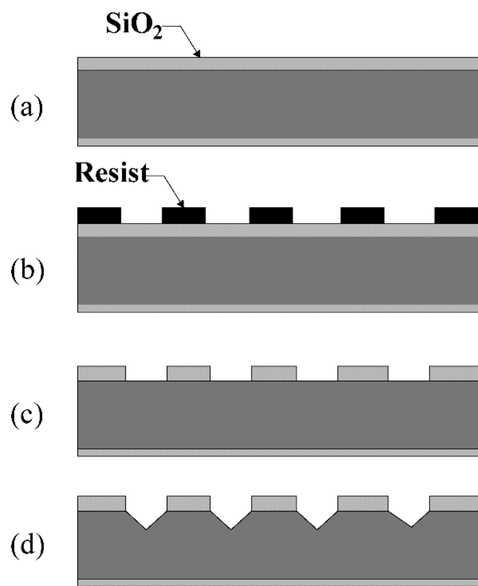

Fig. III. 5 Main process sequence for sample preparation: (a) wafer oxidation; (b) photolithography; (c) oxide layer etching for window opening; (d) TMAH for inverted-pyramids etching.

(a) Thermal growth of SiO_2 mask

After the rear surface n^+ layer implantation, 70 nm of high quality silicon oxide layer is thermally grown. A standard RCA wafer cleaning is carried out just prior to introducing the wafer into the previously cleaned furnace. The starting temperature of oxidation is 600 °C and the set-point is 1150 °C for ensuring a reasonable oxidation rate. The sample wafers are taken out after the process is finalized when the temperature is cooled down to 600 °C.

(b) High resolution lithography

1 Mask preparation: a glass shadow mask is used and it is firstly cleaned with spin coating machine, during which acetone, propanol and deionized water are sprayed onto the glass mask surface consecutively. One must be sure the mask is absolutely dry when this process is completed. Finally, it is assembled at the lithography mask aligner.

2 Wafer cleaning: sample wafer is immersed in acetone and isopropanol solutions for 5 minutes respectively through ultrasonic cleaning, then dried.

3 Photoresist layer spin coating: before spin coating, one must be sure that the wafer stays totally clean and the surrounding ambient stays undisturbed. Optionally an extra cleaning can be done by spraying acetone and propanol onto the spinning wafer. Once the sample is clean and totally dried, a HMDS thin layer (about 10 drops) is spin-coated prior to the photoresist drop for improving the adhesion between this layer and the oxide surface. The positive photoresist used in this step is S1805 and about 500 nm thick layer is formed onto the sample surface after spinning (3000 rpm). Afterwards, the sample is baked for 90 seconds on the hotplate at 115 °C.

4 Photolithography: sample is located under the mask and exposed for 14 seconds under U.V. light.

5 Photoresist developer: the sample is dried again on hotplate for 90 seconds at 115 °C. After cooling down, it is submerged into the developer solution. Finally, the wafer is cleaned by deionized water and dried by nitrogen blowing.

6 Microscope view: the sample is observed under optical microscope to evaluate the photolithography quality. The whole step should be repeated if failed.

(c) SiO_2 etching by RIE

1 Chamber cleaning: the RIE chamber is cleaned with a dummy wafer with gas component: Ar 50 sccm and CHF_3 50 sccm under chamber pressure 30 mTorr. The power used for ion generation is 275 W and the duration is 10 minutes to avoid any unexpected contaminants.

2 SiO_2 etching: the gas recipe and other conditions are the same as in chamber cleaning but the duration is 5 minutes, which is sufficient to etch the 70 nm SiO_2 layer in the area predefined by photolithography. A reasonable Helium flow is also required to maintain the sample well positioned.

3 Photoresist strip: afterwards, the photoresist layer is striped by oxygen ion without taking out the sample. The introduced gas is O_2 with a flow of 50 sccm. The RF (radio frequency) power is set to be 100 W and ICP (inductively coupled plasma) power is 1000 W. The chamber

pressure is 10 mTorr for this process. The duration is 2 minutes according to the thickness of the photoresist layer.

4 Chamber cleaning: A standard chamber cleaning is carried out after taking out the sample. The oxygen flow is 50 sccm while RF and ICP power are 100 W and 2000 W respectively.

(d) Inverted pyramid etching by TMAH solution:

1 Sample cleaning: the wafer is firstly cleaned by acetone and isopropanol following the same steps reported in high resolution lithography.

2 Anisotropic TMAH wet etching: the 25 *wt.*% TMAH solution is heated to 80 °C with a stir bar working continuously. Then the sample is immersed in the etchant solution for some minutes and it is observed under microscope. This step should be repeated until the inverted pyramids are created and confirmed under optical microscope view. These pyramids define the sites where the pores nucleate and grow in the subsequent steps.

3 SiO_2 mask remove: The silicon oxide layer is removed by HF solution at last.

A SEM image of the sample surface morphology after this step is revealed in the Fig. III. 6.

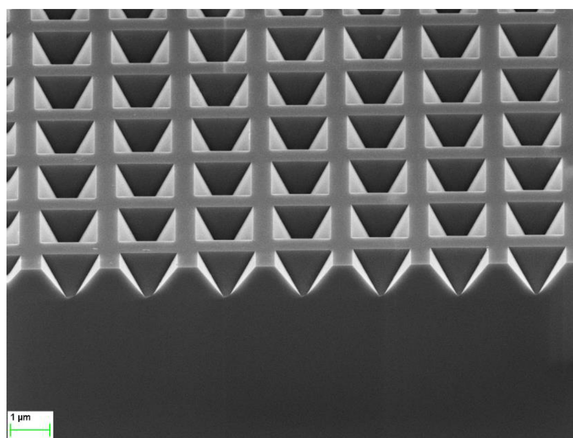

Fig. III. 6 SEM image of cleaved sample inclined front view: 2 µm-pitch inverted pyramids morphology after photolithography, RIE etching, and TMAH etching processes.

III. 3. 2 Electrochemical etching

The electrochemical etching for silicon macropores formation is realized in a circulation pump system, which is made of Polyvinyl Chloride (PVC) because of its resistance to low concentration HF and simplicity of material shaping. The core set-up where the electrochemical process occurs is schematically shown in the Fig. III. 7 [11].

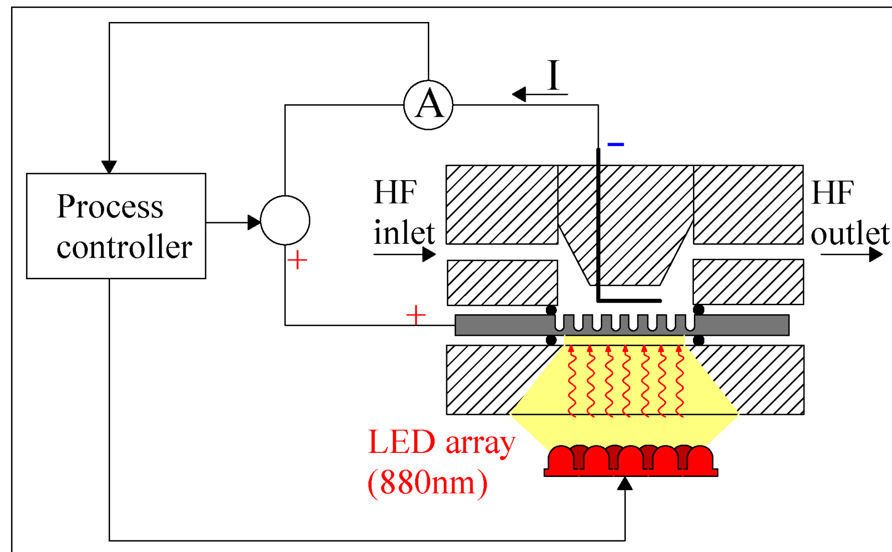

Fig. III. 7 Schematic illustration of the electrochemical etching set-up [11]

A voltage bias is applied on the electrical circuit that is composed by the silicon sample and the circulating HF solution. An array of LEDs with 880 nm light emission wavelength is tightly arranged at the backside of the sample and its light emission intensity is adjustable. By the simultaneous feedback of the circuit current measurement, both light intensity of the LEDs arrays, i.e. the free carrier generation at the Si material backside, and the voltage bias are adjusted by the process controller to ensure that they have the desirable values. The generated free hole carriers diffuse to the Si-solution interface and the etching process takes place as the theory introduced in the previous part resulting in a stable pore growth.

The reaction cell is connected by two tubes, namely inlet and outlet, through which the HF solution as the electrolyte is circulated. The electrolyte is prepared by diluting 50 *wt.*% HF in de-

ionized water up to the concentration of 5 *wt.*%, e.g. 190 ml of 50 *wt.*% HF in 1560 ml of de-ionized water and 440 ml of ethanol. The deposit tanks from where the electrolyte will be pumped are then filled with 1.5 L of this 5 *wt.*% HF solution that ensures a constant HF concentration during the etching.

Other elements of the assembly are a heat exchanger with a thermostat to control the temperature to be constant at 10 °C during the process, a nitrogen conduit to bubble the HF solution to prevent the oxygen dilution and other controller to regulate the LED illumination, voltage and current injected into the sample.

Firstly, the 4 inch wafer is cleaved into individual square samples that should be larger than the rubber band with approximate 2.5 cm^2 circular etching area to avoid any solution leakage. A sample cleaning is necessary under HF solution to remove any native thin oxide layer before assembling with the reaction cell. In order to realize the in-depth pore formation with the desired profile, the supply and surface concentration of hole carriers is accurately controlled through the applied voltage and the back illumination intensity. Then, these two principle variables are transferred to be in function of time instead of depth through an empirical two order relationship (III. 12):

$$t = C_a * l + C_b * l^2 \qquad \text{(III. 12)}$$

where *t* is time and *l* is depth. Hence, the pore diameter in-depth tailoring is enabled.

After the sample cleaning, it is carefully inserted inside the electrochemical cell with the treated front surface in contact with the electrolyte and as soon as the temperature of the solution reaches 10°C, the etching begins. The etching total time depends on the pore modulation profile and depth.

At the end of the etching, the sample is carefully removed and cleaned with de-ionized water to remove the remaining HF. The electrochemical cell is also cleaned to be reused. The sample is cleaved at the edge side to examine under microscope as an immediate assessment of macropores quality. Additionally, SEM images are also taken for the good candidates to confirm the correct

pore formation. Once the macropores are formed as expected, the sample is ready for high temperature annealing to generate the multiple-layer structure.

III. 3. 3 High temperature annealing

Before the annealing, a long dip (20-30 min) in 5% HF solution just before annealing the sample is critical to remove the native oxide layer at the silicon-pore interface. Then, it is annealed in a horizontal furnace in a non-oxidizing environment with gas mixture of 95% Argon and 5% Hydrogen at high temperature, around 1200-1300 °C, enabling the pore morphology evolution by silicon atomic surface diffusion. These high temperatures provide a sufficient mobility to silicon atoms to enable efficient pore transformation, although the diffusion can also take place at lower temperatures but for longer annealing times. Since the tube oven has a large useless space, the Argon/Hydrogen flow is kept high during the annealing process to avoid any impurity gas presence, especially oxygen. To avoid formation of defects in the sample (surface roughening, holes or pillars), the density of particles and the concentration of oxidizing impurities in the atmosphere inside the oven should be as low as possible [22]. During this process, pores collapse forming bubbles first, which later coalesce laterally forming empty layers separating the different final silicon foils. The sample is taken out when temperature falls below 500 °C. Finally, sample structure after annealing is also visualized through SEM images.

III. 4 Experimental design and results

III. 4. 1 Silicon layer formation dependence on macropore profile modulation

The pore surface curvature is the origin of the pore shape evolution and the exact pore profile can be tailored by light intensity control during the electrochemical etching, as explained in the previously parts. Thus, an intended pore surface structure can be modulated for obtaining an appropriate pore profile to realize high quality thin Si layer formation. In order to gain an understanding of the impact of pore profile, a set of experiments with different initial profiles are designed and presented.

Firstly, three different profile shapes and three different in-depth modulation periods are involved resulting in a total of nine silicon samples fabricated by electrochemical etching following the experimental method described previously. The profiles include a square profile, a saw-tooth profile and a sinusoidal profile. For every pore shape, three different samples with modulation period, L_z, of 8 µm, 12 µm and 16 µm are processed, while the number of modulation cycles is 7 for all samples. In the plane, pores follow a perfect square lattice with an in-plane periodicity Λ=2 µm ruled by the patterned surface pyramid. All samples have been designed targeting a minimum pore diameter d_{min}=0.5 µm, a maximum pore diameter d_{max}=1.5 µm and an average pore diameter of d_{av}=1 µm. Finally, all samples are annealed for 3 hours at 1200 ºC in H_2/Argon ambient.

The cleaved side of all processed samples before and after the annealing are revealed by SEM images (see Fig. III. 8-10). As it can be observed, images on the left present the pore shape after electrochemical etching while the right ones show layer formation after annealing. For every pore profile, three modulated periods are shown sharing the same scale bar of 10 µm.

(a) Square profile

This is the original profile shape reported in the *Millefeuille* technique [11, 12]. The idea of this profile design is to modulate the diameter as strong as possible to minimize the amount of silicon atoms that must diffuse and, thus, the annealing time. Since the Si electrochemical etching dynamic does not allow to produce a sudden change in the pore diameter, a transition region with a certain slope (generally large) is introduced to realize the strong modulation. It can be observed that the diameter transition is abrupt between narrow and wide pores, where the most surface curvature difference is observed. Then, it can be assumed the bulk material pinch-off occurs first at the transition regions separating the narrow and the wide pore sections.

As there are 7 modulation cycles, the difference of the etching performance along the depth should be taken into consideration. During the pore growth, the sample surface morphology is changing since the HF electrolyte (F ion density) supply at the pore tips is slightly reducing due to the longer diffusion distance resulting in a lower J_{ps} (equation III. 1) as well as etching speed (equation III. 4). In order to maintain the pore diameter stability, the current density, i.e. the

assisted light intensity, should be reduced correspondingly to compensate the J_{ps} reduction along the process.

For narrow pore section, either a solid Si layer without any bubble or, one or more bubbles are generated from the trapped voids, as shown in the Fig. III. 8. By comparing among three periods, it can be assumed that the bubble formation inside the Si layer depends on the modulation length, i.e., the narrow pore section should be relatively short to avoid any bubble formation during the annealing to obtain a solid thin Si layer. It has been quantitatively concluded by Garín *et al.* [23] that each section will pinch-off into one or more bubbles depending on the length to diameter ratio (l_{min}/d_{min} and l_{max}/d_{max}), that from no bubbles to even more than four bubbles can occurs. In order to make straightforward comparison with other profiles, a fix d_{max}=1.5 µm and l_{max}=l_{min} for all cases are targeted.

Similarly, the wide pore section of the square profile develops into a large bubble (regulated by the dependence with the ratio l_{max}/d_{max}) becoming spherical, eventually touching and coalescing with the neighbouring ones leading to the empty layer formation since they all lie in a periodic matrix along a plane.

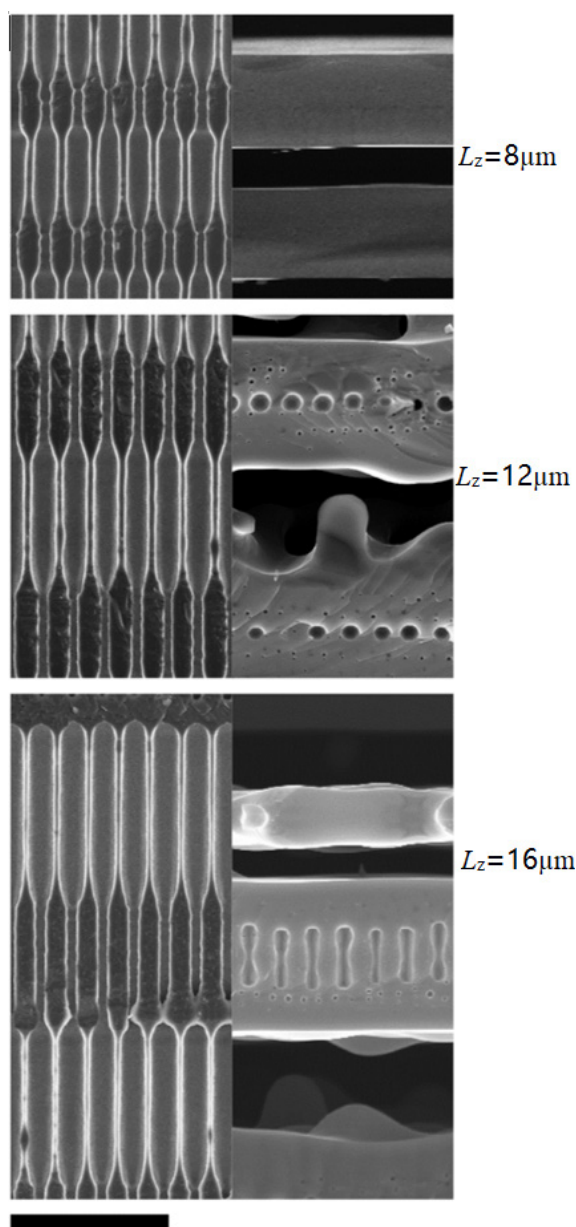

Fig. III. 8 Scanning electron microscope (SEM) images, cross-section view, of samples with square pore profile before and after the high-temperature annealing. The scale bar represents 10 μm.

(b) Conical profile.

As we have seen in the previous sub-section, the square pore modulation profile results in successfully separated thin Si layers that is confirmed by SEM image. For the case of 8 μm period,

there is no bubbles imbedded and the front and rear surfaces are plane and smooth. In order to have an insight on the bubbles formation mechanism, i.e., the bubbles formation dependence, other types of modulation are studied, for instance, the conical profile.

Instead of modulating symmetrical sharp pore transitions like the case of square profile, a steady linear slope of pore diameter is created connecting the widest and narrowest pore points, as revealed in the Fig. III. 9. It should be noticed that a parameter adjustment, such as a pore diameter correction, should be done to compensate the reduction of J_{ps} along the etching like in the previous case to yield a consistent pore diameter among each period.

Similarly, the strong diameter transition regions between each period prone to pinch. Thus, a cone shaped void is trapped at beginning of annealing. Afterwards, the conical voids develop to bubble either with one, as shown in 8 μm case, or three bubble planes in line with a reducing size, as revealed in case of 16 μm period after 3-hours of annealing. The bubbles location is no longer in the middle of the formed layer and theirs sizes are clearly different. The number of bubbles depends on the period distance as only one bubble plane are generated in case of 8 and 12 μm cases but three bubble plane are produced when the periodicity is 16 μm, while the bubbles size follows the progressive change of the pore diameter. It can be concluded that the mirror symmetry distribution of bubbles observed for conical profile is a direct consequence of the mirror symmetry of the pore profile modulation.

Furthermore, it is also worthy to notice that the front and rear surfaces of formed layer does not have equal smoothness, as obviously shown in Fig. III. 8 (L_z=16 μm) where a concave region can be observed due to the asymmetry modulation again. However, the rear surface presents much planar condition in the same annealing duration. Then a smoother front surface is expected if a longer-time annealing is applied.

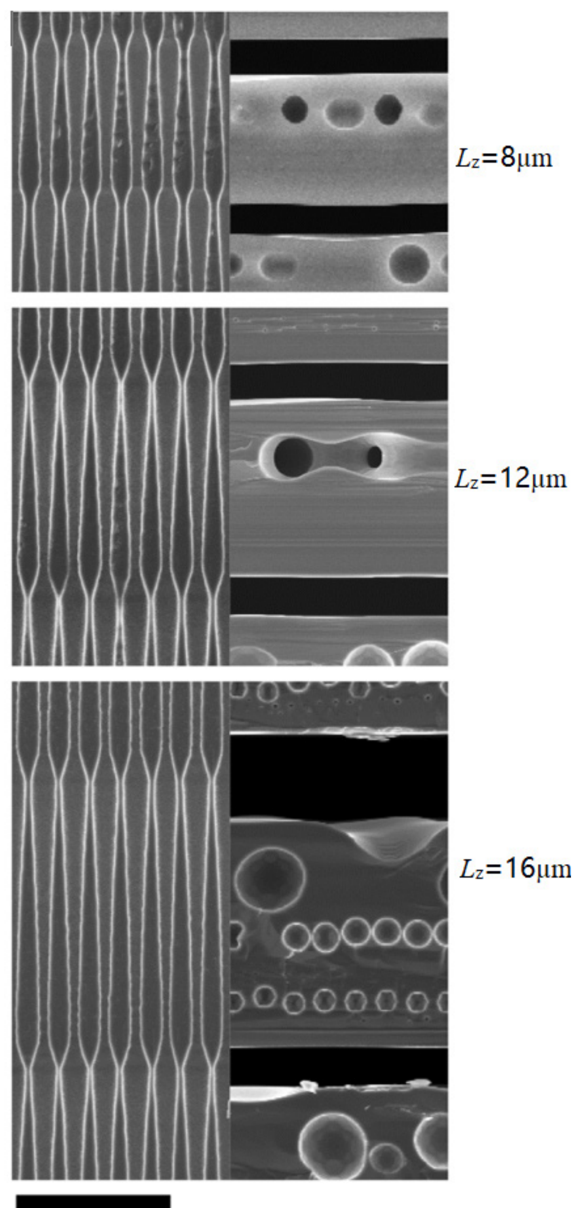

Fig. III. 9 Scanning electron microscope (SEM) images, cross-section view, of samples with conical pore profile before and after the high-temperature annealing. The scale bar represents 10 μm.

(c) Sinusoidal profile

Both square and conical profiles present the possibility of thin Si layer formation with minimized bubbles formation inside. This objective can be approached by reducing the modulation length. However, a consequence of this strategy is that the formed thin Si layer thickness is limited, as shown in case of 8 μm period square profile. In order to particularly avoid the bubble formation

during the pore surface transformation, a sinusoidal profile is proposed. In this profile, the diameter of the etched pores alternates in-depth following a sinusoidal pattern and there is no sharp transition region, as shown in Fig. III. 10. The maximum and minimum diameter as well as the l_{max}/d_{max} ratio follow the same values of the other two profiles.

In Fig. III. 10, thin Si layers are formed with a reasonable thickness in 8 µm case, although there is some imperfection voids left. As for12 µm case, the bubble appearance is largely reduced comparing with the previous profiles and a relatively thicker Si layer is formed. On the contrary to the strong square profile and conical modulation, the sinusoidal profile is assumed to have lower annealing efficiency, since for the same annealing time the 16 µm case is still at the stage before the spacing layer formation. It should be noticed that bubbles are randomly distributed for 12 and 16 µm cases after annealing. Further studies are needed to identify the origin of this scattering, such as imperfections of the fabricated pores. Regarding surface quality, a good surface smoothness can be observed by SEM images in 8 and 12 µm cases.

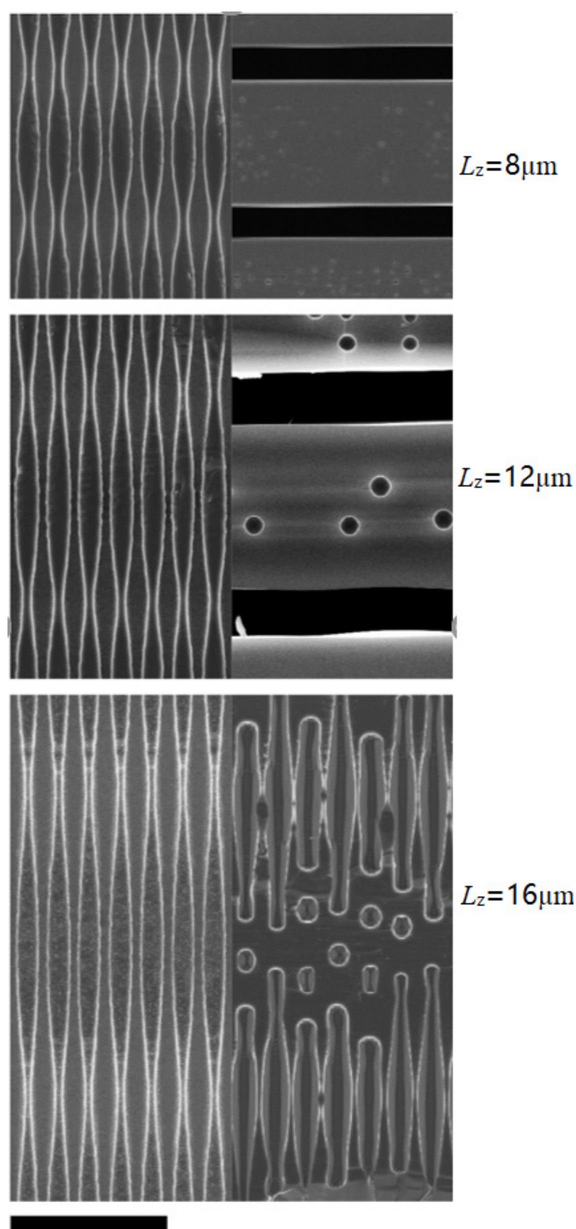

Fig. III. 10 Scanning electron microscope (SEM) images, cross-section view, of samples with sinusoidal pore profile before and after the high-temperature annealing. The scale bar represents 10 μm.

In conclusion, all these three profiles has the potential for thin Si layer fabrication, depending on both pore dimension and periodicity. Respectively, square profile, as the classical profile for *Millefeuille* process, can lead to thin silicon layer formation but the bubbles are tend to be the secondary product buried symmetrically to the middle plane of the Si layer. Conical profile

presents a similar layer formation capacity, but the distribution of bubbles with different sizes follows an asymmetrical order due to the shape of the pore. Both profiles could form perfect thin Si layer once the periodicity is small enough. Sinusoidal profile is more promising regarding the generation of bubble-free thin Si layer. However, due to its relatively low pore transformation efficiency, the annealing time for obtaining a bubble-free Si layer with smooth surfaces should be longer. Alternatively, a similar result can be obtained for square modulation by reducing the depth/diameter ratio at the narrow pore section, as reported in bubble generation simulation [23]. Hence, there are two ways to accomplish this reduction: reducing the depth or increasing the diameter at narrow section of the pore. Thinner layers are expected in the former case, while in the latter case a longer annealing time for effective thin layer formation is required, due to the reduced curvature and surface diffusion velocity.

It is also worthy to mention that, depending on the application, the bubbles appearance can be desired as well. A precise control on bubble distribution and size inside the thin layer is of great interest in multiple application such as micromechanical systems and optical devices.

III. 4. 2 Silicon voids formation evolution:

In the previous experiments, three types of pore profiles of different periodicity are evaluated targeting thin Si layer formation. Depending on the initial pore condition, the pore morphology evolution during the annealing, such as the pinch-off at the curvature transition section and the trapped voids evolution, can be deduced by observing the SEM images of the final structures and comparing all these 9 cases. However, the practical transformation of the pores-layer during the annealing is unknown. In order to learn about the pore and layer structure evolution during high temperature annealing, a square profile sample is cleaved and annealed respectively for different durations. Then, pore evolution at different stages can be observed by SEM images.

Firstly, a sample of square profile with periodicity of 16 μm is prepared. The duration of each process is set to be 35, 60 and 90 minutes and the temperature set-point is 1300 °C. It should be noticed that, although the temperature rises rapidly (about 10 minutes to reach the set-point temperature 1300 °C) and the pore evolution is considered slow in the heating process, the time

duration for each sample annealing includes the heating process after introducing the sample at the initial temperature 600 °C.

Consequently, a detailed silicon and voids evolution is revealed by SEM images in Fig. III. 11 where it can be clearly observed how the pore morphology develops. After 35 minutes of annealing, the adjacent silicon walls coalesce at the diameter transition parts, while a small bubble-shape void forms inside silicon layer at small diameter section and big peanut-shape void is produced outside silicon layers at big diameter section. Then, at the moment of 60 minutes, the silicon layer buried bubbles become elongated vertically while the peanut-shape voids are transformed to a special structure: a thin intermediate solid Si layer is formed in the middle sandwiched by spacing layers after voids coalesce at the top and bottom part of the original peanut. Actually, the peanut-shape void can be regarded as a sinusoidal-like substructure and follows the sinusoidal profile evolution since its formation at about 35 minutes. Finally, this sinusoidal substructure is transformed to a perfect very thin Si layer without any bubbles produced, as another proof that the sinusoidal is a promising profile candidate to achieve bubble-free very thin Si layer. After 90 minutes of annealing, the thin Si layer is successfully created with a bubble plane in the middle. Both this layer and the very thin one in the middle of spacing layer show smooth surfaces.

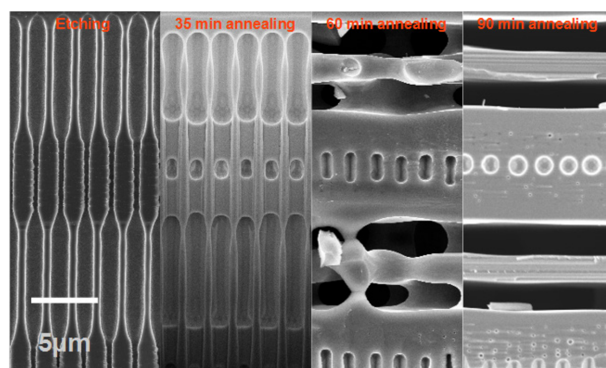

Fig. III. 11 Cross-sectional view SEM images of different samples with identical starting profile after different annealing times. Scale bar is 5 µm.

III. 5 Conclusions

In this chapter, based on the technological know-how of the *Millefeuille* process, the impact of both modulated profile and periodicity of silicon pores on the generated thin layer quality is

explored and discussed. In detail, the initial pore profiles consists of square, conical and sinusoidal pattern with periodicity of 8, 12, and 16 µm defined by precise silicon macropores etching control. It is proved that the sinusoidal profile is more promising in bubble-free silicon layer production than the others. The square profile tends to contain symmetrically distributed bubbles at the middle plane of solid layer, while asymmetrical ones are observed in conical profile. Furthermore, the solid-void transformation evolution during the high temperature annealing is studied by revealing the pore status at 35, 60 and 90 minutes, offering a deeper understanding of the silicon atomic surface diffusion.

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Chapter IV

P-type c-Si solar cells combining heterojunction emitters and laser doped base contacts

In this chapter, a novel structure of Interdigitated Back-Contacted (IBC) solar cells on p-type c-Si substrates is reported. It combines laser processed homojunction base contacts and silicon heterojunction (SHJ) emitters, leading to a hybrid structure. It is based on previous works of fully laser processed IBC solar cells. The alternative SHJ emitter is proposed replacing the laser processed one to boost the photovoltaic efficiency. This low temperature fabrication method also provides a new path for fabricating high efficient thin IBC c-Si solar cells.

IV. 1 Introduction

The application of laser technology for c-Si solar cell fabrication has drawn attention and been actively studied in the past decades. In particular, this technique is especially well-suited to silicon impurity doping since the laser doping process is realized locally in a quite short time leading to effective doping of the c-Si material and allowing a simplified silicon solar cell fabrication process.

Apart from the simplicity of impurity doping compared to conventional high temperature dopant diffusions, the point-like laser doping spot nature permits a whole silicon surface passivation except the laser doped contacts which only occupy a very small proportion. This property gives rise to the novel structure of c-Si solar cell design called DopLa (Doped by Laser). In this structure, all the highly-doped regions are created by laser processing dielectric films [1-4]. The n^+ regions are formed by processing a phosphorus-doped silicon carbide film stack (SiC_x(n)) while the p^+ regions are based on aluminum oxide/silicon carbide (Al_2O_3/SiC_x) film. Apart from working as dopant sources, these films provide c-Si surface passivation and anti-reflection properties. This technology has been applied to Interdigitated Back-Contacted solar cells leading to DopLa-IBC devices [1].

However, the relatively low performance of full-laser processed IBC device compared to that of conventional IBC processed through thermal doping is demonstrated experimentally, and the limitation factors are concluded to be V_{oc} and FF [1]. In reference [1], a conversion efficiency of 15.5 % is reported for DopLa-IBC solar cells with V_{oc} = 644 mV, J_{sc}= 37.2 mA/cm^2 and FF= 65.1 %. The main limitations for those devices were attributed to high recombination at the laser processed emitter regions and the distance between them. In order to avoid the weakness of the laser processed emitter while maintaining a full low temperature fabrication that could be compatible to thin c-Si substrates, silicon heterojunction (SHJ) is introduced as an alternative to create the emitter regions. This technology is based on the formation of selective contacts through the deposition of an intrinsic and doped amorphous silicon films and it has been previously applied to IBC solar cells with excellent results [5-7]. In fact, conversion efficiency record of c-Si solar

cell at 1 sun-illumination (26.7 %) is based on the combination of SHJ technology with an IBC structure [5].

In this work, p-type IBC solar cells are reported where the SHJ emitter is combined together with laser processing to create the base contacts. In particular, the emitter consists of thin intrinsic and phosphorus-doped amorphous silicon films (i/n a-Si:H) contacted by ITO, while for the base contacts, p^+ regions created by laser processed Al_2O_3/SiC_x films are defined. With this hybrid device, it is expected to overcome the V_{oc} and *FF* limitations observed for DopLa-IBC and explore the possible benefits of the combination of both low temperature technologies.

IV. 2 Device fabrication

The solar cell processing is based on a 280 µm-thick 2.5 Ω·cm FZ c-Si wafer with random pyramids textured front surface and polished rear surface. After a standard RCA cleaning, a 50 nm-thick Al_2O_3 film is symmetrically deposited on both surfaces by Atomic Layer Deposition technique, followed by a 10 minutes annealing at 400 ºC to activate the Si surface passivation. Then, the front Al_2O_3 film is capped by a 35 nm-thick SiC_x layer by PECVD in order to reduce optical reflection and protect the Al_2O_3 film from subsequent wet chemical steps. On the rear surface, a 50 nm-thick SiC_x layer is deposited in order to protect Al_2O_3 film and improve the laser process to create the p^+ regions [3]. After a photolithographic step on the rear surface, emitter windows are opened through SiC_x layer by CF_4/O_2 plasma etching realized in the PECVD setup. Next, the sample is treated by RCA1 cleaning and HF (1%) dip to remove the Al_2O_3 film at the emitter regions and expose the c-Si surface. Immediately after the cleaning, an intrinsic a-Si:H (~4 nm, SiH_4: 36 sccm; CH_4: 12 sccm) and phosphorus-doped a-Si:H (~15 nm, SiH_4: 36 sccm; PH_3: 4 sccm) film are deposited continuously onto the rear surface by PECVD at 300 ºC creating the silicon heterojunction at the opened emitter windows which is contacted by a 100 nm ITO layer deposited by RF sputtering (about 100 Ω/square sheet resistance, obtained by four terminal resistivity measurement). A second photolithographic step is used to remove ITO and i/n a-Si:H films by HF (2%) solution and HF/HNO_3 mixture solution respectively from the regions where the base contacts are to be defined. The schematic sample structures of each fabrication step are shown in the Fig. IV. 1.

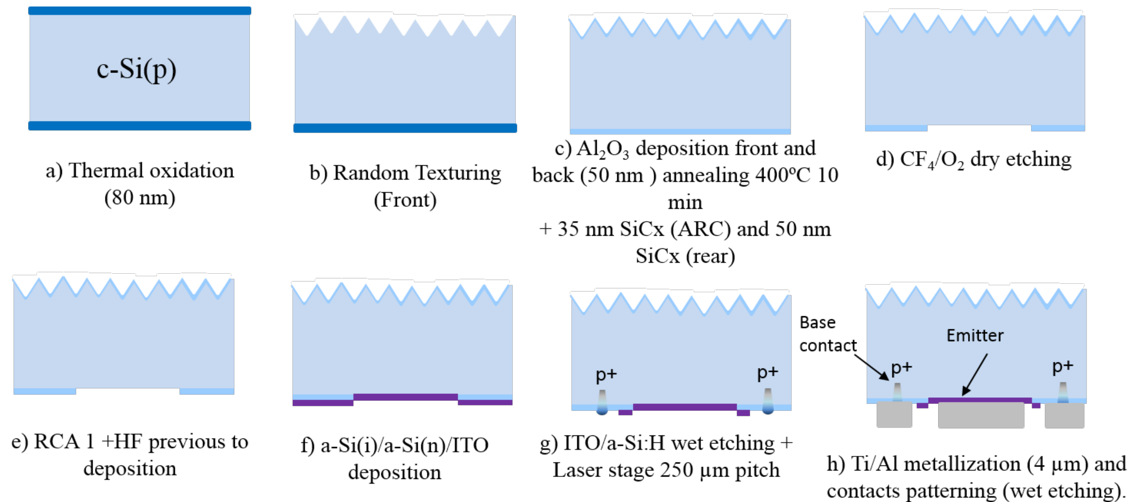

Fig. IV. 1 Schematic sample structures of each fabrication step

Now, p^+ highly-doped regions are created by laser processing Al_2O_3/SiC_x stacks with a Q-switched Nd:YAG laser (StarMark SMP 100II Rofin-Baasel) emitting at 1064 nm in TEM00 with a power of 1.07 W, which is the minimal power for effective laser doping in order to avoid any possible damage on adjacent heterojunction [1]. The distance between each laser spot is 250 µm as developed in previous work [1]. Finally, the sample is metallized just after the laser step by Ti(~20 nm)/Al(~4µm) stack deposited by RF sputtering. In order to separate emitter and base contacts, a 50 µm gap of metal is defined by photolithography and subsequent Al etching with orthophosphoric acid/isopropanol mixture solution at 65 ºC followed by Ti etching with 1% HF solution. It is found that the last Ti/Al metal etching step is the more critical one since several problems could arise:

1 Over etching of metal and the undesired etching of ITO: in this case the amorphous silicon emitter would be not contacted and exposed into air jeopardizing the solar cell performance.

2 Metal residue at some site of the gap between p and n-type fingers short-circuiting the solar cell. If this happens, an additional etching could be done.

3 Peeling-off of the ITO/metal emitter contact layer.

In order to conquer this problem, one should be observing during all the etching process and decide the moment to take the sample out. Taking out the sample occasionally and cleaning with

DI water during the etching process can help to improve the etching quality and avoid the metal and ITO over etching.

A detailed fabrication process of these hybrid devices on p-type substrate are summarized in Table IV. 1, while the resulting device structure is sketched in Fig. IV. 2(a) and a microscope picture of the finger structure on rear surface is shown in Fig. IV. 2(b).

Table IV. 1 Fabrication process of hybrid devices on p-type substrate.

Standard RCA cleaning
50 nm Al_2O_3 ALD deposition
SiC_x PECVD deposition on front surface (35 nm ARC coating) and rear surface (50 nm)
Emitter windows lithography and plasma etching
RCA1 and HF (1%) dip
Intrinsic and n-type a-Si:H PECVD deposition
ITO sputtering deposition
Base region lithography and ITO/a-Si:H wet etching
Base laser doping process
Sputtering 20 nm Ti and 4 µm Al deposition
Interdigitated contact definition

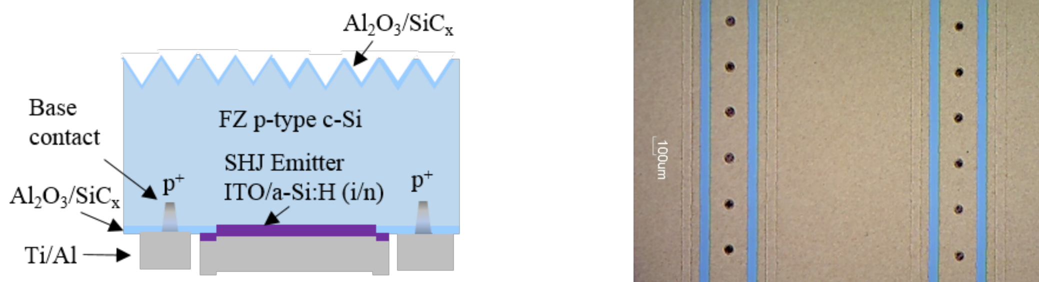

Fig. IV. 2 (a) Cell structure of the fabricated p-type hybrid devices; **(b)** Microscope picture of the finger structure with 250 µm pitch

IV. 3 Results and discussion

IV. 3. 1 Surface passivation measurement

As it can be seen in the fabrication process shown in Table IV. 1, a crucial point of the combination of SHJ and laser doping technology is the passivation quality of the a-Si:H films after the etching the Al_2O_3 film previously deposited onto c-Si surface. To check out this passivation, test samples are fabricated reproducing the conditions that would be found in the final devices. In Fig. IV. 3, the lifetime measurements of a sample is shown, which is symmetrically covered with 50 nm of Al_2O_3 deposited by ALD and 50 nm of stoichiometric SiC_x film deposited by PECVD. As it can be seen, lifetime is very close to the intrinsic lifetime (where only Auger and radiative recombination is considered [8]) indicating an excellent surface passivation quality. Then, SiC_x film is etched by plasma etching based on CF_4/O_2 mixture on one side leaving the Al_2O_3 film still fully covering the c-Si surface. Surprisingly, lifetime dramatically decreases below 10 μs indicating a poor surface passivation at the Al_2O_3/c-Si interface that has been exposed to the plasma. In the final solar cells, the highly recombining interface is only located at places where the Al_2O_3 will be chemically etched during the RCA1 cleaning prior to a-Si:H deposition. In the test sample, we performed the cleaning steps and the a-Si:H+ITO deposition. As it can be seen in Fig. IV. 3, lifetime is recovered to the initial passivation levels. This result indicates that the poor passivation is related to a modification of Al_2O_3/c-Si interface properties.

In order to get a deeper knowledge of the impact of CF_4/O_2 plasma etching on passivation of Al_2O_3, a Metal Insulator Semiconductor (MIS) capacitors consisting of Al/Al_2O_3/c-Si is prepared. For this experiment we used two types of samples. On the one hand, the deposition of 50 nm thick Al_2O_3 film onto c-Si surface and a 400 ºC annealing for 10 minutes was carried out to increase the negative fixed charge density [9]. On the other hand, an Al_2O_3 (50 nm)/SiC_x (50 nm) stack is deposited then SiC_x was subsequently etched by CF_4/O_2 plasma etching. As a result, a similar 50 nm-thick Al_2O_3 film than in the previous case is left onto c-Si surface. A uniform aluminum layer is deposited onto rear surface of both samples by e-beam method followed by a full-area intensive

point-laser firing forming ohmic contacts. Round-shape Aluminum dots with a nominal diameter of 2 mm are thermally evaporated onto the front surface using a shadow mask.

The measured high frequency (1 MHz) Capacitance-Voltage (C-V) curves for both samples are shown in Fig. IV. 4 where the measured capacitance is normalized by the maximum capacitance measured under accumulation conditions. As it can be seen, the C-V curve is shifted to negative values after CF_4/O_2 plasma etching indicating the appearance of positive fixed charge (Q_f). Using conventional MIS theory [10], we could quantify Q_f for both samples from the shift of the flat band voltage and using a difference between metal and semiconductor workfunction of -0.628 eV. For the case without plasma etching, we obtain $Q_f = -1.9\times10^{12}$ cm^{-2} while after CF_4/O_2 plasma etching Q_f is positive and equal to 2.0×10^{12} cm^{-2}. This big difference indicates a strong impact of plasma etching on Al_2O_3 film configuration. Notice that the determined Q_f value is an equivalent charge located at the dielectric/c-Si interface, but the real charge distribution is not known. Probably, the positive charge is related to the first nanometers of the film that have been exposed to the plasma modifying surface configuration from accumulation to high inversion.

Additionally, we applied the method proposed by Terman [11] to calculate the interface state density (D_{it}) from the high-frequency C-V curve. In this method, D_{it} is obtained from the stretching out of the C-V curve along the voltage axis. It is more precise when surface is under depletion or low inversion conditions and capacitance is not constant. As a consequence, D_{it} is determined in an energy range around midgap which is the region of more interest from the recombination point of view. The obtained D_{it} values are plotted in the inset of Fig. IV. 4 where we can see that this parameter increases in all the explored energy range and more significantly close to the valence band when CF_4/O_2 plasma is applied. A quantitative justification of the dramatic lifetime decreases after plasma etching by the measured interface parameters is beyond the scope of this work. However, we can conclude that C-V measurements reveal a strong impact of CF_4/O_2 plasma on Al_2O_3/c-Si interface.

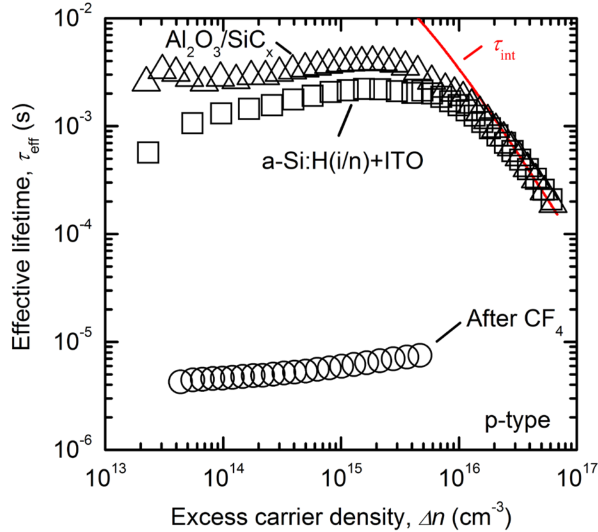

Fig. IV. 3 Lifetime measurements p-type hybrid device

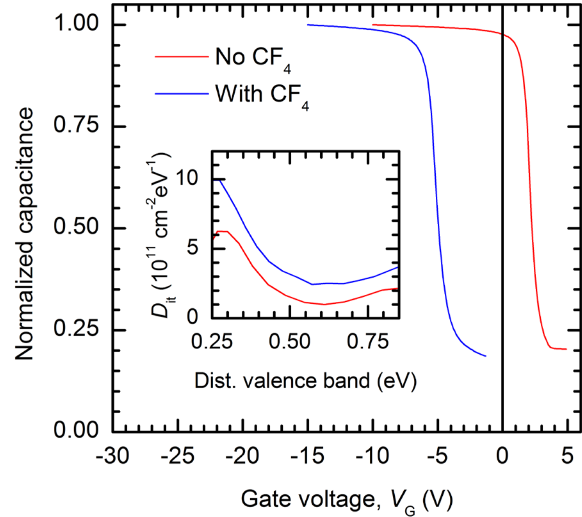

Fig. IV. 4 Normalized capacitance voltage measures acquired at 1 MHz

IV. 3. 2 Contact resistance on ITO

In previous experiments, p^+ laser doped regions were successfully contacted by Aluminum [4] and Titanium [1] while in the heterojunction solar cells developed in our group ITO is typically contacted by Silver [12]. Since Silver is not a good option for p^+ doped c-Si, the contact quality of Aluminum and Titanium on ITO is evaluated using the Transfer Line Method (TLM) [13]. In this method, metal contacts with different spacing between them are defined and the resistance between them is measured. Then, the total resistance (R_T) follows a linear trend depending on the distance between contacts (L) as follows (IV. 1):

$$R_T = \frac{R_S}{W_c} \times (L + 2L_T) \qquad \text{(IV. 1)}$$

where W_C is the width of the contact and L_T is the transfer length indicating the average distance that a carrier travels in the silicon beneath the contact before it flows up into the contact. Consequently, the effective contact area can be regarded as $L_T \times W_C$. Finally, the specific contact resistance (R_C) is calculated as two times the y-axis intercept applying a corrected contact area following equation (IV. 2):

$$\rho_c = R_C \times L_T \times W_c \tag{IV.2}$$

Al and Ti are deposited by sputtering onto samples covered by same ITO through shadow mask that defines a series of rectangular-shape metal contacts with distinct spacing. In Fig. IV. 5, the I-V curves of ITO/Al and ITO/Ti contacts with the same spacing for ±1 V is shown. It can be seen that Aluminum is creating a poorer contact on ITO even showing a rectifying trend for high voltages. On the contrary, ITO/Ti is perfectly linear with lower resistance. Based on these results, the TLM measurements only for the ITO/Ti contact is performed. The explored voltage range is reduced to ±0.1 V in order to get a linear relation between current and voltage and R_T was measured from the inverse of the slope at V= 0.1 V for every contact spacing. The obtained values are shown in Fig. IV. 6 with the best linear fit. Applying equation (1) and (2), it can be deduced that specific contact resistance is about 1.1 mΩ·cm^2 for ITO/Ti. Given that emitter fractions in the range of 49-71 % are defined in the solar cells (see Table IV. 2), this value is low enough to introduce a negligible impact on *FF*. Consequently, Ti is used as metal contact in the final devices.

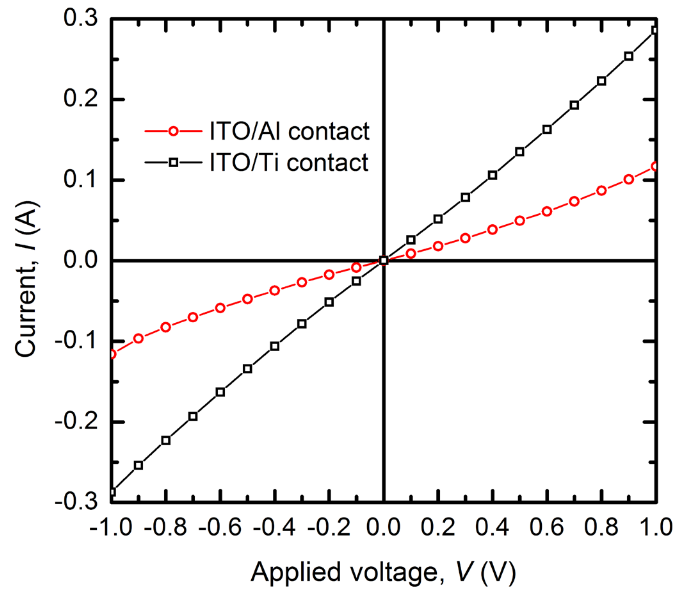

Fig. IV. 5 Measured current of ITO/Al contact and ITO/Ti contact

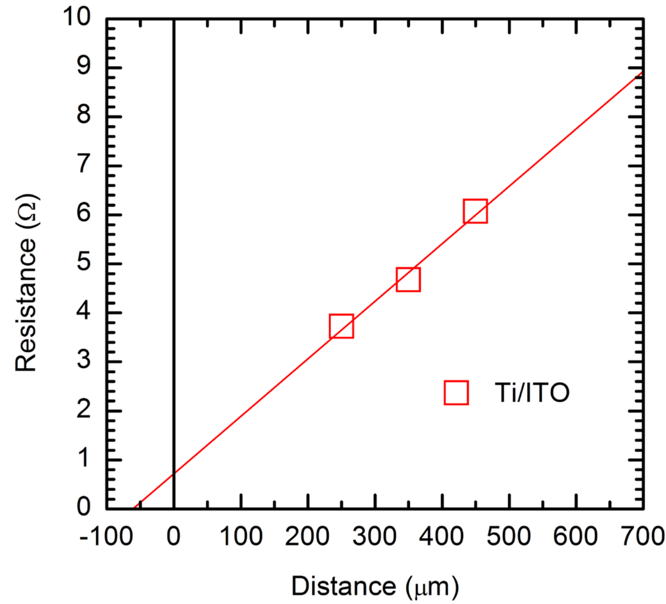

Fig. IV. 6 Total resistance as a function of contact spacing

IV. 3. 3 Solar cells results

Following the fabrication process explained above, six 3x3 cm^2 solar cells in two 4" wafers are finished. The photovoltaic parameters as a function of the emitter contact fraction (f_e) are shown in Table IV. 2. As it can be seen, except for one cell, the rest have a conversion efficiency in the 18-19 % range with a champion cell of 19.0 % with V_{oc} = 677 mV, J_{sc} = 40.7 mA/cm^2 and FF = 68.8 %. Focusing on J_{sc}, the obtained values are higher than the ones reported in reference [1] for fully laser-processed cells. The measured External Quantum Efficiency (*EQE*) curve of the champion cell is shown in Fig. IV. 7 together with the one reported in reference [1] for a direct comparison. The increase in J_{sc} corresponds to higher *EQE* values for $\lambda < 1000$ nm. This constant increase is attributed to a better front surface passivation. On the other hand, V_{oc} values have significantly increased from the 620-644 mV reported in reference [1] to 665-684 mV, demonstrating a lower recombination in the SHJ emitter compared to the laser-doped one. Finally, despite *FF* values are better than the ones related to fully laser doped cells (57-65 %), this parameter is clearly limiting cell efficiency.

Table IV. 2 Photovoltaic figures of 3x3 cm^2 p-type hybrid cells with ITO of ~80 Ω/square

f_e (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF*(*pFF*) (%)	η (%)
71%(wafer1, cell4)	39.6	666	58.3(77.1)	15.4
71%(wafer2)	41.2	674	65.0(77.2)	18.0
60%(wafer1, cell1)	39.8	665	71.0(82.1)	18.8
60%(wafer2)	40.7	677	68.8(81.0)	19.0
49%(wafer1, cell2)	40.5	684	65.7(81.8)	18.2
49%(wafer2)	40.9	671	69.1(80.7)	19.0

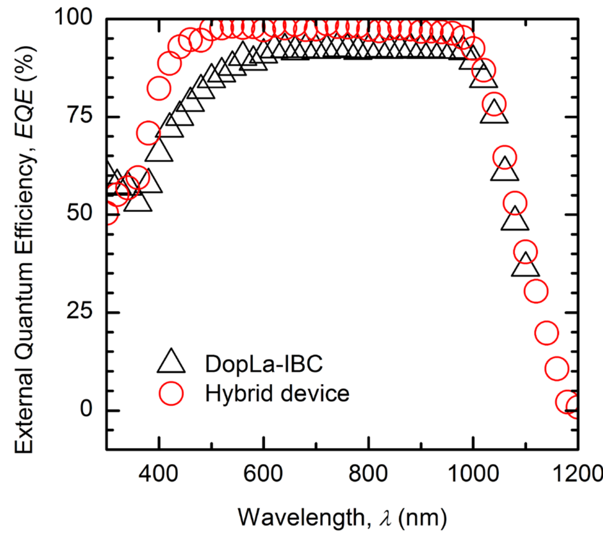

Fig. IV. 7 EQE measurements of fabricated devices.

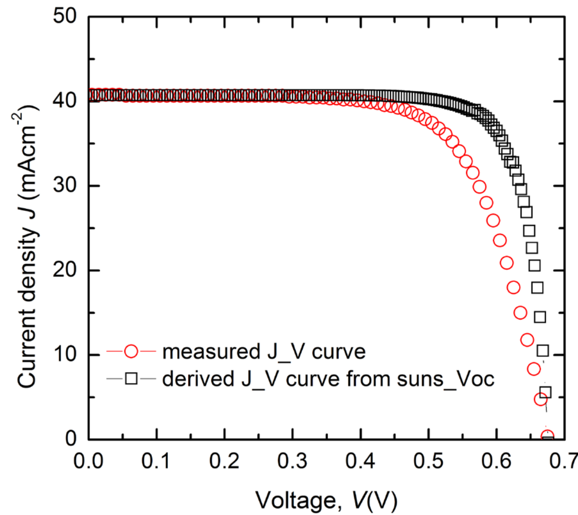

Fig. IV. 8 J-V curve (cell1) of the solar cell with best efficiency.

In order to get a deeper insight of the origin of the low *FF*, Suns-V_{oc} curves is measured and the corresponding pseudo-*FF* (*pFF*) is calculated, where ohmic losses have no impact [14], as shown in Fig. IV. 8. Apart from cells with f_e= 71 % that show *pFF* of about 77 % limiting the *FF* to even lower values, the rest of the cells have a *pFF* well beyond 80 % indicating a good junction formation with low shunting. Thus, a transport problem must be behind the low *FF* values. A possible candidate is the distance between base contacts. However, *FF* as high as 74 % have been reported in reference [15] where we applied identical geometry to the base contacts. Thus, the origin of the low *FF* in these hybrid solar cells should be related to the amorphous silicon emitter.

In the previous section, we determined a low contact resistance of ITO/Ti contact that in any case could significantly contribute to the series resistance of the device. Therefore, the most probable origin of the low *FF* is the low conductivity of the phosphorus-doped a-Si:H film. Our group developed this film contacted by ITO to be located at the front surface where the light impinges the cell [12, 16]. There, the conductivity of amorphous silicon layer is enhanced due to photogenerated carriers allowing an efficient transport of majority carriers. However, in the case of back contact heterojunction, photogeneration is negligible and the low conductivity cannot be compensated. Moreover, a small reduction in the slope in *J-V* curves close to V_{oc} is also observed in some of our hybrid cells resembling an “S” shape. This type of *J-V* curve distortion is reported for low doped a-Si:H layers in rear emitter configuration cells [17].

IV. 4 Improvement of SHJ emitter

As mentioned in the previous part, the SHJ in this case is located at the rear side and due to the negligible photogeneration of a-Si layers, a higher material conductivity is required. To fulfill this requirement, a collaboration with INES (Institute Nationale Energie Solaire, Chambery, France) is carried out. This institute has been working in SHJ for the last years with excellent results (see for example reference [18]).

Several sample wafers were fabricated and sent to INES after the definition of SHJ emitter area. At that laboratory, a complete RCA cleaning was carried out followed by the a-Si:H(i/n) layer deposition onto the full rear surface and the sputtering of the ITO layer. The sheet resistance

of the ITO layer is measured with a four-probe setup resulting in 30-40 Ω/square which is much smaller than that the one used at UPC.

After receiving the samples back, a photolithography is carried out to define the SHJ emitter regions. Then the exposed SHJ layers above the base regions are removed by wet chemical etching. ITO layer is etched by 4% HF for about 15 minutes to totally remove it followed by a soft-baking step to maintain the photoresist protection. Then, the amorphous silicon layer is etched by a mixed etchant solution consisting of 200ml deionized wafer, 8 ml 50% HF and 200ml HNO_3 for 15 seconds. Due to the different properties of the ITO layer, the duration of etching is evidently longer than that of UPC-made, thus a severe over-etching problem is occurred due to the difficulty in controlling lateral etching rate which is revealed by microscope picture in the Fig. IV. 9. For each individual finger of the solar cell more than 50 µm of over-etching on each edge is observed. This ITO over-etching exposed the amorphous silicon layers that could be also etched in the subsequent wet-etching step. As a result, part of the rear passivation could be lost negatively impacting the solar cell performance.

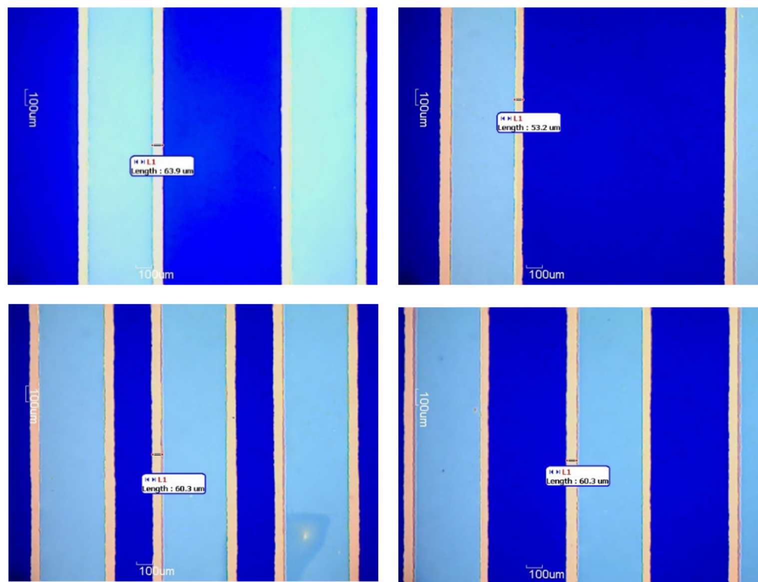

Fig. IV. 9 Microscope pictures of the ITO over-etching

Finally, laser doping and metallization steps are carried out with the same conditions mentioned before. In Table IV. 3, the photovoltaic parameters of the fabricated solar cells are

shown. As it can be seen, results are highly scattered probably due to the ITO over-etching problem. Despite this technological issue, solar cell with f_e= 60 % shows higher efficiency than the best one reported with the SHJ technology developed at UPC (see Table IV. 2) demonstrating the technology. The improvement is based on a higher *FF* value, as expected from the introduction of the more mature SHJ technology of INES.

Table IV. 3 Photovoltaic figures of 3x3 cm^2 p-type hybrid cells with ITO of ~35 Ω/square

f_e (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF*(*pFF*) (%)	η (%)
71%(wafer3, cell4)	39.55	667	71.4(79.2)	18.8
60%(wafer3, cell1)	39.50	674	72.7(79.6)	19.4
49%(wafer3, cell2)	40.05	679	69.6(81.7)	18.9
80%(wafer3, cell3, no counterpart for comparison)	37.60	660	74.0(79.9)	18.4

As a conclusion, the replacement of SHJ layers with higher conductivity indeed led to better device performance, and the assumption previously proposed, where the low FF was related to the heterojunction emitter, is confirmed. Thus, a further efficiency enhancement is expected if the SHJ layers are correctly processed, i.e., a correct control of layers etching.

IV. 5 Conclusions

In this work, the hybrid p-type solar cells are reported where the emitter is based on SHJ technology while the base contacts are created by laser processing Al_2O_3/SiC_x films. Special attention of the compatibility of both technologies has been paid in the proposed fabrication process. Firstly, the re-passivation of silicon heterojunction emitter region is evaluated and confirmed by depositing on the silicon surface after removing the aluminum oxide and silicon carbide layer stack needed for base laser doping process. Based on the high-frequency capacitance-voltage characterization, an increased Aluminum oxide/silicon interface state density and a strong impact on the fixed charge density is concluded after the CF_4 etching of silicon carbide layer. Secondly, the contact quality of Titanium and Aluminum on ITO is evaluated due to the different metal contacts property between the ITO of heterojunction stack and the homojunction p^+/p laser processed region. It is revealed that titanium is a better option with a specific contact resistance of

1.1 mΩ·cm^2. Finally, a finished hybrid IBC solar cells with conversion efficiencies in the 18-19% range are reported. Next, following the same fabrication process, the impact of heterojunction layer stack on device efficiency is explored. A nearly 1% efficiency increase is obtained by using a heterojunction layer stack with better conductivity positively impacting on better fill factor.

The viability of this novel structure is demonstrated and a significant efficiency improvement has been reported compared to fully laser processed DopLa-IBC. This work provides a new approach for achieving low-temperature high efficiency c-Si solar cells that could be compatible with IBC device based on thin c-Si substrate.

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Chapter V

3D Simulations of Interdigitated Back-Contacted Crystalline Silicon Solar Cells on Thin Substrates

This chapter explores the efficiency potential of IBC c-Si solar cells applied to thin c-Si substrates through 3D device simulations. In the first part of the chapter, we explore the impact of substrate thickness and front surface recombination velocity on cell performance with special attention to the different behavior in carrier collection of two different rear-surface doping structures: a conventional structure with fully-doped base and emitter regions, and a locally-doped structure with point-like doped regions beneath metal contacts. In the second part, the rear contact geometry for point-like doped thin IBC device is numerically explored for guiding the rear surface structure design and predicting the device performance.

V. 1 Fully-doped *vs.* locally-doped structure

V. 1. 1 Brief introduction on the simulated thin IBC c-Si solar cell structures

From the published results as presented in chapter II, it can be concluded that an effective light absorption is a strong requirement for achieving efficient thin c-Si solar cell, which normally brings a difficulty of surface passivation. As it was also mentioned, IBC structure can help in overcoming these problems.

In the last years, our research group has developed high efficiency IBC c-Si solar cells with excellent results [1, 2]. These devices are based on conventional technologies, namely photolithography, thermal diffusions and silicon oxide passivation, applied to thick (~300 µm) high quality substrates. These solar cells show stripe-like doped emitter and base regions fully contacted. We will call this structure as "fully-doped". Apart from these devices, IBC solar cells based on local point contacts defined through laser technology have been also successfully developed [3]. In this case, no stripe-like doped regions are used and all the n^+ and p^+ regions are created by locally laser processing the passivating layer that is also used as dopant source. These structures are labeled as "locally-doped". As a result, a simplified and fully low temperature IBC cell process is proposed demonstrating efficiencies in the 20 % range [3].

This chapter explores the efficiency potential of IBC c-Si solar cells applied to thin c-Si substrates with special attention to the different behavior in carrier collection of both fully-doped and locally-doped structures. First of all, an optical model is proposed using 2D ray tracing method for reducing the complexity of optical-electrical simulation tasks. Then a 3D numerical model is developed using commercial TCAD software (Silvaco-ATLAS, Silvaco Inc., Santa Clara, CA, USA) that reproduces the main features of our p-type IBC c-Si solar cell technology [1]. The optical-electrical model for final device simulation is validated by comparing simulation results to a fabricated device on 280 µm-thick substrates with stripe-like p^+ and n^+ diffusions. We focus our simulations on the effect of reduced substrate thickness combined with the front surface recombination velocity (S_{front}) which plays a major role in carrier collection and it is critical in thin

devices, as mentioned earlier. Finally, locally-doped structures are analyzed in order to underline the pros and cons of both device architectures when dealing with thin substrates.

V. 1. 2 Simulation parameter definition and validation

The rear contact structure to be used in simulation mimics one from a 2.5×2.5 cm p-type IBC c-Si prototype solar cell, whose main features are stripe-like n^+ and p^+ diffusions with square-like n^{++} region under the emitter contacts, as shown in Fig. V. 1 (a) and Fig. V. 1 (b). As it can be observed, the unit cell is 200 µm long and 100 µm wide while thickness is set as a variable ranging from 280 to 10 µm. It includes both contacts, an anode and a cathode, allowing to extract voltage and current. The calculated current value is then scaled up in order to obtain the total current density of the cell. By doing so, we assume that the simulation unit cell is repeated along the full cell area and we exclude any perimeter effect.

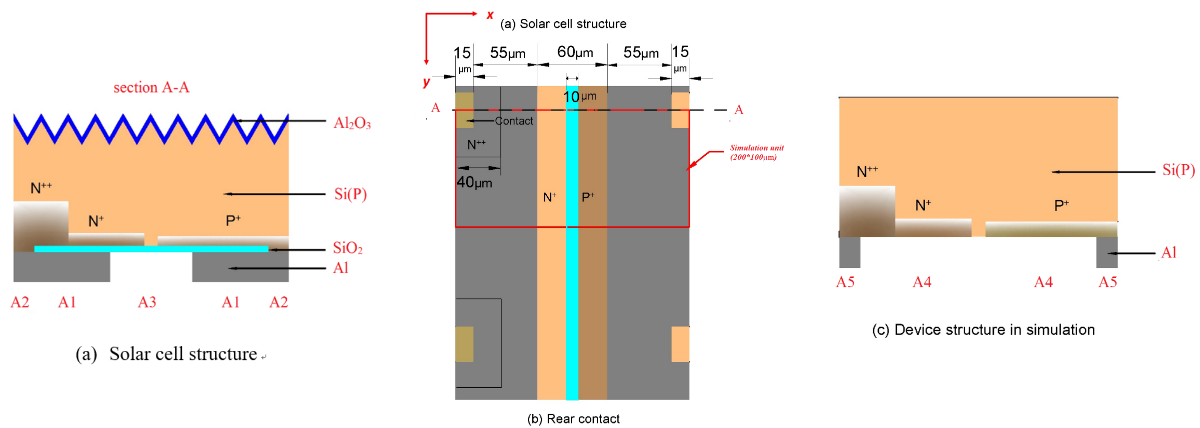

Fig. V. 1 Schematic figure of solar cell structure: (a) Schematic figure of practical solar cell structure: A1-67.75% area [Al_2O_3-90nm/Si-textured/SiO_2-100nm/Al]; A2-2.25% area [Al_2O_3-90nm/Si-textured/Al]; A3-30% area [Al_2O_3-90nm/Si-textured/SiO_2-100nm]. (b) Unit region for simulation. (c) Schematic figure of device structure in ATLAS simulation: A4-97.75% area [Air/Si-flat/Air]; A5-2.25% area [Air/Si-flat/Al].

The calculation of optical absorption in Silvaco ATLAS is time-consuming and complex, since this software is more oriented to reproduce electron device physics. In order to simplify the simulations, we perform the calculation of the light absorption using the wafer ray tracer provided by PV lighthouse, which is much more optimized for this task.

Once we have checked out the validity of the wafer ray tracer, the obtained absorption information is transferred to Silvaco ATLAS applying the following procedure. Firstly, we calculate the light absorption with the ray tracer software using a c-Si substrate whose front surface consists of front pyramids 3.536 µm high, 5 µm wide and with an angle of 54.78 º. These parameters are provided as default values and they represent the random texturing technology of our cells. In the simulations and for the sake of clarity, this front surface random pyramids texturing is considered in all IBC cells regardless the substrate thickness. Although this technology could not be feasible when very thin substrates are used, this approach allows us to compare the results underlining the effect of the front surface passivation.

At the rear surface, we define a flat surface with three possible configurations: c-Si/SiO_2/Al, c-Si/Al, and c-Si/SiO_2/air corresponding to regions A1, A2 and A3 in Fig. V. 1 (a) respectively. The different rear configurations lead to variations in the rear internal reflectance impacting photon absorption for very thin substrates. For every wavelength, the absorption for each rear surface configuration is simulated. Finally, the total absorption ($A_{raytracer}$ (λ)) is calculated by weighting the absorption of every region by its area coverage (see Fig. V. 1 caption where these data are shown).

On the other hand, we carry out similar calculations but in the simplified structure introduced into Silvaco ATLAS (see Fig. V. 1(c)). In this case, flat bare c-Si surfaces are considered with Aluminum pads at the rear contacts resulting in two different configurations A4 and A5 (see Fig. V. 1 caption for the area coverage of every region). Then, we can calculate the total absorption of ATLAS (A_{ATLAS} (λ)) applying the same procedure explained above to the simplified structure: simulated absorption for the two rear configurations weighted by their area coverage. Finally, the spectrum introduced to ATLAS (S_{ATLAS}(λ)) for the solar cell simulation is modified from AM1.5G combining the absorption of both softwares using equation (V. 1). By doing so, simplified simulations in Silvaco ATLAS reproduce the optical absorptance that has been accurately simulated by the ray tracer software.

$$S_{ATLAS} = S_{AM1.5}(\lambda)\frac{A_{raytracer}(\lambda)}{A_{ATLAS}(\lambda)} \qquad (V.1)$$

Regarding the electrical modeling, a detailed description of the parameters used in the simulated structure is included in the Table V. 1. The most important features of the structure, like doping profiles, surface recombination velocities at the doped surfaces and geometrical dimensions, have been obtained from experimental characterization performed during the device development in our research group. From the final device characterization, we were able to determine three important parameters namely the front surface recombination (S_{front}= 100 cm/s), the surface recombination at the gap between doped regions (S_{gap}= 80 cm/s) and the series resistance due to the metal grid (0.7 Ω·cm^2).

Table V.1 Simulation parameters

Carrier statistics	Fermi-Dirac, complete ionization of impurities
Bandgap narrowing	Slotboom and de Graaf model [4]
Carrier mobility	The Analytic Low Field Mobility Model (Concentration and temperature dependent Caughey-Thomas model [5])
Bulk Recombination	
Shockley-Read-Hall (bulk)	Shockley-Read-Hall (SRH) Recombination model. τ_{n0}=0.5 s τ_{p0}=0.5 s , E_t= E_i
Auger	Injection-dependent Auger coefficients
Radiative	C = 4.7×10^{-15} cm^{3}s^{-1}
Surface recombination	
Passivated front surface Passivated rear surface	Recombination velocity (S_n=S_p) varies from 1 to 5×10^6 cm/s Recombination velocity (S_n=S_p) of thermal SiO_2 passivated rear surface at each region is determined by fabricated 280 µm cell as discussed in the text. SRV_{N+}=SRV_{P+}=16000 cm/s, SRV_{N++}=56000 cm/s, SRV_{SiO2}=80 cm/s.
Doping parameters	
Bulk acceptor density, N_A	5.71×10^{15} cm^{-3}
n^{++} region	Gaussian distribution of Donor, Characteristic length=characteristic length of lateral profile=0.84 Concentration=6.1×10^{19}
n$^+$ region	Gaussian distribution of Donor, Characteristic length=characteristic length of lateral profile=0.5483 Concentration=9×10^{18}

p^+ regions	Gaussian distribution of acceptor, Characteristic length=characteristic length of lateral profile=2.094 Concentration=2×10^{18}
Contact parameters	
Anode and cathode contact for thermal/laser doping	Material=aluminum (ohmic contact) Finite surface recombination velocities=5×10^6 cm/s
Lumped series resistance	0.7 Ω·cm^2
Optical parameters	
Incident light spectrum	Spectrally enhanced AM 1.5G
Front reflectivity	Front reflections determined by 2D ray tracer and 3D Luminous
Back reflectivity	number of reflections traced=2

The measured PV figures and the simulated ones are presented in Table V. 2, and also depicted in Fig. V. 3 by star symbol. Fig. V. 2 shows the measured and simulated External Quantum Efficiency (*EQE*) data. As it can be seen, a reasonable agreement is found demonstrating the accuracy of the model.

Table V. 2 Experimental and Simulated PV Figures of the Fabricated Solar Cell

	J_{sc} (mA/cm2)	V_{oc} (mV)	*FF* (%)	η (%)
Experimental	37.7	638	79.4	19.1
Simulated	37.5	641	79.4	19.1

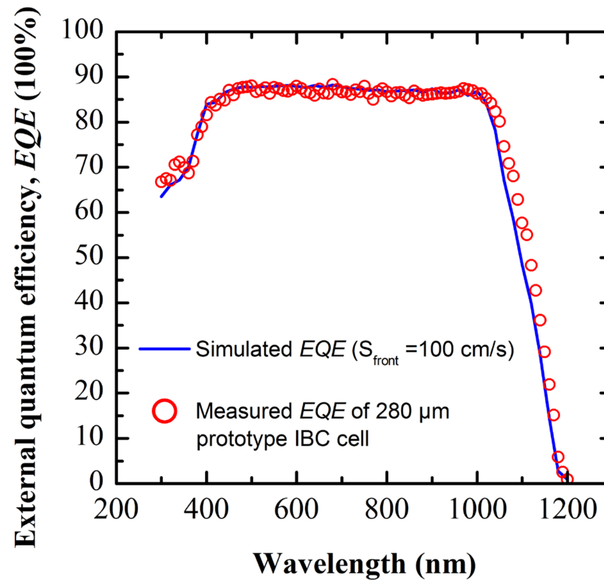

Fig. V. 2 EQE comparison between simulation results and measurement of the fabricated 280 µm-thick c-Si IBC

It should be mentioned that surface recombination is modeled by transferring surface recombination velocity to carrier lifetime in a 10 nm thick region beneath every surface region following the procedure reported in [6].

V. 1. 3 Simulation results of solar cells

(a) Fully-doped structure

In Fig. V. 3, we plot the simulated photovoltaic characteristics with substrate thickness ranging from 10 to 280 µm and S_{front} from 1 to 5×10^{6} cm/s. Regarding the short-circuit current (J_{sc}), front surface passivation strongly impacts it, as expected. For well passivated front surfaces, S_{front}= 1 cm/s, J_{sc} reduces with substrate thickness mainly due to the lower light absorption resulting in 30.7 mA/cm^{2} for 10 µm compared to 40.7 mA/cm^{2} for 280 µm. On the other hand, for highly recombining front surfaces thinner substrates performs better, since carriers are photogenerated closer to the junction and they are more efficiently collected leading to 6.4 mA/cm^{2} and 3.4 mA/cm^{2} for 10 and 280 µm, respectively.

Focusing on V_{oc}, a weak dependence of this parameter with substrate thickness is observed resulting in similar values for all substrates except for very high S_{front} values, where lower values are obtained for thinner substrates. This result indicates that, given a reasonable level of front surface passivation, no degradation of V_{oc} is expected when c-Si substrates thickness is reduced. This weak dependence of V_{oc} on substrate thickness is unexpected considering the significant photocurrent drop when substrate thickness is slimmed down from 280 to 10 µm. For example, one would expect that the mentioned change in J_{sc} for S_{front}= 1 cm/s would result in a V_{oc} reduction of about 8 mV assuming a constant reverse saturation current density. Notice that due to the high quality of the substrate and surface passivation, the main recombination zones are located at the doped regions which are not modified by the reduced thickness. This controversy demands a deeper explanation that will be presented in the discussion section of this chapter.

Fill Factor (FF) shows a complex dependence on the front surface passivation. For low S_{front} values, FF is limited due to the relatively high lumped resistance value 0.7 Ω·cm^{2} related to the

metal grid combined with high J_{sc} values. Notice that in this range, higher *FF* values are obtained for thinner substrates due to lower J_{sc} values. For $S_{front} \geq 10^3$ cm/s, J_{sc} decreases revealing the impact of substrate thickness on *FF*. Now *FF* is limited by the maximum obtainable value due to V_{oc} [7]. As it can be seen, thicker substrates lead to higher V_{oc} and thus, higher *FF* values. Interestingly, *FF* higher than 75 % are obtained even for substrates as thin as 10 µm indicating that the *FF* loss is not the limiting effect when thin c-Si substrates are used.

Finally, conversion efficiency (η) is dominated by the trend observed for J_{sc}. It shows that remarkable efficiencies of 16-17 % for substrates in the 10-15 µm range are reachable without changing the rear surface technology. Interestingly, front surface passivation requirements are relaxed for such thinner cells with constant efficiencies up to $S_{front} \approx 100$ cm/s whereas significant drop in efficiency is observed for thick substrates.

(b) Locally-doped structure

The fully-doped architecture presented in the previous subsection demonstrates excellent performance potential, but relying on complex fabrication procedures including several high-temperature diffusion doping steps. Additionally, these processes are not easily transferred to thin c-Si substrates. One alternative to avoid them is the formation of highly-doped regions by laser processing dielectric films [3]. The main feature of such structures is that n^+ and p^+ regions are locally created under the contacts without any further doped region.

In this part, we are interested in exploring the effect of such architecture applied to thin c-Si substrates while, detailed modeling of laser doped regions will be addressed in future works. Thus, in order to get results that could be directly compared to the ones obtained in the previous section, the fully-doped structure is modified as follows. Regarding doping parameters, the emitter shallow doped n^+ region is cancelled and the dimensions of p^+ and heavily doped n^{++} regions are reduced to square point-like regions located just beneath the 30×30 µm metal contacts with the same doping profiles. In other words, we just keep the doped regions under the contacts with the same doping distribution. Additionally, distance between contacts is also maintained to 200 µm. This distance is in the range of optimized laser point-doping gap considering the trade-off between series resistance and surface recombination [3]. Recombination velocity at rear surface between doped

regions is also kept to 80 cm/s. Finally, since the layer structure of the solar cell is not changed, the optical approach previously applied is still valid.

In Fig. V. 4, the predicted performance of such a locally-doped IBC solar cell is plotted. Comparing the J_{sc} trend to that of fully-doped structure, we can observe a significant J_{sc} decrease for all thicknesses and well passivated front surfaces. In addition, J_{sc} is less tolerant to the increasing S_{front} until becoming scarce for $S_{front} \geq 10^4$ cm/s. As a result, thinner substrates are not favorable anymore for poor front passivated surfaces. A deep analysis of these differences is presented in the discussion section.

Regarding V_{oc}, it shows a similar trend as the fully-doped counterpart, but with higher values of about 680 mV for low S_{front} values. This higher value can be explained by the fact that doped regions at the rear surface are replaced by a passivated surface leading to lower recombination. Again, we find a weak dependence of V_{oc} on thickness which is a surprising result given the big change in J_{sc} for S_{front}= 1 cm/s. This effect will be also explained in detail in the discussion section.

Comparing *FF* values between both structures, it shows a similar trend with values dominated by the series resistance value for high J_{sc} or $S_{front} < 10^3$ cm/s. Once J_{sc} values decrease, *FF* trend is correlated to the different V_{oc} values for every device thickness in a similar way than for the previous structure but with lower *FF* values. The general decrease in *FF* is related to the inherent increment of ohmic losses of the locally-doped structure. Again reasonable values higher than 75 % are predicted for all substrates.

Finally, conversion efficiency follows the J_{sc} tendency for all substrates as in the previous case, with best values lower than for fully-doped structure. Then, we can conclude that the increase in V_{oc} is not able to compensate the stronger decrease in J_{sc}. Furthermore, locally-doped structure is more sensitive to the front passivation and, as consequence, the demand of a very low S_{front} is even more crucial. This is an important conclusion whose origin is addressed in the following section.

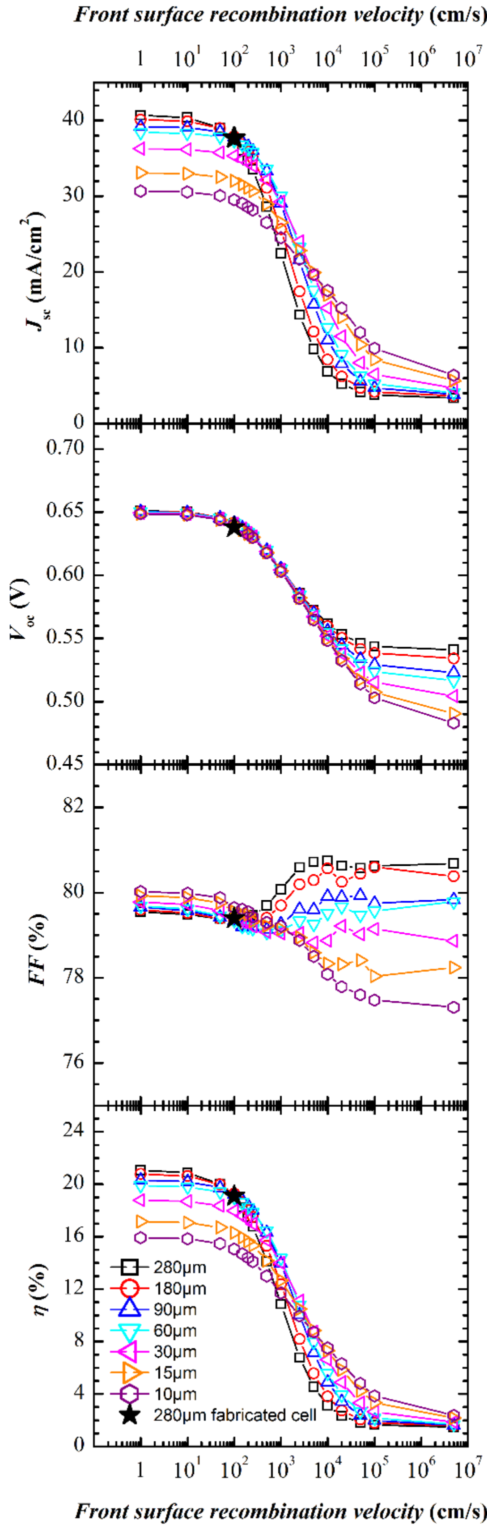

Fig. V. 3 ATLAS simulation of fully-doped c-Si IBC solar cell (0.7 Ω·cm^2 are added in a lumped element to the series resistance) with different bulk Si thickness and front surface S_{front}. PV figures of the fabricated cell are indicated by the star symbol.

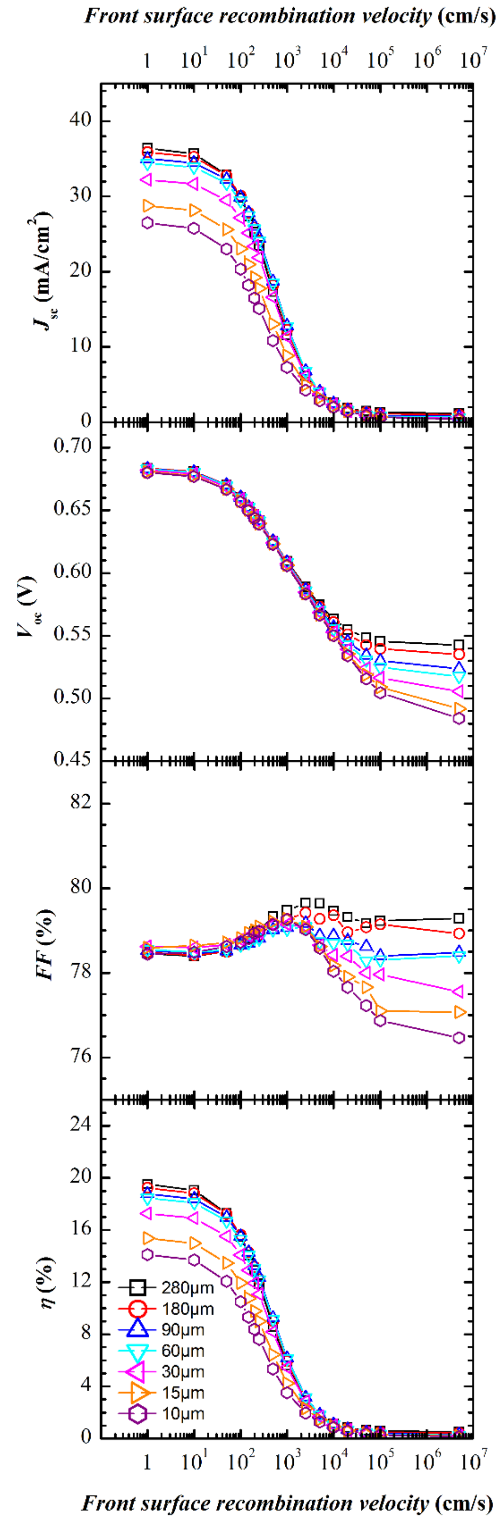

Fig. V. 4 ATLAS simulation of locally-doped c-Si IBC solar cell (0.7 Ω·cm^2 are added in a lumped element to the series resistance) with different bulk Si thickness and front surface S_{front}

V. 1. 4 Discussion

(a) Carrier collection efficiency mapping

As observed in the simulation results, short-circuit current loss is the main factor limiting the thin IBC solar cell efficiency, mainly for the locally-doped structure. This loss can be divided into two aspects: the external optical loss and internal photocurrent collection loss due to carrier recombination. As mentioned in the definition of the simulation procedure, the optical response is identical for both structures, so the difference in J_{sc} for any given S_{front} value should be related to a change in the carrier collection efficiency.

By setting a moveable unique light source beam in ATLAS simulation, the carrier collection efficiency of the specific region (5×5 μm) where light impinges is revealed. For each light scan point, the photogenerated current and collected current are calculated. The ratio of these two values is the carrier collection efficiency of the relevant point-like region that takes into account only the recombination losses. Both fully-doped and locally-doped structures on 10 μm and 280 μm-thick substrate with S_{front} values of 1, 500, and 5×10^{6} cm/s are illustrated respectively in contour plots of Fig. V. 5 and Fig. V. 6. The emitter and base metal contact regions are denoted by solid line square at the bottom corners. The dashed lines in Fig. V. 5 indicates the boundary between doped zones while for the locally-doped case the locally doped areas are just beneath metal contacts (see Fig. V. 6).

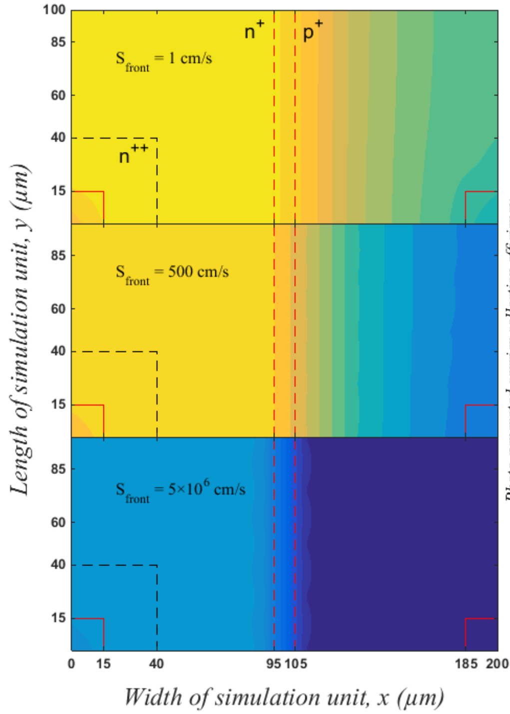

Fig. V. 5 Photogenerated carrier collection efficiency mapping of 10 µm-thick fully-doped cell with S_{front} equals 1, 500, and 5×10^6 cm/s

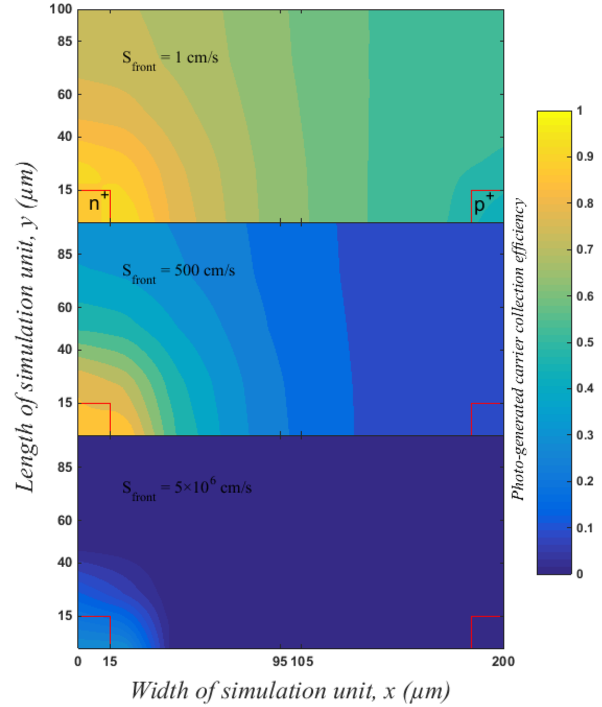

Fig. V. 6 Photogenerated carrier collection efficiency mapping of 10 µm-thick locally-doped cell with S_{front} equals 1, 500, and 5×10^6 cm/s

As can be observed in these two figures, photocarriers generated over the emitter doped regions are the ones that are most efficiently collected for any S_{front} value, as expected. Obviously, the emitter regions under short-circuit conditions are attracting and collecting the photocarriers generated over it competing only against the front surface recombination. This effect can be clearly seen in the fully-doped case (Fig. V. 5) where the collection efficiency decreases from almost 100 % to about 20 % in the emitter region for S_{front} increasing from 1 to 5×10^6 cm/s. Additionally, the emitter is able to extend its influence out of the doped areas. In this case, the collection is negatively impacted by recombination at both front and rear surfaces. In fact, the decay of collection efficiency out of the n$^+$ doped regions is associated to the effective diffusion length of electrons (L_{eff}) along the bulk. In order to obtain this parameter, the effective lifetime (τ_{eff}) is calculated using the following equation (V. 2):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front}}{w} + \frac{S_{rear}}{w} \qquad (V.2)$$

where w is the thickness of the substrate and S_{rear} is the effective surface recombination velocity at the rear surface corresponding to 195 cm/s for the p^+ doped region in fully-doped structure (obtained by auxiliary simulations) and 80 cm/s for the rear passivated surface of locally-doped structure. Neglecting bulk recombination (see Table V.1 for the lifetime definition at the c-Si substrate):

$$\tau_{eff} \approx \frac{w}{S_{front} + S_{rear}} \qquad \text{(V.3)}$$

Based on the Caughey-Thomas model [5] used in simulations, the electron diffusion constant D_{n} is 33.4 cm^2/s, so effective diffusion lengths for electrons are obtained and summarized in Table V. 3.

Table V. 3 Calculated Effective Minority Electron Diffusion Length

	S_{front} 1 cm/s	S_{front} 500 cm/s	S_{front} 5×10^6 cm/s
L_{eff}, Fully-doped	131 µm	69 µm	0.8 µm
L_{eff}, Locally-doped	203 µm	76 µm	0.8 µm

These values indicate the average distance that an electron can travel before recombining and agree well with the contour plots shown in Fig. V. 5 and Fig. V. 6. Recombination at the rear surface out of the emitter region is a well-known effect in IBC solar cells called electrical shading [9]. The electrical shading effect is the consequence of the reduced minority carrier collection due to the rear recombination of the noncollecting regions (all except for emitter regions). Since the emitter region is not fully covering the rear surface, photogenerated carriers have to be transported laterally to the junction. Then, the difference in J_{sc} trend between both structures could be explained as follows. Fully-doped structure is able to efficiently collect carriers in about half of the surface. On the other half, electrical shading is significant leading to L_{eff} values shorter than for the locally-doped case. On the other hand for this last structure, rear surface shows better surface passivation which results in overall lower recombination, i.e. higher V_{oc} values. However, despite longer L_{eff} values, the relatively long distances that photogenerated carriers must travel before finding the emitter region jeopardize carrier collection. Additionally, the locally-doped

structure is more sensitive to a highly recombining front surface due to the longer L_{eff} requirement. As a result, J_{sc} almost vanishes for $S_{front} > 10^4$ cm/s for any substrate thickness.

As a summary of this analysis, we can say that extremely well passivated surfaces are necessary in locally-doped structures for high J_{sc} values. In particular, electrical shading should be taken into account due to the longer distances needed to reach emitter contacts that harden L_{eff} requirements. Strikingly, a rear surface with relatively good surface passivation, like the one used in the simulations (80 cm/s), negatively impacts on carrier collection while simultaneously showing high V_{oc} values. In addition, these V_{oc} values are not reflecting the decrease in J_{sc} due to thinner substrates on neither of the structures. The analysis of this effect is addressed in the following subsection.

(b) J_0 reduction with thickness

As reported previously, V_{oc} for low S_{front} values is weakly dependent on thickness despite the strong reduction in J_{sc} for thinner substrates. This behavior could be only explained by a reduction of saturation current density of the diode (J_0) under dark conditions. Since we are interested in J_0 values at the particular voltage value of V_{oc}, the corresponding J_0 values for every simulated structure can be calculated through (V. 4):

$$J_0 = \frac{J_{sc}}{exp\left({}^{V_{oc}}/_{V_t} \right) - 1} \qquad \text{(V. 4)}$$

Fig. V. 7 (a) shows the calculated J_0 values for S_{front}= 1 cm/s as a function of the inverse of thickness (1/w). As it can be seen, a clear decrease in J_0 is observed for thinner substrates. It should be mentioned that a reduction of bulk recombination cannot justify this J_0 drop. Given the high lifetime values used in the simulations (see Table V.1), only intrinsic recombination processes take place being responsible for only 2-3 fA/cm^2 in the thickest substrate under study. This type of argument is valid when bulk recombination is dominant, as in the case of extremely high quality amorphous silicon passivation where V_{oc} even increases for thinner substrates [10].

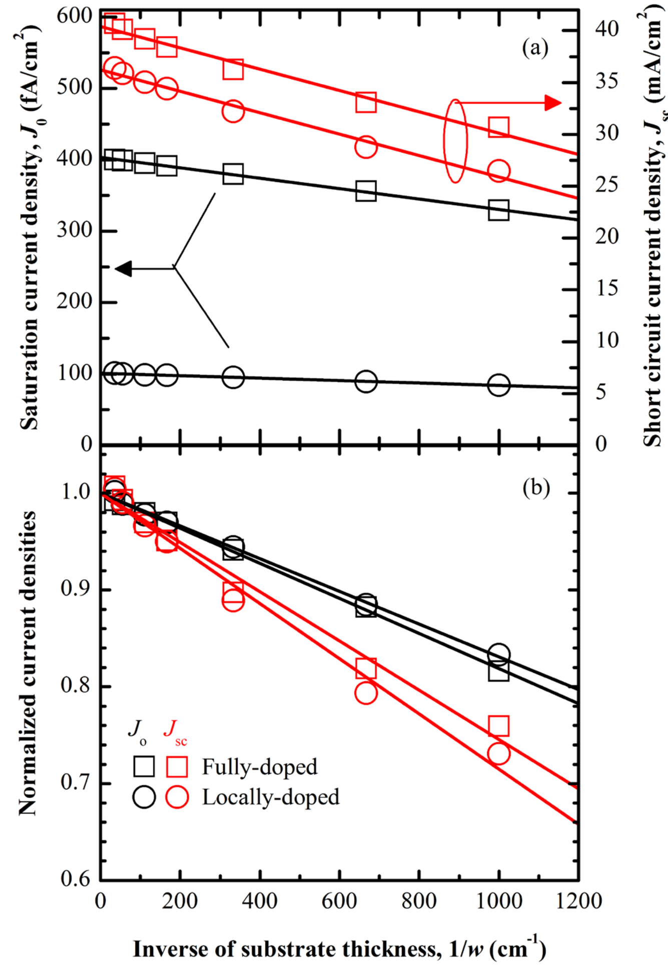

Fig. V. 7 (a) Saturation current density and short-circuit current density *vs.* inverse of substrate thickness. The reduction in J_0 with thickness can be excellently fitted by the proposed equation (V. 5). A similar approach is applied to J_{sc} with slightly worse results. **(b)** The same curves normalized to the maximum values obtained at $1/w = 0$.

In the IBC structures under study, the main recombination occurs at the doped regions (notice the relatively low surface recombination velocities at the non-doped surfaces: S_{front}= 1 cm/s and S_{gap} = 80 cm/s). Then, diode current under dark conditions is mainly flowing parallel to the rear surface. Moreover, current density is higher close to that surface and decreases as one moves away from it. Notice that the current density flows through a surface whose section is different from the typical area of the device used for J_0 calculations. In our particular structures, the area of the simulation unit is 200 × 100 µm and this is the value used to calculate J_{sc} and the corresponding J_0. However, dark current flows through a section which is 100 µm × w and, then, it is impacted

by a reduction in thickness. Focusing on the locally-doped structure Fig. V. 8 shows the current density parallel to the surface under dark conditions for such structure with thicknesses of 280, 90 and 15 µm along a cut line indicated by the inset sketch.

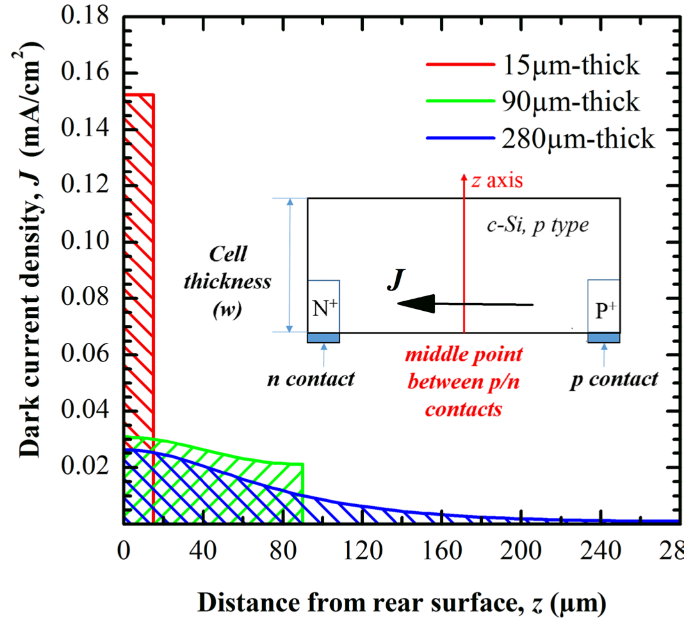

Fig. V. 8 Current density under dark conditions along a cutline defined at the middle point between p and n contacts for w = 15, 90 and 280 µm. For the thickest substrate, current flow is almost null at the front surface, while for the thinnest one current density is constant along all the device thickness.

As it can be seen, current density distribution is highly impacted by device thickness. Almost no current is flowing close to the front surface for 280 µm-thick substrates, while a homogeneous distribution along device thickness is found in 15 µm-thick substrates. Furthermore, for thinner substrates we can consider that thickness reduction results in a decrease of the section through which dark current flows and, consequently, a decrease in J_0 would be expected. The relation between J_0 values and thickness is complex and further research is needed to fully understand this effect. However, as a first approach, a dependence like the one shown in (V. 5) is a reasonable guess. In this expression, J_0 reduces linearly with the inverse of substrate thickness. This maximum value is the one obtained for infinite thick substrates, i.e. with no current flowing close to the front surface. On the other hand, $I_{0,reduction}$ is the current that is reduced divided by the section through

which it flows: 100 µm × w. Notice that in equation (V. 5), $I_{0,reduction}$ is expressed in Amps while the section is be expressed in centimeters, leading to J_0 in A/cm^2, as expected.

$$J_0 = J_{0,max} - \frac{I_{0,reduction}}{100 \cdot 10^{-4}} \cdot \left({}^{1}/_{w} \right) \quad (V.5)$$

Fig. V. 7 shows the dependence of J_0 values for the simulated structures on the inverse of substrate thickness (1/w). Additionally, using these axis, equation (V. 5) results in a straight line and the best fit for both structures is also shown. Interestingly, the theoretical model accurately fits the experimental data suggesting that, despite the problem demands further research, the first approach proposed in this work is reflecting somehow the main physical mechanisms involved. $J_{0,max}$ values of 399.6 fA/cm^2 and 100.2 fA/cm^2 are obtained for fully-doped and locally-doped structures, respectively, which agrees well with the obtained V_{oc} values for the thickest substrate.

From the point of view of J_{sc}, despite not so well fundamented on device physics, a similar approach than equation (V. 5) can be used:

$$J_{sc} = J_{sc,max} - \frac{I_{sc,reduction}}{100 \cdot 10^{-4}} \cdot \left({}^{1}/_{w} \right) \quad (V.6)$$

The simulated values and the best fit are also shown in Fig. V. 7, where we can see that the theoretical model reasonable agrees with the experimental data with $J_{sc,max}$ values of 40.40 mA/cm^2 and 36.23 mA/cm^2 for fully-doped and locally-doped structures, respectively.

Finally, we can plot the same curves, but normalized to the maximum current values. Doing so, we can see how both J_{sc} and J_0 magnitudes decrease with 1/w. The corresponding plot is shown in the Fig. V. 7(b). As it can be observed, for both structures the obtained trend lines for J_0 values show a very similar slope. This suggests again that the decrease of J_0 with thinner substrates is not related to its absolute value, but to the particular current flow close and parallel to the rear surface. On the other hand, J_{sc} values decrease more for locally-doped structure than its fully-doped counterpart, as expected from the current mapping discussion in the previous subsection.

Combining this information, we can gain a new insight into the V_{oc} dependence for S_{front} = 1 cm/s. For both structures, J_{sc} drops slightly faster than dark J_0 leading to V_{oc} values that are only

marginally reduced. Furthermore, while J_0 follows the same trend, J_{sc} is reduced more with thinner substrates for locally-doped structures. This difference could explain the fact that V_{oc} values for this structure decreases about 3.4 mV whereas only a reduction of 2.2 mV is obtained for fully-doped one when thickness is reduced from 280 µm to 10 µm.

From these results, we can conclude that for the IBC structures under study V_{oc} will not be negatively impacted on thinner substrates. The discussion suggests that this effect could be found in any IBC solar cell where the dark current flow is mainly located between the contacts at the rear surface and parallel to it. However, further research is needed to clarify the conditions that must be fulfilled to get the observed J_0 reduction.

V. 1. 5 Conclusion

In this part, by employing 3D TCAD simulation tool, we forecast the efficiency potential of thin IBC c-Si solar cells involving two typical rear surface doping structures: fully and locally-doped. The optical properties of random pyramids texturing on these devices is reproduced by complementary wafer ray tracer simulation while the electrical modeling is validated by a fabricated prototype IBC cell. Simulation results of fully-doped structure reveal an efficiency potential of 16-17 % for thin c-Si IBC solar cell based on substrates of 10-15 µm without changing the technology developed for thick ones. Front surface passivation requirements are relaxed for thinner cells with constant efficiencies up to $S_{front} \approx 100$ cm/s. Regarding the locally-doped structure, its performance is less tolerant to the degradation of front surface passivation. Additionally, the replacement of rear doped regions by a passivated surface results in an increase in V_{oc} which does not compensate the stronger decrease in J_{sc}. This reduction is related to stronger requirements in L_{eff} which is highly impacted by the electrical shading effect. Finally, we focused on the almost constant V_{oc} values for low S_{front} values despite the significant reduction in J_{sc} for thinner substrates. This effect is explained by the reduction of J_0, probably related to a change in the distribution of current that flow parallel to the rear surface. As a consequence, for the IBC structures under study V_{oc} will not be negatively impacted on thinner substrates.

V. 2 Simulation on rear contact pitch variation

In this section, the efficiency potential of thin IBC c-Si solar cells based on locally-doped structures is explored for different rear contact distances or pitches. The objective is guiding the design of such devices.

V. 2. 1 Parameters in simulation and pitch variables

Instead of using a fixed contacts distribution geometry defined by the fabricated prototype IBC solar cell as reported in the previous section, now the laser processed point-like contact pitch is altered and optimized in order to explore the device efficiency potential. Similarly, only p and n contacts of same quantity arranged in the horizontal and vertical directions of the rectangular solar cell area plane is considered, as shown in Fig. V. 9. The distance of the laser spots between different doped regions are defined as horizontal pitch variable x while that of the same region is defined as vertical pitch variable y. Thus the extracted simulation unit has vertical side length of x and the horizontal side length of $y/2$. Considering the technological limit of the laser spots size and metal etching at the contact gap, the variable x are set to be 250, 500, 750 and 1000 µm, while the variables y are 200, 300, and 400 µm.

The c-Si substrate used in simulation are n type material and the thicknesses are 10, 20 and 40 µm referring the commercial available c-Si wafers in the research group. The uniform background donor doping density is 1.89×10^{15} cm^{-3} according to the resistivity datasheet of wafers provided by the manufacturer (2.5 Ω·cm). The front and rear surface recombination velocity are fixed to be 10 cm/s to approach the passivation of thermal ALD deposited aluminum oxide. Using the same approach of optical model reported previously, devices of each pitch case is optically divided into three different structures which are Al_2O_3-90nm/Si-textured/SiO_2-100nm/Al, Al_2O_3-90nm/Si-textured/Al and Al_2O_3-90nm/Si-textured/SiO_2-100nm. According to the practical area proportion of each optical structure and substrate thickness, the spectral irradiances used in each simulation are adjusted by the light absorptivity ratio of the pyramids-textured structure and the corresponding simplified plane-front-surface structure.

Laser spot is a circle-like region under microscope observation, and the diameter is about 30 μm in case of ultra-violet laser ablation. The reason of using ultra-violet laser is its shallow surface doping effect which is preferable to be used to thin c-Si substrate and a less recombining region is expected [3]. Considering that the objective of this study is finding the efficiency tendency on pitch variation, an accurate reproduction of laser doping electrical property is out of the framework. Thus a simplified approach that roughly represents the electrical performance of laser doped region is used. Based on the N type substrate, the emitter p type doping concentration is defined to be 1×10^{20} cm^{-3} at depth with Gaussian distribution and the electron and hole carrier recombination velocities are all 5×10^{6} cm/s at the interface with metal contact. Then, the n type doping at base region is not included in the simulated structure, but it is modeled by different recombination velocities at contact interface for the electron and hole carriers which are 5×10^{6} and 2500 cm/s respectively. The latter has been experimentally determined by test structures [11]. In order to simplify the structure description in simulation, the circular laser spot is reformed as square area with side length of 30 μm. A schematic figure (Fig. V. 9) of this simulated device structure is shown from a rear surface view.

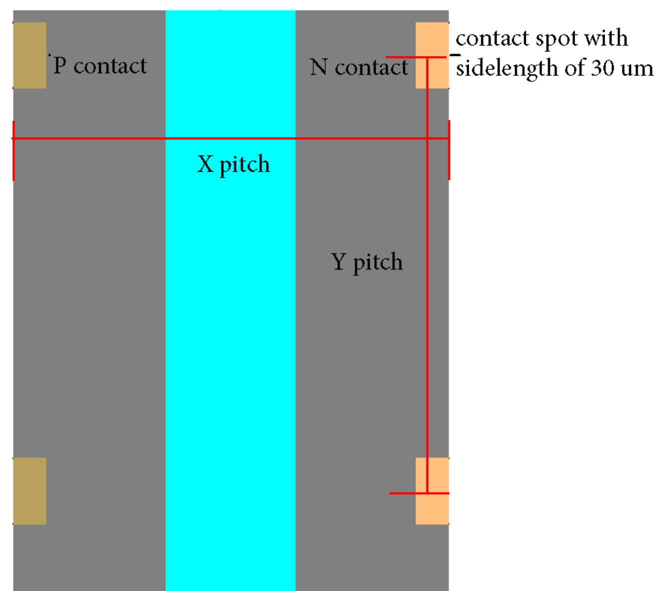

Fig. V. 9 Rear view of the laser contact spot pitch

Except these parameters indicated specifically, the others are the same as previous simulation set and the details can be found in the Table V. 1.

V. 2. 2 Simulation results and discussion

The simulation results are revealed in the following figures for the three explored substrate thicknesses: 10 µm (Fig. V. 10), 20 µm (Fig. V. 11) and 40 µm (Fig. V. 12).

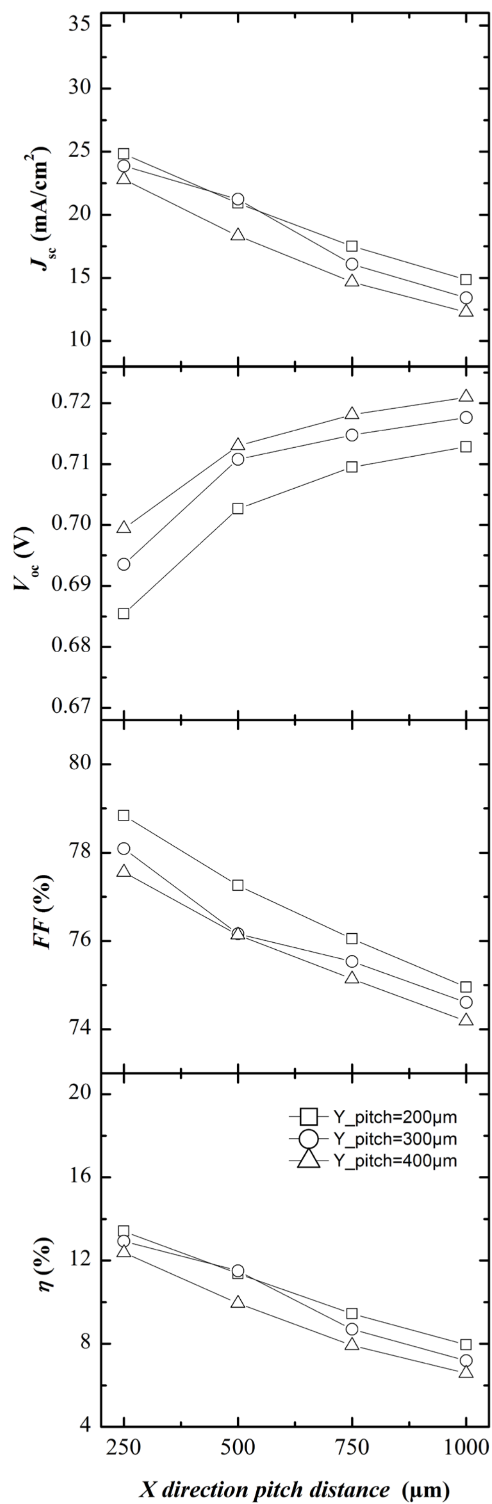

Fig. V. 10 Simulation results of 10 um-thick c-Si substrate

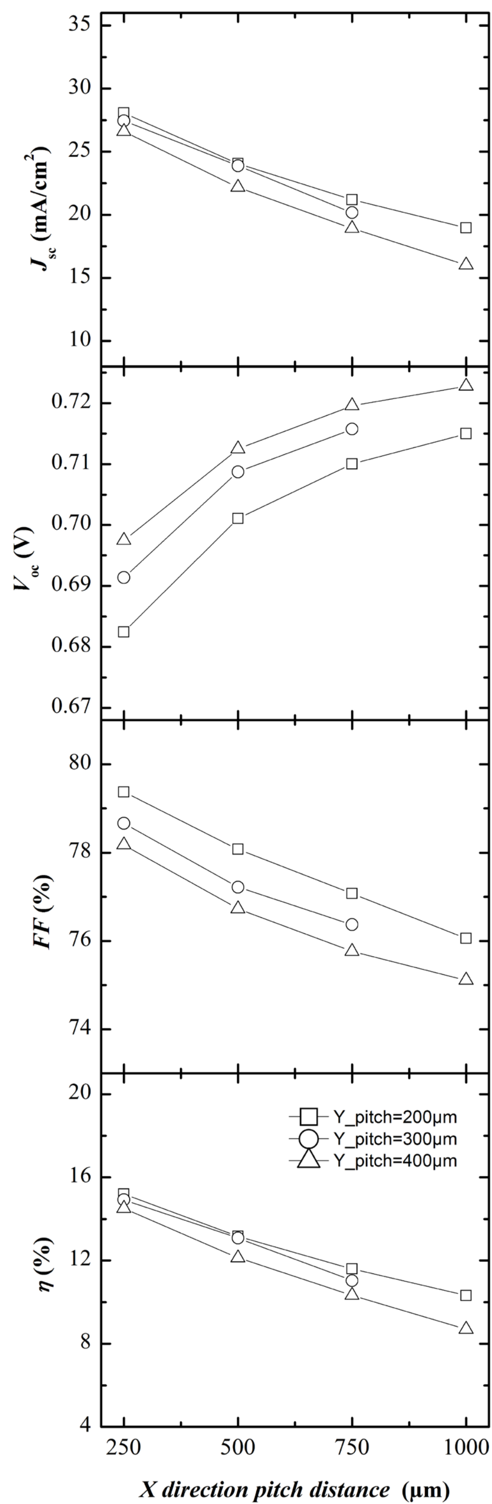

Fig. V. 11 Simulation results of 20 µm-thick c-Si substrate

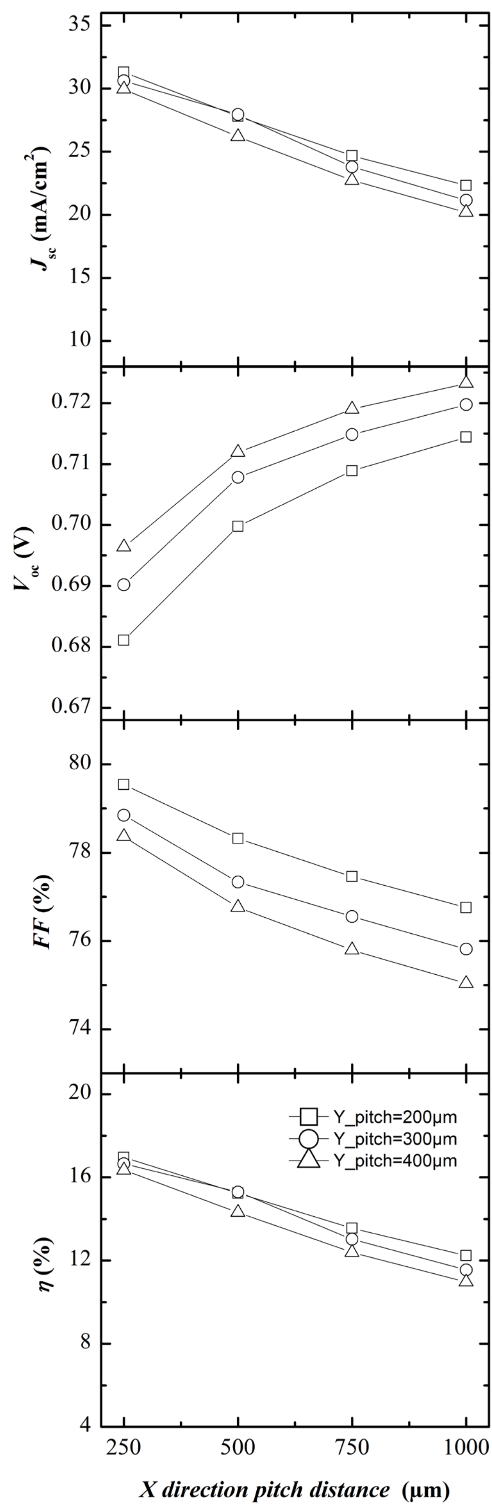

Fig. V. 12 Simulation results of 40 μm-thick c-Si substrate

Compared to simulation results of the previous section, similar trends for J_{sc} can be found as J_{sc} decreases with substrate thickness due to reduction of light absorption. Interestingly, long pitches clearly degrade this parameter with a stronger impact of horizontal pitch. This trend can be explained by a reduction of carrier collection due to the longer L_{eff} requirements. Simultaneously, ohmic losses increases with longer pitches resulting in lower *FF*. On the contrary, longer pitches results in lower recombination in the device and better V_{oc}. However, this improvement is not able to compensate the J_{sc} and *FF* decreases that dominate the resulting efficiency. As a consequence, the shortest explored pitches of 250 µm and 200 µm for horizontal and vertical directions are the ones that report the highest efficiencies.

V. 2. 3 Conclusions

In this part, the rear point-like doping structure geometry is evaluated simulating a full laser doping approach. PV figures for each geometry are presented for guiding the rear laser doping structure design. Efficiency is dominated by J_{sc} and *FF* trends that decrease with longer pitches. Additionally, horizontal contact pitch variation is more sensitive than vertical pitch on conversion efficiency. As a consequence, short pitches in the range of 200-250 µm is preferred to approach the best results. It should be mentioned that, despite probably lower distance would be desirable, this range is the minimum limit available with our alignment technology that combines laser processing and a subsequent photolithography for contact definition.

References V

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Chapter VI

Thin IBC c-Si solar cell fabrication based on silicon etching

In this chapter, a detailed fabrication method based on bulk material etching towards thin IBC c-Si solar cell is presented. The etching technique is firstly developed combining dry and wet etching. Then passivation on thinned Si samples is characterized with aluminum oxide symmetrically deposited demonstrating that the thinning down process do not introduce a significant bulk damage. Additionally, front surface is texturized again after thickness reduction in order to improve optical properties. Passivation of this surface results of reasonable values with front surface recombination velocities in the range of 500-600 cm/s.

The proposed etching technique is applied to IBC solar cells fabricated on thick substrates resulting in a thin IBC solar cell with a thickness of ~30 µm and an efficiency of 12.1 %. This finished device provides a first approach of thin IBC solar cell fabrication and it reveals the efficiency potential for transferring IBC device technology from thick to thin substrates.

VI. 1 Introduction

In previous chapters, several fabrication methods are reported compatible with thin c-Si solar cells with different experimental design and processing methods. In this chapter, as a first approach to the fabrication of thin c-Si IBC solar cells in our research group, we propose a process where we start from a finished IBC cell fabricated on thick c-Si substrates which is subsequently thinned down. In Fig. VI. 1 we show the proposed fabrication process. Firstly, an IBC c-Si solar cell based on conventional high temperature technologies is fabricated following reference [1]. Next, the rear surface is protected by polyimide in order to give a mechanical support to the device once it is slimmed down. Now, silicon is etched from the front surface by different methods. As it will be shown later, a combination of RIE etching with a final wet etching is found as a feasible option. Once the substrate has the desired thickness, front surface is cleaned, texturized and passivated again. By doing so, we could obtain a thin IBC solar cells minimizing the handling problems of such thin substrates. In the following subsections the different fabrication steps are described in detail.

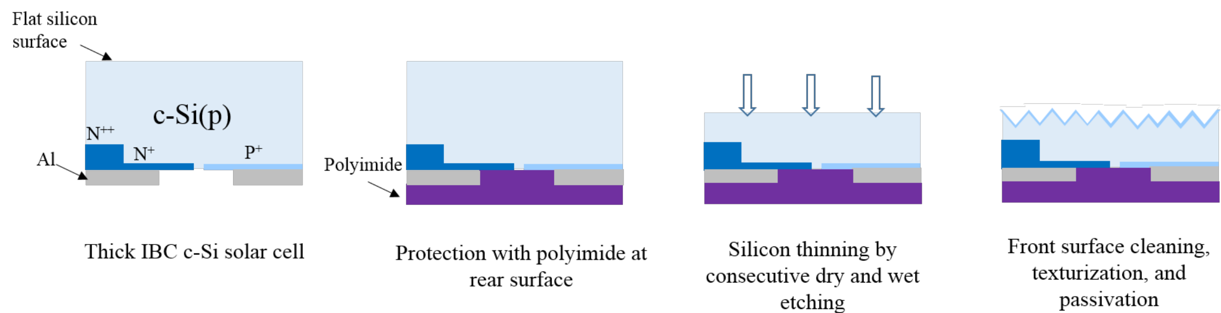

Fig. VI. 1 Fabrication process of thin IBC c-Si solar cell

VI. 2 Polyimide coating

VI. 2. 1 Manufacturing process

The etching sample is a 3.5×3.5cm^2 silicon square cut from a 4-inch wafer. The original thickness of the silicon square is about 280 μm and resistivity is 1~5 ohms·cm. The sample size

should be precise to avoid any mismatch with the setup that will be used to etch the silicon from the front surface (see below, such as Fig. VI. 3 and Fig. VI. 4), thus laser processing is employed for accurate cutting. The laser power used for cutting is set to 2 W and multiple passing times is applied to make sure an easy breakage afterward.

Silicon is generally a brittle material and the flexibility is low, however, this mechanical property is expected to change once the thickness is tremendously reduced. Then, an extra support layer is required for improving the handling of thin c-Si samples.

To fulfill this requirement, an extra layer of polyimide is chosen with brand of Durimide 7320, Fujifilm. The composition is N-Methyl-2 Pyrrolidone (872-50-4) Polyamic acid ester (PMN-98-799) Tetraethylene glycol dimethacrylate (109-17-1) Organo-titanium complex, and the density is 1.39 g/cc. The glass transition temperature is 285°C and the thermal decomposition temperature: 525°C.

The polyimide attaching process is reported as following:

1. Standard sample cleaning by acetone, isopropanol and water
2. The spinner is used to uniformly cover the polyimide onto the smooth surface of the silicon square with 1700 RPM (results in ~20 µm-thick).
3. Sample with polyimide attached is baked at 100 °C for 3 minutes
4. The negative photoresist is exposed under 270 nm wavelength light
5. 30 minutes of exposure to ambient temperature and one hour of heating at 335 °C is carried out to realize the glass-transition of the polyimide. This step is carried on inside a limited space under N_2 environment with a digital temperature controller assisted, the whole process takes one hour including 20 minutes of temperature increase from 25° C to the set-point 335° C with an increasing rate of 15 ° C/minutes and 40 minutes stable temperature at 335° C.

Then the silicon square sample with polyimide support layer is prepared and ready for assembling.

VI. 2. 2 Impact on surface passivation

In this part, the impact on passivation of polyimide layer is evaluated firstly on samples with normal thickness.

The polyimide support layer is assumed to be attached to the final device for an easier operation and rear surface contacts protection. Thus it is essential to know how this extra layer affects the minority carrier lifetime, which is an important indicator of the surface passivation quality.

The initial material is n type FZ crystalline silicon, 278 μm of thickness, and polish surface. The 4 inch silicon wafer is processed primarily by RCA cleaning. Then the 90 nm aluminum oxide layer is deposited on both side surface by atomic layer deposition (ALD) method. Afterwards, a 10 minutes annealing is conducted in the forming gas, a mixture of hydrogen and nitrogen, at 375 ° C to activate the c-Si surface passivation. Ultimately, the entire wafer is cut to 4 squares with 3.5×3.5 cm edge length, and the effective lifetime is measured.

Afterwards, the polyimide layer attachment is completed following the procedure reported previously. Minority carrier lifetime of these samples are measured again. The results of prior and after the polyimide layer processing is presented by Fig. VI. 2 below.

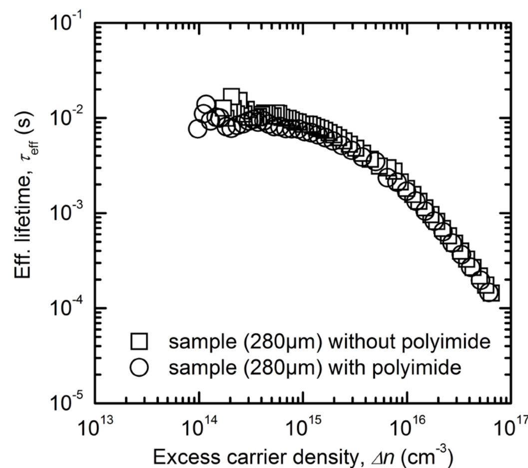

Fig. VI. 2 Lifetime of minority carrier density in case of 90 nm Al_2O_3 passivation at both sides (annealing with 10 minutes of forming gas) and polyimide attached at one side (annealing process is stated in text)

As a conclusion, it can be reported that there is not any significant impact on effective minority carrier lifetime of crystalline silicon induced by extra polyimide layer attachment process.

VI. 3 Thinning down of c-Si substrates

VI. 3. 1 Experimental setup

As a first approach, we propose to thin down c-Si substrates by means of wet etching. In particular, we would like to use TMAH which is the short term of Tetramethylammonium hydroxide. It is commonly used diluted in water or ethanol to anisotropically etch silicon with temperatures between 70 and 90 °C. The etching rate generally increases with temperature and decreases with increasing TMAH concentration. The chemical solution used in this experiment is 25 *wt.* % TMAH in water since the etched silicon <100> surface roughness decreases with increasing TMAH concentration and a smooth surface is preferred.

Since we want to expose only front surface to the chemical etchant, an especial setup is designed and fabricated. The setup for the experiment consists of a set of Teflon pieces for sample assembling and a compatible solution container. The sample is sandwiched between two Teflon pieces which are fixed with screws. A window is opened on the top piece allowing unique front surface exposure to etching solution with the other surface sealed. A stir bar is positioned just above the sample exposure window connected to a motor which is supported on top of the container. A picture of assembled setup in etching solution is shown in the Fig. VI. 3.

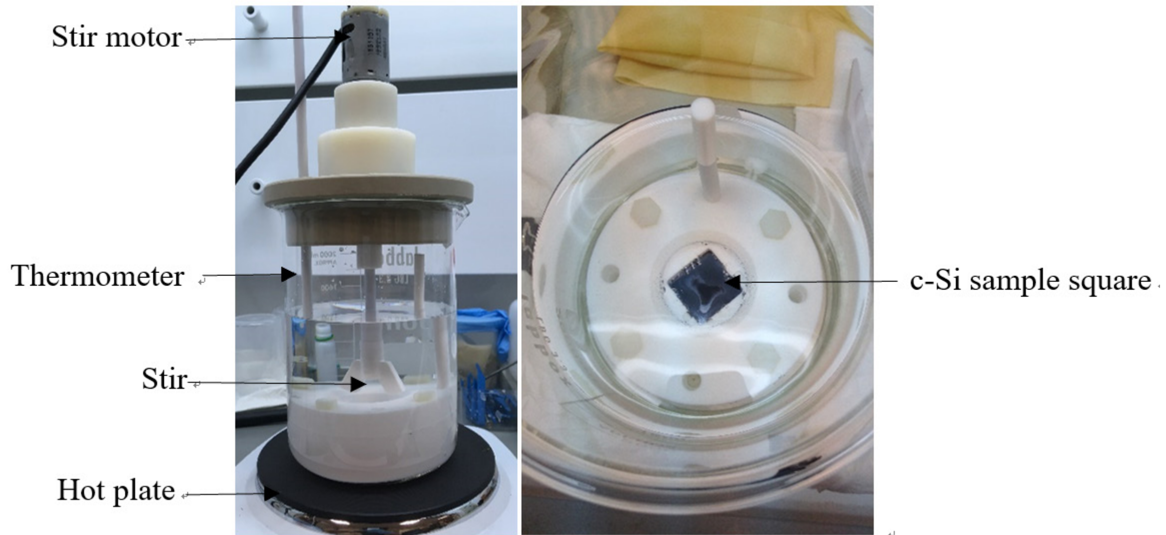

Fig. VI. 3 Lateral and front views of assembled setup for silicon sample TMAH etching

Etching solution volume is about 900 ml in each process to make the setup totally sunk. The solution temperature during etching is 80 °C assisted by a hotplate and thermometer system (about 30 minutes preheating is required for temperature stability after sinking the setup into the solution).

VI. 3. 2 Silicon etching by combined methods

First tests revealed that the etching rate is not efficient and that it takes nearly ten hours etching to reach a reasonable thin substrate of around 50 µm. Besides, some cracks can be observed after the long etching and the polyimide below c-Si becomes visible at some edge zones on the exposed area of the silicon square. Under these circumstances, the exposed polyimide will quickly react with etchant and dissolves, then more TMAH solution will permeate into the photoresist side leading to the breakage of sample. Additionally, TMAH solution cannot be recycled due to contamination. From these results, we conclude that, although the setup works well for short etching times, the sealing of the setup cannot stand during so many hours of contact with the etchant.

In order to avoid this limitation, a dry and wet etching combined method is proposed consisting of a combination of RIE and chemical etching. Firstly, a 1 hour and 50 minutes Reactive-Ion Etching (RIE) is conducted. Sulfur hexafluoride (SF_6) is used to generate ionized

particles to realize the bombardment to the c-Si surface. This process is carried out in the RIE setup at ICFO. The mentioned duration is chosen to obtain a c-Si substrate of about 110 μm. After this dry etching step, a very rough c-Si surface is obtained with poor thickness uniformity. Differences of ± 10 μm are measured.

Fortunately, the surface roughness and uniformity problem is solved to a large extent through wet etching process with 25 *wt.* % TMAH to the desired thickness. The TMAH etching time is about 4 hours resulting in a smooth surface with differences in thickness of only ±3 μm. After several tests, it is concluded this dry-wet combined etching method is highly reliable and repeatable. A sample picture is shown in Fig. VI. 4 after the RIE dry etching and TMAH wet chemical etching.

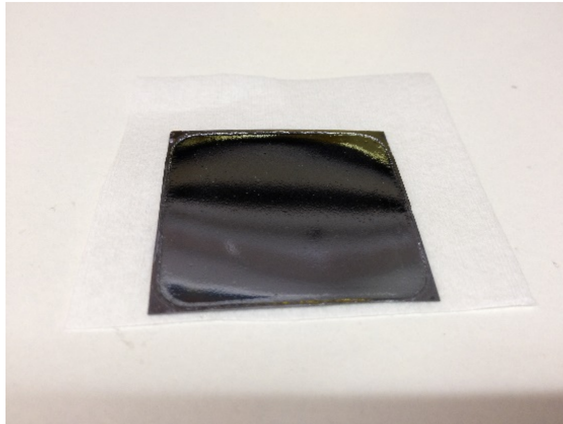

Fig. VI. 4 Picture of a silicon sample after dry and wet etching

VI. 3. 3 Surface passivation for thinned c-Si substrate

In order to investigate the surface passivation on thin c-Si substrates, several c-Si square samples without polyimide support layer are fabricated by combined SF_6 dry and TMAH wet etching. The passivation layer is aluminum oxide deposited by thermal ALD. The ALD deposited aluminum oxide has demonstrated outstanding passivation properties for crystalline silicon surface employing the built-in electric field effect and silicon surface dangling bonds passivation simultaneously, which has been reported by many publications [2, 3].

Through the RIE dry etching of SF_6 on silicon, the sample thinning can be processed in a relatively safe way. It should be noticed that the RIE machine is not designed for the processing of long-time silicon etching, but the previous dry etching can effectively reduce the following wet chemical etching duration leading to a more reliable substrate thinning.

In this case, an even longer RIE dry etching is carried out. N or p type silicon square is etched by RIE for 3 hours, reaches about 45 µm-thickness. The etching rate is 80 µm/h, which is a little higher than the ones with polyimide layer at backside. Then, the RIE etched samples are submerged into the 25 *wt.*%, 80 °C TMAH for further thinning, at the meantime, repairing the damaged surface left by the ion etching.

Once the thin samples are prepared, they are cleaned by a standard RCA1 cleaning (1 liter solution with standard proportion, Water: NH_3:H_2O_2=6:1:1). Extreme carefulness is demanded during the wet chemical etching and RCA1 cleaning since the free-stranding thin samples are prone to adhere with each other. Immediately after the cleaning, 90 nm Al_2O_3 is deposited at both surface through thermal ALD system followed by 10 minutes of annealing under N_2/H_2 mixed gas. The effective lifetime is measured and presented in the Fig. VI. 5.

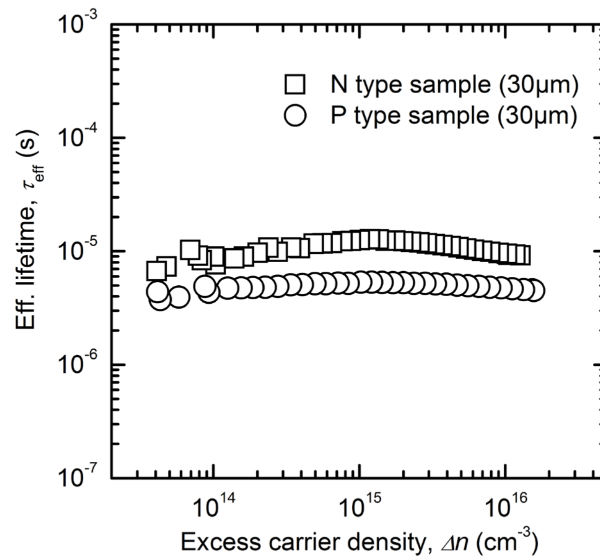

Fig. VI. 5 30 µm-thick N and P type silicon square samples effective lifetime measurement by Quasi-steady-state photoconductance method

According to the QSSPC measurement, the effective carrier lifetime of n and p type 30 µm-thick samples are 10 µs and 5.5 µs at the 1×10^{15} cm^{-3} excess carrier concentration level respectively.

Since the samples are symmetrically passivated by 90 nm aluminum oxide and a very low recombination in bulk material is assumed, the effective surface recombination velocity (S_{eff}) can be calculated by equation (VI. 1), where W is the sample thickness.

$$\frac{1}{\tau_{eff}} = \frac{2S_{eff}}{W} \qquad \text{(VI. 1)}$$

Thus, S_{eff} of ~140 cm/s and ~245 cm/s are deduced for n and p type free-standing thin silicon samples. These values are worse than the ones obtained for thick c-Si substrates which are in the range of 10 cm/s (see for example Fig. VI. 2 where lifetime in the millisecond range is measured). Two main reasons can be given for such worse values. On the one hand, the handling and cleaning of free-standing thin samples is not easy and could result to an interface with poor quality before passivation. On the other hand, it is also suggested that not only a surface damage, but also a certain bulk material damage is probably occurred during the ion etching leading to a higher crystal defects. Part of this bulk damage is removed in some extend during the TMAH wet etching, but only 15 µm are etched for these samples. With the material degradation, the recombination in bulk silicon is no longer negligible and the S_{eff} should be lower than the calculated results under this assumption. In any case, it should be noticed that a S_{eff} of around 200 cm/s is still good enough for achieving high efficient device according to the simulation results reported in chapter V. So we can conclude that the surface left by the thinning down process could be passivated with enough quality.

VI. 4 Textured thin c-Si substrates

VI. 4. 1 Surface passivation

Once we have demonstrated the viability of the thinning down process, we want to explore the impact of texturization of the front surface. To do so, we prepared dummy samples using the following process. Firstly, a 90 nm Al_2O_3 film is deposited on both surfaces to passivate them and rear surface is covered with a polyimide film as described in the previous section. Next, c-Si

substrates are thinning down through RIE dry and TMAH wet etching. Keeping the sample in the teflon setup, the front surface is then cleaned by standard RCA followed by random pyramids texturing formation in a TMAH bath with TMAH: H_2O: IPA (320ml: 3320ml: 360ml) proportion at 80 ºC. Finally, another standard RCA cleaning is carried out. After finishing it, the sample is immediately taken out from the setup and introduced into the ALD chamber to deposit 90 nm aluminum oxide film. After the 10 minutes annealing at 375 °C, minority carrier effective lifetime is measured for all the finished samples and the results are presented in the Fig. VI. 6.

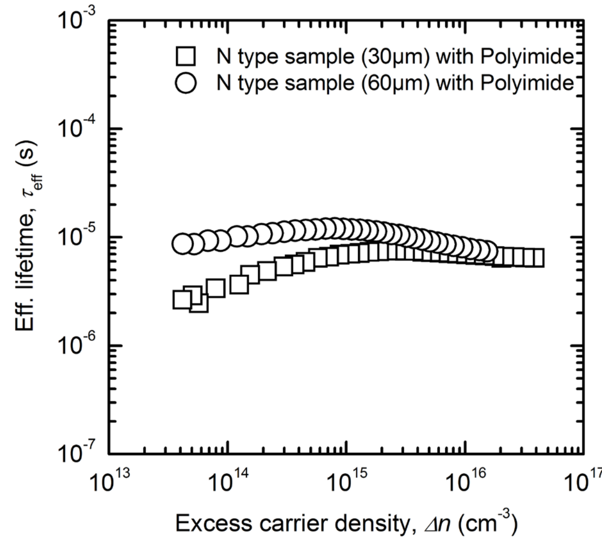

Fig. VI. 6 30 and 60 μm-thick N type samples with 90 nm Al_2O_3 on textured front surface and flat rear surface and with polyimide attached

In Fig. VI. 6, the effective lifetime of 30 μm-thick and 60 μm-thick n type samples are presented. The data at excess carrier density 1×10^{15} cm^{-3} are extracted and the front surface S_{eff} is calculated using the equation (VI. 2):

$$\frac{1}{\tau_{eff}} = \frac{S_{eff,1} + S_{eff,2}}{W} \qquad \text{(VI. 2)}$$

where $S_{\text{eff,rear}}$ is the rear surface effective recombination velocity. This value is assumed to be constant to the one measured after polyimide deposition onto the symmetrically passivated thick sample. As shown in Fig. VI. 2, effective lifetime at 1×10^{15} cm^{-3} is ~10 ms and, thus, a $S_{\text{eff,rear}}$= 1.4 cm/s is calculated.

The calculated front surface effective recombination velocities for all samples are summarized in the Table VI. 1.

Table VI. 1 Calculated front surface effective recombination velocities

Sample (thickness)	τ_{eff} (s) (at 1×10^{15} cm^{-3} excess carrier density)	$S_{eff,rear}$ (cm/s)	$S_{eff,front}$ (cm/s)
N type (30 µm)	4.8 µs	1.4	624
N type (60 µm)	11.9 µs	1.4	503

As it can be seen, the obtained values are higher than the ones measured for flat surfaces on thin substrates presented in the previous section (see Fig. VI. 5). This increase could be related to the random pyramid texturization that increases surface by a factor of 1.7. In addition, some negative impact on surface cleaning is also expected. Although this increase in front surface recombination, $S_{eff,front}$ values in the range of 500-600 cm/s are still good enough to fabricate devices with reasonable efficiencies, as demonstrated by simulations in chapter V.

VI. 4. 2 Optical properties of texturized thin c-Si substrates

As the solar cell thickness is reduced largely, a great light absorption loss is expected depending on the silicon absorber optical property. However, to fabricate an efficient device, a strong light absorption is required since the efficiency generally follows the tendency of photogenerated current as reported in chapter V about device simulation. In this part, the optical properties of flat and texturized thin c-Si substrates are analyzed in order to calculate the potential photocurrent expected in the devices.

To do so, we measure reflectance and transmittance of samples using UV-visible-NIR Spectrometer (Shimadzu 3600) with the wavelength ranged from 300 to 1200 nm. Once we have this information, raytracing software GenPro4 is used to accurately measure the c-Si absorption and the corresponding potential photocurrent density.

GenPro4 is a MATLAB based simulator provided by Rudi Santbergen from Photovoltaic Materials and Devices of the Delft University of Technology [4]. Ray tracing method are employed

by this simulator considering the internal reflection, scattering and optical trapping. The potential photogeneration of each layer is deduced by the knowledge of calculated absorption. To obtain the layer optical property by this simulator, the refractive index (n) and extinction coefficient (k) of the involved layers are required in addition to the thickness of each material and the surface topography between them. Since the final device generally consists of c-Si layer, Al_2O_3 and the back reflector aluminium (the extra support polyimide layer is regarded none optical-active in this case since no light passes through back reflector Al), the n and k data of these three materials are collected. Respectively, n and k of c-Si and aluminium are given from literature [5, 6], those of Al_2O_3 are provided by spectroscopic ellipsometry measurement of the thermal ALD deposited material. The n and k data of these material are presented in the Fig. VI. 7-9 below.

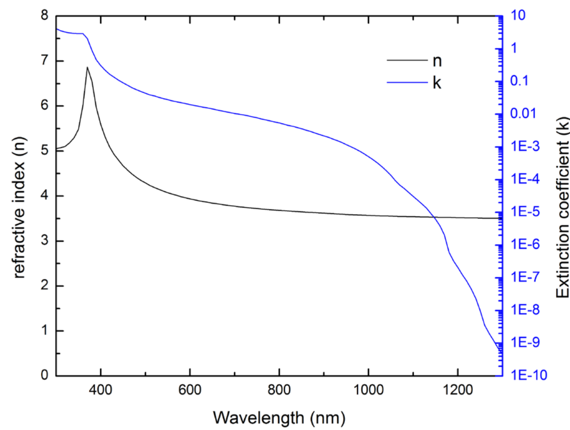

Fig. VI. 7 Refractive index (n) and extinction coefficient (k) of c-Si, data from literature [5]

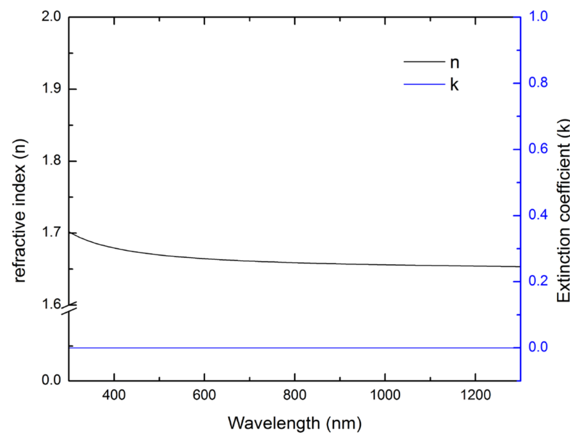

Fig. VI. 8 Refractive index (n) and extinction coefficient (k) of Al_2O_3, data from experimental measurement

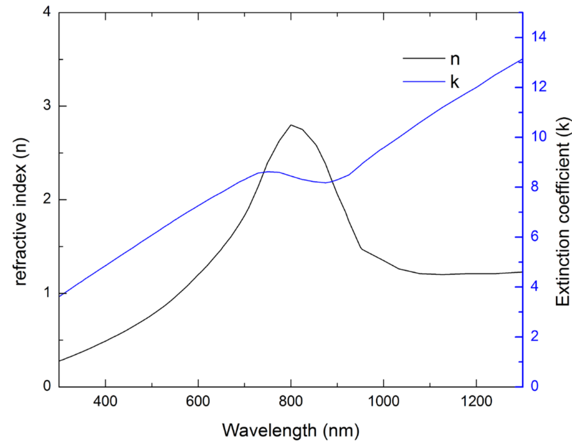

Fig. VI. 9 Refractive index (n) and extinction coefficient (k) of back reflector aluminium, data from literature [6]

As it can be observed, the extinction coefficient (k) of Al_2O_3 are null, indicating that no light can be absorbed by this layer in the shown wavelength range.

Firstly, in order to validate the GenPro4 potential photocurrent deduction, the optical property of flat and textured c-Si samples, 30 μm-thick free-standing and pyramids textured 30 μm-thick c-Si sample with 90nm Al_2O_3 on both surfaces and Al back reflector, are experimentally measured and simulated by GenPro4. Then the comparison results of reflection and transmittance and shown in the Fig. VI. 10 and Fig. VI. 11.

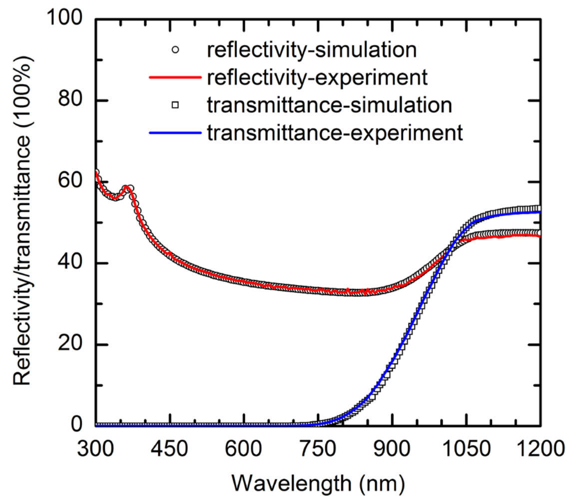

Fig. VI. 10 reflectivity and transmittance from experiment and simulation of 30 μm-thick free-standing c-Si sample without nothing

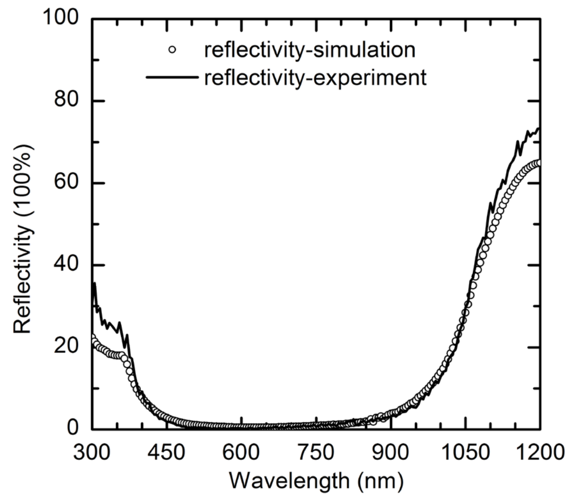

Fig. VI. 11 reflectivity from experiment and simulation of textured 30 μm-thick c-Si sample with 90nm Al_2O_3 on both surfaces and Al back reflector

For flat free-standing sample, a very good accordance of reflectivity and transmittance is shown. For pyramids textured sample, no light transmittance is assumed since Aluminium is employed as back reflector. In this case, some deviation of reflectivity can be seen at short and long wavelengths. This mismatch could be explained by the difference between the practical textured surface morphology of the sample and the pyramids definition used in simulation.

After the optical calculation validation, the simulator is used for estimating the photocurrent under standard light irradiance condition for both flat and front textured samples. The calculated results includes all the path media that the light pass through, shown in the Fig. VI. 12 and Fig. VI. 13.

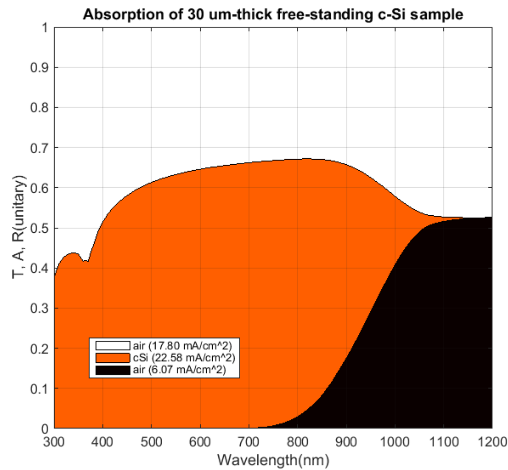

Fig. VI. 12 Absorption of 30 µm-thick free-standing c-Si sample and the maximal photocurrent

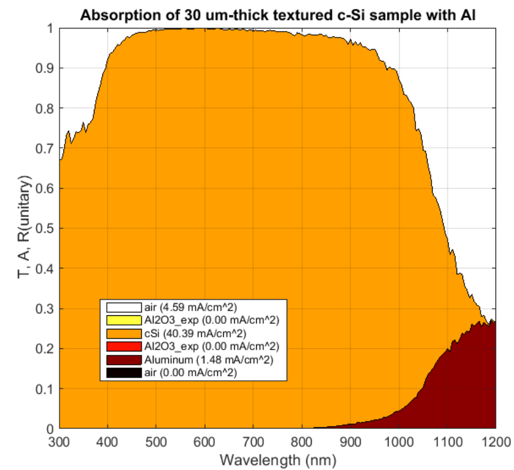

Fig. VI. 13 Absorption of 30 µm-thick textured c-Si sample with 90nm Al_2O_3 on both surfaces and Al back reflector, and the maximal photocurrent

As can be observed, more than 40 mA/cm^2 potential photocurrent is concluded for textured c-Si sample, while only 22.56 mA/cm^2 are obtained for flat surfaces. At a first glance, the potential photocurrent for textured sample could seem too high. However, as it was shown in Table II.1, 38.5 mA/cm^2 has been reported for 35 µm thick c-Si substrate finished solar cells. Taking into account that some recombination must be present in the real device, a potential photogenerated current of 40.39 mA/cm^2 could be feasible.

VI. 5 Thin IBC c-Si solar cell fabrication and characterization

Following the silicon etching sequences, one of the finished IBC prototype solar cell is slimed down to ~30 µm, which has identical structure as fully-doped structure presented in chapter V. The rear surface where the contacts are located is protected by a ~20 µm polyimide film to improve the operability. Then, RIE plasma etching is conducted firstly to reduce the cell thickness to about 100 µm, followed by a further wet TMAH (25 *wt.* %) etching on the front surface. After these steps, random pyramids are defined on the front surface and passivated by a 90 nm Al_2O_3 layer. Finally, a 375 °C annealing is performed to activate the front surface passivation. Pictures of the finished device before (left) and after processing (middle and right) are shown in Fig. VI. 14.

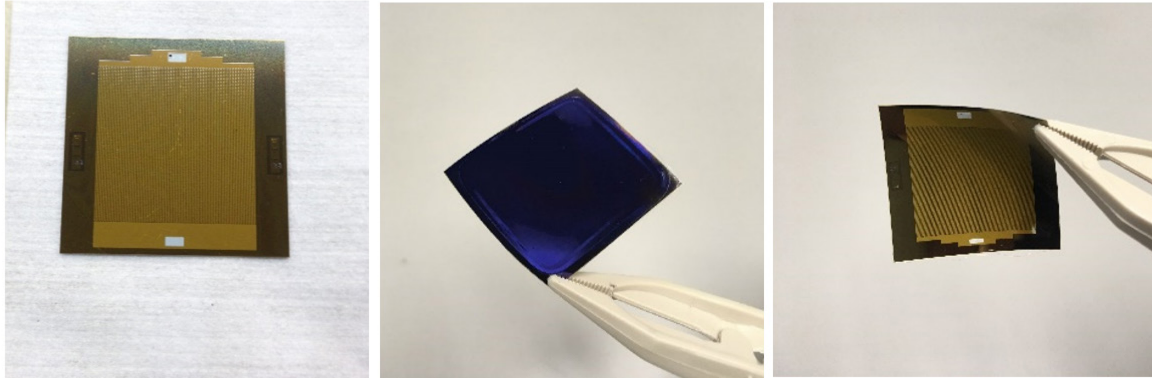

Fig. VI. 14 Pictures of a thin c-Si IBC solar cell. (Left) finished IBC solar cell before thinning; (middle) front surface after thinning, texturing and passivation; (right) rear surface after thinning, texturing and passivation

The measured current-voltage curve as well as the one derived from Suns-V_{oc} measurement are presented in Fig. VI. 15, under standard conditions (AM1.5G, 100 mW/cm^2, 25 ºC). The obtained photovoltaic figures measured are summarized in Table VI. 2.

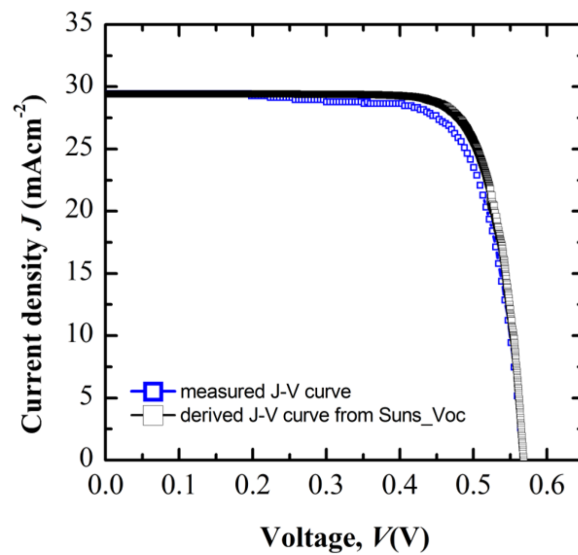

Fig. VI. 15 *J-V* and Sun-V_{oc} measured curves of fabricated ~30μm IBC solar cell.

Table VI. 2 Photovoltaic figures of fabricated ~30 μm IBC solar cell and S_{front} value deduced from *EQE* measurements, the bottom row presents the simulation results at the corresponding S_{front} and device thickness 30 μm

	J_{sc} (mA/cm^2)	V_{oc} (mV)	$FF(pFF)$ (%)	η (%)	Deduced S_{front} (cm/s)
Experiment results	28.1	569	75.5(81.5)	12.1	-
Simulation results	27.5	597	79	13.0	1500

In order to compare the PV characteristics of the real cell with the calculated values from simulation, the front surface recombination velocity of the real device should be determined. Since quantum efficiency in short wavelength range is largely determined by S_{front}, the External Quantum Efficiency (*EQE*) of the fabricated IBC cell is measured for comparing with those from simulation and determine S_{front}. The Internal Quantum Efficiency (*IQE*), i.e., the electrical loss via recombination, is extracted from ATLAS simulation under different S_{front} values. Then, the optical losses are calculated by the wafer ray tracer software and *EQE* is obtained by multiplying both results.

Fig. VI. 16 shows the best fit of the *EQE* experimental data with our model resulting in a S_{front} of 1500cm/s. It can be observed that the measured and simulated *EQE* coincide well in blue/visible part of the spectrum while a small deviation can be seen in the infrared part. This difference is probably attributed to an inaccurate model of the light confinement properties, since these photons are the ones that could reach the rear surface of the device. For example, polyimide has not been included in the model and it could have an effect in regions where there is no metal covering the rear surface.

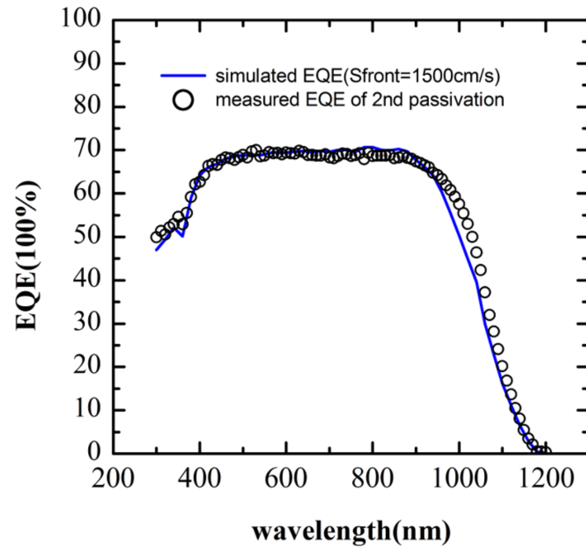

Fig. VI. 16 *EQE* comparison between simulation result and measurement of the fabricated ~30 μm cell

Using the S_{front} value determined by *EQE*, we can see Table VI. 2 that the measured V_{oc} and *FF* values are lower than the ones predicted by simulation. Regarding V_{oc}, a possible origin for this deviation could be the RIE plasma etching used for silicon thinning. The plasma etching process may damage the Si crystal that degrades the substrate quality [7]. Focusing on *FF*, the big difference between its value and the *pFF* value indicates a high series resistance which is not included in the simulations (0.7 $\Omega \cdot cm^2$ are added in a lumped element to the series resistance in simulation).

VI. 6 Conclusions

In this chapter, a detailed fabrication method and characterization of thin c-Si samples and IBC solar cell is presented. The thinning/etching technique is firstly developed on silicon samples without devices at rear surface but a polyimide support layer, then a combined dry and wet etching is proposed. Based on the thinning technique, passivation of aluminum oxide on thin silicon samples is characterized under photoconductance measurement and optical performance of these samples is revealed for light wavelength ranging from 300 to 1200 nm. With the values of surface recombination velocity and optical absorptivity, a promising final device efficiency is expected referencing the simulation results shown in the previous chapter.

Under the same thinning technique, an IBC solar cell with thickness ~30 µm is fabricated. The front surface is textured by random pyramids and passivated by 90 nm aluminum oxide through ALD. 12.1 % efficiency is achieved and the front surface recombination velocity is deduced to be 1500 cm/s by comparing *EQE* with simulation results. Despite V_{oc} and *FF* values are lower than expected, the obtained result demonstrates that IBC technology developed for thick cells could be transferred to thin substrate based devices with promising efficiencies, giving a first approach of fabricating and characterizing IBC solar cells based on thin c-Si substrate in our research group.

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Chapter VII

Conclusions and future work

VII. 1 Conclusions

In this thesis, experiments and simulations have been carried out focused on developing and fabricating high efficient IBC solar cell based on thin c-Si substrates. Since wide areas are involved in this topic, several related aspects have been studied including innovative thin c-Si substrate fabrication method *Millefeuille* process, novel IBC solar cell structures combining laser doping and heterojunction technologies and thin IBC solar cell performance prediction through simulation concerning different doping and rear surface contact structures. Finally, as a first approach to fabrication of IBC c-Si solar cells in our research group, a 30 µm thick c-Si solar cell is fabricated by thinning down a finished device applying a silicon etching technique that combines dry and wet etching. The conclusions of all these activities are reported below.

Considering the *Millefeuille* process, based on the technological know-how the impact of both modulated profile and periodicity of silicon pores on the generated thin layer quality is explored and the results are visualized by SEM images. It is proved that the sinusoidal profile is more promising in bubble-free silicon layer production. Further, the solid-void transformation evolution during the high temperature annealing reveals the pore status at 35, 60 and 90 minutes, allowing a deeper understanding of the practical silicon atomic surface diffusion and the shape evolution. It should be mentioned that due to the difficulty for detaching the fabricated thin silicon substrates and time limitation, the solar cell processing on thin silicon substrate derived from this method will be considered in a future work.

In order to find a viable and promising device structure that can be used in case of thin silicon substrates, a hybrid p-type solar cell structure is reported. In this case, emitter is based on SHJ technology while the base contacts are created by laser processing Al_2O_3/SiC_x films. Special attention of the compatibility of both technologies has been paid in the proposed fabrication process. Firstly, the re-passivation of silicon heterojunction emitter region is evaluated and confirmed by depositing on the silicon surface after removing the aluminum oxide and silicon carbide layer stack needed for base laser doping process. Secondly, the contact quality of titanium and aluminum on ITO is evaluated due to the different metal contact properties of the ITO of the heterojunction stack and the homojunction point-like laser-doped base contact region. It is revealed

that titanium is a better option with a specific contact resistance of 1.1 mΩ·cm^2 on ITO. Finally, finished hybrid IBC solar cells with conversion efficiencies in the 18-19% range are reported. Next, following the same fabrication process, a more mature heterojunction layer stack is introduced in collaboration with INES. A nearly 0.5 $\%_{abs}$ efficiency increase is obtained by using a heterojunction layer stack with a better conductivity and, thus, a better fill factor. This work provides a new approach for achieving low-temperature high efficiency c-Si solar cell, as well as a novel pathway compatible to the fabrication of IBC devices based on thin c-Si substrate.

In parallel with experimental progress, the simulation on thin c-Si IBC solar cell is carried out for performance study and prediction. By employing 3D TCAD simulation tool, we forecast the efficiency potential of thin IBC c-Si solar cells involving two typical rear surface doping structures: fully- and locally-doped. The optical properties of random pyramids texturing on these devices is reproduced by complementary wafer ray tracer simulation while the electrical modelling is validated by a fabricated prototype IBC cell. Simulation results of fully-doped structure reveal an efficiency potential of 16-17 % for thin c-Si IBC solar cell based on substrates of 10-15 µm without changing the technology developed for thick ones. Front surface passivation requirements are relaxed for thinner cells with constant efficiencies up to $S_{front} \approx 100$ cm/s. Regarding the locally-doped structure, its performance is less tolerant to the degradation of front surface passivation. Additionally, the replacement of rear doped regions by a passivated surface results in an increase in V_{oc} which does not compensate the stronger decrease in J_{sc}. This reduction is related to stronger requirements in L_{eff} which is highly impacted by the electrical shading effect. Finally, we focused on the almost constant V_{oc} values for low S_{front} values despite the significant reduction in J_{sc} for thinner substrates. This effect is explained by the reduction of J_0, probably related to a change in the distribution of current that flow parallel to the rear surface. As a consequence, for the IBC structures under study V_{oc} will not be negatively impacted on thinner substrates. On the other hand, a thin IBC c-Si solar cell efficiency potential is explored through rear contacts pitch study and the highest conversion efficiency is expected when contact pitches are minimum in the range of study. This minimum pitch is considered in the range of 200-250 µm due to technological limitations in the laser alignment process.

Finally, efforts are paid to get a thin c-Si solar cell through thinning down an already finished device of thick substrate. A silicon etching process based on RIE and wet chemical etching is proposed. Different experiments demonstrate that the front surface can be successfully repassivated after etching process. Additionally, random pyramids are created on that surface and the optical response of thin c-Si substrates is measured revealing a potential photogenerated current in the range of 40 mA/cm^2 for 30 μm-thick substrates. Applying all these techniques to a final device, a 12.1 % efficiency is achieved and the front surface recombination velocity is deduced to be 1500 cm/s by comparing EQE with simulation results. However, a slightly lower solar cell performance is measured with V_{oc} and FF values lower than the simulation prediction. In any case, the obtained result demonstrates that IBC technology developed for thick cells could be transferred to thin substrate based devices with promising efficiencies, giving a first approach of fabricating, characterizing and improving the IBC solar cell based on thin c-Si substrate in our research group.

VII. 2 Future works

Due to time limitations, a solar cell starting from a thin c-Si substrate has not been fabricated. However, some current results are reported hereby giving a feasible strategy for achieving high efficient thin device. In particular, in Fig. VII.1 the proposed fabrication process is shown. As it can be seen, since the IBC structure is chosen for device processing, the thin c-Si substrate used is assumed to be attached onto an extra support layer, such as glass, for improving the sample operability without producing any inconvenience for rear surface device fabrication. Laser doping technique is employed for contacts formation after the p and n layers stack definition. Although the final device is not finished, some critical progress has been made indicating a promising future result.

Considering that the commercial available thin c-Si samples as well as the ones fabricated from *Millefeuille* process are n types, the silicon substrate used for thin IBC device processing design of this work is also n type. In detail, the p and n contacts formation follows the DopLa-IBC [1] technologies which have been successfully applied to thick c-Si wafers. As it can be seen, n type contact is formed by spot-like laser processed a-Si(n)/SiC_x stack which is deposited on the

whole rear surface, while the p type one is formed by spot-like laser doping through aluminium oxide layer that is previously deposited and patterned by sputtering with shadow mask [2]. For both contacts regions, a PECVD deposited 22 nm-thick intrinsic a-Si layer is located between doping layer stack and c-Si for a better passivation [3], as shown in Fig. 1(b). Regarding light absorption strategy, a method of texturing onto the support layer is preferred instead of processing directly on the c-Si front surface. In particular, PDMS foils that reproduce random pyramid texturization have been successfully developed in our research group following reference [4]. These foils can be placed on top of the glass once the device fabrication is finished. As a consequence, front surface of the c-Si substrate could be maintained flat which helps in its surface passivation and adhesion on the glass by means of a transparent epoxy. In fact, thin c-Si substrates of 10, 20 and 40 μm have been already passivated and successfully glued onto glass using epoxy EPO-TEK 302-3M.

Among all the experimental steps revealed in Fig. VII. 1, the one that should be developed is the p-type contact formation. On one hand, the aluminium oxide (AlO_x) layer stack for p-region definition is deposited by sputtering and, thus, the deposition conditions should be explored. The traditional Al_2O_3 layer deposition equipment is ALD, but it is not convenient for incorporating shadow mask for defining p type region. Additionally, notice that the n type layer stack is covered all the device area including the p type region. Both phosphorus and aluminium atoms will be mixed and diffused inside c-Si substrate during laser processing. However, the idea is that the higher quantity of aluminium atoms and the closer position of the AlO_x layer respect to the c-Si surface could lead to a functional net p-type doping. A similar approach has been already demonstrated in [1] by our research group. In any case, the n-type layer stack impact on p-type contact formation should be studied by diode fabrication. First experiments without a spacer between the AlO_x and the n-type stack led to poor junction formation. Thus, currently we propose a separation 30 nm SiO_2 layer deposited also by sputtering in-between the p and n layer stack to limit the n type layer impact.

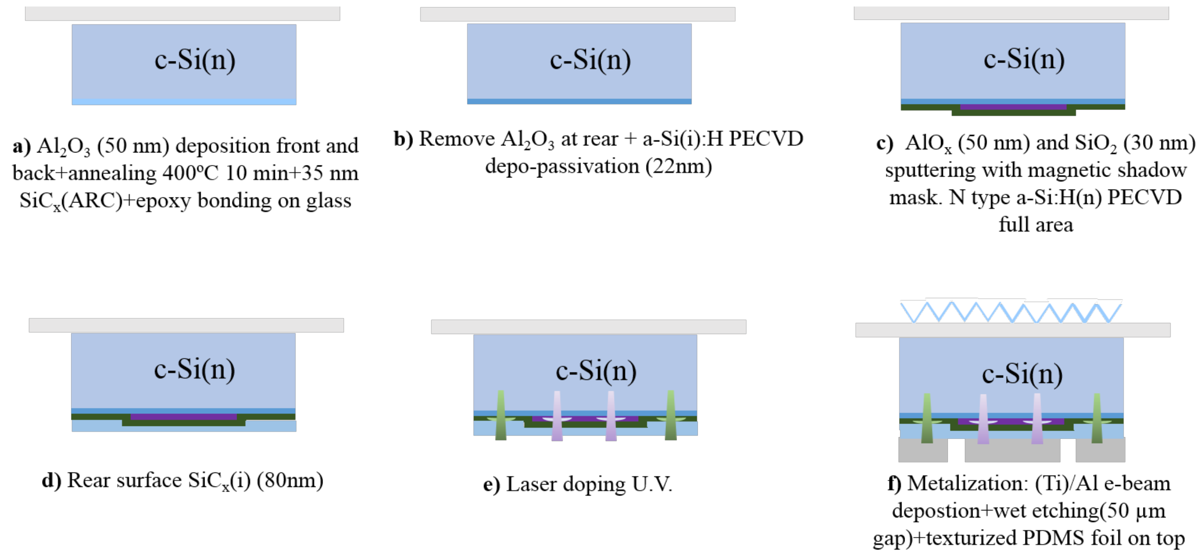

Fig. VII. 1 fabrication procedure of thin IBC c-Si solar cell

Regarding AlO_x deposition by sputtering, according to the reported results in [2], different modes of reactive sputtering deposited aluminium oxide can happen depending on the Ar/O_2 proportion leading to that the deposited layer performs either as metal or dielectric layer. Thus a reasonable deposition condition for approaching a similar material composition as the one from ALD should be approached. Firstly, the RF power is fixed to be 110W and the Ar is 24 sccm considering the 2 inch-size aluminium target and the deposition efficiency. Then the O_2, as the reactive element with aluminium is altered by 0.3, 0.5, 0.8 and 1.0 sccm. A 1×10^{-5} mbar chamber vacuum is reached prior to the deposition and the duration is set to be 30 minutes for all cases. Thickness as well as the refractive index is measured by ellipsometry at λ= 632 nm. The results of these four condition are summarized in the Table VII. 1.

Table VII. 1 AlO_x sputtering deposition condition

Gas flow Ar/O_2 (sccm)	Layer thickness (nm)	Measured refraction index @ 632nm
24/1	No deposition	N/A
24/0.8	≈53	1.66
24/0.5	≈65	1.66
24/0.3	Metal-like layer	N/A

In order to compare the material composition with the one from ALD, as a first approach we can compare the measured refractive index through spectroscopic ellipsometry, as shown in Fig. VII. 2. Condition with O_2 flow of 0.8 sccm shows very similar refractive index as the ALD deposited layer indicating that this deposition conditions could lead to viable layers. These layers have been also deposited through shadow mask with similar properties. SEM images reveal that AlO_x thickness decreases from the nominal value to no deposition in about 20 µm indicating that the mask is able to prevent deposition under it. This means that finger width in the range of 200 µm should be enough to keep a reasonable region free of AlO_x where the n-type contact could be created.

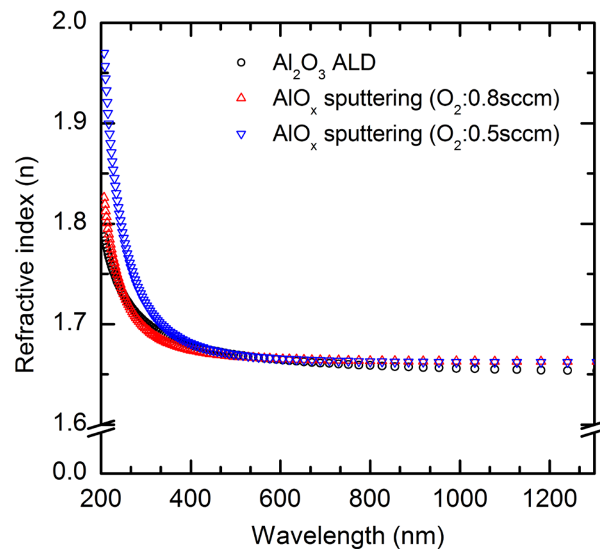

Fig. VII. 2 Refractive index measured by spectroscopic ellipsometry

As a summary, the p/n junction formation from the proposed film stack is the main point to be developed in the next future. Once we have this technology, we will be able to combine it with the rest of the key steps that have been already demonstrated: n-type contact formation, front surface passivation, adhesion of thin c-Si substrates on glass and PDMS foils to improve optical properties. It should be mentioned that metal contact is planned to be defined by photolithography as in thick substrates. However, preliminary results show that laser ablation of photoresist is also possible, avoiding any lithography step in the whole fabrication process.

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