HOKKAIDO UNIVERSITY

Title	Growth of InGaAs nanowires on Ge(111) by selective-area metal-organic vapor-phase epitaxy
Author(s)	Yoshida, Akinobu; Tomioka, Katsuhiro; Ishizaka, Fumiya; Motohisa, Junichi
Citation	Journal of Crystal Growth, 464, 75-79 https://doi.org/10.1016/j.jcrysgro.2016.10.083
Issue Date	2017-04-15
Doc URL	http://hdl.handle.net/2115/73581
Rights	© 2016, Elsevier. Licensed under the Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International http://creativecommons.org/licenses/by-nc-nd/4.0/
Rights(URL)	http://creativecommons.org/licenses/by-nc-nd/4.0/
Type	article (author version)
File Information	Manuscript_revised_yoshida.pdf

Growth of InGaAs nanowires on Ge(111) by selective-area metal-organic vapor-phase epitaxy

Akinobu Yoshida[1,2*], Katsuhiro Tomioka[1,2,3], Fumiya Ishizaka [1,2], Junichi Motohisa[1,2]

[1]Graduate School of Information Science and Technology, Hokkaido University, North 14 West 9, Sapporo 060-0814, Japan

[2] Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, North 13 West 8, Sapporo 060-8628, Japan

[3]Japan Science and Technology Agency–PRESTO, Kawaguchi, Saitama 332-0012, Japan

* Corresponding Author. Tel.: +81 11 706 7172; fax: +81 11 716 6004

E-mail address: yoshida@rciqe.hokudai.ac.jp (A. Yoshida)

Abstract

We report the growth of InGaAs nanowires (NWs) on Ge(111) substrates using selective-area metal-organic vapor-phase epitaxy (SA-MOVPE) for novel InGaAs/Ge hybrid complementary metal-oxide-semiconductor (CMOS) applications. Ge(111) substrates with periodic arrays of mask opening were prepared, and InGaAs was

selectively grown on the opening region of Ge(111). A uniform array of InGaAs NWs with a diameter around 100 nm was successfully grown using appropriate preparation of the initial surfaces with an AsH_3 thermal treatment and flow-rate modulation epitaxy (FME). We found that optimizing partial pressure of AsH_3 and the number of FME cycles improved the yield of vertical InGaAs NWs. Line-scan profile analysis of energy dispersive X-ray (EDX) spectrometry showed that the In composition in the InGaAs NW was almost constant from the bottom to the top. Transmission electron microscope (TEM) analysis revealed that the interface between InGaAs NW and Ge had misfit dislocations, but their distance was longer than that expected from the difference in their lattice constants.

Key words

A1. Nanostructures, A3. Metalorganic vapor phase epitaxy, A3. Selective epitaxy, B1. Nanomaterials, B2. Semiconducting germanium, B2. Semiconducting III-V materials

1. Introduction

Miniaturization of Si-based field-effect transistors (FETs) is being limited by enhanced short-channel effect and leakage current. Thus, novel technologies such as

multi-gate structures and non-Si channel materials are required for overcoming these issues [1-7]. In this study, we focus on III-V compound semiconductors and Ge for channel materials of the FETs because of the small effective mass of their carriers, or large carrier mobility. Co-integration of III-V/Ge channels is needed to be used for the high-mobility channel materials of FETs, thereby enabling the fabrication of high-performance and low-power integrated complementary metal-oxide-semiconductor (CMOS) circuits. However serious issues remain in integrating III-V materials with Ge, for instance, mismatches in the lattice constant, polarity, and carrier mobility, and the latter is the most critical for practical CMOS applications. For example, when the electron mobility of InGaAs is 12000 cm^2/Vs and the hole mobility of Ge is 1200 cm^2/Vs, the carrier mobility mismatch is 10 times, so the channel width of a Ge p-channel MOSFET must be 10 times wider than that of an InGaAs n-channel MOSFET to compensate current level mismatch. Thus, native integration is not very effective, and rational integration is required.

In this study, we report on direct integration of vertically aligned InGaAs nanowires (NWs) on planar Ge(111) substrates using selective-area metal-organic vapor phase epitaxy (SA-MOVPE) ~~to match~~ toward a matching current levels of III-V n-MOSFETs and Ge p-MOSFETs via hybrid integration of NWs and planar FETs.

Vertical surrounding-gate transistors (SGTs) using NWs can reduce the surface area occupied by FETs by about one quarter compared with the area occupied by planar Si-MOSFETs [8, 9], and their extremely small diameter allows current level matching in narrow-width planar FETs. Furthermore, direct integration of the III-V NWs using SA-MOVPE would suppress the ~~formation of misfit dislocations~~ lattice relaxation at the III-V/Ge interface originating from lattice mismatch [10]. Among III-V materials, InGaAs is an especially promising channel materials because of its high electron mobility. Furthermore, we expect good electrostatic gate control in InGaAs for an In composition of about 70-80% due to the small energy difference between the conduction band edge and the Fermi level stabilization energy and small interface charges around them [11]. Thus, FETs based on the InGaAs channels are expected to outperform their InAs counterpart. In this study, we investigated the SA-MOVPE of InGaAs NWs with an emphasis on the preparation of initial surfaces before InGaAs NW growth, which is important to overcome the polarity mismatch, and to achieve vertical alignment of InGaAs NWs on Ge. We performed AsH_3 treatment and flow-rate modulation epitaxy (FME) for the special care to form (111)B polarity. We expect AsH_3 treatment replaces the outermost Ge with As and forms As-incorporated Ge^{3+} surfaces. In FME growth, or by supplying group-III materials without As, In/Ga atoms are

expected to terminate not only As-incorporated Ge^{3+} surfaces with, but also terminate

Ge surface without As incorporation and to form group-III terminated Ge^{+} surfaces. The

advantage of FME is also in the ability of low temperature growth, as demonstrated in

Ref. 16. Low-temperature growth in FME mode thus expected to promote nucleation

without sacrificing the crystal quality in FME. We will discuss about FME in detail at

chapter 3.   We describe the results of energy dispersive X-ray (EDX) spectrometry and

transmission electron microscopy (TEM) for compositional and structural analysis.

2. Experimental procedure

The growth process of NWs started with the preparation of Ge(111) substrates

partially masked with SiN. After a 22-nm-thick SiN film was deposited on Ge(111)

substrates using plasma enhanced chemical vapor deposition (PECVD) [Fig. 1(a)], the

mask opening was defined using electron-beam lithography and wet chemical etching

with buffered hydrofluoric acid (BHF) [Fig. 1(b)]. The mask opening with diameter d_0

was formed periodically in a triangular lattice with pitch a. Then, NWs were formed

using a horizontal MOVPE system at a working pressure of 0.1 atm. Trimethylgallium

(TMGa) and trimethylindium (TMIn) and 5% arsine (AsH_3) in hydrogen were used as

the source precursors for MOVPE growth [Fig. 1(c)].

The following procedures were used [12, 13] to form (111)B polarity on non-polar Ge(111) surfaces. After native oxide was removed on Ge surfaces by thermal cleaning in a hydrogen atmosphere [(i) in Fig. 1(d)] [14], AsH_3 was supplied to replace the outermost Ge with As [(ii) in Fig. 1(d)]. Note that the formation of a flat surface is important with H_2 annealing. However, the optimal temperature window for the annealing remains unclear. Although we set the temperature to 550°C, temperatures below 500°C were assumed to be enough to obtain a smooth surface because the decomposition of Ge surface occurs at 200-300°C [15]. Then, InGaAs layers were grown, first using flow-rate modulation epitaxy (FME) [(iii) in Fig. 1(d)] [16], that is, by supplying TMIn/TMGa, and AsH_3 alternately with hydrogen intervals, followed by conventional MOVPE growth [(iv) in Fig. 1(d)]. The number of FME cycles was 7 to 30. The growth temperature was 670°C, and the partial pressure of TMGa and TMIn was 5.68×10^{-7} atm and 9.74×10^{-7} atm, respectively, and the composition of TMIn in the vapor phase was 63%.

3. Results and discussions

We grew InGaAs on Ge without AsH_3 surface treatment and FME cycles shown in Fig. 2(a). Figure 2(b) shows the results of the growth; three types of InGaAs, that is,

vertical hexagonal pillars [(i) in Fig. 2(b)], inclined NWs [(ii) in Fig. 2(b)], and hillocks [(iii) in Fig. 2(b)], can be seen to have formed. Vertical hexagonal pillars appeared on the (111)B-like polar surfaces (more specifically, As-incorporated Ge^{3+} surfaces [14]) of the openings. However, inclined NWs were formed on the (111)A-polar ones, and hillocks appeared due to the mixture of (111)B/A surfaces. Similar inclined NWs were observed in the case of vapor-liquid-solid grown InP NWs on Ge(111) [17]. The formation of multiple nuclei at the early stage and their coalescence in the subsequent growth resulted in hillocks that were unlike those with NWs. In any case, polarity mismatch and imperfect formation of (111)B-like polar surfaces deteriorated the growth direction and morphology.

Figure 3 shows the results of growth with AsH_3 surface treatment and FME. The opening diameter d_0 was 100 nm, the pitch a was 1000 nm, and the number of FME cycles was 30. The formation of inclined NWs was suppressed by introducing the AsH_3 surface treatment and FME, indicating that a (111)B-polar surface was formed on Ge(111). That is, a substitution reaction of outermost Ge atoms with As atoms occurred to form an As-incorporated Ge^{3+} surface, or In/Ga adsorption on Ge occurred to form an In/Ga-terminated Ge^+ surface. As a result, InGaAs in the NW shape was grown vertically. However, lateral overgrowth structures as well as hillocks also appeared.

Both the lateral overgrowth structure and hillocks had a much larger diameter than that

of the mask openings, but the former had vertical {-110} facet sidewalls, while the

hillocks did not. Thus, the hillocks were formed due to the mixture of the (111)A and

(111)B polar surfaces, similar to the case of Fig. 2(b). The mechanism of the lateral

overgrowth, which was thought to take place with all the formation of the (111)B

surface, is discussed later. Figure 3(c) shows the percentage of the NWs, lateral

overgrowth, and hillocks at an AsH_3 partial pressure [AsH_3] of 5×10^{-4} atm and $1.25 \times$

10^{-4} atm. Because the lateral over grown structures were aligned along the vertical

<111>B axis, the percentage of the (111)B-polar was approximately 74% by summing

up with the NW growth at [AsH_3] = 1.25×10^{-4} atm. At higher [AsH_3], the InGaAs grew

laterally rather than vertically, and some of the grown InGaAs exhibited short and thick

NW shape, or hillock-like shape with unclear facets. The origin of these hillocks was

also thought to be a mixture of (111)A and (111)B surfaces or the formation of multiple

nuclei at an early growth stage and their coalescence, as aforementioned.

Next, we characterized the effect of the number of cycles on the FME to enhance

the yield of the NW growth, and the results are summarized in Fig. 4. Fewer FME

cycles clearly resulted in an improved yield of NWs. Figure 4 (d) shows the percentage

of the growth of the NWs, lateral over growth, and hillocks for 30, 15, and 7 FME

cycles with d_0 of 100 nm and a of 1000 nm. The yield of NW growth was over 90%

when the number of FME cycles was 7. In addition, the diameter of the grown NWs

became closer to the d_0 as the FME cycles decreased, as shown in Fig. 5. To explain

these results, the influence of excess FME growth was considered based on the model

shown in Fig. 4(e). In this FME growth, the amount of In/Ga supply for 1 FME cycles

was estimated to correspond to about 1.5-2 nm by calculating the growth rate of NWs.

Thus, too many FME cycles resulted in the InGaAs layers becoming thicker than the

mask thickness (~ 22 nm). This gave rise to the overfilling of InGaAs at the opening,

and InGaAs grew laterally over the mask in the FME growth, resulting in thick InGaAs

NWs or lateral overgrowth structures in the subsequent InGaAs growth. Fewer FME

cycles reduced the overfilling and lateral overgrowth of InGaAs, and if the number of

FME cycles was appropriate, the FME layer could be thinner than that of an SiN-mask,

and lateral over growth was suppressed. Therefore, we conclude that the formation of

the (111)B-polar surfaces and the optimization of an initial FME layer were critical for

integrating the vertical InGaAs NWs on Ge.

Next, we characterized the crystal structure of an InGaAs NW, the diameter and

height of which were about 150 and 700 nm using EDX and TEM, respectively. The

results are summarized in Fig. 6. In this case, the NWs were grown with the

FME-cycles of 30. Figure 6(a) shows a TEM image of a whole NW, and line 1 (A-B) and line 2 (A'-B') show the position of the EDX line-scan analysis for profiles shown in Fig. 6(b) and (c), respectively. The EDX line-scan profile revealed the In composition in the InGaAs NW was about 80% and was almost constant throughout the NW except at its bottom [The distance was 70-150 nm in Fig. 6(b)]. At part of the bottom, the In composition was about 64%, close to that in the vapor phase. This composition difference was assumed to be the FME. As aforementioned, excess numbers of FME cycles resulted in overflow growth on the SiN mask [see panel (i) in Fig. 4(e)], and the behavior can be seen in Fig. 6(a). Thus, part of the NW-bottom was dominantly grown by the overflow growth of the FME, and the In-content of the FME grown-layer was assumed to follow that of the vapor phase. However, the In composition in the InGaAs NW was larger than that of the composition of the In precursor (63%) in the vapor phase. This suggests that the surface diffusion length of the In atoms was longer than that of Ga atoms, and In incorporation was enhanced in the NW growth. TEM images showed that InGaAs NWs had no threading dislocations. Instead, periodic misfit dislocations were formed at the InGaAs/Ge heterointerface, as shown in a blown-up image of Fig. 6(d). The period of misfit dislocation was about 8.95 nm longer than the calculated value (4.37 nm) based on their lattice mismatch (5.3%). In selective-area

growth of InGaAs NW on Ge, lattice relaxation was suppressed more than the case of Ref. 13 (InAs NW on Ge). It is noted that the diameter of analyzed NW was different between InAs and InGaAs. Similar results were obtained compared with Ref. 4 (InGaAs NW on Si). From these results, the suppression of lattice relaxation depended on the lattice mismatch and the effect became stronger in the case of small lattice mismatch. This clearly indicates that the nanometer-scale footprint of NWs allows lateral deformation due to lattice mismatch [10]. A further reduction in the NW diameter would suppress the misfit dislocation and enable coherent growth [10]. The novel integration of the InGaAs NWs with Ge would open a new approach for tandem solar cells as well as the hybrid InGaAs NW/Ge CMOS.

4. Summary

We achieved integration of the vertical InGaAs NWs on Ge(111) substrates using selective-area MOVPE. We found that the percentage of vertical NWs was improved by changing the AsH_3 treatment temperature, partial pressure of AsH_3, and the number of FME cycles. Thinning of the FME layer while forming (111)B-polar was critical to align vertical InGaAs NWs on Ge. We evaluated the composition of InGaAs NWs and conducted an analysis of the InGaAs/Ge heterointerface. A further reduction in the mask

opening and NW diameter should enable dislocation-free interfaces for device

applications.

Acknowledgements

References

[1]   S. Takagi, R. Zhang, J. Suh, S. -H. Kim, M. Yokoyama, K. Nishi, M. Takenaka,

III–V/Ge channel MOS device technologies in nano CMOS era, Jpn. J. Appl.

Phys. **54** (2015) 06FA01.

[2]   I. Ferrain, A. A. Colinge, J -P. Colinge, Multigate transistors as the future of

classical metal-oxide semiconductor field-effect transistors, Nature **479** (2011)

310.

[3]   J. A. del. Alamo, Nanometre-scale electronics with III-V compound

semiconductors, Nature **479** (2011) 317.

[4]   K. Tomioka, M. Yoshimura, T. Fukui, A III-V nanowire channel on silicon for

high-performance vertical transistors, Nature **488** (2012) 189.

[5]   M. J. H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, T.M Shen, C.C. Wu, R.

Oxland, K. Bhuwalka, M. Holland, T. L. Lee, C. Wann, C. H. Hsieh, B. H. Lee,

K. M. Yin, Z. Q. Wu, M. Passlack, C. H. Diaz, Demonstration of scaled Ge

p-channel FinFETs integrated on Si, IEDM Tech. Dig. **521** (2012) 23.5.1.

[6]   K. J. Kuhn, Considerations for ultimate CMOS scaling, IEEE Trans. Elec. Dev.

59 (2012) 1813.

[7]   R. Pillarisetty, Academic and industry research progress in germanium

nanodevices, Nature **479** (2011) 324.

[8]   H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, F.

Masuoka, Impact of surrounding gate transistor (SGT) for ultra-high-density

LSI's, IEEE Trans. Elec. Dev. **3** (1991) 573.

[9]   D. Yakimets, G. Eneman, P. Schuddinck, T. H. Bao, M. G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. V. Thean, K. D. Meyer, Vertical GAAFETs for the ultimate CMOS scaling, IEEE Trans. Elec. Dev. **62** (2015) 1433.

[10]   F. Glas, Critical dimensions for the plastic relaxation of strained axial heterostructures in free-standing nanowires, Phys. Rev. B **74** (2006) 121302-1.

[11]   H. H. Wieder, Surface and interface barriers of $In_xGa_{1-x}As$ binary and ternary alloys, J. Vac. Sci. Technol. B 21 (2003) 1915.

[12]   K. Tomioka, J. Motohisa, S. Hara, T. Fukui, Control of InAs nanowire growth directions on Si, Nano Lett. **8** (2008) 3475.

[13]   K. Tomioka, F. Ishizaka, T. Fukui, Selective-area growth of InAs nanowires on Ge and vertical transistor application, Nano Lett. **15** (2015) 7253.

[14]   T. Nishimura, S. Kabuyanagi, W. Zhang, C. H. Lee, T. Yajima, K. Nagao, A. Toriumi, Atomically flat planarization of Ge(100), (110), and (111) surfaces in H_2 annealing, Appl. Phys. Exp. **7** (2014) 051301-1.

[15]   J. R. Arthur, Surface structure and surface migration of germanium by field

emission microscopy, J. Phys. Chem. Solids, **25** (1964) 583.

[16]   N. Kobayashi, T. Makimoto, Y. Horikoshi, Flow-rate modulation epitaxy of

GaAs, Jpn. J. Appl. Phys. **24** (1985) L962.

[17]   E. P. A. M. Bakkers, J. A. V. Dam, S. D. Franceschi, L. P. Kouwenhoven, M.

Kaiser, M. Verheijen, H. Wondergem, P. V. D. Sluis, Epitaxy growth of InP
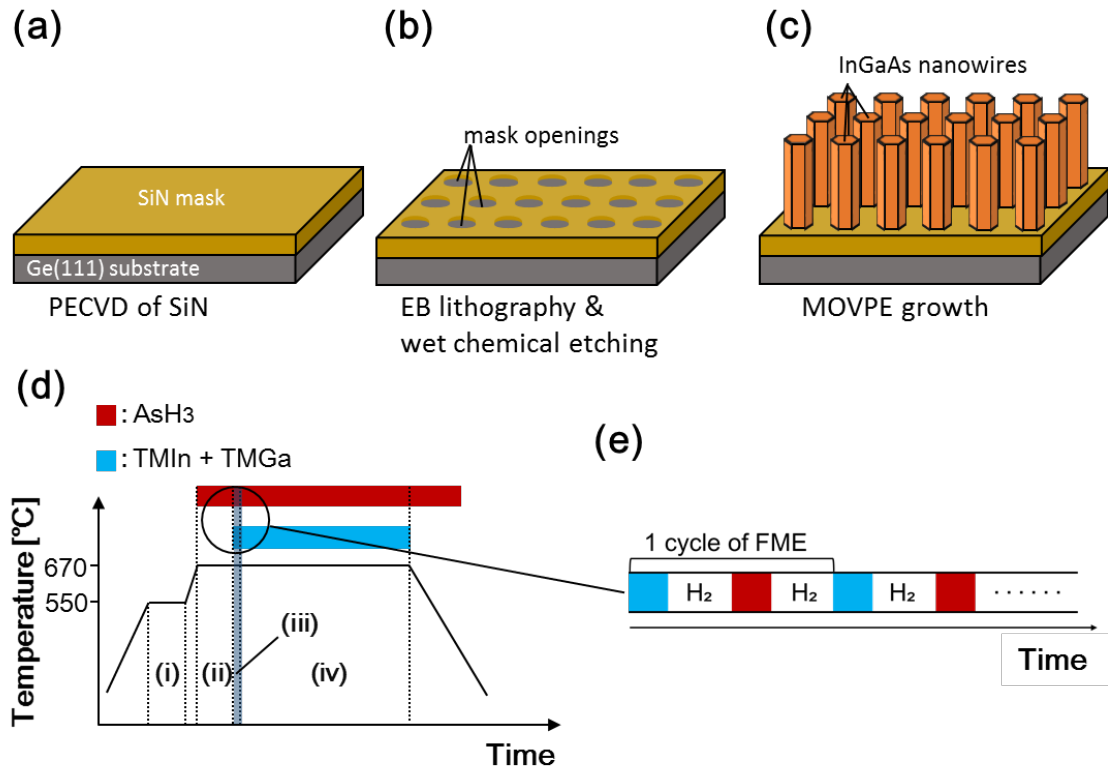
nanowires on germanium, Nature Mat, **3** (2004) 769.

Figures

Fig. 1. Schematic diagram of SA-MOVPE : (a) Deposition of 22-nm-thick SiN film on Ge(111) substrate by PECVD, (b) definition of opening patterns using electron-beam lithography and wet chemical etching, (c) MOVPE growth of InGaAs NWs, and (d) MOVPE growth sequence of InGaAs nanowires. (i) Removal of native oxide on Ge surface by thermal cleaning in hydrogen atmosphere. (ii) AsH_3 surface treatment to replace outermost Ge with As. (iii) FME growth (iv) Growth of InGaAs NWs. (e) The duration of each pulse for FME.
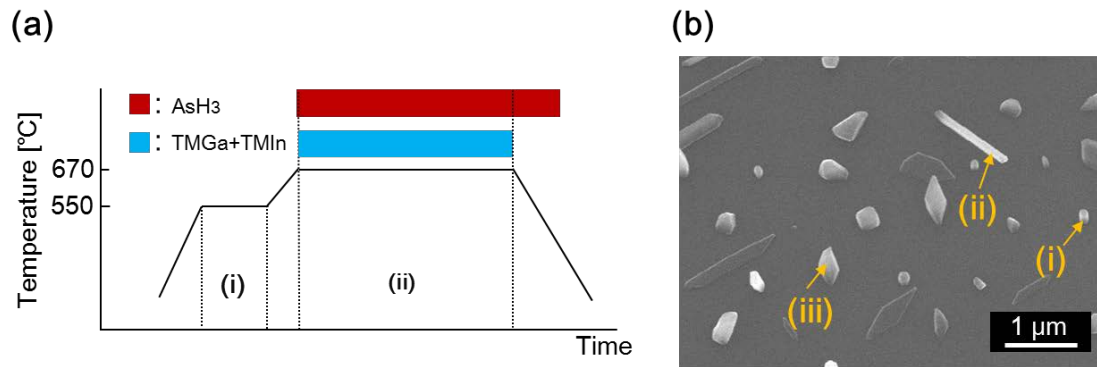
Fig. 2. Growth of InGaAs NWs on Ge(111) by original sequence : (a) Growth sequence

(b) 30°-tilted SEM image : (i) vertical hexagonal pillars, (ii) inclined NWs, and (iii)
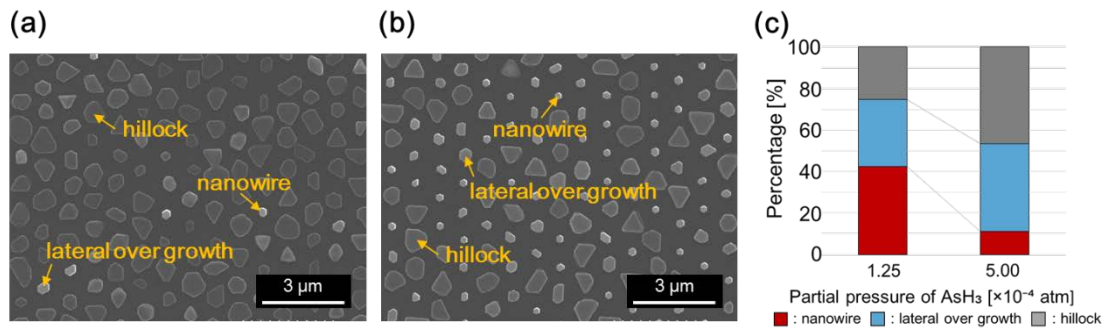
hillocks.

Fig. 3. Dependence on the partial AsH_3 pressure : (a) SEM image at $[AsH_3]$ of 1.25×10^{-4} atm. (b) SEM image at $[AsH_3]$ of 5.00×10^{-4} atm. (c) Percentage of nanowire, lateral over growth, and hillock at $[AsH_3]$ of 1.25×10^{-4} atm and 5.00×10^{-4} atm.
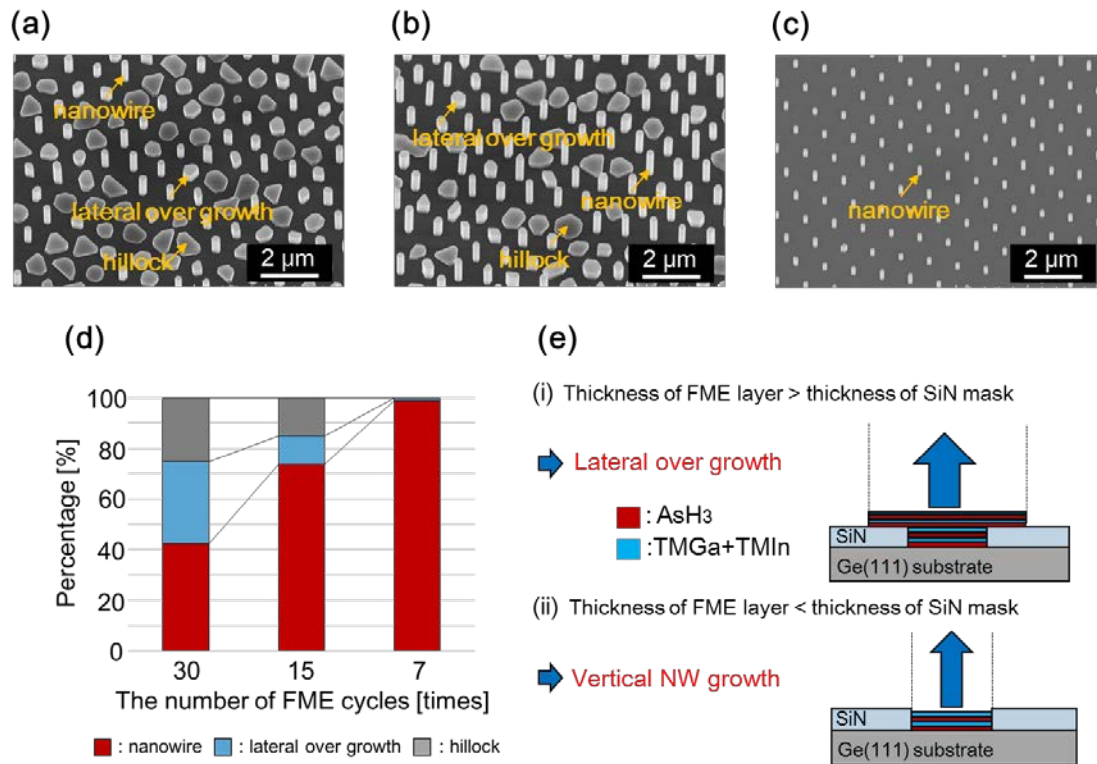
Fig. 4. Dependence on the number of FME cycles : (a) SEM image at 30 FME cycles. (b) SEM image at 15 FME cycles. (c) SEM image at 7 FME cycles. (d) Percentage of nanowire, lateral over growth, and hillock at 30, 15, and 7 FME cycles. (e) Schematic images of relationship between thickness of FME layer and that of SiN mask.
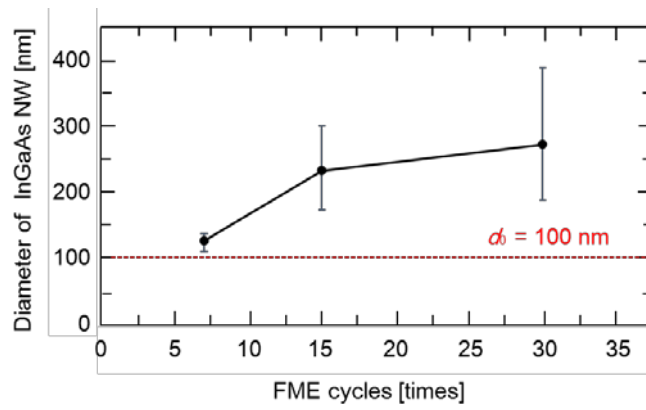
Fig. 5. Diameter of grown InGaAs NW as a function of FME cycles. d_0 is opening
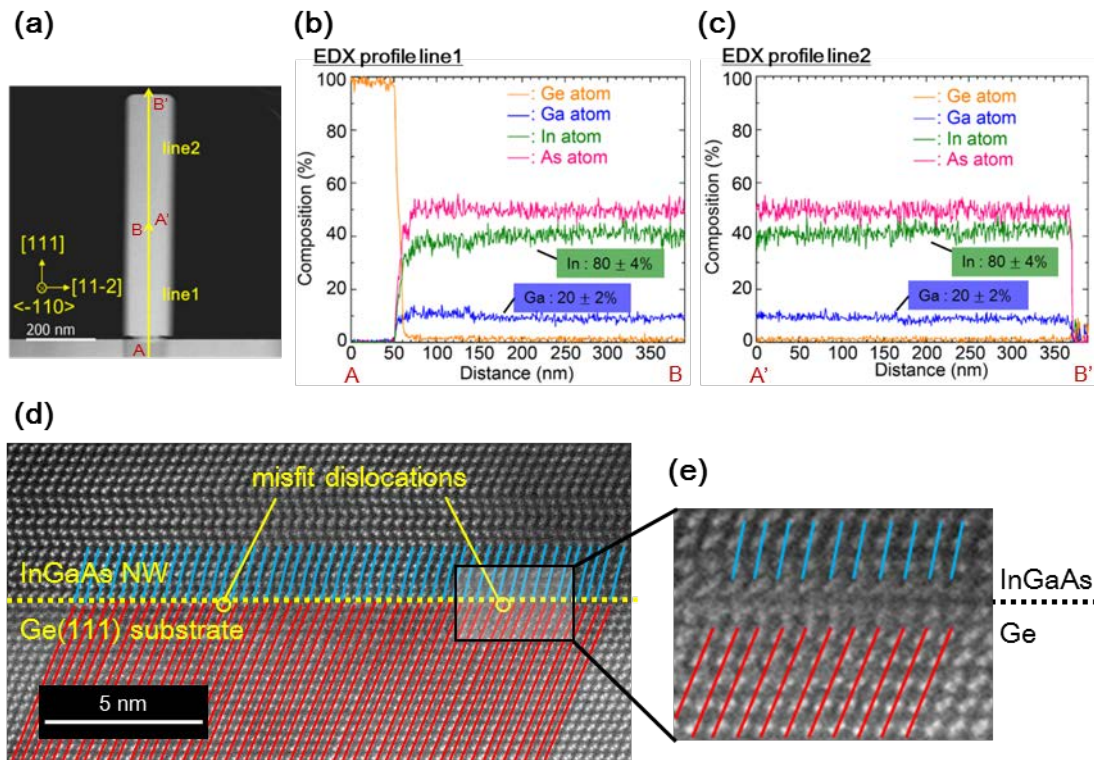
diameter, 100 nm.

Fig. 6. EDX line-scan profile and TEM image : (a) HAADF-TEM image of InGaAs nanowire. In this case, the NWs were grown with the FME-cycles of 30. (b) EDX from Ge(111) substrate to the bottom of InGaAs NW and (c) from the bottom to top of InGaAs NW. (d) HAADF-TEM image of heterointerface between InGaAs and Ge(111). The red lines depict (111) lattice planes of Ge, and the blue lines are those of InGaAs. (e) Magnified TEM micrograph of InGaAs/Ge heterointerface.