Radiation Hardness Comparison of CMOS Image Sensor Technologies at High Total Ionizing Dose Levels

S. Rizzolo, V. Goiffon, F. Corbière, R. Molina, A. Chabane, S. Girard, P. Paillet, P. Magnan, A. Boukenter, T. Allanche, C. Muller, C. Monsanglant Louvet, M. Osmond, H. Desjonqueres, J-R Macé, P. Burnichon, J-P Baudu, S. Plumeri

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OPTSYS Smart Protected Vision
IRSN INSTITUT DE RADIOPROTECTION ET DE SÛRETÉ NUCLÉAIRE
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INVESTISSEMENTS D'AVENIR

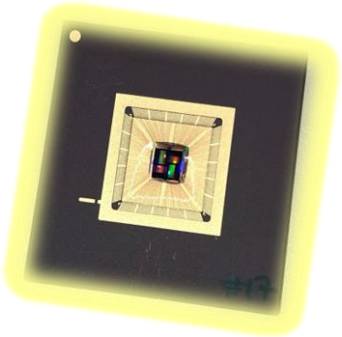
Context and motivation

CAMRAD project looks to develop and test under real conditions a high-performance imaging system:

- Characterization and monitoring of **nuclear wastes**
- Maintenance and instrumentation of **nuclear facilities**

Characteristics of the prototype:

- CMOS based color camera
- High resolution
- Compact design
- Radiation hardness at TID > 1 MGy(SiO_2)



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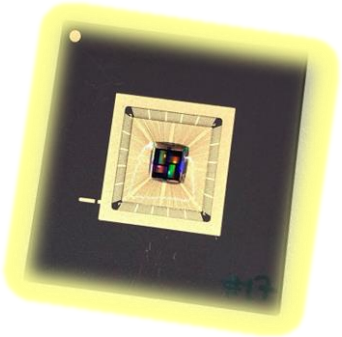
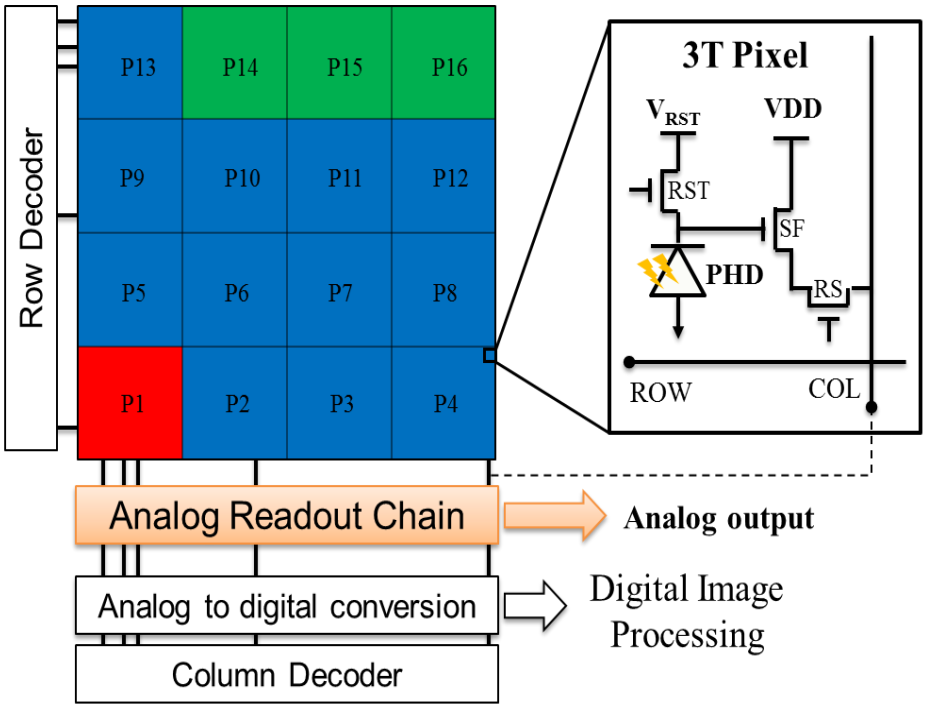


Exploration study on lab test chips to identify the best candidate for the final prototype

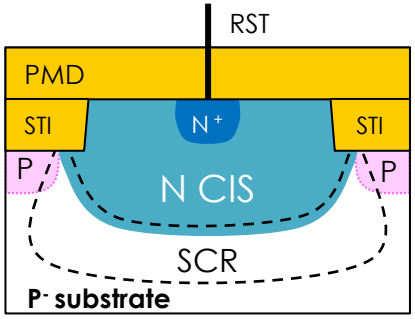
CAMRAD investigated CMOS Image Sensors



- ❑ TID up to 1MGy(SiO_2)
- ❑ 4 CMOS Image Sensors designed at ISAE-SUPAERO
- ❑ 3 180 nm CIS processes
- ❑2 readout chain architectures
  - Mixed 3.3 V and 1.8 V MOSFETs
  - Full 1.8 V MOSFETs
- ❑ 16 pixel designs
  - Standard 3T photodiode
  - Partially Pinned 3T photodiode
  - Radiation hardened by design photodiodes

Overview on the standard CIS photodiodes

Standard 3T Photodiode



- Widely evaluated under irradiation.
- STI positive trapped charges lead to a short circuits between pixels
- Change of the photodiode capacitance

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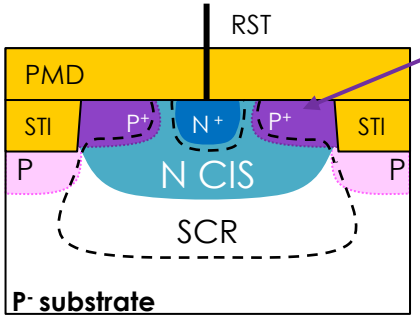
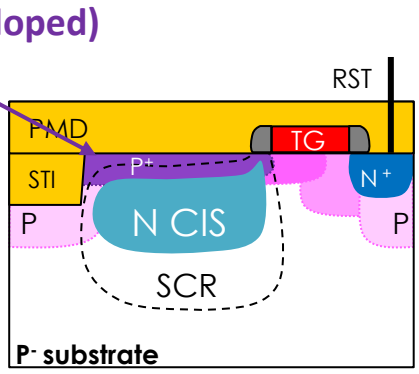
Partially Pinned Photodiode



- Never investigated under irradiation
- P+ implant to cover the N region
- Prevent the contact between the depletion region and the oxides

Pinned Photodiode



- PPD suffers from severe degradation due to TID
  - Charge transfer degradation
  - dark current increase
- Trapped charges in the PMD and in the spacers.

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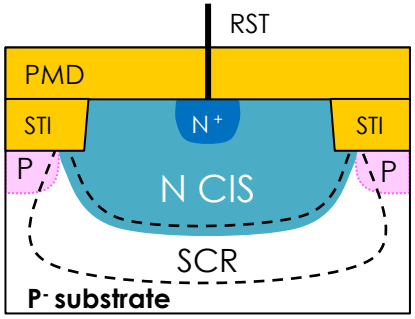

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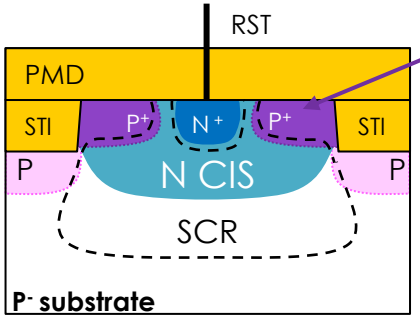

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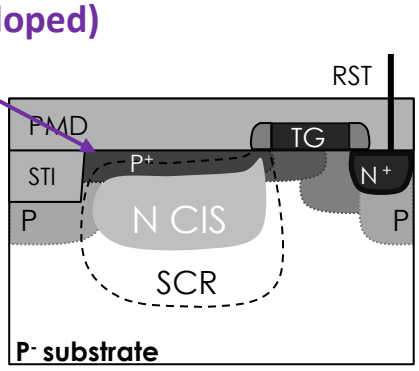

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CAMRAD Project: Studied photodiode structures

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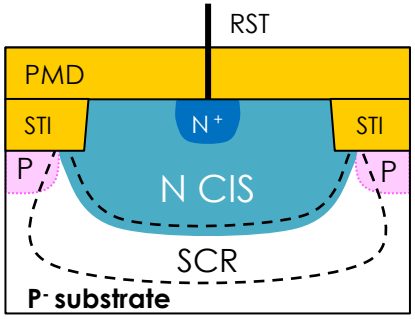

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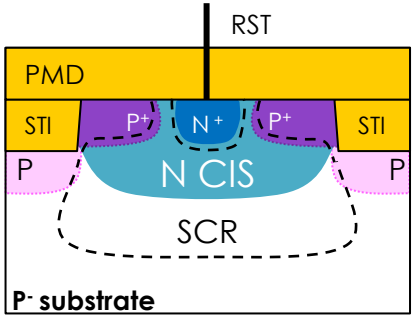

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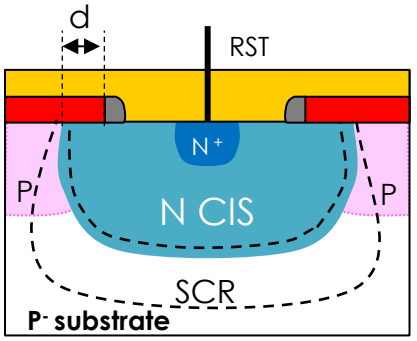
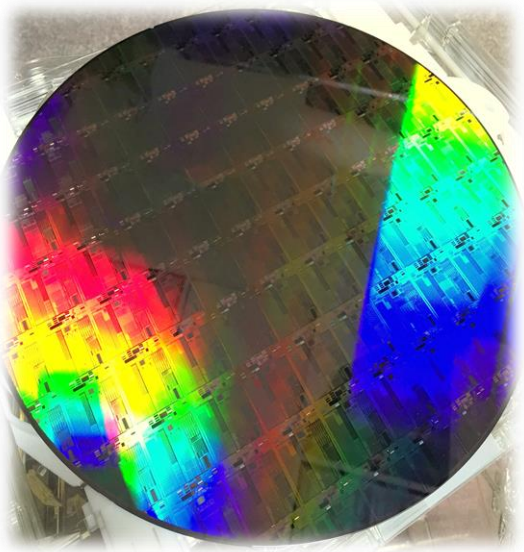


1. Study the influence of the manufacturing process on the CIS radiation hardness
2. Investigate the radiation effects in different photodiodes design and radiation hardened by design solutions

CAMRAD investigated CMOS Image Sensors



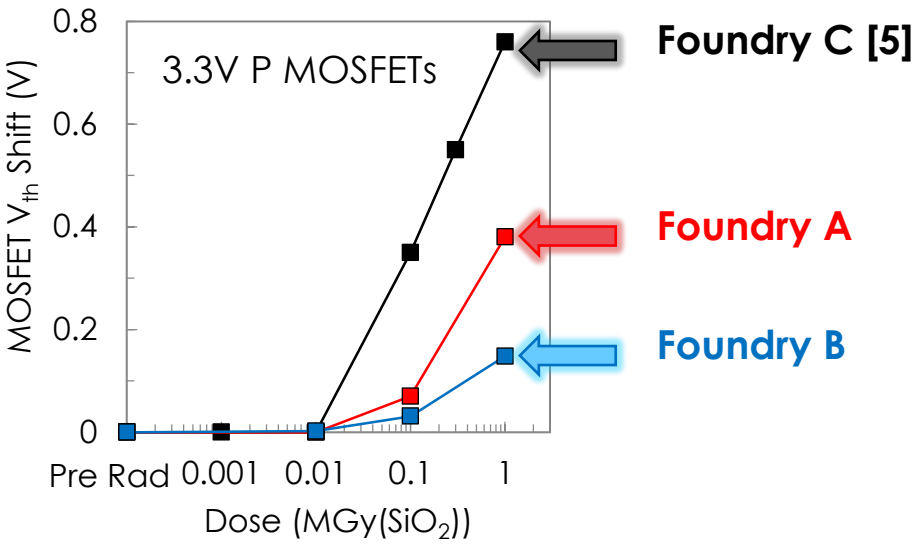
- ❑ TID up to 1MGy(SiO_2)
- ❑ 4 CMOS Image Sensors
- ❑ 3 180 nm CIS processes
- ❑ 2 readout chain architectures
  - Mixed 3.3 V and 1.8 V MOSFETs
  - Full 1.8 V MOSFETs

1. Study the influence of the manufacturing process on the CIS radiation hardness

Readout chain degradation at TID up to 100 Mrad

- Manufacturing process impacts the radiation hardness of the readout chain:

→**TID MOSFETs V_{th} shift depends on the technology**



[5] V. Goiffon, IEEE NSREC 2017, New Orleans, LA

Readout chain degradation at TID up to 100 Mrad

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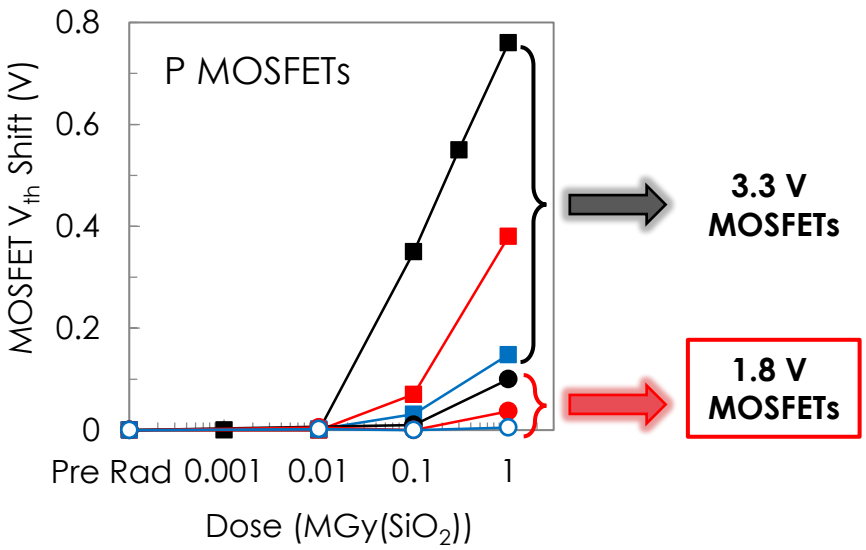
- 1.8 V MOSFETs exhibit the lower threshold voltage shift



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- Manufacturing process impacts the radiation hardness of the readout chain:

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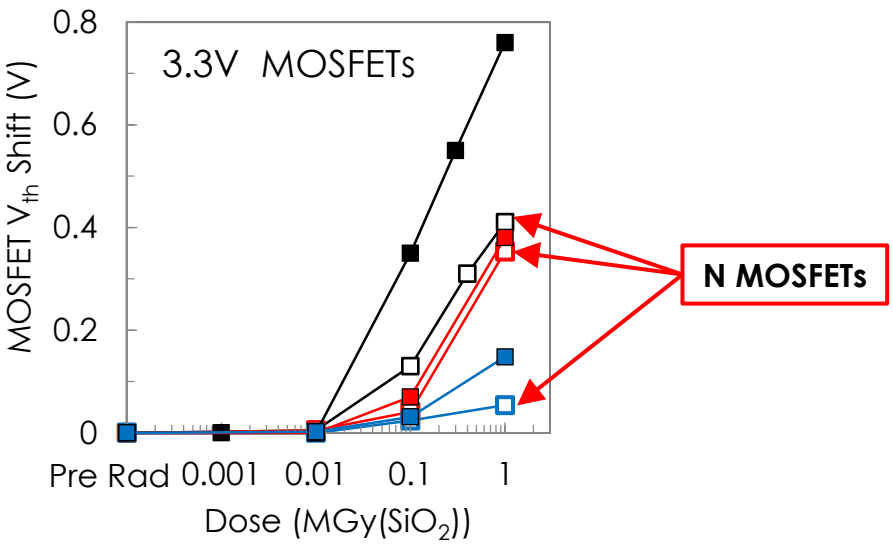
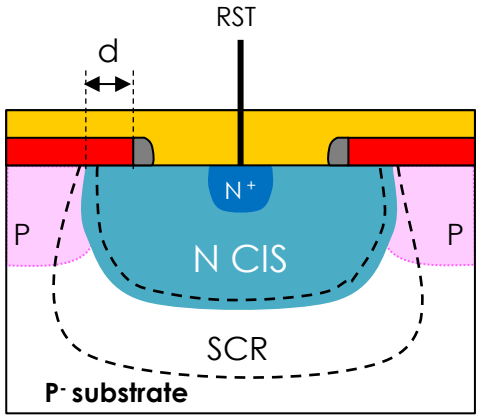
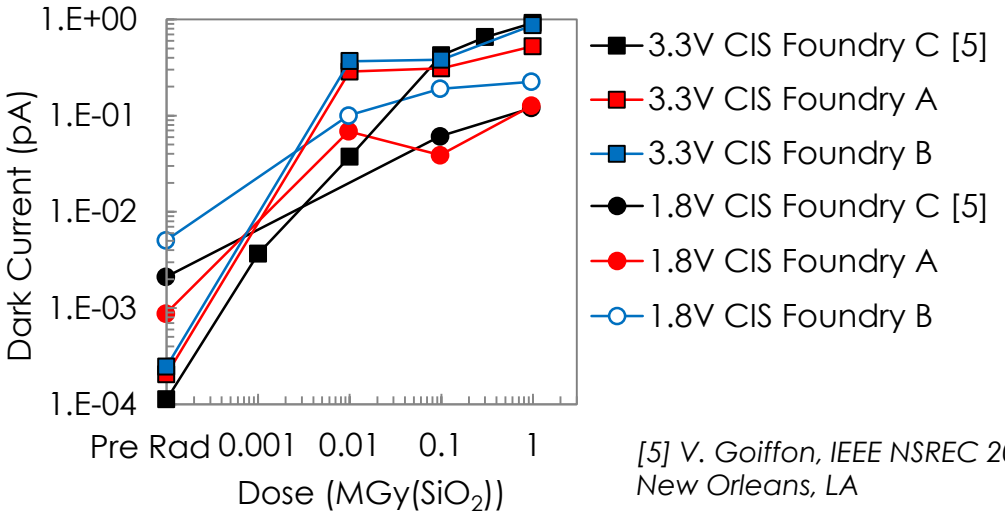
- 1.8 V MOSFETs exhibit the lower threshold voltage shift
- N MOSFETs threshold voltage induced shift is less than in P MOSFETs



TID induced dark current increase

Gate Overlap pixel design





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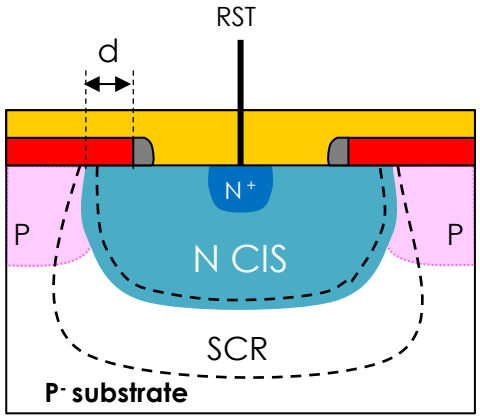

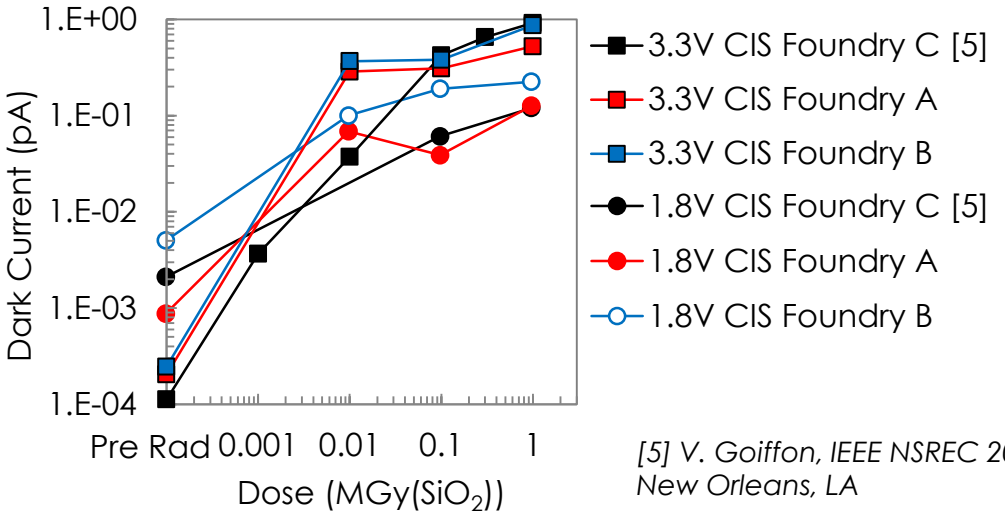

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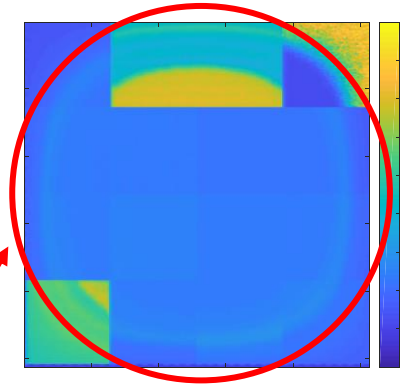
1. Manufacturing process impacts dark current CIS performances before and after TID up to 100 Mrad → **CISs from foundry B have the highest dark current**
2. 1.8 V CISs exhibit the best dark current values after irradiation
   → **7X reduction @100 Mrad for foundry C**

Sum up 1/2: Manufacturing process impact

- **Manufacturing process impacts the two main radiation induced degradations:**
  - Readout chain MOSFETs threshold voltage shift is **minimized in Foundry B CISs**
  - Lower dark current values are exhibited by **Foundry A CISs**
  - Non-uniformity appears in the pixel array for **Foundry B** CISs

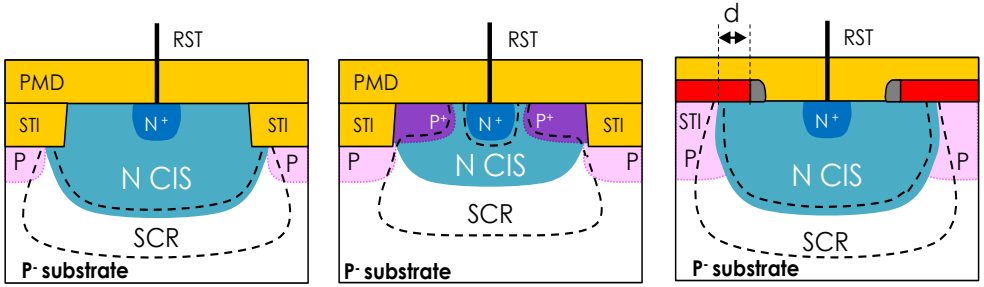


Sensor B 3.3 V
after 1 MGy(SiO_2)

- For all the tested technologies:
  - 1.8V MOSFETs exhibit the **lower threshold voltage shift**
  - N MOSFETs are the most **radiation tolerant**.
  - 1.8V sensors exhibit the **best dark current** performances →

Dark current reduction:
5X Foundry A
4X Foundry B
7X Foundry C

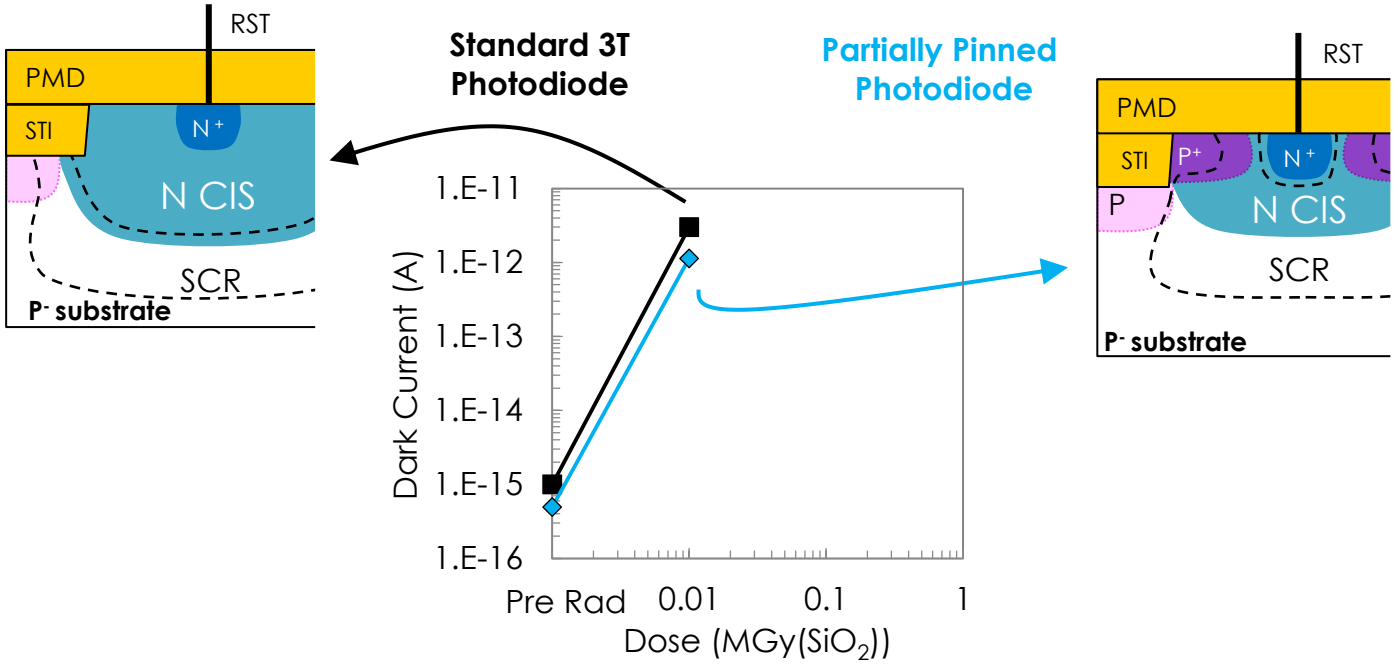
CAMRAD investigated CMOS Image Sensors



- TID up to 1MGy(SiO_2)
- 16 pixel designs
  - Standard 3T photodiode
  - Partially Pinned 3T photodiode
  - Radiation hardened by design photodiodes

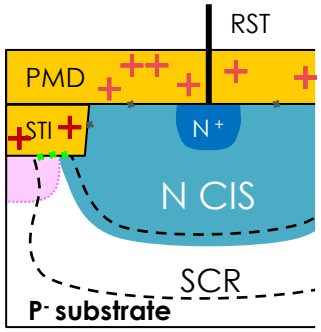
2. Improve TID degradation understanding in different photodiodes design

Dark current evolution with TID: Radiation hardness of partially pinned photodiode



Dark current evolution with TID: Radiation hardness of partially pinned photodiode

Trapped charges and interface states in PMD and STI



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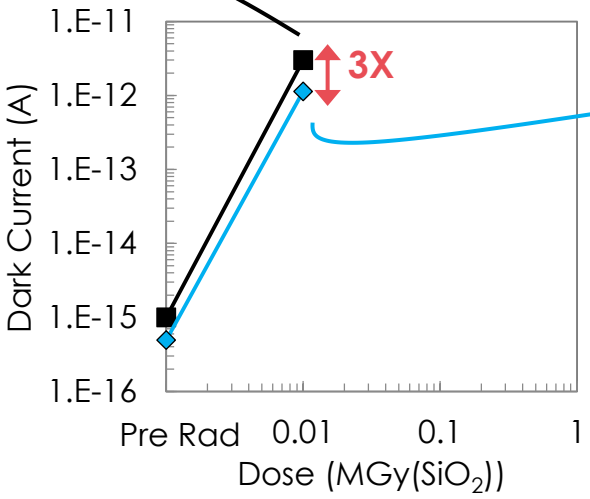

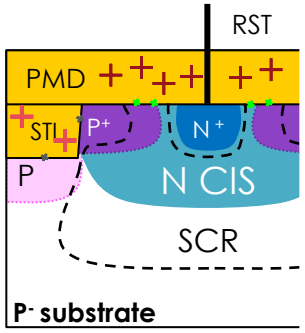

Trapped charges in the PMD

↓

P+ effective doping reduction

Partially pinned photodiode fails after 1 Mrad (SiO_2)!!

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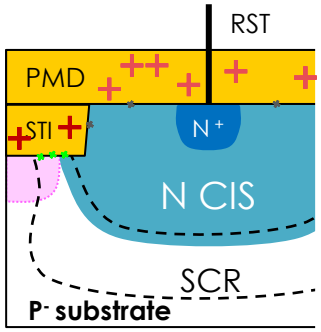

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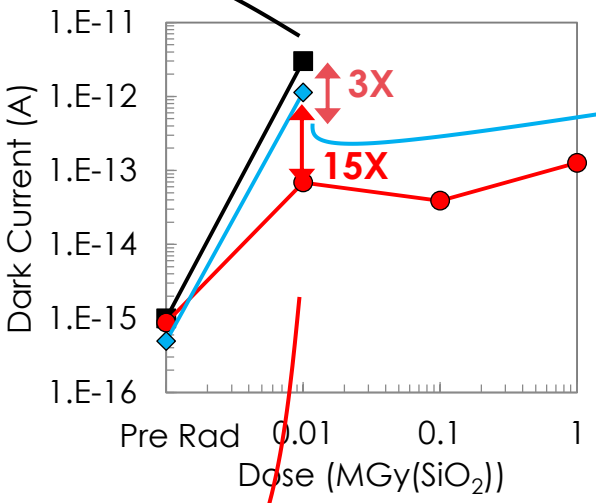

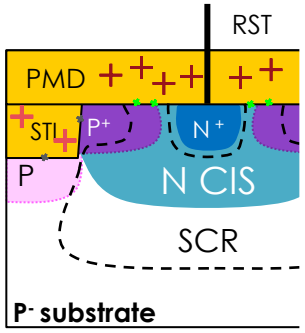

Trapped charges in the PMD

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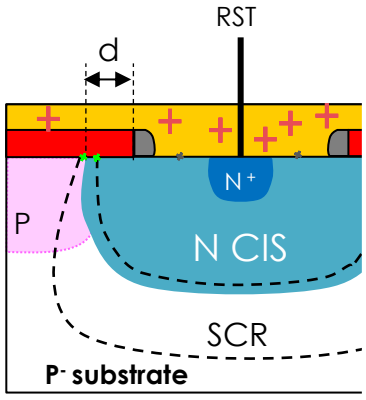
P+ effective doping reduction

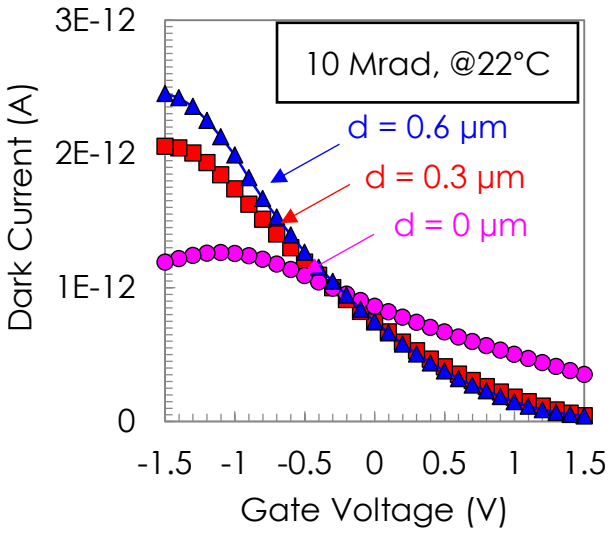
Polysilicon gate shields the junction from positive charges

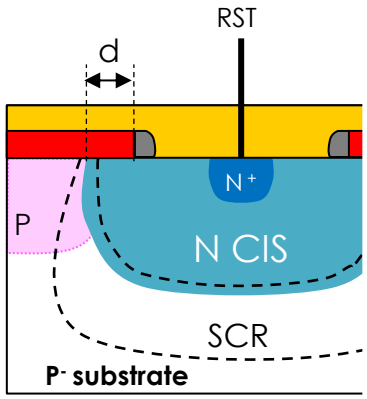


Gate overlap design

Partially pinned photodiode fails after 1 Mrad (SiO_2)!!

Dark current VS Gate voltage: The influence of the gate overlap





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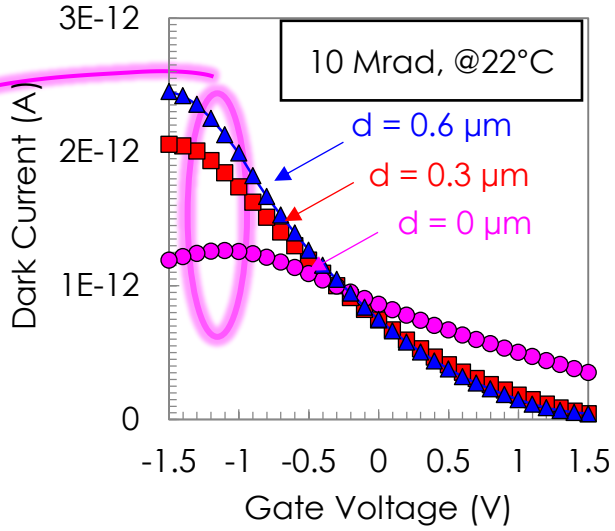
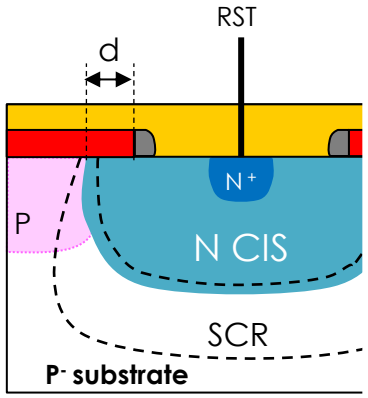
Dark current VS Gate voltage: The influence of the gate overlap

Negative Gate Voltages

Enhanced Gate Induced Drain Leakage (GIDL) in the gate overlap structures





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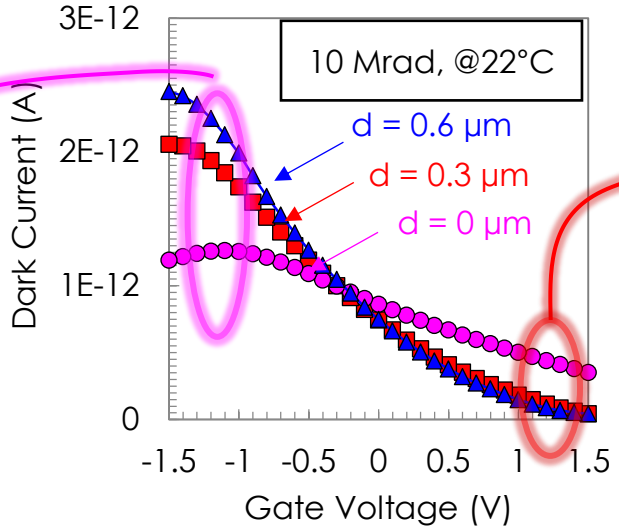

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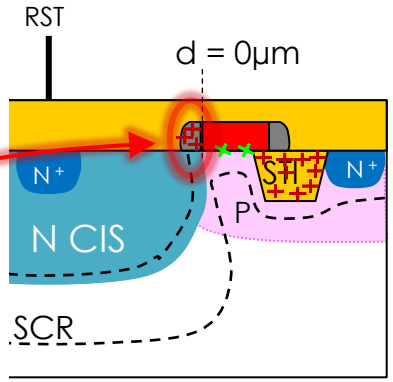
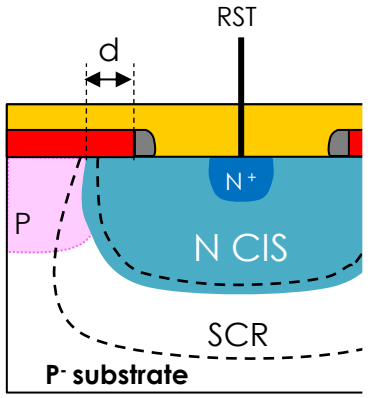


Induced defects in the spacer contribute to the dark current



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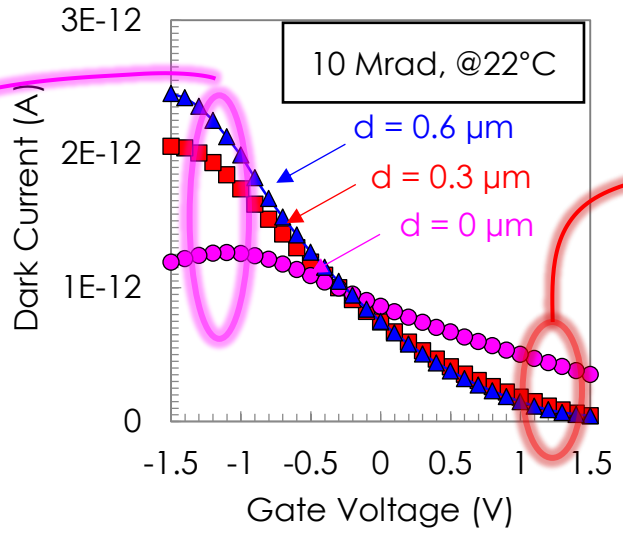

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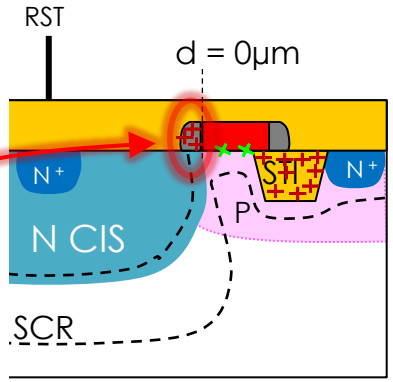

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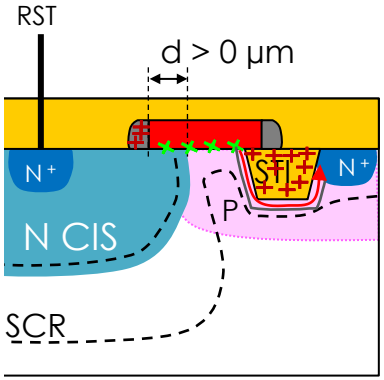
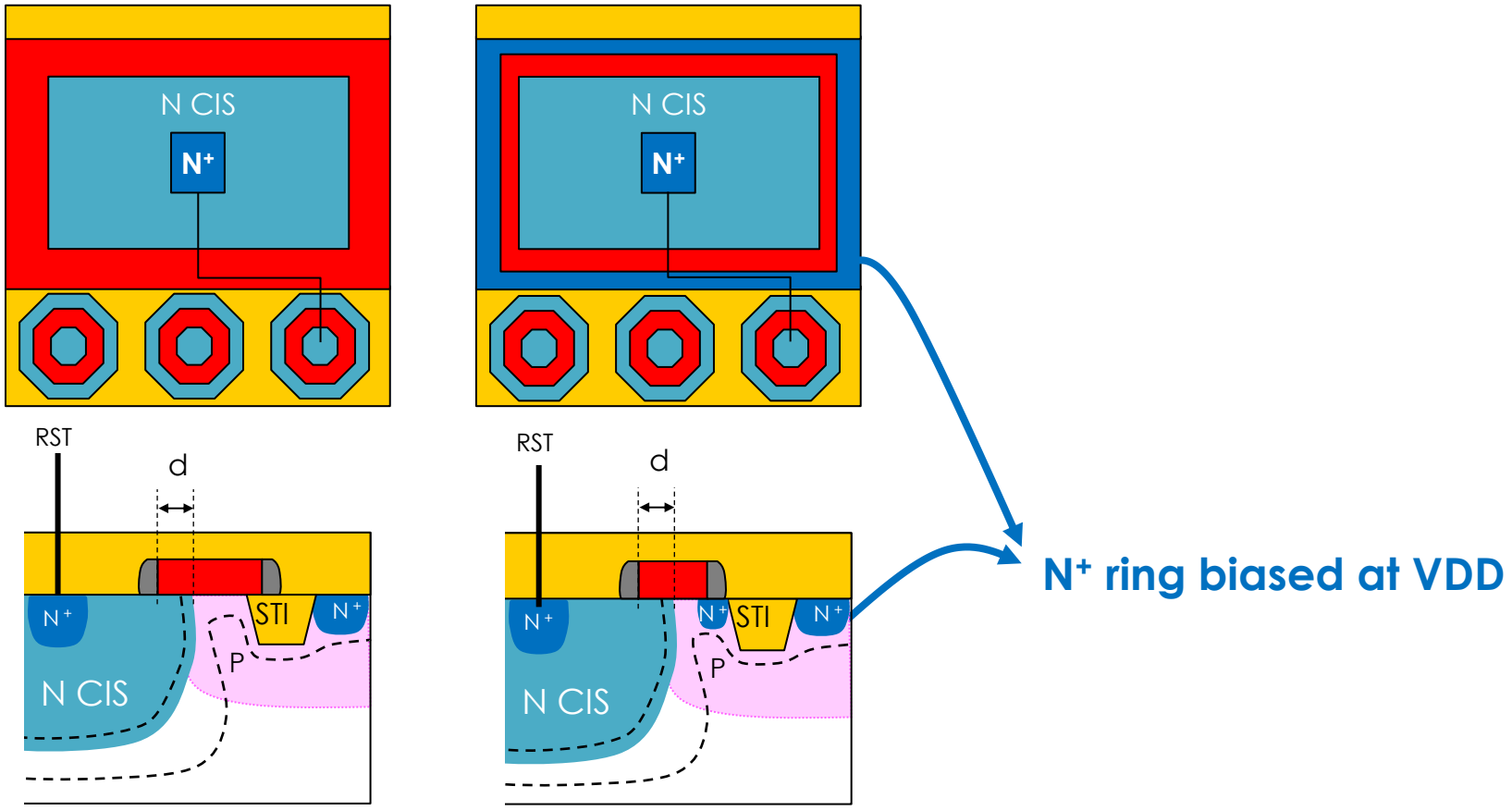


The overlap between the gate and the photodiode protect from TID induced defects in the spacer
Best dark current for Gate Voltage > 0 V
→ Charge drain mechanism?

Investigation on the charge drain mechanism: The proposed drain design

Gate Overlap **Gate Overlap and N⁺ Drain**



Investigation on the charge drain mechanism: Dark current VS TID

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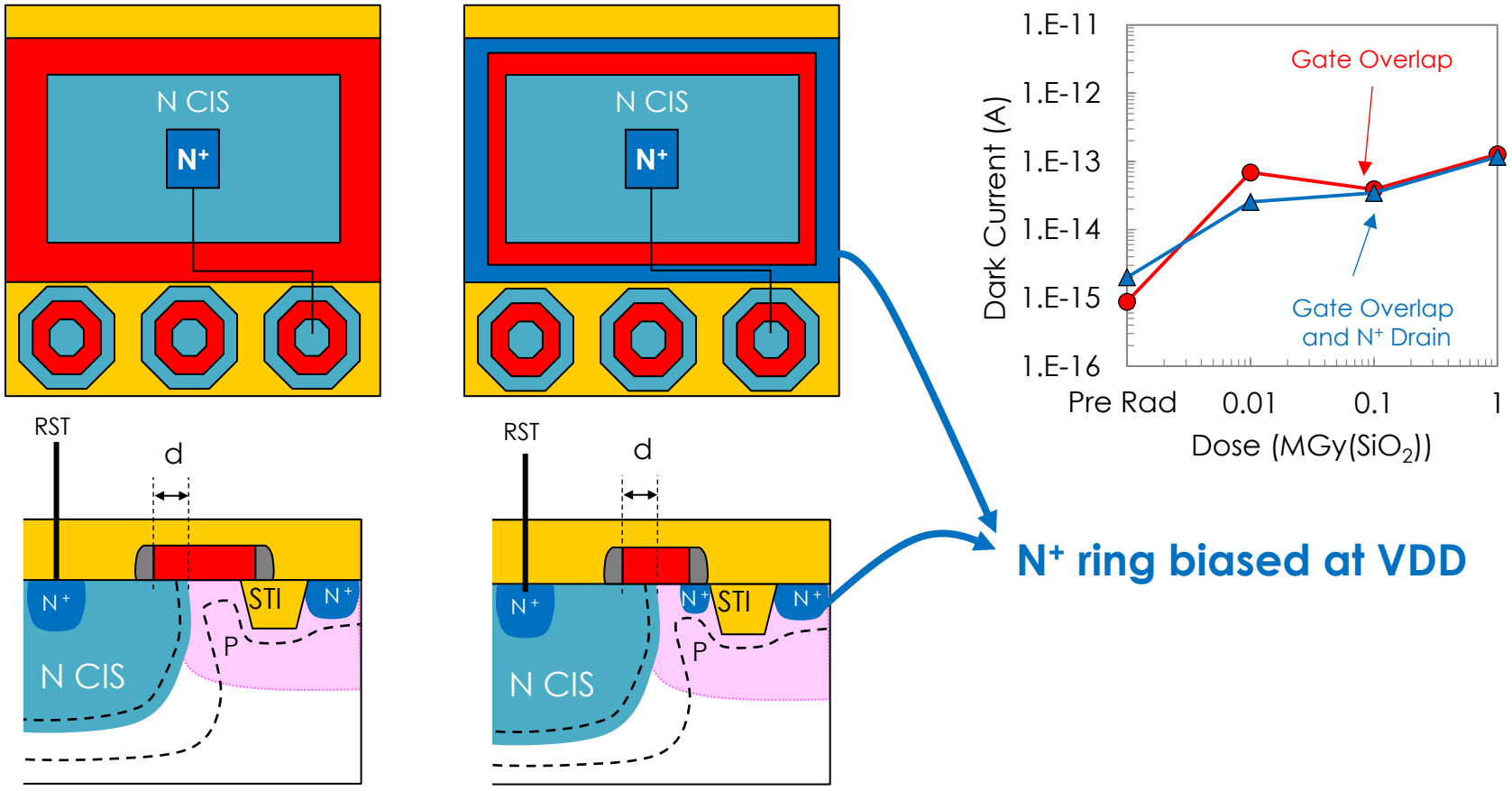
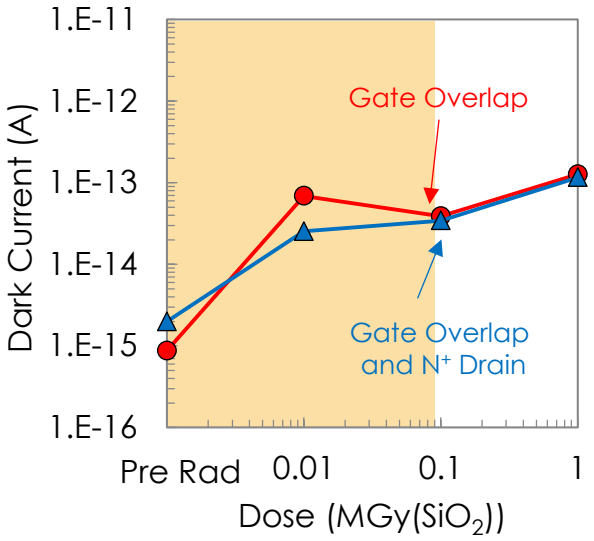
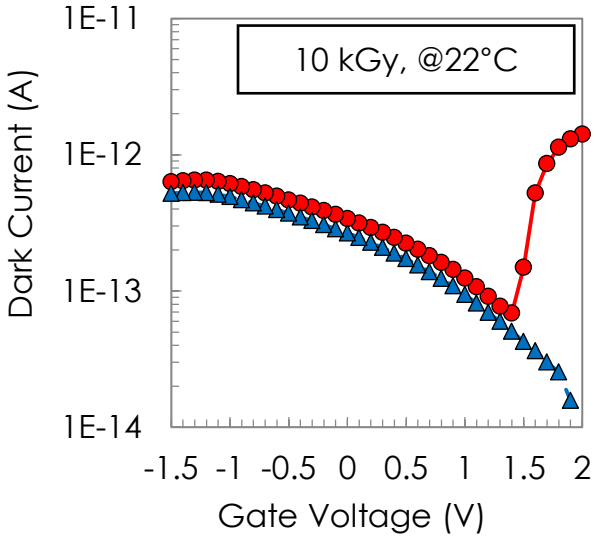


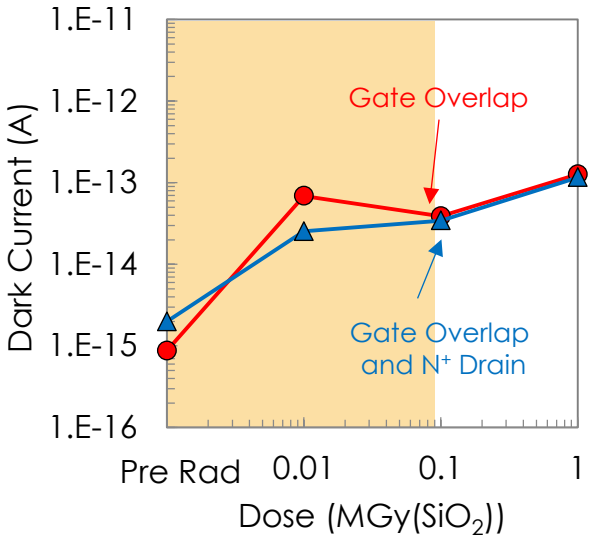
Investigation on the charge drain mechanism: Dark current VS Gate voltage at moderate TID

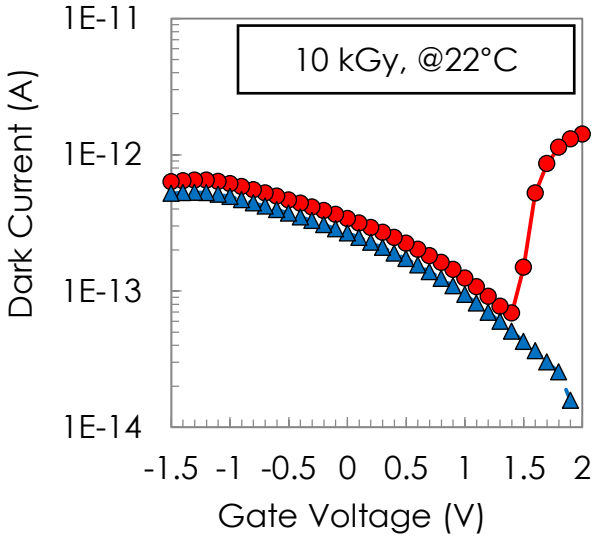




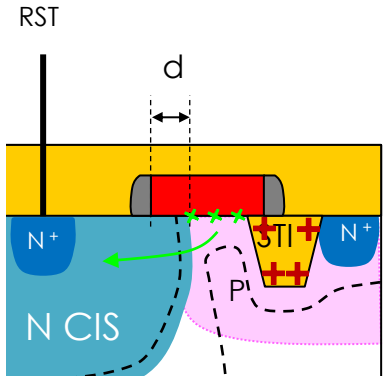
- At TID < 10 Mrad **dark current decrease** with the **increase of gate voltage** is observed in N+ Drain design pixels

Investigation on the charge drain mechanism: Dark current VS Gate voltage at moderate TID

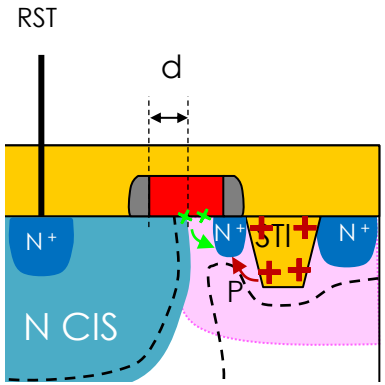




Gate Overlap

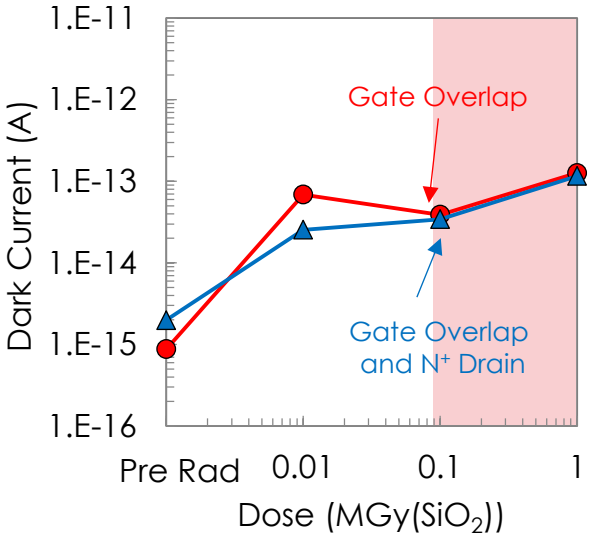


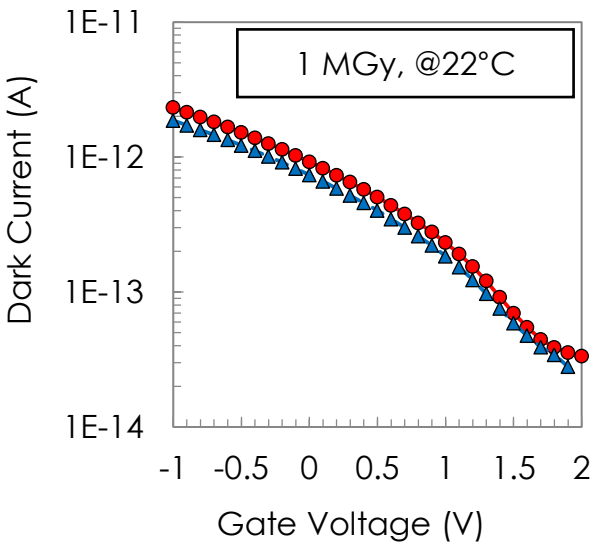
Gate Overlap and N⁺ Drain



- At TID < 10 Mrad **dark current decrease** with the **increase of gate voltage** is observed in N⁺ Drain design pixels
- The **charge drain mechanism is confirmed** thanks to **VDD N⁺ drain**

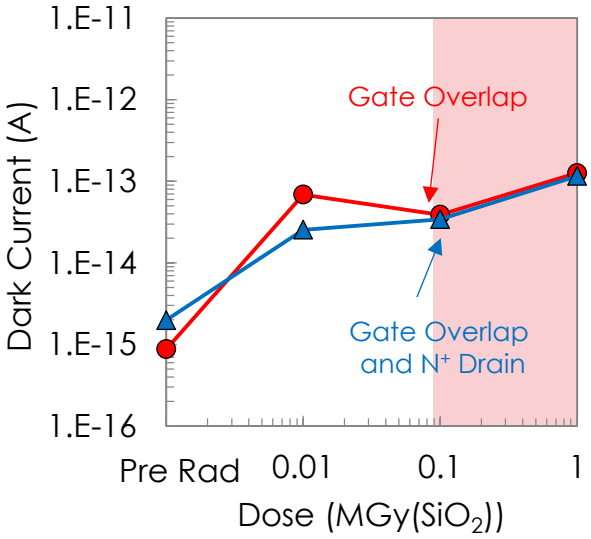
Investigation on the charge drain mechanism: Dark current VS Gate voltage at high TID

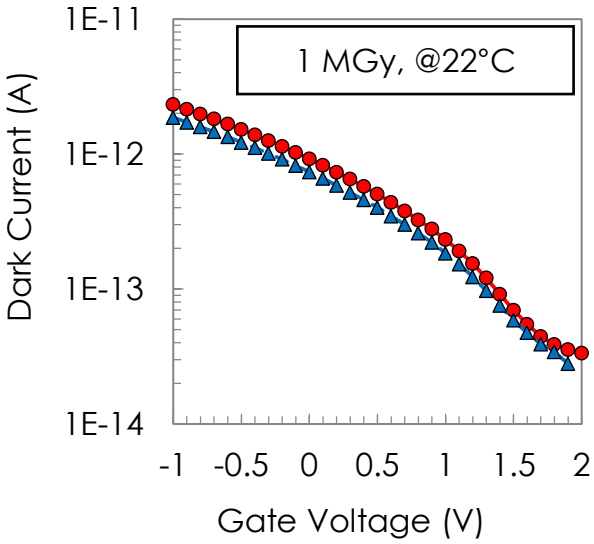




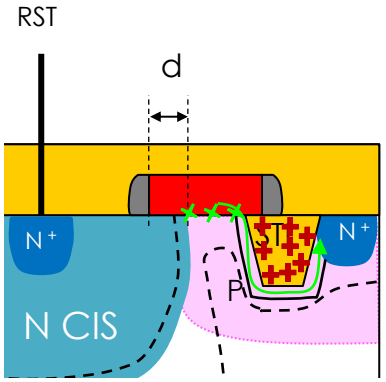
- At TID > 10 Mrad **dark current decreases** with the **increase of gate voltage** in both pixels

Investigation on the charge drain mechanism: Dark current VS Gate voltage at high TID

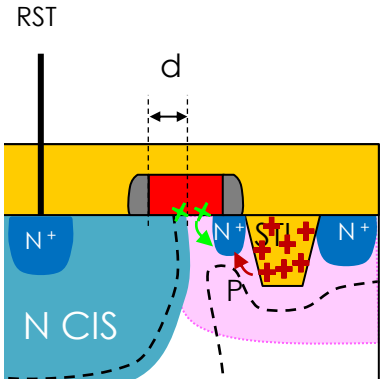




Gate Overlap



Gate Overlap and N⁺ Drain



- At TID > 10 Mrad **dark current decreases** with the **increase of gate voltage** in both pixels
- The **charge drain mechanism is active** in gate overlap design because of the **STI inversion**

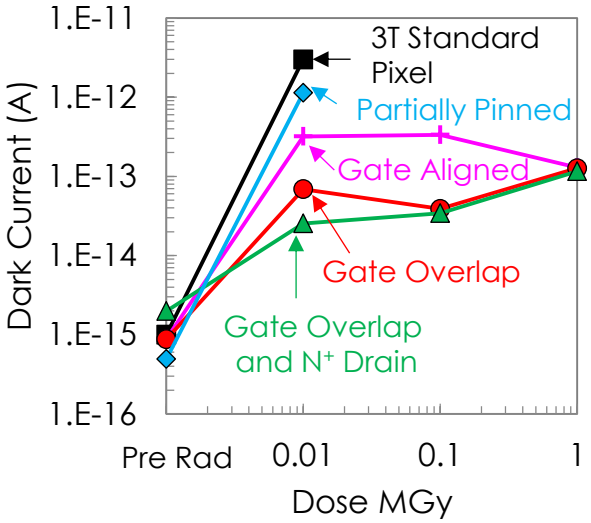
Sum up 2/2: Pixel design influence

- 3T Partially pinned photodiode **is more radiation tolerant** than standard 3T photodiode for TID < 1 Mrad

  → **P^+ layer limits the Si/SiO_2 contact**

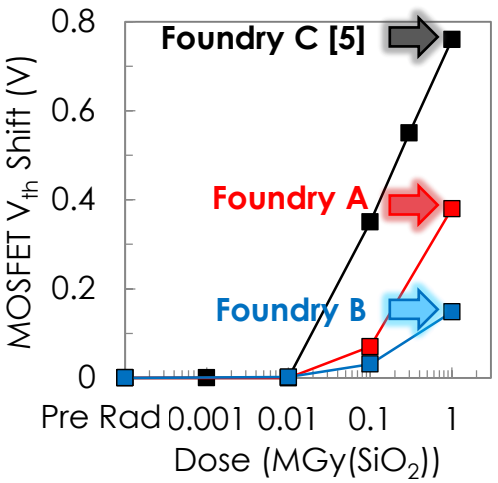
- At TID > 1 Mrad partially pinned **functionality is lost**

- Gate overlap design gives **best performances** in term of dark current for positive voltages applied to the gate:
  - **Gate overlap has to be optimized**
  - **N^+ Drain biased at VDD allow to control dark charges draining mechanisms**



Conclusions and perspectives

- **The manufacturing process** has an **important impact** on the absolute radiation hardness of CIS
  - **MOSFET performances**
  - **Dark Current**
- **The gate overlap design is required** for TID beyond 100 Mrad
  - **Optimization of Gate overlap**
  - **Influence of N^+ Drain size on optoelectrical performances**
- The **charge drain mechanism** is **confirmed thanks to VDD N+ drain design**

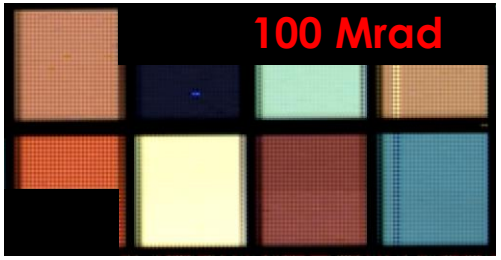


Further development:

→ **Integration of all the functions in a single HD sensor (ADC, Sequencer…)**

→ **Exploration of other radiation conditions to evaluate the radiation response of these CISs (Charged particles, Neutrons…) for future spatial applications such as Jupiter Missions**

Only Gate overlap designs are functional



Thank you for your attention!

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