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Radiation Hardening of Digital Color CMOS Camera-on-a-Chip Building Blocks for Grad Total Ionizing Dose Environments

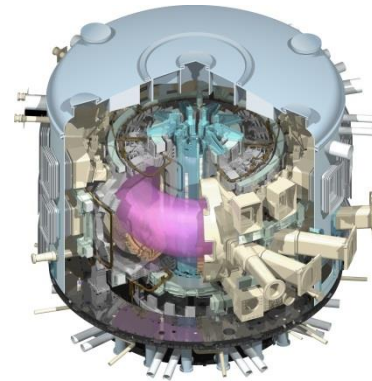
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S. Girard and T. Allanche; *Univ. Saint-Etienne, Laboratoire Hubert Curien, France*
P. Paillet, M. Gaillardin and C. Marcandella; *CEA DAM DIF, Arpajon, France*
M. Van Uffelen and L. Mont Casellas; *Fusion for Energy (F4E), Barcelona, Spain*
R. Scott; *Oxford Technologies Ltd.(OTL), Abingdon, UK*

Context and Motivations

- **ITER remote handling operations require imaging systems**
 - Compact, lightweight and low power/voltage
 - Radiation hard (failure TID $\gg 1\text{MGy}(\text{SiO}_2)$ ($\gg 100\text{ Mrad}$))
Gamma radiation only (plasma OFF)
 - Color and high definition ($\geq 1\text{Mpix}$)
- **Tube camera, **not suitable** because of**
 - Size, cabling, voltage, resolution and reliability
- **Existing solid-state image sensor based camera**
 - **Limited** by their radiation **hardness: $\leq 100\text{ kGy}$**



**FUSION
FOR
ENERGY**



Dedicated development required

Rad-Hard CIS State of the art (MGy range)

● What can be found in literature:

- A few dark current measurements on STAR250 **Active Pixel Sensor (APS)** up to 1MGy (*Bogaerts et al. 2003*) (**old non-CIS process**)
- A few dark current measurements up to 2 MGy on CMOS APS developed for Electron Microscopy based on standard (**non-CIS**) CMOS process (*Contarato et al. 2012*)

● What is missing:

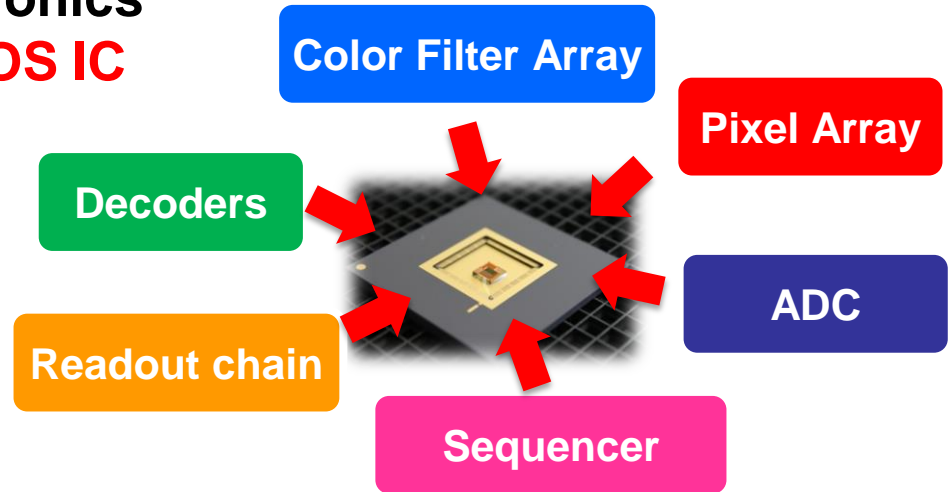
- No result ever published on **CIS processes** in the MGy range
- An **image** captured with an **APS/CIS** exposed to 1MGy (=100Mrad) or more has **never been published**
- No data on the TID effects on **opto-electrical performances** of **APS/CIS** in the MGy range

Camera Radiation Hardening Strategy

- Integrate all the required electronics on a **single** Rad Hard (RH) **CMOS IC**

➔ **RH Camera-on-a-Chip
(this work)**

- No need for additional MGy RH electronics
- Very compact
- Complete control of the radiation hardness

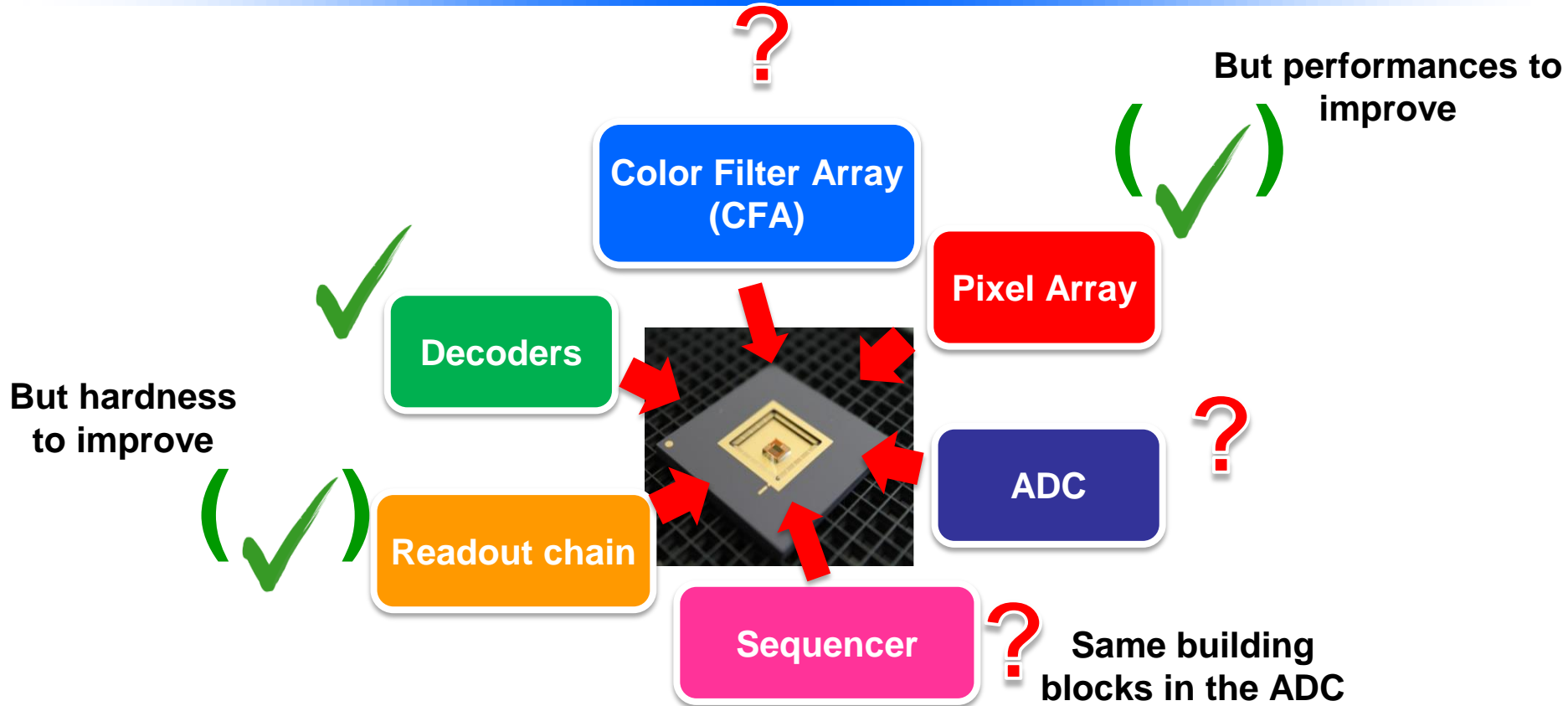


- **Associated RH developments**

- Rad-Hard **optical system** (led by *Univ. Saint-Etienne*)
- Rad-Hard LED based **illumination system** (led by CEA)



Feasibility of a CMOS based Multi-MGy Rad-Hard Color Camera-on-a-Chip?



- **Goal of this work:**

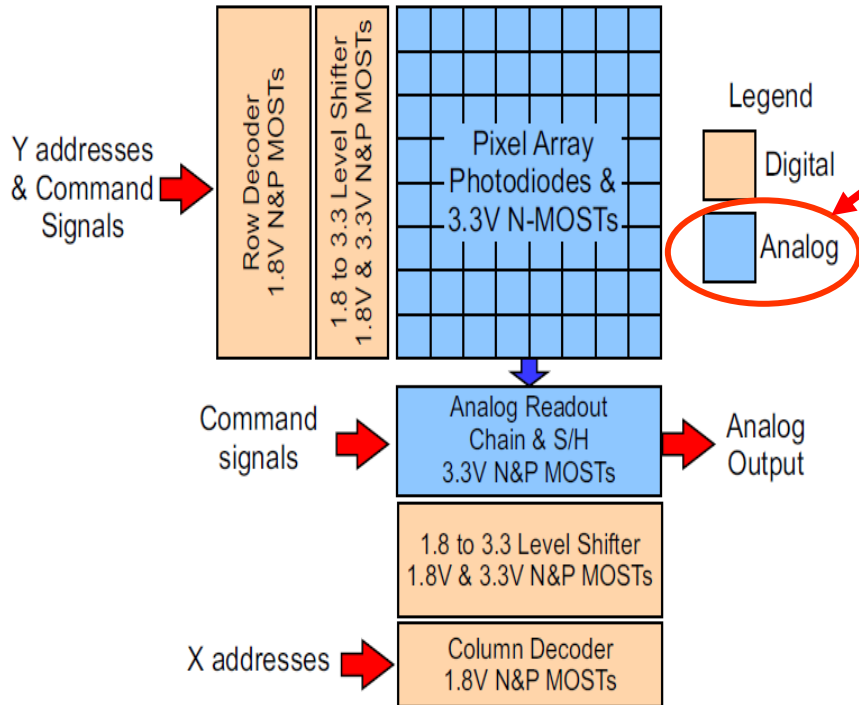
- Demonstrate that CMOS Image Sensor (CIS) can withstand a TID of 1MGy or more
- Explore original mitigation techniques to **improve the image sensor performances**
- Analyze MGy radiation effects on **CFA** and on a basic imager **ADC**

-
- **Presentazione della strategia con i due sensori**

 - **RAD HARD**
 - **FUSEV**

Experimental Details: CIS overview & Irradiation Details

128x128 10 μ m pitch pixels



Most sensitive part: 3.3V analog circuits

180 nm commercial CIS technology

Irradiation details:

- 10keV X-rays
- CIS biased (see ⁶⁰Co γ -ray in the paper)
- Room temperature
- Dose rate: 180kGy/h
- Dose values in Gy(SiO₂)

Additional notes in green boxes:
 - GND in the paper
 - 18kGy/h in the paper

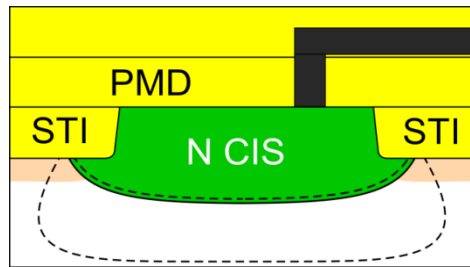
**FULL ELT DESIGN
(N&P MOSTs)**

- Pure 1.8V digital and I/O pads: **IMEC-ESA Rad-Hard DARE Library**
- 3.3V Analog/Mixed signal circuits and pixels ← **Rad-Hard by ISAE**

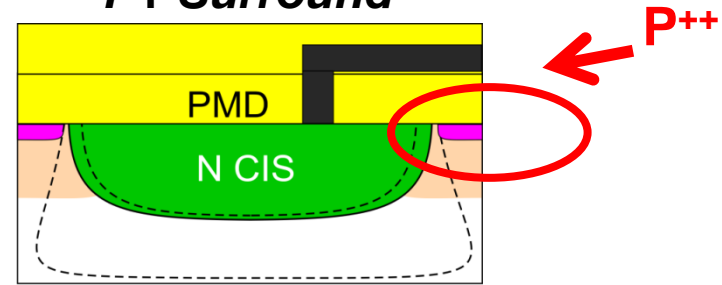
CMOS Image Sensor (CIS) Design : photodiode radiation hardening

- Four 3T photodiode designs have been studied:

Standard Photodiode

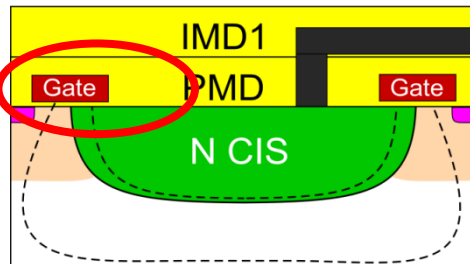


P+ Surround

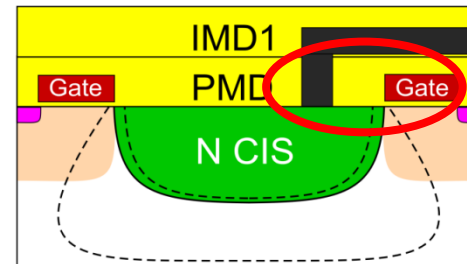


- Most Promising Designs for High Dose :

*Proposed Improvement:
Gate Overlap Design*



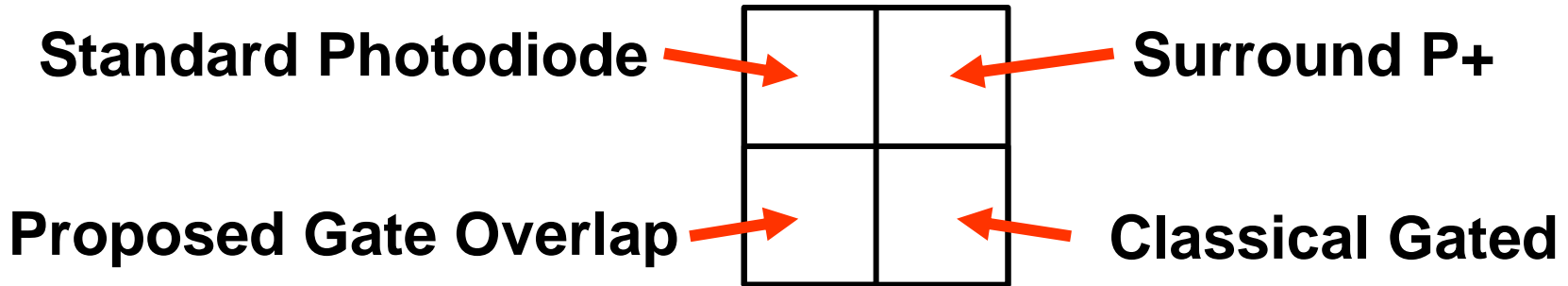
*Classical Gated Diode
(gate aligned N implant)*



Gate with voluntary N-overlap ($\approx 0.3 \mu\text{m}$)

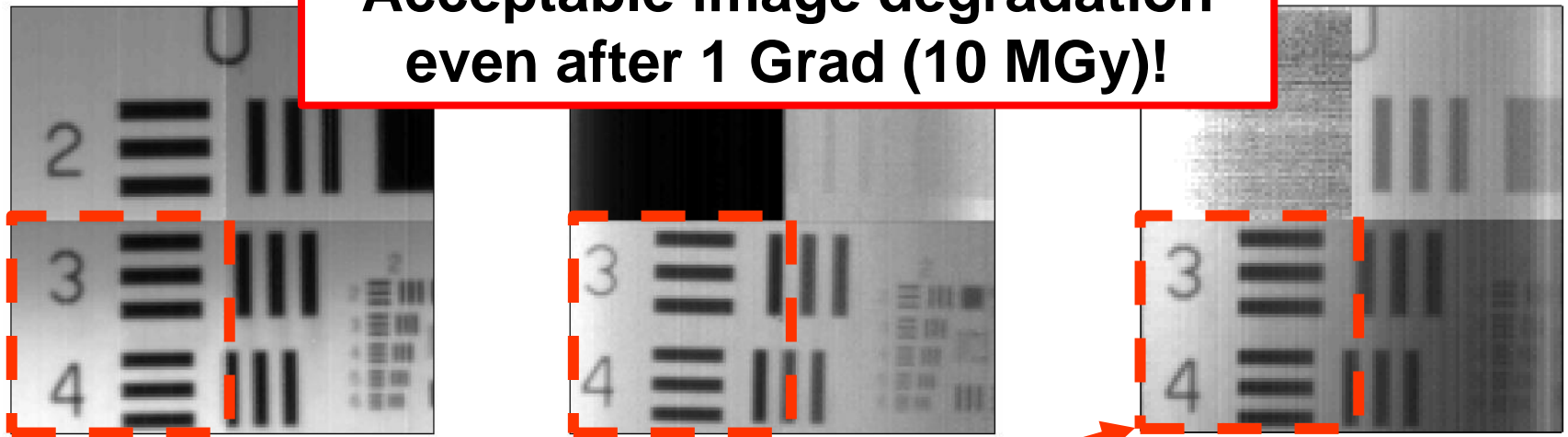
Gate (N-aligned)

Post Irradiation Results: Raw Images (no image correction)



Before Irradiation @4 MGy (400 Mrad) @10 MGy (1 Grad)

Acceptable image degradation
even after 1 Grad (10 MGy)!

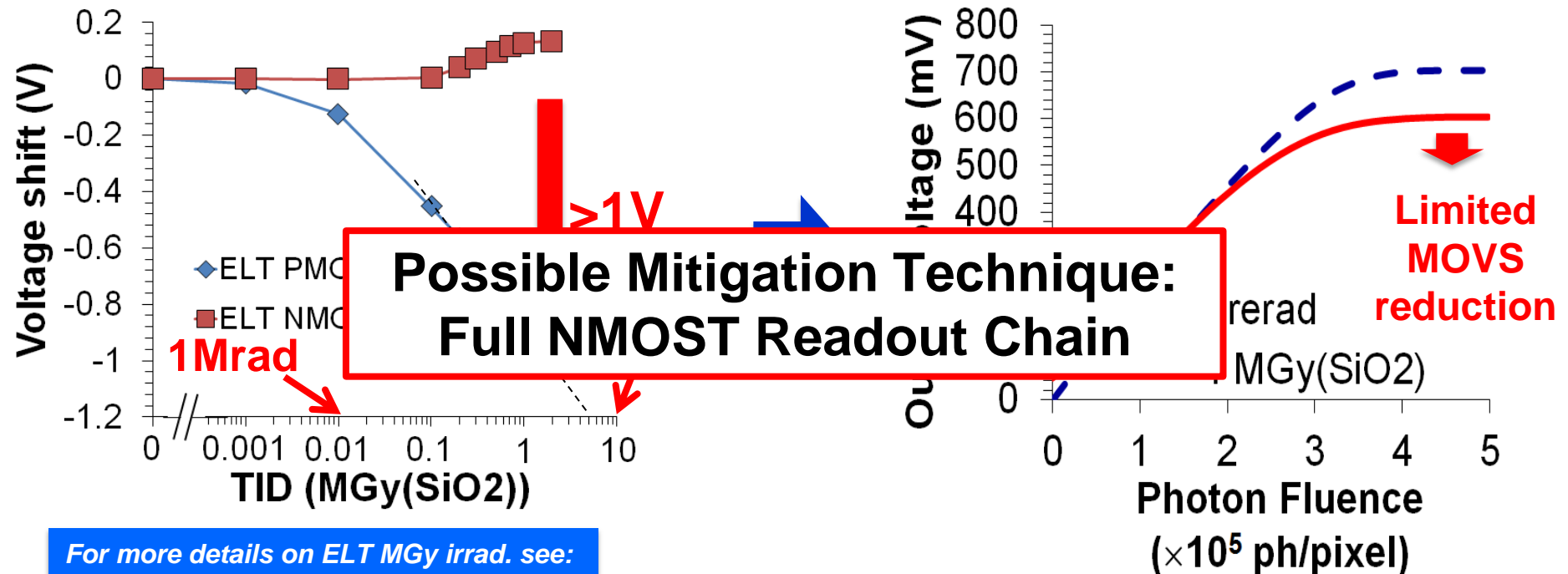


Gate Overlap

Main Radiation Effects: 3.3V ELT PMOST Threshold Voltage Shift

- Very limited 3.3V NMOST ELT degradation ($<200\text{mV } \Delta V_{th}$)
- Large (& surprising) **3.3V PMOST ELT ΔV_{th} ($>1\text{V!}$)**
 - Compensated by decreasing PMOST current source bias voltage

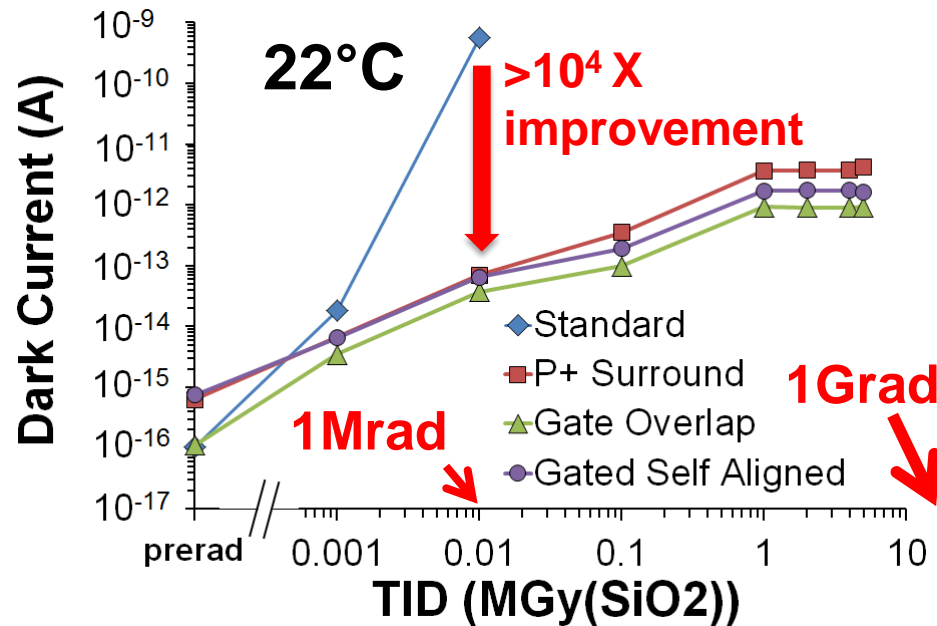
➔ Limited Maximum Output Voltage Swing (MOVS) decrease



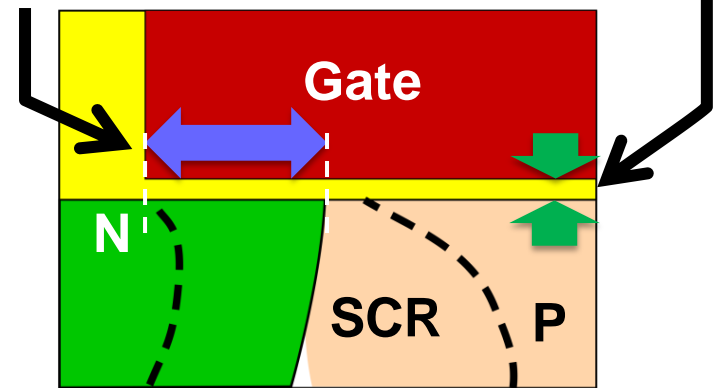
For more details on ELT MGy irradiation, see:
M. Gaillardin & al. "Multi-MGy ionizing dose effects in CMOS devices: from micron to decanometer technologies"

Main Radiation Effects: Dark Current Increase

- **Standard PD: 10^7 X dark current rise @10kGy (1Mrad)**
 - no longer functional at higher radiation dose
- **Gate Overlap: best performances over the whole range**



- Possible further improvements:**
- Thinner gate oxide (GO2 → GO1)
 - Overlap distance optimization



10X or more possible improvement?

Strategy for Hardness Improvement

Large threshold voltage shifts in
3.3V ELT* P-MOSFETs
(>1V after several MGy)

2 mitigation techniques
proposed

Only use 1.8V
ELT* MOSFETs

Studied here

Only use ELT*
N-MOSFETs (3.3V)

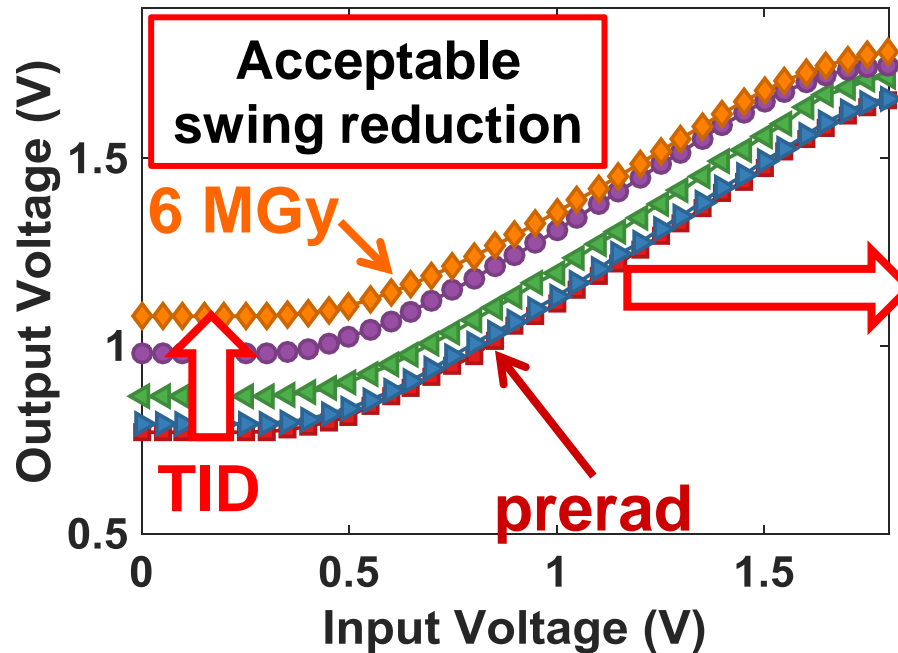
Future work

- **CMOS process:**
 - ✦ Commercial CMOS Image Sensor 180 nm
- **Irradiation:**
 - ✦ ^{60}Co gamma irradiation (SCK-CEN) up to 6MGy(SiO_2) (600Mrad)

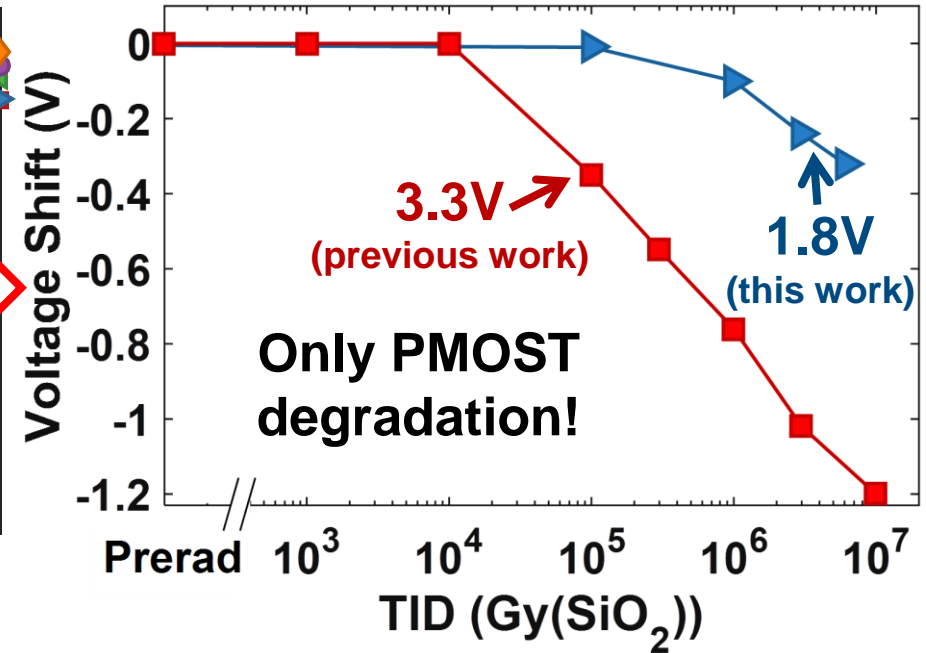
* = Enclosed Layout Transistor

RHBD Analog Readout Chain: Hardness Improvement

Electrical Transfer Function



ELT P-MOSFET $\Delta V_{\text{threshold}}$



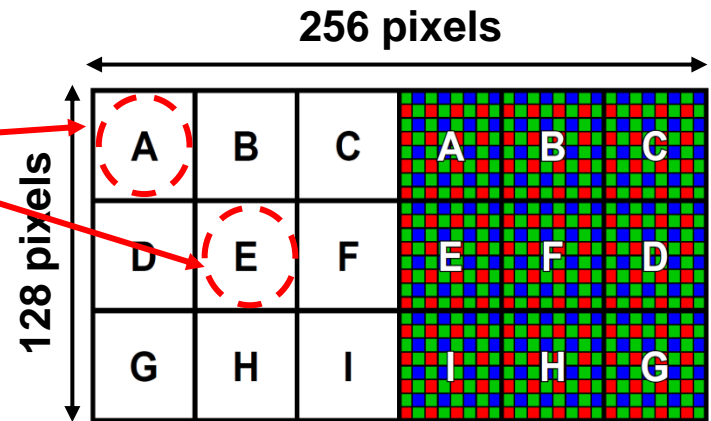
1.8V architecture



clear radiation hardness improvement

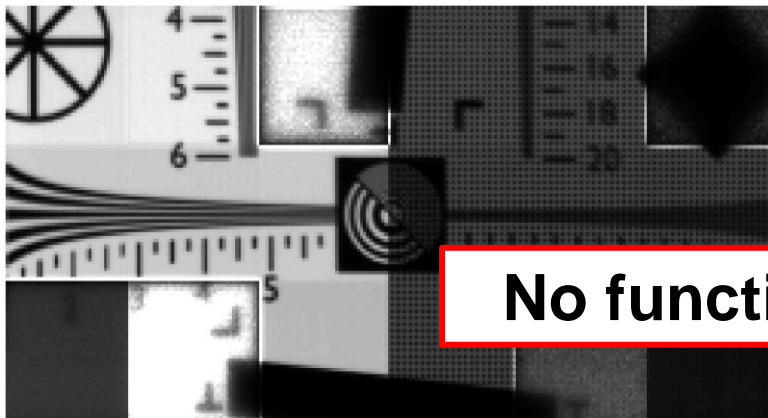
1.8V RHBD pixel array organization

- 9 pixel design variations
- 2 discussed here (A and E)
- Half of the sensor covered by a **Color Filter Array (CFA)**

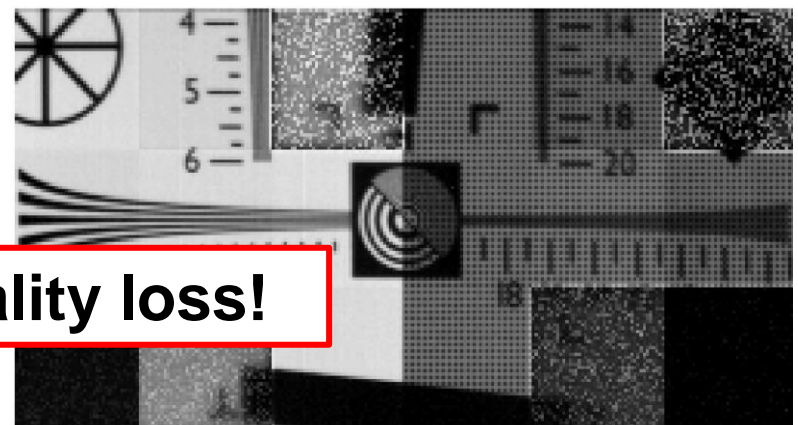


Raw images captured by the manufactured CMOS image sensor:

Non-irradiated



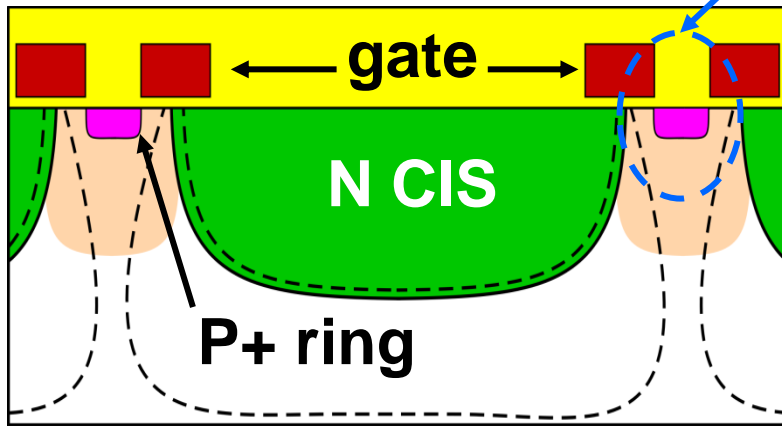
6 MGy(SiO₂) / 600 Mrad



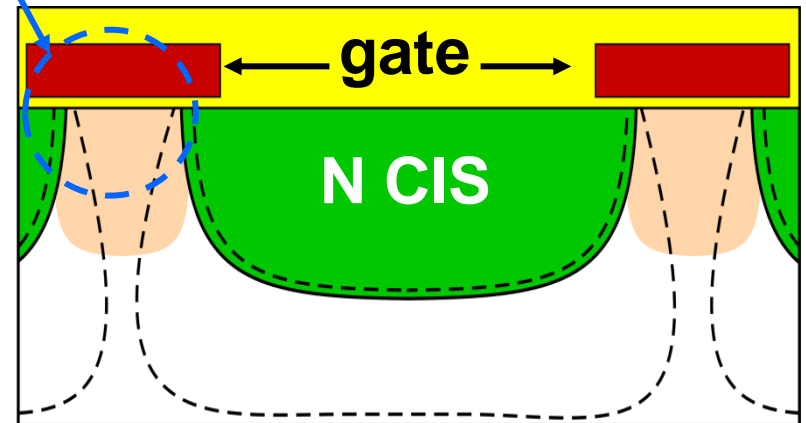
No functionality loss!

Studied RHBD photodiode designs

- Two gated photodiodes:
 - ✦ with an **overlap** between the gate and the N region
- Which differ by their **pixel-to-pixel isolation**

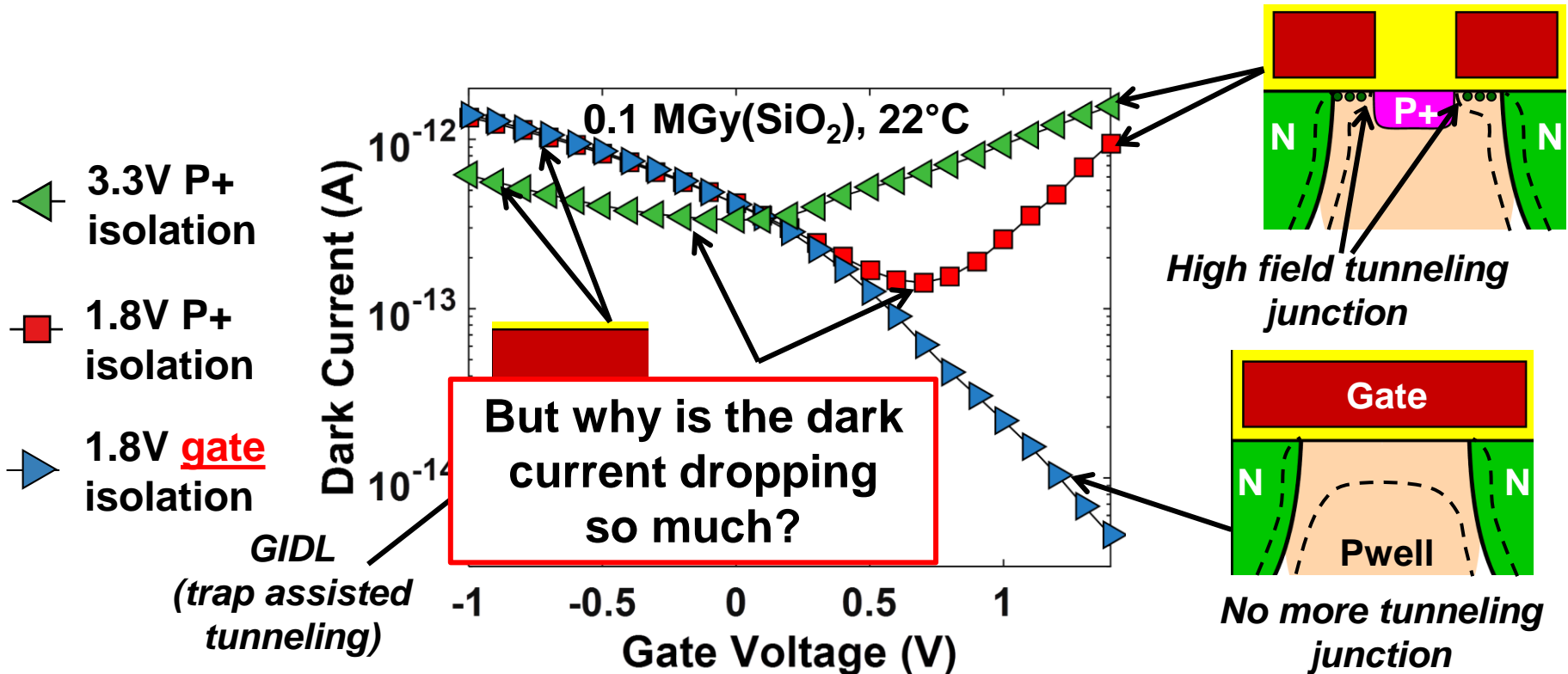


Pixel A: **P+ isolation**



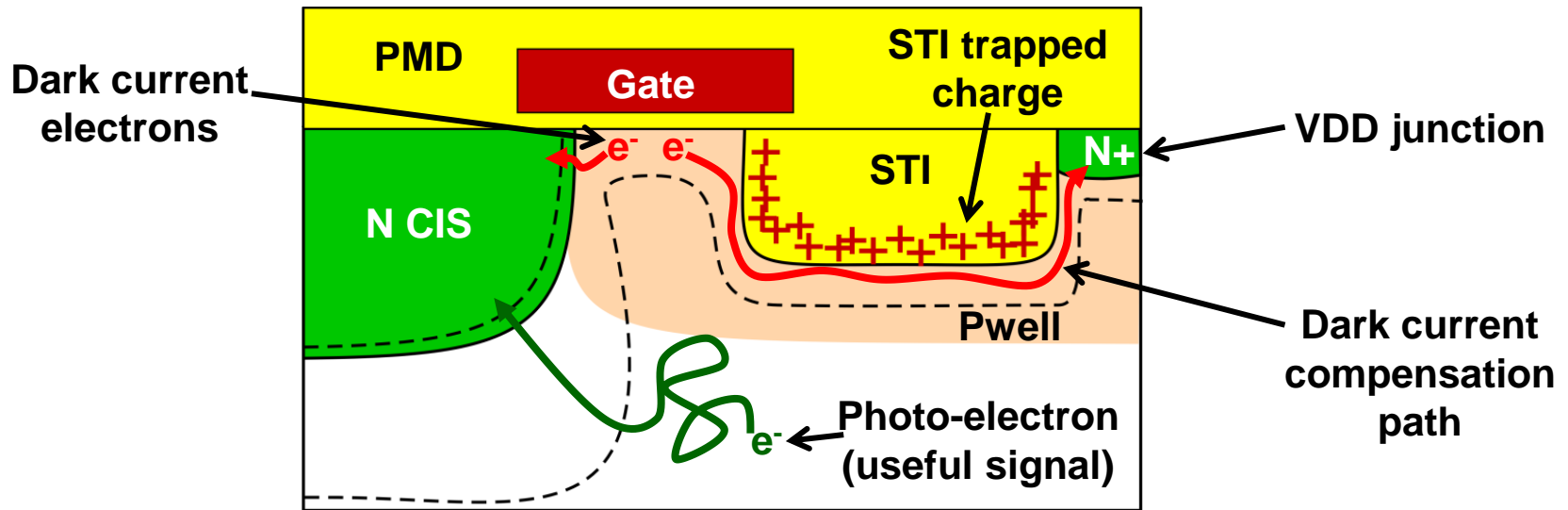
Pixel E: **gate isolation**

Dark Current: Influence of Gate Voltage



- Similar behavior between 3.3V and 1.8V pixels
- **Same behavior** between P+ and gate isolation for $V_{gate} < 0$
- Gate isolation pixel : large **dark current reduction** for $V_{gate} > 0$

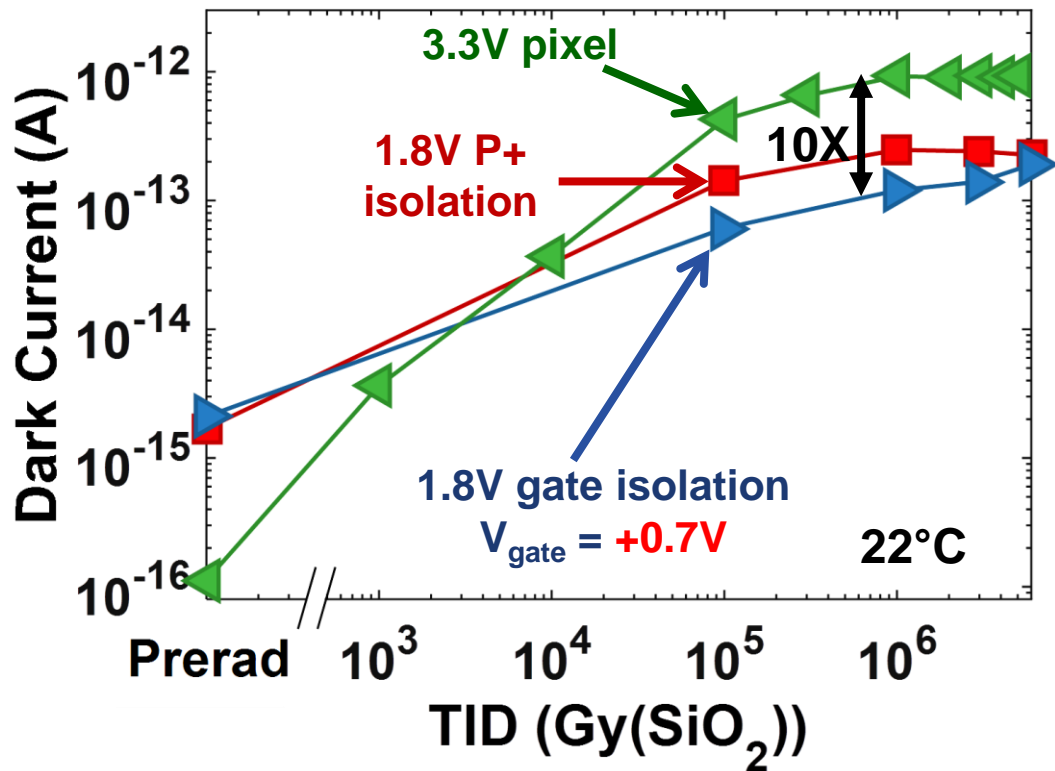
Dark Current Compensation Mechanism?



- Possible explanation:

- When the gate is depleted, **part of the dark electrons diffuse toward the nearest N+ VDD contact** through the STI weak inversion region
- Photo-electrons are not collected by STI thanks to the P-Well barrier

Dark Current: Evolution with TID

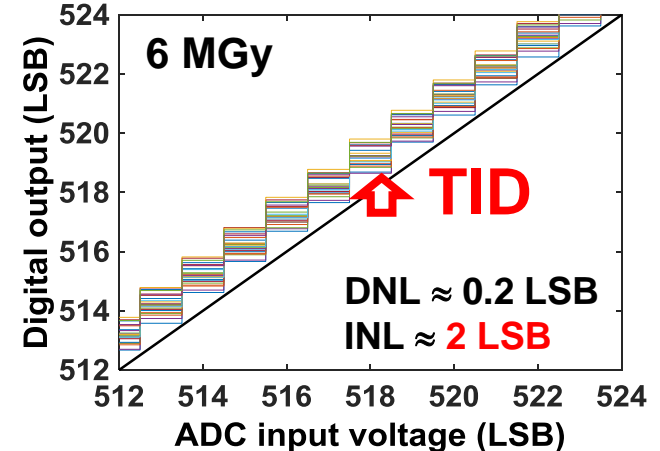
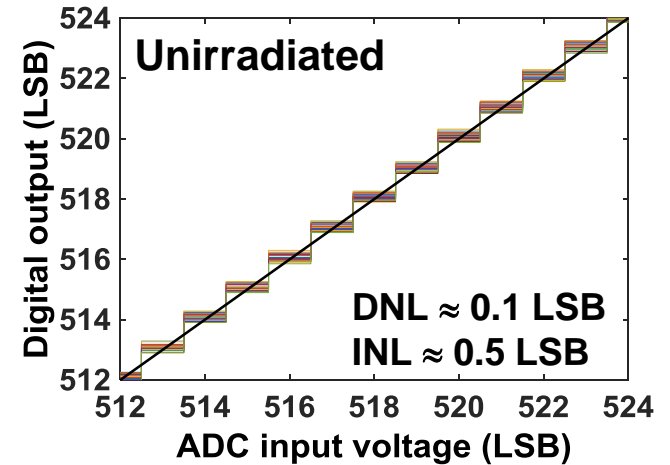
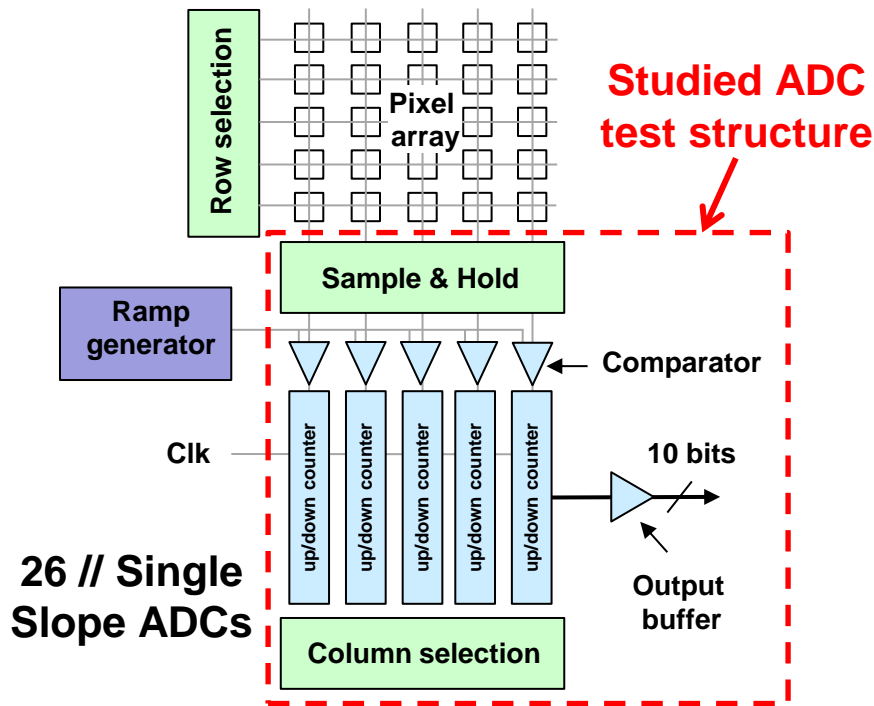


After irradiation

- 1.8V design
➔ $\approx 5\text{X}$ reduction
- Gate isolation pixel
➔ $\approx 2\text{X}$ further reduction
 - Even larger reduction if V_{gate} is increased further

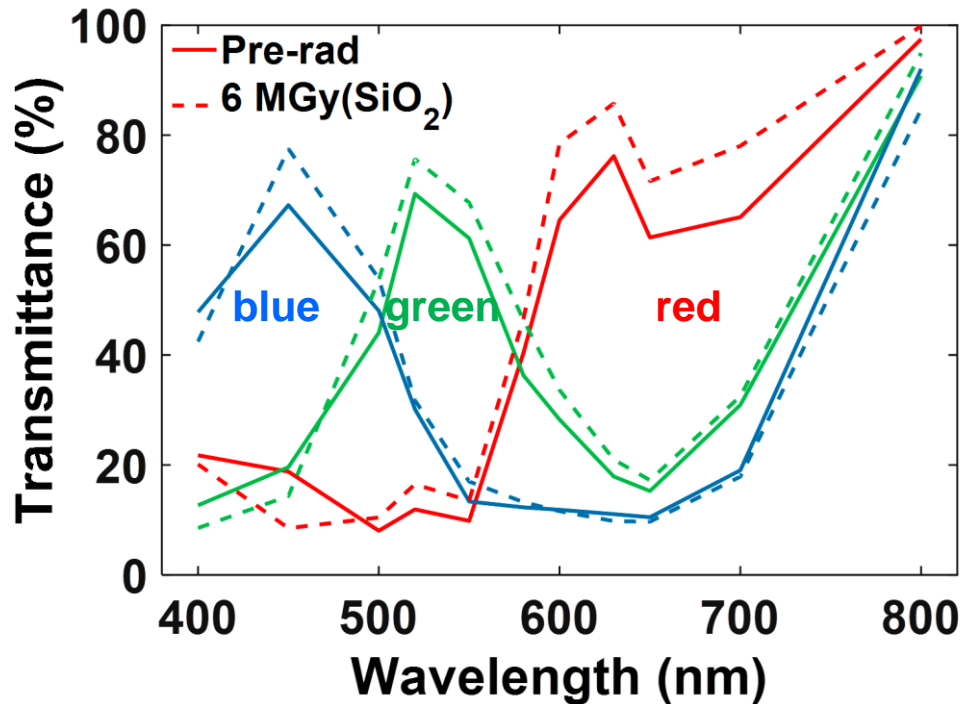
Between **5X** and **10X** dark current reduction compared to previous 3.3V design

RHBD Analog to Digital Converter (ADC)

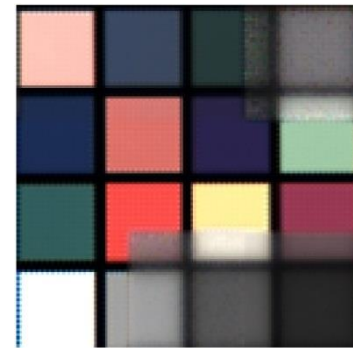


- Reasonable degradation after 6 MGy
- Not limiting the performance

Color Filter Array: Radiation Hardness Evaluation



*Color images captured by
the manufactured CMOS
image sensor:*



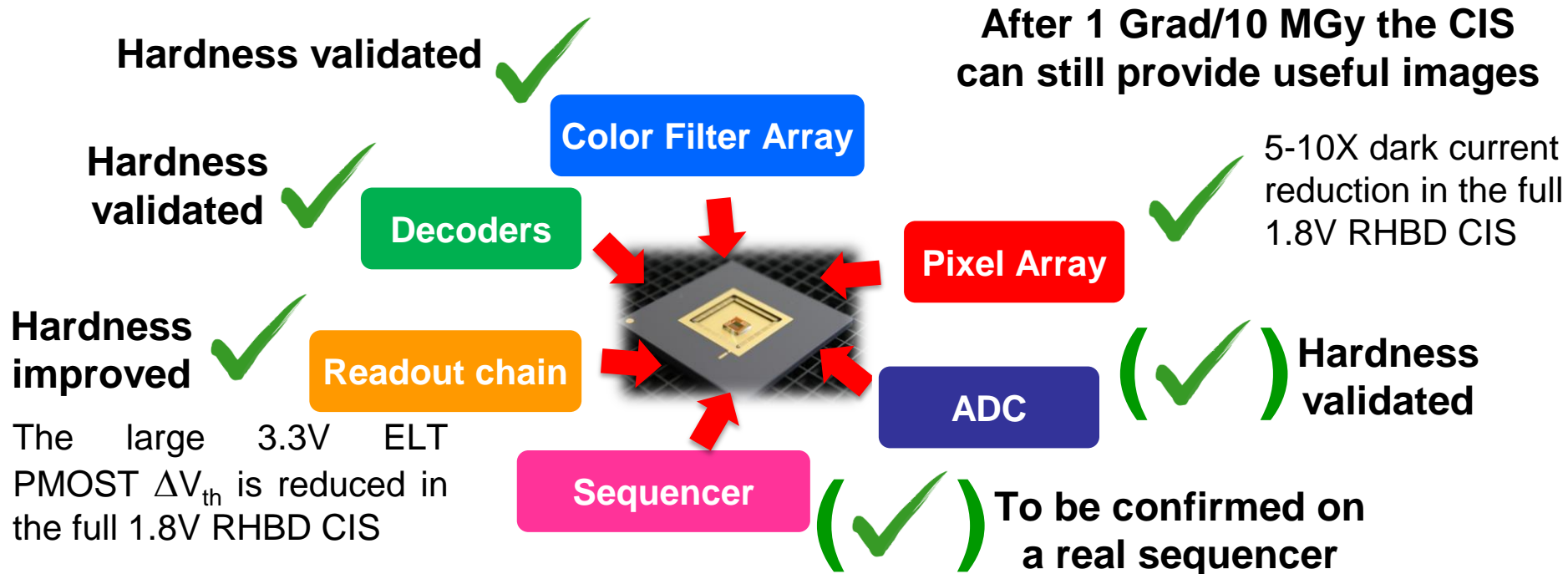
Unirradiated



6 MGy(SiO₂)

- **No significant color filter degradation**

Conclusions



- Multi MGy Rad-Hard Color Digital Camera-on-a-chip **appears feasible**
- Development shall continue:
 - **Integrate all the functions** in a single HD sensor
- Exploration of alternative solutions to **improve further the performances** (e.g. dark current? dynamic range?)



oxford technologies

Thank you!
