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MODULAR MULTILEVEL CONVERTER-BASED HVDC TRANSMISSION SYSTEMS

BY

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ABSTRACT

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Title: MODULAR MULTILEVEL CONVERTER-BASED HVDC TRANSMISSION SYSTEMS

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High-Voltage Direct Current (HVDC) transmission systems based on Voltage Source Converter (VSC) technology has attracted significant interest recently for transmitting large amounts of power over long distances using back-to-back or point-to-point configurations. VSC-HVDC has been addressed for various HV applications such as DC interconnections, Multi-Terminal HVDC Transmission (MT-HVDC), installation of off-shore wind power generation such as Europe super DC grid and installation of other renewable energy sources. Several classes of VSC topologies can be employed in HVDC systems including the conventional two and three-level converters, multilevel converters, and Modular Multilevel Converters (MMCs) that has been recently introduced and investigated for HVDC applications. MMC is penetrating the modern HVDC transmission market, due to its inherent features such as scalability, modularity, and fault ride through capability. Therefore, this thesis investigates and models a point-to-point VSC-based HVDC transmission system using nine-level MMC transient model, and 25-level MMC averaged model using MATLAB/Simulink platform to meet the requirements of HVDC systems such as HV requirements and fault ride through capability. However, a point-to-point HVDC system using conventional two-level converter is modeled and simulated using MATLAB/Simulink as a starting and benchmarking model. MMC transient model

employed in this study is based on Half-Bridge Sub-Modules (HB-SMs) due to its simple structure, yet, other structures are discussed. Nevertheless, balancing of the floating capacitors is one of the challenges associated with MMCs. Therefore, capacitor voltage balancing and its modeling is addressed. Then the average model of the MMC-based HVDC system is investigated. Moreover, the behavior during DC side faults is investigated, and the employment of hybrid DC circuit breakers and Hybrid Current Limiting Circuit (HCLC) are introduced for protection and limiting the DC fault current. This introduces a platform for studying large MMC-based HVDC systems in normal operation and during faults.

DEDICATION

This work is dedicated to my family for their continuous support.

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My sincere gratitude goes to my family and friends for their continuous support throughout my Master degree studies, especially their encouragement during my thesis work. Special thanks to my thesis supervisor Dr. Ahmed Massoud for his patience, guidance, support, encouragement, and for being always there for help. Many thanks to the Department of Electrical Engineering, faculty, and staff, for their support and encouragement. It has been a pleasure being a part of the department.

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LIST OF ABBREVIATIONS

HVDC	High Voltage Direct Current
VSC	Voltage Source Converter
VSC-HVDC	Voltage Source Converter-based High Voltage Direct Current
MT-HVDC	Multi-Terminal High Voltage Direct Current
MMC	Modular Multilevel Converter
SM	Submodule
HB-SMs	Half-Bridge Sub-Modules
FB-SM	Full-Bridge Sub-Modules
HCLC	Hybrid Current Limiting Circuit
IGBT	Insulated Gate Bipolar Transistor
HVAC	High Voltage Alternating Current
AVM-MMC	Modular Multilevel Converter Averaged Model
DCCB	Direct Current Circuit Breaker
CB	Circuit Breaker
LCC	Line Commutated Converter
CSC-HVDC	Current Source Converter-based HVDC
PWM	Pulse Width Modulation
PD-PWM	Phase Disposition Pulse Width Modulation
ST	Sending Terminal
RT	Receiving Terminal
$\boldsymbol{V_{DC}}$	DC link voltage
$\boldsymbol{f_s}$	Switching frequency

f_c	Corner frequency
PLL	Phase Locked Loop
θ_S	The phase angle of the ST voltage
V	The voltage amplitude of AC ST
$v_{S,abc}$	abc components of the sending terminal AC voltage
v_{Sdq}	dq components of the sending terminal AC voltage
$i_{S,abc}$	abc components of the sending terminal AC current
i_{Sdq}	dq components of the sending terminal AC current
P_S	Active power provided by the sending terminal
Q_S	Reactive power provided by the sending terminal
i^*_{Sdq}	Reference dq components of the sending terminal current
P^*_S	Reference active power provided by the sending terminal
Q^*_S	Reference reactive power provided by the sending terminal
$V_{R,DC}$	DC link voltage
$V^*_{R,DC}$	Reference DC link voltage
i^*_{Rdq}	Reference dq components of the receiving terminal current
P_R	Active power of receiving terminal
Q_R	Reactive power of receiving terminal
v_{Rdq}	dq-components of the receiving terminal voltage
v^*_{dq}	dq-components of reference modulation signals
v^*_{abc}	Reference abc modulation signal components
L_f	High pass filter inductor

C_f	LCL filter capacitor
L_{inv}	Inverter side inductor of the LCL filter
L_T	Grid side inductor of the LCL filter
L_{lim}	DCCB limiting reactor
L_{CL}	HCLC reactor
R_{CL}	HCLC Resistance
T_1, T_2	HCLC Thyristor Switches
v_j	Total Phase voltage
v_{jl}, v_{ju}	Upper and Lower SMs voltages of phase *j*
I_{ju}, I_{jl}	Upper and Lower arm currents of phase *j*
i_{ccj}	Circulating current of phase *j*
v_{armuj}, v_{armlj}	Upper and Lower arm voltage of phase *j*
i_{armuj}, i_{armlj}	Upper and Lower arm current of phase *j*
n	Number of SMs per arm
v_{cuj}, v_{clj}	Upper and Lower arm SM capacitor voltages
C_{arm}	Equivalent arm capacitance
n_u, n_l	Modulating signal
ω	Angular frequency
m_a	Modulation index
m_f	Frequency modulation index

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CHAPTER 1: INTRODUCTION

1.1. Background

Power transmission systems have experienced a development process from DC with Edison DC generators to AC and then to hybrid AC/DC transmission systems [1], [2]. Originally, DC transmission systems were not the best technical solution, as the technology was primitive and suffers from several drawbacks such as the absence of DC-DC transformers, which led to transferring power at low voltage levels over short distances [2]. Thus, the AC system was then adopted worldwide to operate power systems, as transformers allows stepping up the voltage level while transmitting power, to minimize the system losses [2]. Nevertheless, increasing the power demand, showed a number of concerns related to the AC transmission system such as synchronized operation of synchronous machines, voltage drop because of the transmission line reactance, transient stability and voltage stability [2]. Therefore, developing power transmission systems have become the main concern especially for long distances. Consequently, High-Voltage Direct Current (HVDC) technology was introduced and first used in 1954 in the under-sea cable interconnection between the island of Gotland (Sweden) and Sweden. In this HVDC transmission system, thyristors of the ratings 50 kV and 100 A were used [3]. Since 1954 until the mid of 1970s, the HVDC transmissions were based on mercury arc valves. However, in the following years, line commutated converters using thyristors were used in HVDC transmission systems [3],[2]. In 1990's, with the development of high-power semi-conductor switches (specially Insulated-Gate Bipolar Transistors (IGBTs)) and their availability at affordable prices, self-commutated converters (typically Voltage Source Converters (VSCs)) have been used for HVDC transmission, where the first VSC-HVDC

link came in service in 1999 [2],[3]. HVDC systems are considered a preferable technical solution for long cable connections compared to High-Voltage Alternating Current (HVAC) systems, because of the high charging current of AC cables. Also, the power oscillations of an AC grid can be damped by the fast modulation of the DC transmission system, and hence, improve the system stability [4],[5]. Furthermore, HVDC transmission systems offer fast and accurate control of power flow in contrast to HVAC systems. Another advantage of HVDC transmission systems is that inductive and capacitive parameters of overhead lines or cables do not limit the transmission capacity or the transmission distance unlike AC transmission links [5], [4]. In addition, HVDC transmission allows the connection of two AC systems of same or different frequencies [4],[5],[6]. The HVDC system is a highly efficient alternative for transmitting large amounts of power over long distances and for special purpose applications. As the future energy system is based on renewable energy sources, HVDC truly models the grid of the future [4] as, some renewable energy sources are located far away from the consumption area. For example, the installation of large-scale offshore wind farms [7], and the integration of solar energy in the Middle East and North Africa for the interconnection of Europe super DC grid (EUMENA) by 2050 as shown in Figure 1 in order to supply about 15% of the European electricity demand [8]. For such projects, HVDC transmission systems are technically and economically efficient more than HVAC systems [9]. Moreover, offshore power transmission using submarine cables became a crucial source for large-scale renewable energy sources because of the high wind speeds in offshore areas resulting in 70% energy greater than onshore [4]. The installation and connection of such offshore wind farms to the grid over long distances became much powerful and efficient

using VSC-HVDC transmission systems [10]. In addition, submarine power transmission cables have improved its capacity [11]. For example, the Basslink cable installed in 2005, was the world's longest HVDC cable at that time. However, a 580 km submarine cable in Norway – Netherlands system was completed in 2008 [11], [12]. Further improvements in submarine cable and interconnected grids encourage the mitigation of grids interconnection challenges.

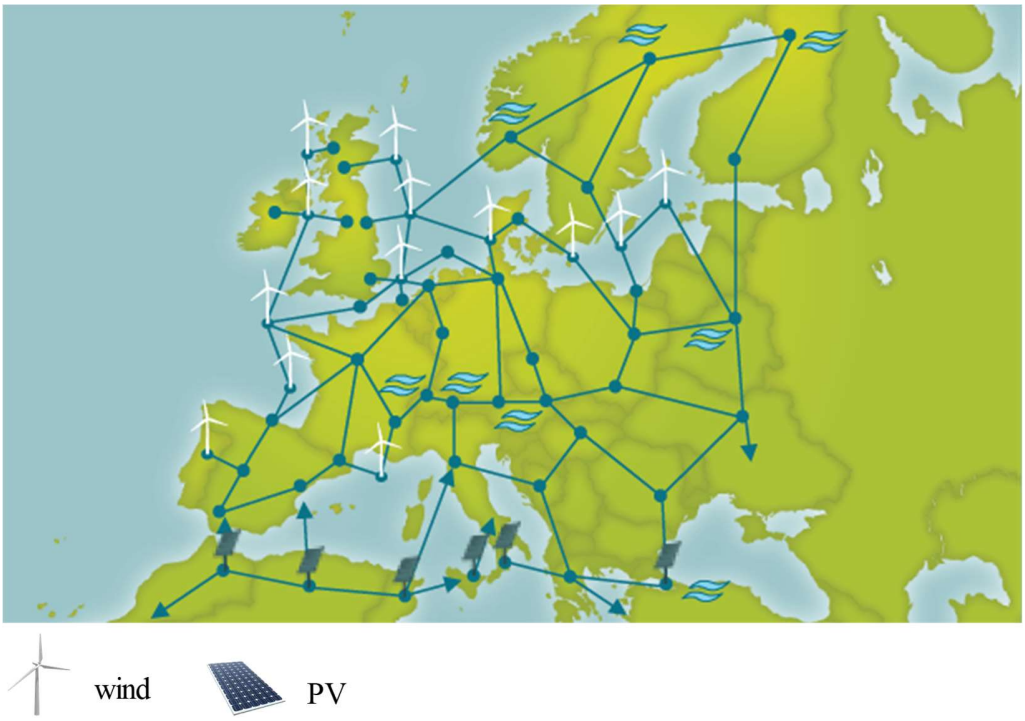

Figure 1: EUMENA Super DC Grid interconnection map [13]

From an economical point of view, and for short distances, HVAC systems are superior to HVDC, and this is basically due to the need for AC-DC and DC-AC converter stages in

HVDC. However, for long distances, HVDC systems are advantageous because HVAC transmission requires reactive power compensation, consequently more cost [3],[4],[5],[6]. Hence, the breakeven point is in the range of 40-70 km for submarine cables for the application of offshore wind energy in HVDC, and in the range of 400-800 km for overhead lines as displayed in Figure 2 [14].

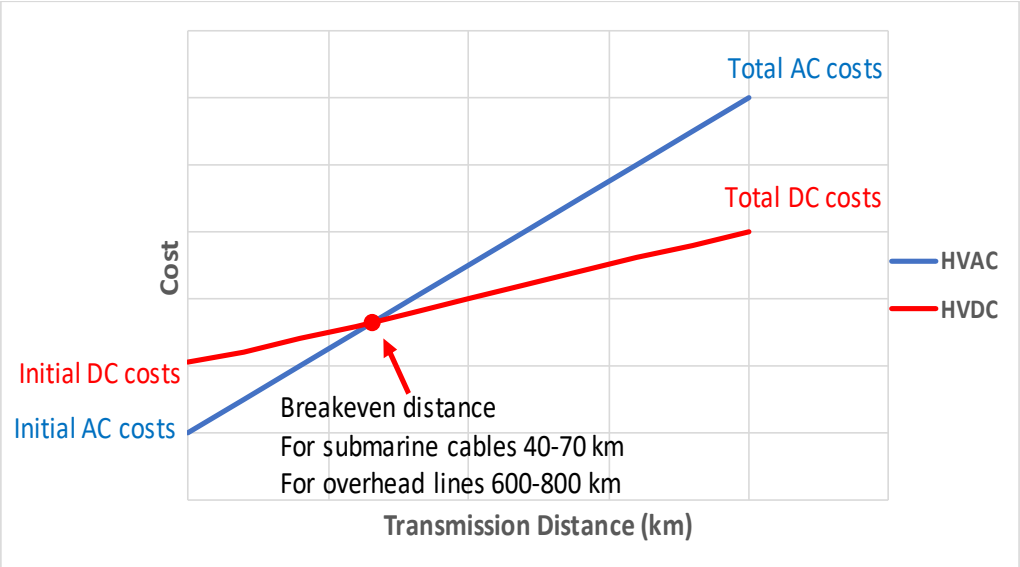

Figure 2: Breakeven Distance of HVDC against HVAC

As a conclusion to this comparison, HVDC transmission technology is attractive and advantageous for long power transmissions, bulk power delivery, submarine power and asynchronous interconnections [4], [15].

1.2. Thesis Objective

The objective of this thesis is to investigate and model a point-to-point VSC-based HVDC transmission system using Modular Multilevel Converter (MMC) transient model, and MMC averaged model. Considering the requirements of HVDC systems such as HV requirements and fault ride through capability. The design of the MMC transient model in this study is based on Half-Bridge Sub-Modules (HB-SMs) because of its simple structure. However, other structures are discussed highlighting their pros and cons. Nevertheless, balancing of the floating capacitors is one of the challenges associated with MMCs, therefore capacitor voltage balancing, and its modeling is tackled. Then the average model of the MMC-based HVDC system is explored, that presents a platform for studying large and multi-terminal HVDC systems. Also, the behavior during DC side faults is investigated, and the employment of hybrid DC circuit breakers and Hybrid Current Limiting Circuit (HCLC) are addressed. This introduces a platform for investigating and studying MMC-based HVDC systems in normal operation and during faults.

The thesis contribution can be stated as follows:

- Surveying and modeling of conventional VSC-based point-to-point HVDC systems
- Building a transient model for MMC-based point-to-point HVDC system considering nine-level as a case study.
- Building of an Averaged MMC model (AVM-MMC) considering 25-level as a case study.
- Building of a point-to-point VSC-HVDC transmission system model using an AVM-MMC.

- Employment of High-voltage DC side protection using hybrid DC Circuit Breakers (DCCB) and Hybrid Current Limiting Circuit (HCLC).

1.3. Thesis Outline

The thesis report is structured firstly with an introductory overview of the requirements and the importance of HVDC transmission systems in chapter 1. This is followed by a literature survey on the history of HVDC systems and their topologies in chapter 2. A two-terminal two-level converter-based HVDC system model is presented, and a DC side fault is introduced to the HVDC system in chapter 3. In chapter 4, a model of the two-terminal MMC-based HVDC system is presented as well as, a comprehensive study and modeling of HB-MMC including balancing the SM capacitor voltages. In addition to studying the MMC-HVDC under DC side fault, an MMC Averaged Model (AVM-MMC) is presented, and a two-terminal AVM-MMC HVDC is studied in chapter 5. Chapter 6 presents a comparison between the different VSC topologies introduced in this study to model a back-to-back or point-to-point HVDC transmission system. Finally, conclusions and further improvements are presented.

CHAPTER 2: VSC-BASED HVDC SYSTEMS

2.1 VSC-HVDC Systems

HVDC transmission systems are considered a promising power transmission technology, especially for long distances. With the great development of the VSC technologies (namely topologies, control, and semiconductor devices), the field of applications of VSC-HVDC transmission systems and Flexible AC Transmission Systems (FACTS) are expanded in power systems. VSC-HVDC systems combine VSC with DC transmission lines to transmit power up to several GWs [16]. VSC-HVDC is considered one of the preferred solutions for DC interconnections, Multi-Terminal Direct Current (MT-HVDC) transmission, and installation of offshore wind power generation [15], [17-20]. VSC-HVDC systems are superior to classical HVDC systems (i.e. line commutated converters HVDC systems) for the following advantages [3], [5],[21-25]:

- It can independently control active and reactive powers at both terminals by sustaining stable voltage and frequency [22], which enables the supply of weak grids and even passive networks [16].
- The commutation failures caused by disturbances in the AC network can be avoided by using VSC-HVDC technology [3], [21], [23].
- Black start capability [5].
- VSC technology does not require large AC filters, which enables the design of compact converter station [24].
- As it has a standardized construction, the converter system can be easily installed and replaced [5].

2.1.1. Applications of VSC-HVDC systems

The HVDC market is growing rapidly and has become an important part of many transmission grids through overhead lines and submarine cables. It allows the connection of remote generations, interconnecting grids, connecting offshore wind turbines, connecting remote loads, transmitting power from offshore and stabilization of power flow. ABB is a leading company in the field of HVDC systems, for more than 60 years of HVDC experience and more than 170 projects worldwide [4]. Several VSC-HVDC systems developed by ABB under the name HVDC Light. Some recent projects of ABB are listed here [4]:

- BorWin1, which is one of the most remote offshore wind farm generations in the world, has been connected to the German grid through 400 MW +/- 150 kV two-level VSC-HVDC in 2010.
- Also in Ireland, ABB has grid-integrated a 500 MW two-level VSC-HVDC through +/-200 kV submarine cables in 2013. This HVDC link provides an opportunity to export excess power into the UK market.
- Moreover, ABB is integrating a 410 MW HVDC station that connects Kriegers Flak offshore-grid to the German grid in Bentwisch, northern Germany by the end of 2018. This interconnection through HVDC system helps securing the energy supply in Denmark and supports the energy trading in Germany.
- ABB is integrating the first 1,100 kV UHVDC power link in China that transmits power from the Xinjiang region in the Northwest, to Anhui province in eastern China, and sets a new world record in terms of voltage level, transmission capacity and distance in 2016. This system is capable of transmitting 12 GW over a distance of around 2000 km–

3000 km. This facilitates transmitting power over greater distances and grid interconnection.

Another leading company in the HVDC market is Siemens. VSC-HVDC systems developed by Siemens are called HVDC Plus ("Plus" -Power Link Universal Systems) [26], which have projects worldwide such as [22]:

- ALEGrO interconnector project: installing the two MMC-HVDC converter stations for the first electricity interconnection between Germany and Belgium along 90 km distance with a capacity of 1000 MW through underground cable by 2020.
- ElecLink interconnector project: to increase the capacity of the existing interconnection between Britain and France by 50%, using MMC-HVDC system with a rating of 1000 MW and ± 320 kV DC link, linked by a 51 km long DC power cable, which will be fully commissioned by 2020.

ALSTOM is another leading company in HVDC and UHVDC market for over 50 years, which plays a role in the development of HVDC networks and connections in the coming years [27]. The company has delivered more than 40 projects over the world. Some of the projects developed by ALSTOM worldwide are as presented in Figure 3 and the following points:

Figure 3: ALSTOM HVDC projects worldwide [28].

- In 2015, ALSTOM was awarded a contract to build an HVDC transmission link between France and Italy using ALSTOM's VSC MaxSine technology which is MMC technology with ratings of 2×600 MW of power and ±320kV voltage level.
- ALSTOM has installed a multi-terminal HVDC grid from Sweden's south-west link to central and southern networks of Sweden using ALSTOM's VSC MaxSine technology (MMC) by 2014 for a total distance of 250 km delivering power of 1440 MW and ±300 kV voltage level.
- The Dolwin3 HVDC project using ALSTOM's VSC MaxSine technology (MMC) to install the third grid in the Dolwin cluster connecting 900 MW offshore wind energy from the North Sea to the German grid over a distance of 162 km by 2017.

2.1.2. VSC-HVDC system structure

VSC is the main block for a specific class of HVDC converters. The first generation technology uses two-level or there-level converters, because of the simple structure and less capacitors. However, this configuration suffers from the series connection of semiconductor devices' problems (static and dynamic voltage sharing), high switching losses, high *dv/dt,* hence introduces high harmonic levels and poor output voltage waveform [28], [29-30]. The basic configuration of a VSC-HVDC system is the two-terminal HVDC system. This configuration consists of two VSC stations linked by a DC transmission line as shown in Figure 4. Mainly, there are two schemes for two-terminal HVDC transmissions, which are point-to-point scheme and back-to-back scheme. Point-to-point transmission is used for long distances transmission through overhead line, underground or submarine cables also for grid interconnection between asynchronous AC systems [31]. However, back-to-back transmission scheme is mostly used to link two asynchronous AC systems at the same station.

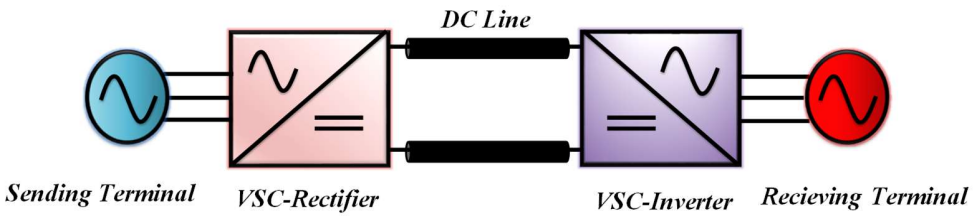

Figure 4: Two-Terminal VSC-HVDC transmission scheme

Similarly, an MT-HVDC system can be implemented but using more than two VSC stations. There are three main configurations for MT-HVDC transmission, which are series, parallel, and meshed configurations as shown in Figure 5, Figure 6, and Figure 7, respectively. The parallel configuration has several advantages when compared to the series configuration such as less insulation complexity and more reliability in case one of the converters is lost. Therefore, in practice parallel configuration is highly preferred [2]. On the other hand, the meshed HVDC topology is used when more than three converter stations are interconnected through DC link. This topology provides some benefits as higher reliability. Also, meshed topology provides increased transmission capacity. However, the enhancement of the meshed HVDC topologies has been braked by the unavailability of the HVDC Circuit Breakers (CBs) in the market. Nevertheless, ABB has introduced hybrid HVDC CB as in [31], [32] thus; it is expected that the meshed topology will be utilized as the HVDC CBs are improved. Although, MT-HVDC is out of the thesis scope, the contribution presented in the thesis provides a platform for studying such complicated systems.

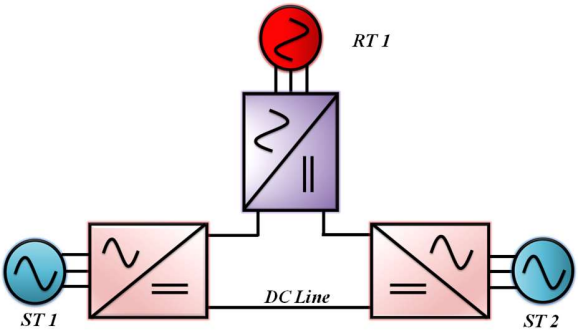

Figure 5: MT-HVDC series configuration

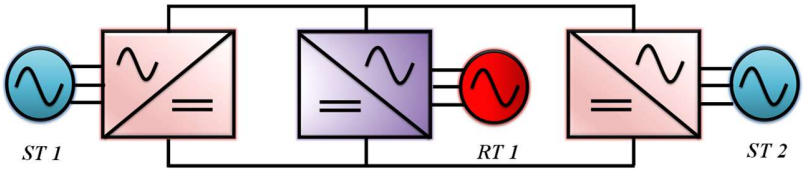

Figure 6: MT-HVDC parallel configuration

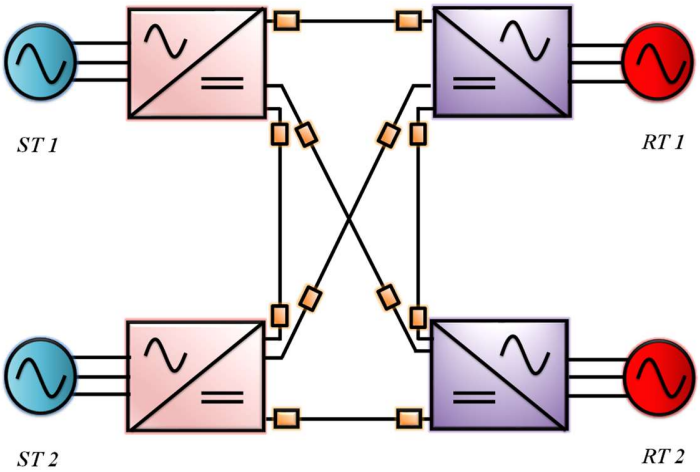

Figure 7: MT-HVDC meshed configuration

2.2. Two-Level Inverter HVDC system

The development of the VSC technologies with off-the-shelf semiconductor devices is significantly expanding the applications of HVDC transmission systems. The first generation of VSC-HVDC has been introduced and manufactured by ABB [33]. This generation utilizes the two-level converter topology. This topology is the basic configuration of a VSC. It consists of six semiconductor devices (mostly IGBTs) with their six antiparallel diodes as shown in Figure 8. The drawbacks of this configuration are that it produces high harmonic distortion, and it causes high stresses on the switches especially in HVDC applications due to HV requirements. Typically, a series connection of multiple IGBTs allows meeting the requirements of high DC transmission voltage [33], [34]. However it introduces another problem, which is the voltage sharing of the switches at both static and dynamic phases. Therefore, multilevel converters have attracted significant interest in the last three decades, particularly for high power applications. Typically, multilevel converters consist of semiconductor devices, and voltage clamping approaches as isolated power supplies in cascaded H-bridge multilevel converter, didoes in diode-clamped multilevel converter [35], [36] and capacitors in flying capacitor multilevel converter [37],[38]. Nevertheless, increasing the number of levels increases the complexity of control and implementation [39]. Based on this, a new type of multi-level converters, Modular Multilevel Converter (MMC) [40], [41] has been developed to overcome the limitations of other multilevel converters specially in high power applications, considering the requirements of semiconductor devices and passive elements, the required isolated DC supplies, modularity, and capacitor voltages' balancing. Therefore, MMC is advantageous due to its scalability, modularity, and fault ride through

capability [42],[43],[44].

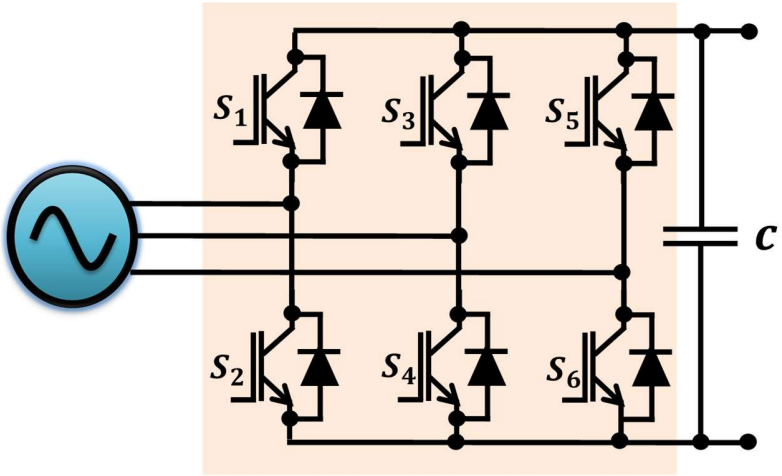

Figure 8: Two-level VSC configuration

2.3. MMC-Based HVAC

2.3.1. MMC

MMC is considered as a potential candidate for high power applications, due to its modularity and scalability. In addition, filter requirements can be significantly reduced by using a high number of levels per phase [16]. Scalability to higher voltages is easily achieved, and reliability is improved by increasing the number of SMs per arm [45]. Also, conventional VSCs use concentrated reservoir capacitors at the converter DC input, while MMC uses distributed capacitors that improve the flexibility of the VSC-HVDC transmission systems [46]. For the aforementioned reasons, MMC has become the preferred topology for large-scale HVDC links and DC grids that could ensure safe and

reliable operation during AC and DC network disturbances [46].

MMC employs multiple SMs connected in series from their AC side terminals in order to construct a multilevel AC voltage waveform. Each phase or leg has upper and lower arms; each arm is constructed by (N-1) SMs connected in series for N-level MMC. Every arm has an inductor to protect the switches from the inrush current caused by the capacitors as well as to limit the circulating current during normal operation [47]. In general, the number of cells in an MMC is dependent on the DC link voltage and the ratings of each cell. SMs can be constructed using Half-Bridge SM (HB-SM) [48],[49], Full-Bridge SM (FB-SM) [48],[49], Clamped Diode SM (CD-SM) [49], Switched Capacitor SM (SC-SM) [48] or other combined topologies as in [48]. The typical structure of an MMC is shown in

In this study, HB-SMs are used to model the MMC. Each HB-SM is a simple chopper cell composed of two semiconductor devices S_1 and S_2, two anti-parallel diodes $D_1$and D_2, and a capacitor C.

Due to the required enormous number of cells in MMC for HVDC applications, MMC modeling has been addressed widely in the literature. In [50], an improved transient simulation model for the HB-SM and FB-SM-based MMCs that can be used for full-scale simulation of HVDC transmission systems, with hundreds of cells per arm, has been introduced. In [51], the dynamic performance of MMC-based, back-to-back HVDC system using Phase Disposition (PD) Sinusoidal Pulse Width Modulation (SPWM) strategy, including a voltage balancing method, for the operation of an MMC has been presented. However, in [52] a comparative study of the dynamic performance of conventional VSC-HVDC and MMC-based HVDC operating in back-to-back configuration has been addressed. Furthermore, a novel high frequency conducted Electro-Magnetic Interference

(EMI) for an MMC-based HVDC system has been proposed in [53]. Based on the proposed model, the influence of parasitic parameters of the switches and the switching frequency on the leakage current has been also studied in detail. In this thesis, a point-to-point VSC-based HVDC transmission system using MMC transient model and AVM-MMC-based HVDC systems are modeled and simulated using MATLAB/Simulink platform, where the design of the MMC transient model in this study is based on HB-SMs. Hence, SM capacitor voltage balancing and its model is addressed. Also, the behavior during DC side faults is investigated, and the employment of hybrid DC circuit breakers and Hybrid Current Limiting Circuit (HCLC) are addressed as in the following chapters.

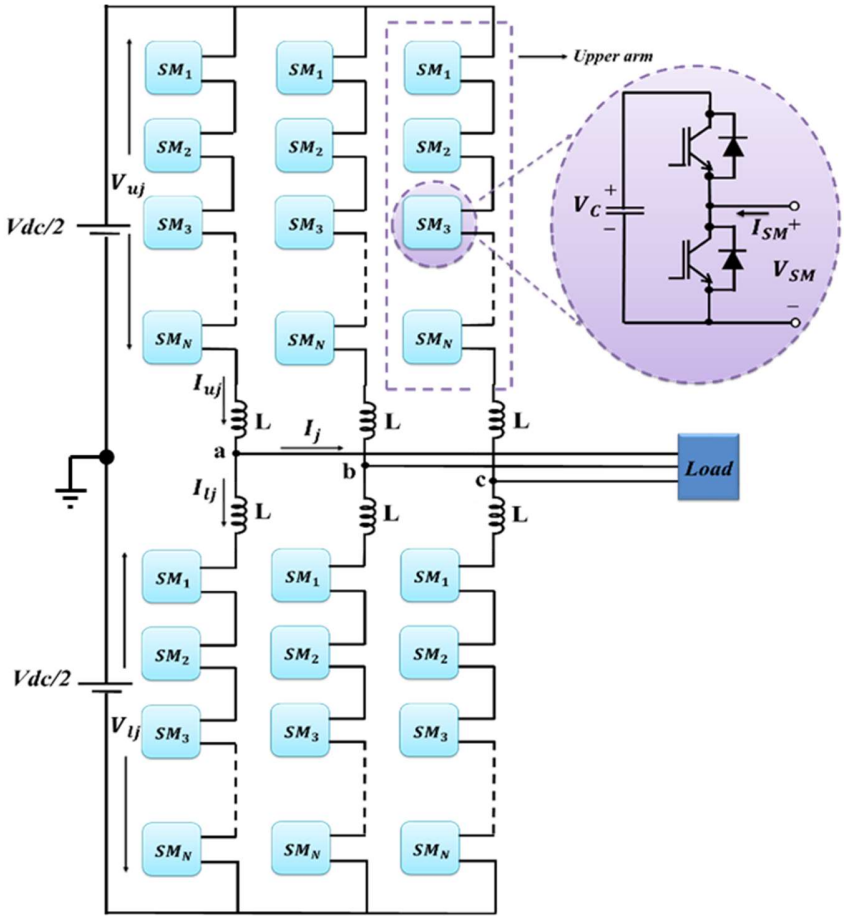

Figure 9: Modular multilevel converter structure

2.3.2. MMC during fault at DC side

HB-SMs and FB-SMs are commonly used SMs in MMCs. Generally, HB-SM is the simplest configuration. Hence it offers less losses and lower cost. The FB-SM is well known for its bi-direction AC voltage, and most importantly, it offers blocking capability for the contribution of AC side current due to a fault in the DC side. Unlike, the HB-SM and the conventional two-level VSC, where a DC short circuit fault is a critical scenario for VSCs [54].

The effect of DC side faults on the conventional two-level VSC-HVDC system has different analysis from the one based on MMC. In the case of two-level VSC, the IGBT switches are blocked for self-protection, leaving the freewheeling diodes subjected to overcurrent due to the AC grid current contribution into DC fault as shown in Figure 10 [48-50],[55]. An overview of the present methods for VSC system protection has been studied in [4], [55]. Based on this, DC Circuit Breakers (CBs) are required to protect the system. However, DC CBs for HV applications are not mature as AC HV CBs [54], [55]. Another alternative, in this case, is the installation of press-pack thyristors at the AC side of the system, in order to share the short-circuit current with the diodes until the AC CBs trips, as thyristors are known for their capability to withstand surge current [54-57]. But, also AC CBs are not considered fast enough, and the power electronic devices can be damaged because of the increase in the fault current [56].

On the other hand, MMC is more advantageous when compared to conventional and other multilevel VSCs, as some SMs are defensive against DC side faults such as: FB-SM [54], CD-SM [55], SC-SM, mixed cells-based MMC [8], [9], [54], boost/buck-boost SM [54], [49]. These SMs have the ability to suppress the DC side fault because of the existence of opposing capacitor voltage after the IGBTs are turned off due to the fault such as FB-SM and CD-SM shown in Figure 11 and Figure 12 [54], where, the figures show the different current paths in each topology during the fault. It is clear that the SM capacitor is included in all paths except in the HB-SM topology, which explains why some SMs have fault blocking capability among others. But, this is at the expense of a large number of employed switches, which increases the losses, cost, and size [49], [58]-[59]. Nevertheless, HB-SM-based MMC is one of the most promising HVDC converters, although HB-SM does not

have the ability to inherently block the DC fault current. When DC fault is detected, and IGBTs are switched off typically the diodes are exposed to high fault current due to the contribution of the AC grid current as illustrated in Figure 13. To limit this, a proper design of the arm inductor can help avoiding this issue in MMCs [54]. Yet, HVDC CBs will be a necessity for interrupting the fault.

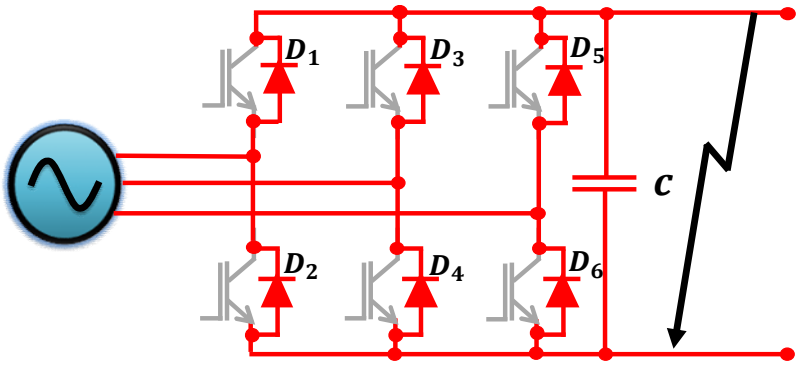

Figure 10: DC side fault in two-level converter

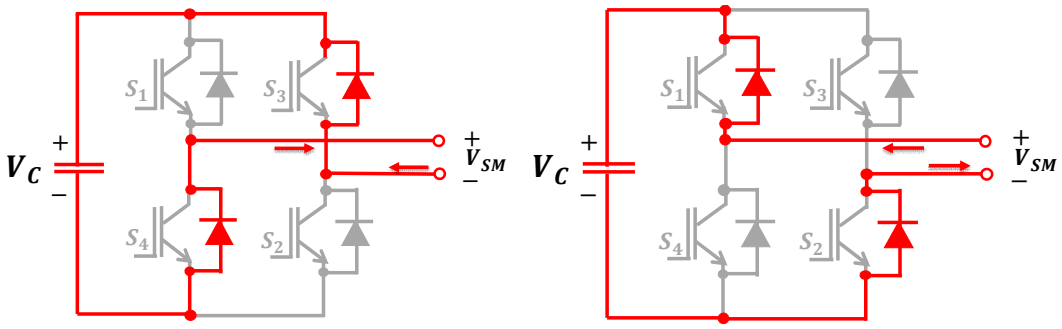

Figure 11: FB-SM possible current paths during a DC side fault

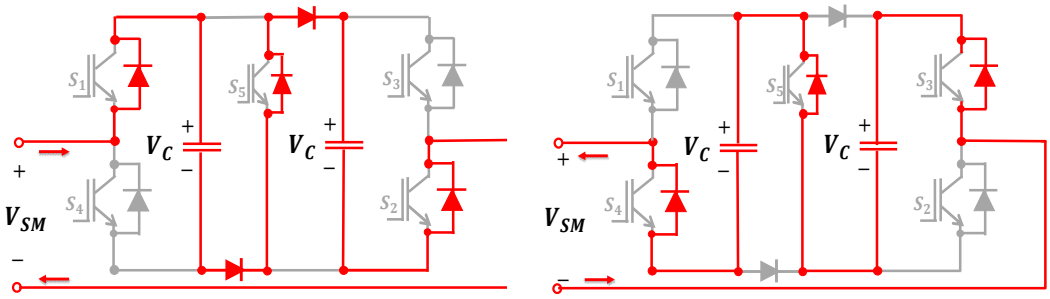

Figure 12: CD-SM possible current paths during DC side fault

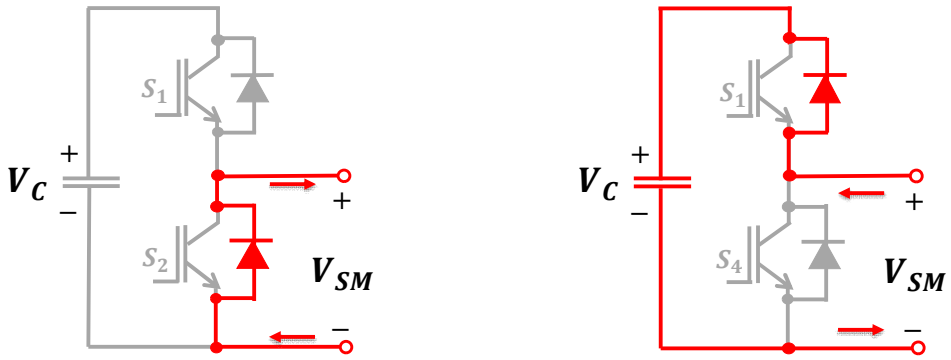

Figure 13: HB-SM current path during DC side fault

2.4. Conclusion

In conclusion, in this chapter the VSC-based HVDC system has been addressed, and the advantages of VSC-HVDC over the classical HVDC using LCC have been identified, highlighting, some of the recent worldwide projects that have been developed by the major

companies in the area of HVDC systems such as ABB, Siemens, and ALSTOM. Also, the typical structure of a VSC-HVDC has been discussed, including modeling of VSC topologies used in this study which are a two-level converter, and detailed MMC. Furthermore, studying the dynamic behavior during DC side faults.

CHAPTER 3: TWO-TERMINAL TWO-LEVEL VSC-BASED HVDC SYSTEM

Two-terminal VSC-HVDC system can be implemented using different types of VSCs (two-level or multilevel VSCs). This chapter studies the implementation of the conventional two-level VSC in two-terminal HVDC systems. In addition, MMC and AVM-MMC are studied in the following chapters.

3.1. System overview

The two-terminal bipole HVDC system basically consists of two back-to-back connected VSCs, transformers, phase reactors, AC filters, DC capacitors, and DC transmission lines as shown in Figure 14. Two-level VSC technology is widely used in many applications at a wide range of power. This converter is constructed from six IGBTs connected with antiparallel diodes as illustrated earlier in Figure 8. It is capable of generating two output voltage levels $\pm V_{DC}$, where V_{DC} is the DC voltage. One converter operates as a rectifier in the Sending Terminal (ST) and the other as an inverter in the Receiving Terminal (RT). Several PWM techniques can be used for VSCs to generate the desired switching pattern.

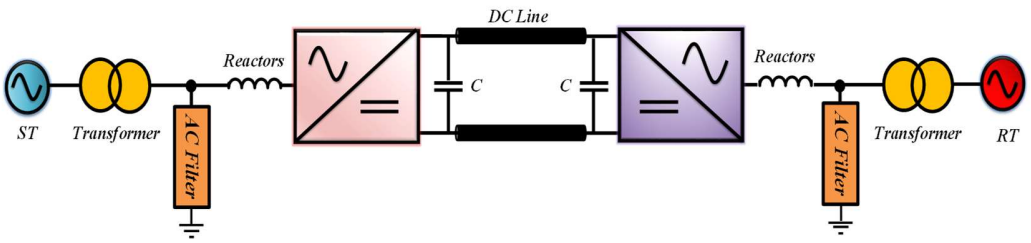

Figure 14: Two-terminal VSC-HVDC system.

Second, transformers are required to connect the VSC to the grid. Most importantly, phase

reactors and AC filters have to be installed, in which phase reactors reduce the AC current harmonics caused by the switching operation of the VSCs [60]. However, high pass filter is tuned and installed to mitigate the high order current harmonics generated by the converters [60]. The passive filter implemented in this study acts as an LCL filter with embedded high pass filter. This is because of the existence of the transformer's leakage inductance as in Figure 15, where $L_{inv}, L_T, L_f, R_f, and\ C_f$ are inverter side inductance (reactor), transformer's inductance, and shunt high pass filer inductance, resistance and capacitance, respectively.

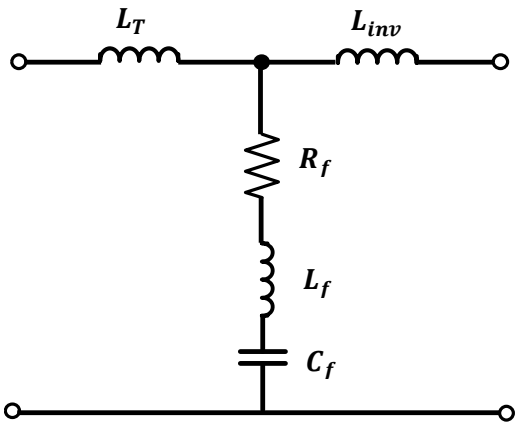

Figure 15: LCL Passive filter used in the Study

The high pass filter is tuned at both switching frequency f_s as in (1), and the LCL filter is tuned at corner or resonance frequency f_c as in (2) [61],[62]:

$$f_s = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (1)$$

$$f_c = \frac{1}{2\pi\sqrt{\frac{L_{inv}L_T}{L_{inv}+L_T}C_f}} \quad (2)$$

Moreover, DC capacitors are used to keep the power balance between transients and reduce the voltage ripples on the DC side that is caused by the switching action [60]. Finally, back-to-back connected VSCs are connected through DC transmission line. DC transmission lines are considered an essential link in HVDC transmission systems. In a transmission line, the resistance, inductance, and capacitance are uniformly distributed as cascaded π network representation along the line. However, in steady state ,a resistor can be used to represent the DC transmission line [60],[63].

3.2. Control of Two-terminal two-level VSC-based HVDC system

A two-terminal VSC-HVDC system is mainly used to transmit power from one AC network known as Sending Terminal (ST) to another AC network known as Receiving Terminal (RT). The power flows from the ST, which is rectifier towards the RT, which is inverter. This study adopts the method of coordinate transformation from three-phase stationary frame to two-phase synchronously rotating reference frame, i.e. dq-axes, that are then converted back to three-phase coordinates. The generated continuous signal is the modulation signal that is used later to perform the Sinusoidal Pulse Width Modulation (SPWM) that controls the semi-conductor switches used (i.e. the IGBTs). The cascaded control structure used provides tracking, as the objective of the inner control loops is to adapt with the reference dq currents at both the sending and receiving terminals in order to exchange the desired amount of power between both terminals. Nevertheless, the outer

control loop produces the reference dq currents based on the reference powers and DC link set in order to regulate the actual dq currents to be equivalent to the reference values.

3.2.1. Control of Sending Terminal Converter

The main advantage of VSC-HVDC systems is that it provides independent control of active and reactive powers. The ST generally can be connected to an AC grid or offshore wind energy system; however, it is represented here typically as AC grid. The ST mainly is responsible for controlling the active and reactive powers. Therefore, the three-phase currents and voltages are transformed to dq reference frame using Park's transformation as in (3-4). Using the dq reference frame gives the advantage of decoupling the active and the reactive powers, where the d-component is responsible for the active power transfer. However, q-component is responsible for the reactive power transfer. The final step of the control is to transform the d and q components into three-phase quantities as illustrated in Figure 16.

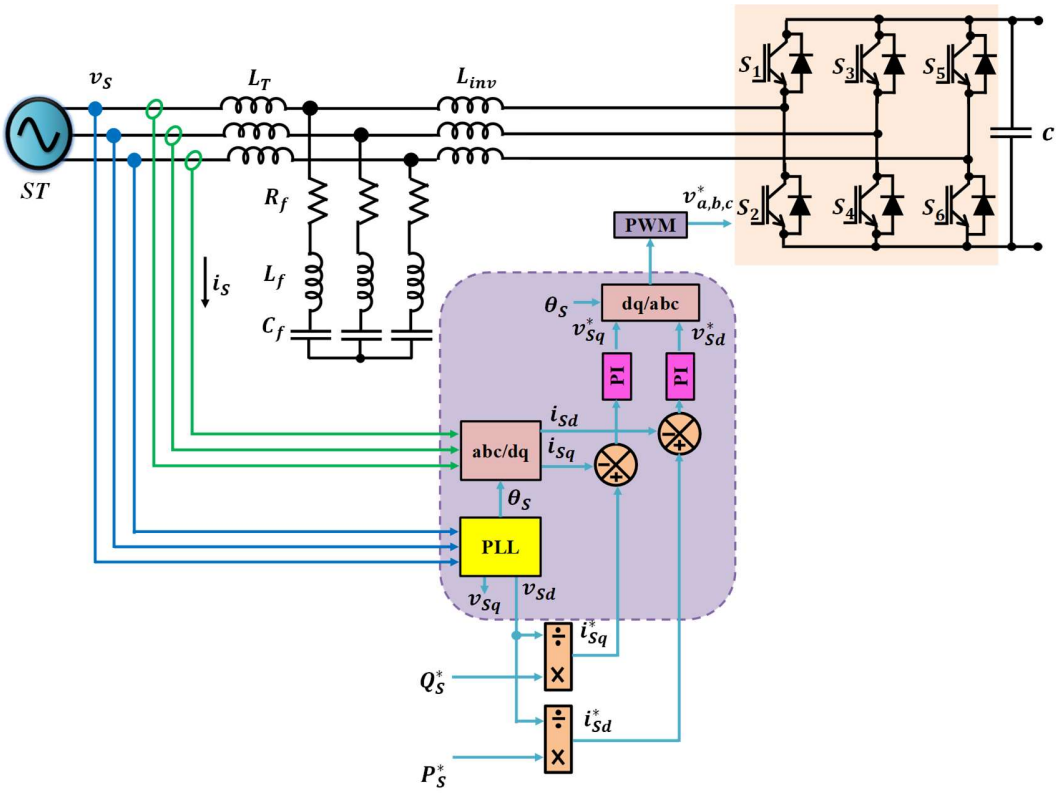

Figure 16: Sending end control scheme

The AC network of the ST is represented by equation (3)

$$v_S = \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} = \mathrm{V} \begin{bmatrix} \sin(\theta_S) \\ \sin(\theta_S - \frac{2\pi}{3}) \\ \sin(\theta_S + \frac{2\pi}{3}) \end{bmatrix} \quad (3)$$

Where v_{Sa},v_{Sb}, v_{Sc} are the ST three-phase voltages, θ_S is the phase angle of the ST voltage, and V is the voltage amplitude.

Applying Park-Clarke transformation, to convert the three-phase stationary reference frame abc to the two-phase rotating frame dq. Equation (4) represents the abc to dq transformation, in which the zero component is zero as it is a three-wire three-phase

balanced system [60], [62].

$$v_{Sdq} = \begin{bmatrix} v_{Sd} \\ v_{Sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta_S) & \sin(\theta_S - \frac{2\pi}{3}) & \sin(\theta_S + \frac{2\pi}{3}) \\ \cos(\theta_S) & \cos(\theta_S - \frac{2\pi}{3}) & \cos(\theta_S + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} \quad (4)$$

Where v_{Sd}, v_{Sq} are the dq components of the ST voltage. Similarly, the dq components of the currents are obtained as in (5):

$$i_{Sdq} = \begin{bmatrix} i_{Sd} \\ i_{Sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta_S) & \sin(\theta_S - \frac{2\pi}{3}) & \sin(\theta_S + \frac{2\pi}{3}) \\ \cos(\theta_S) & \cos(\theta_S - \frac{2\pi}{3}) & \cos(\theta_S + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} \quad (5)$$

Where i_{Sa}, i_{Sb}, i_{Sc} are the ST three-phase currents.

As the v_{Sq} is zero, the ST powers can be obtained by (6) and (7), also the reference dq-component currents can be obtained by (8) and (9) [62]:

$$P_S = v_{Sd}.i_{Sd} \quad (6)$$

$$Q_S = -v_{Sd}.i_{Sq} \quad (7)$$

$$i^*_{Sq} = \frac{-Q^*_S}{v_{Sd}} \quad (8)$$

$$i^*_{Sd} = \frac{P^*_S}{v_{Sd}} \quad (9)$$

Where P_S, Q_S, i^*_{Sd}, i^*_{Sq} are the active power, reactive power, and reference dq-component currents of the ST, respectively.

3.2.2. Control Of Receiving Terminal Converter

The Receiving Terminal (RT) converter mainly controls the reactive power and the DC link at the RT as shown in Figure 17. At the ST, the reference d-component current of ST i_{Sd}^{*} is generated by setting the reference active power. However, in the RT, i_{Rd}^{*} is regulated such that the DC voltage at the RT, $V_{R,DC}$ matches a reference voltage $V_{R,DC}^{*}$. In this study, active power is transmitted at unity power factor thus i_{Sq}^{*} and i_{Rq}^{*} are set to zero by setting the reference reactive powers of both terminals to zero.

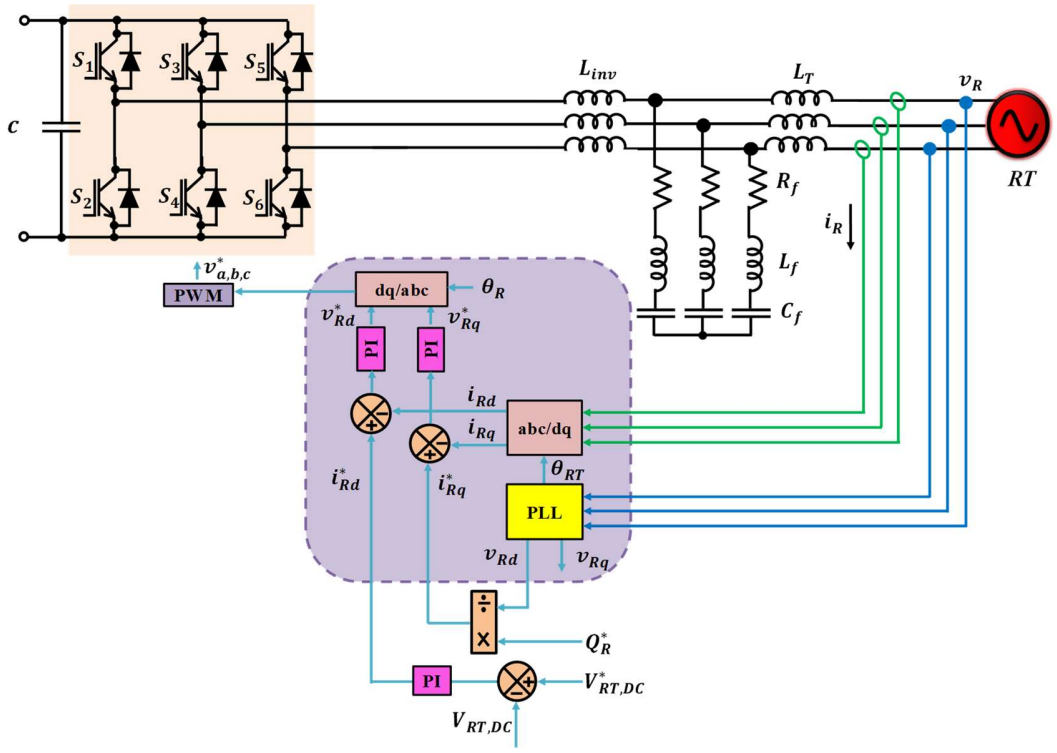

Figure 17: Receiving end control scheme

Following the same procedure to obtain the powers at the RT as given by (10) and (11), also the reference q-component current can be obtained by (8) and (9) as shown in (12) below:

$$P_R = v_{Rd}.i_{Rd} \tag{10}$$

$$Q_R = -v_{Rd}.i_{Rq} \tag{11}$$

$$i_{Sq}^* = \frac{-Q_R^*}{v_{Sd}} \tag{12}$$

where v_{Rd}, i_{Rd}, i_{Rq}, P_R,Q_R , i_{Sq}^*, Q_R^* are the d-component of the voltage, the d-component of the current, the q-component of the current, the active power, the reactive power of the RT, the reference q-component current of the ST and the reference reactive power of the RT, respectively. Finally, the adjusted dq components are transferred back to abc as in (13), in order to be fed to the PWM as reference signals to get the desired switching pattern.

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ \sin(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \tag{13}$$

Where, v_a^*, v_b^*, v_c^* are the reference abc components used as modulation signals and v_d^*, v_q^* are the reference dq-components of those modulation signals.

3.2.3. Simulation Results

The two-terminal VSC-HVDC system has been modeled and simulated using MATLAB-Simulink platform. In this study, the LCL filter is designed based on (1) and (2) mentioned earlier in this chapter. As the switching frequency of the system is assumed 2 kHz, the

corner frequency is located between the fundamental and the switching frequencies to avoid any resonance. Assuming that $f_c = 250\,Hz$, the values of L_f and C_f could be designed based on (1) as follows: Assume that C_f = 100μF, then $L_f = 0.0634\,mH$. Let $L_{inv} = L_T$ = 8 mH according to (2). The overall system's parameters referring to [62] are as presented in Table 1. In this study, active power is transmitted however, reactive power, is set to zero. Also, the DC link at the RT is regulated at a pre-determined reference value. Figure 18 and Figure 19 represent active and reactive powers respectively against their pre-determined reference value. At steady state, the active power of the ST becomes equivalent to the reference value P_{ST}^{*}. In addition, Figure 20 and Figure 21 show the dq currents respectively versus their reference value. However, Figure 22 represents active and reactive powers of the ST and RT. The reactive power of both terminals is set to zero equivalent to the reference value. Figure 23 represents the dq currents of both ST and RT, where they perform similar to their corresponding power.

Table 1: VSC-HVDC System's Parameter

Parameter	Value
Grid Voltage (line-line)	400 kV
Fundamental Frequency	50 Hz
Switching Frequency ($\boldsymbol{f_s}$)	2 kHz
DC Voltage	640 kV
AC Line Damping Resistance (R)	1 Ω
LCL Filter Inductance ($\boldsymbol{L_g, L_{inv}}$)	8 mH
LCL Filter Capacitance ($\boldsymbol{C_f}$)	100 μF
High pass Filter Resistance ($\boldsymbol{R_f}$)	0.01 Ω
High pass Filter Inductance ($\boldsymbol{L_f}$)	0.0634 mH
DC Capacitance ($\boldsymbol{C}$)	94 μF
DC Line Resistance	0.0121 Ω/km
DC Line Length	400 km
DCCB limiting reactor	20 mH

The system is tested for the following case:

$$P_S^* = \begin{cases} 800\ MW & 0 \le t < 2\ s \\ 2\ GW & 2 \le t \le 4\ s \end{cases}$$

$Q_S^* = Q_R^* = 0$ MVAR,

$V_{R,DC}^* = 640$ kV

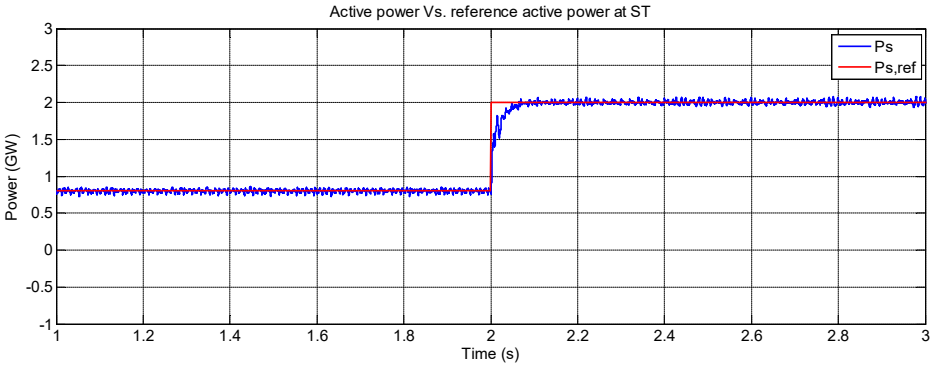

Figure 18: Active power and reference active power at ST

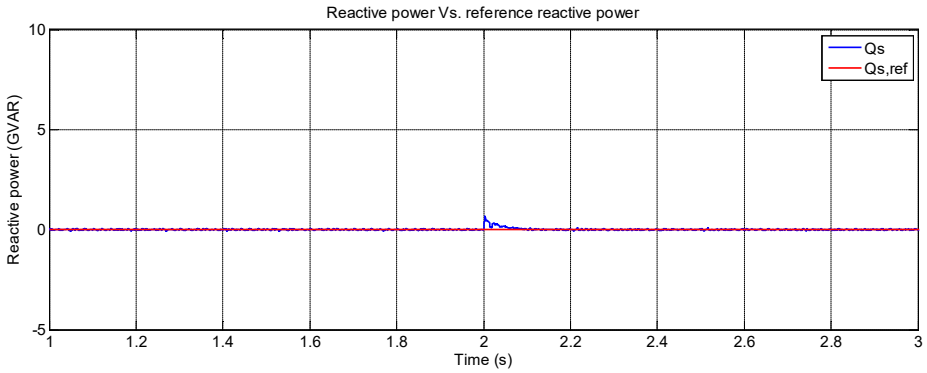

Figure 19: Reactive power and reference reactive power at ST

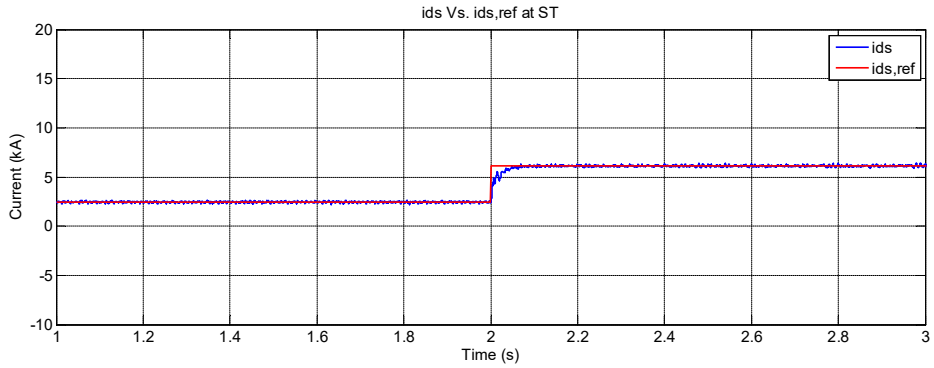

Figure 20: d-component current and reference d-component current at ST

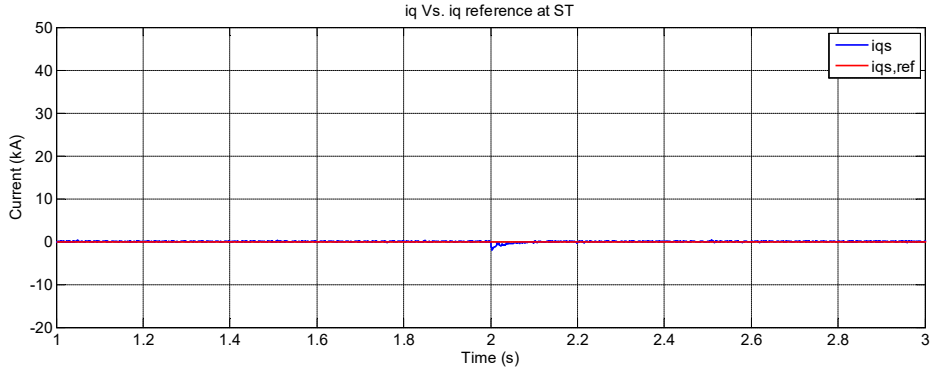

Figure 21: q-component current vs. reference q-component current at ST

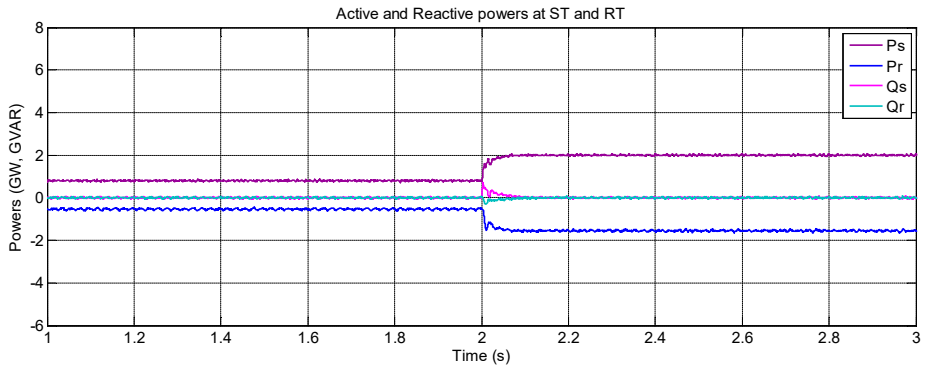

Figure 22: Active and reactive powers of ST and RT

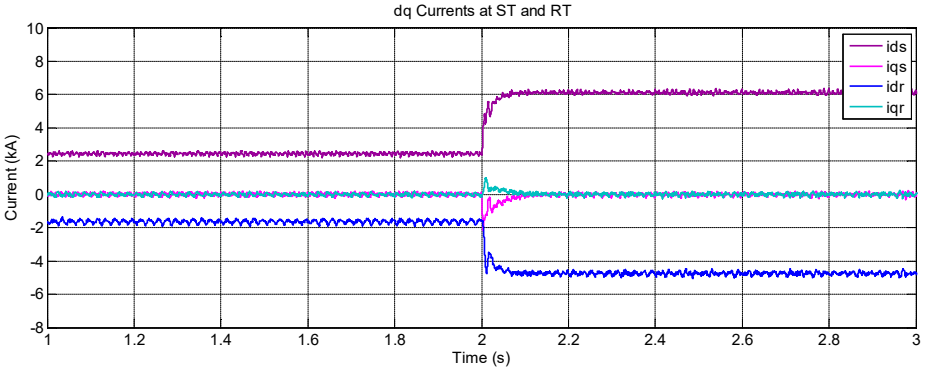

Figure 23: dq Currents of ST and RT

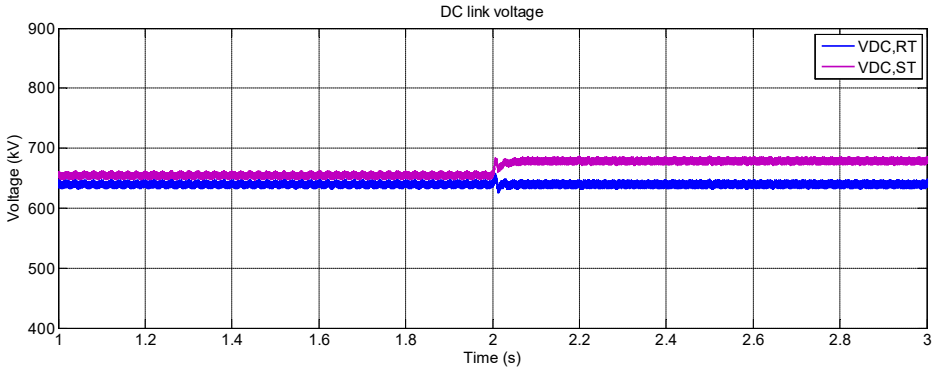

Figure 24: DC voltages of ST and RT

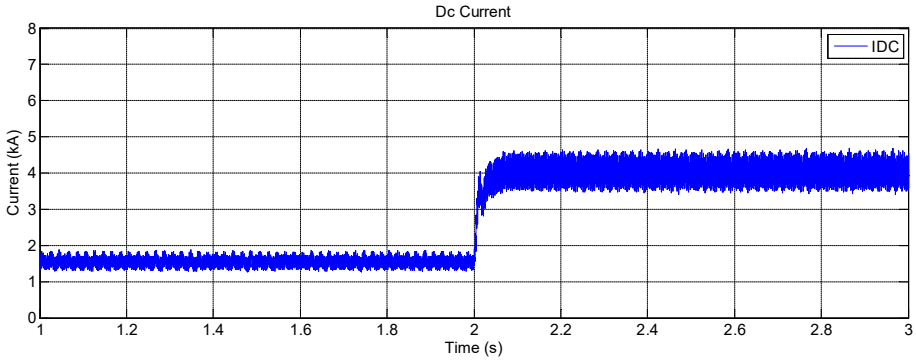

Figure 25: DC current

Figure 24, shows the DC voltages of the ST and RT. The DC voltage at RT is kept constant at the reference value while a slight change occurred at the ST DC link due to, the change in the reference power. Figure 25 represents the DC current through the DC transmission line from ST to RT. A step change is shown clearly in the DC current, that represents the change in the power flowing from ST to RT. Figure 26 and Figure 27 show the three-phase

current and voltage at ST. In addition to, the three-phase current and voltage of RT shown in Figure 28 and Figure 29.

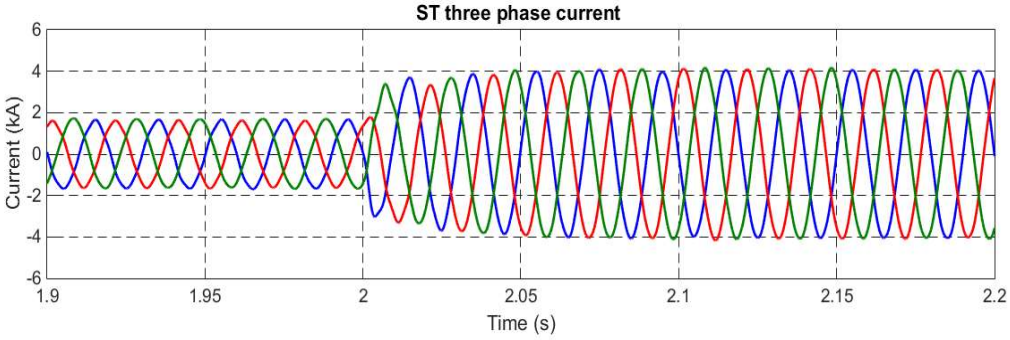

Figure 26: ST Three-phase grid side current of VSC-HVDC

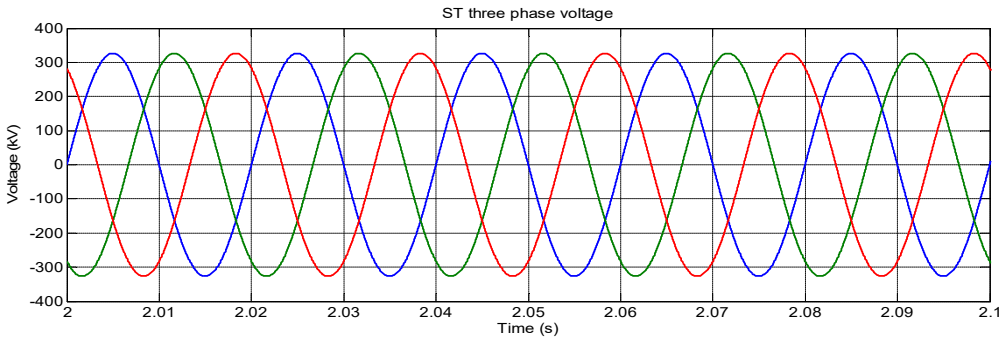

Figure 27: ST Three-phase voltage of VSC-HVDC

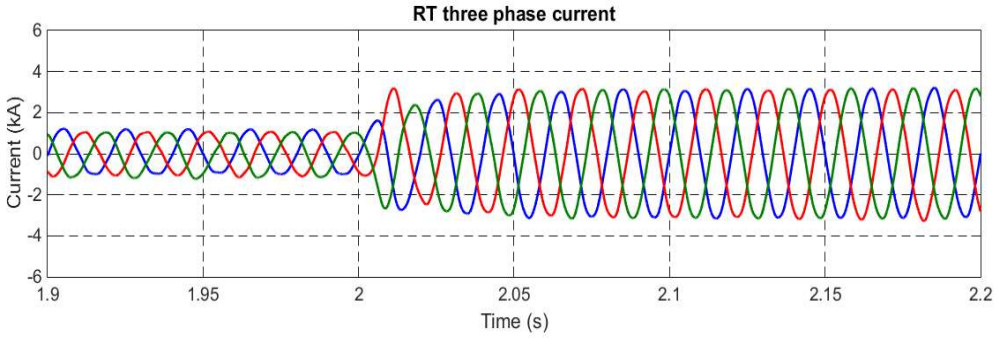

Figure 28: RT Three-phase grid side current of VSC-HVDC

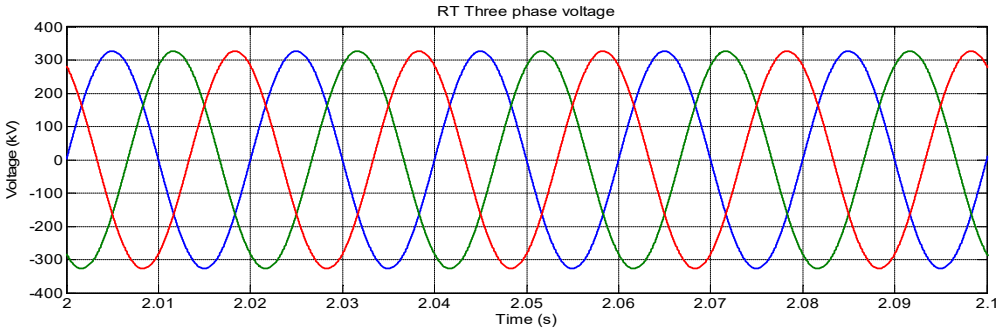

Figure 29: RT Three-Phase Voltage of VSC-HVDC

3.3. DC Side Fault

In VSC-HVDC transmission systems, DC side faults such as pole-to-pole and pole-to-ground faults, comprise major concern in the development of VSC-based DC networks [66]. Pole-to-pole DC fault is considered as a severe fault condition for VSC-HVDC systems regardless of the fault position along the DC cable. Generally, a pole-to-pole DC

fault analysis can be described by the representation shown in Figure 30. Once the DC fault occurs, the fault current goes through the following steps [67]:

• **Capacitor discharge:** The DC link capacitors start to discharge rapidly. Hence the DC link voltage drops near to zero, where the natural response of the capacitor discharge current is known by its high peak and the exponential decay with time [67].

• **Diode freewheeling:** Once the capacitors discharge to a level less than the grid peak voltage, the switches are disabled, and the freewheeling diodes are forward biased as represented in Figure 30. The impedance of the cable drives the grid current into the DC fault passing through the freewheeling diodes path, in which the freewheeling diodes function as an uncontrolled rectifier feeding the DC fault. Each converter leg carries one-third of the fault current that may damage the diodes [67]

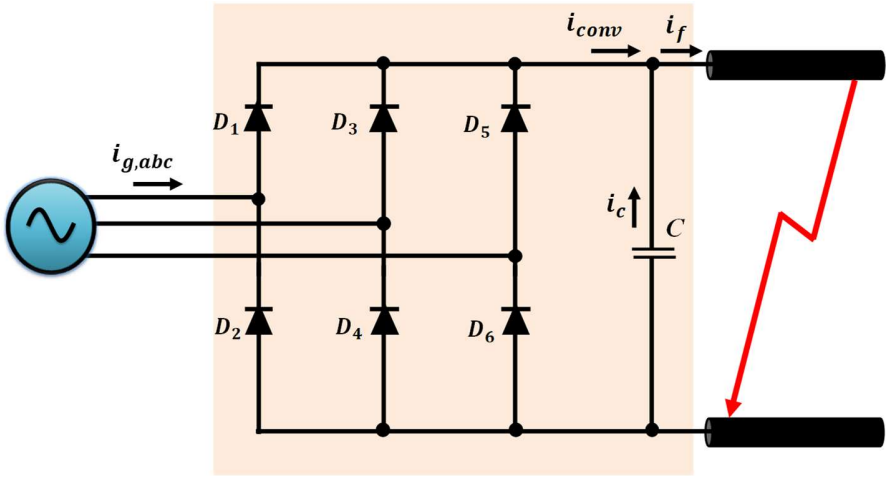

Figure 30: VSC-HVDC pole-to-pole fault schematic diagram

3.4. HVDC Systems Protection

Currently, protection of point-to-point VSC-HVDC systems during fault at the DC side entail disconnection of the faulted line through AC circuit breakers and isolation of the whole DC system. However, this may not be a feasible option. Integrating HVDC Circuit Breakers (DCCB) may be another option [66], [67]. The clearance of the fault on such large systems, especially when more than two-terminals are connected should be fast enough to fulfill the requirements of a reliable HVDC system. Hence, existing mechanical HV DCCBs can clear the fault within several tens of milliseconds, but this is considered very slow. However, HV DCCBs based on semiconductor devices are fast enough to overcome the limitations of operating speed, but it generates higher losses. To overcome these problems, ABB has developed a hybrid DCCB that combines semiconductor switches and a mechanical switch as shown in Figure 31[69]. In normal operation mode, the current flows through the bypass branch which consists of the mechanical switch and the semiconductor switch (load commutation switch), while the current is zero in the main breaker [69]. When a fault occurs, the mechanical switch opens and hence, the current flows through the main breaker path to break the current [69]. The key features of this hybrid HV DCCB design are that it provides reduced conduction losses as there are no active semiconductor switches in the conduction path while maintaining fast current interruption capability [68], [69]. Also, the series-connected reactor is placed along with hybrid HV DCCB at the DC side in order to limit the fault current peak [68-70]. Large inductors with several hundreds of mH are deployed for the limitation of fault current, in which the peak and rising rate of fault current can be reduced within the breaking capability of DCCB [70]. However, large reactors cause overlap to the performance of the system

controller and have a larger footprint as well as higher cost. Furthermore, the overvoltage limitation of the switching transients is not more than 1.4 times the nominal DC link voltage. Hence, it provides high reliability due to inherent redundant topology [71], [72].

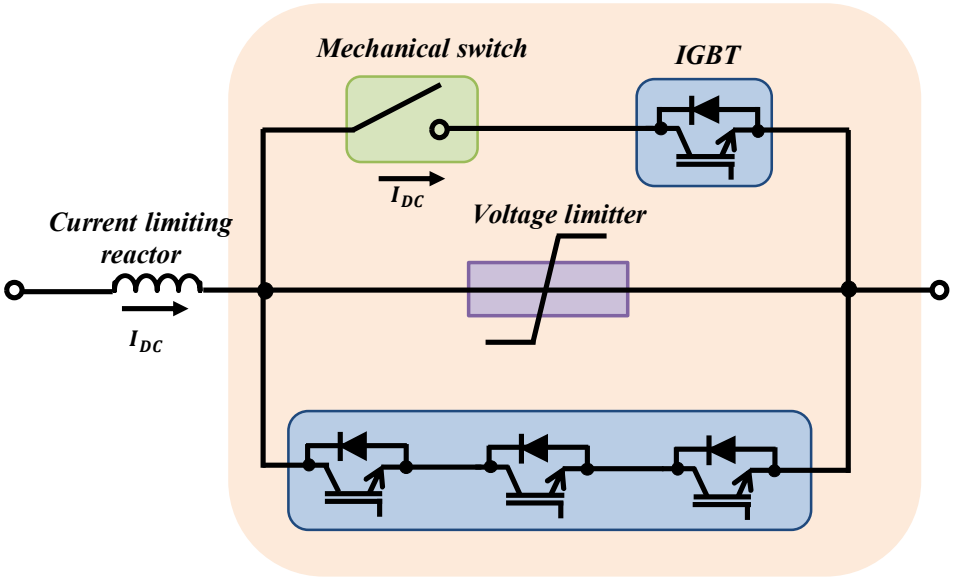

Figure 31: Hybrid DC circuit breakers

To, better understand the system under DC side faults, the studied two-terminal two-level HVDC system has been subjected to a pole-to-pole permanent fault at the ST side as in Figure 32 in order to investigate the behavior of the VSC-HVDC. The fault has been applied at t=2 sec for two cases high and low fault resistance.

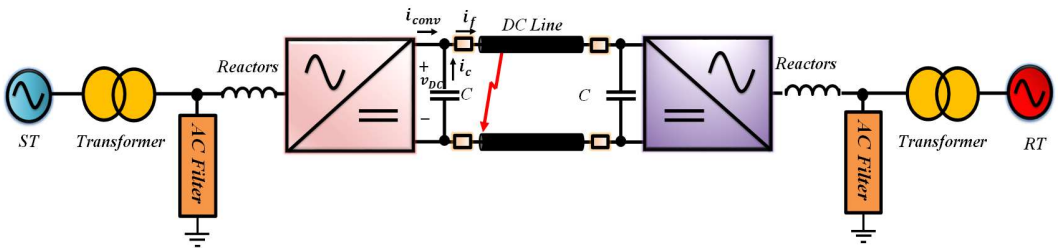

Figure 32: A pole-to-pole DC side fault at VSC-HVDC ST

3.4.1. Case 1: Low resistance Fault

A pole-to-pole DC fault has been applied through R=0.5 Ω at t= 2 sec as in Figure 32. The results generated show that the DC link voltage of the ST drops near to zero as shown in Figure 33, DC capacitor starts to discharge high amplitude current as in Figure 34 according to the time constant of the elements as in (14):

$$\tau = RC \tag{14}$$

where, R represents the reactor and the fault resistance, and C represents the DC link capacitor. Also, VSC is subjected to high amplitude current passing through the freewheeling diodes as presented in Figure 35. In addition, to the high peak fault current shown in Figure 36. As well as, Figure 37 and Figure 38 represent the grid and converter side three-phase currents, respectively, during DC side fault at the ST, where the current in both sides have increased during the fault.

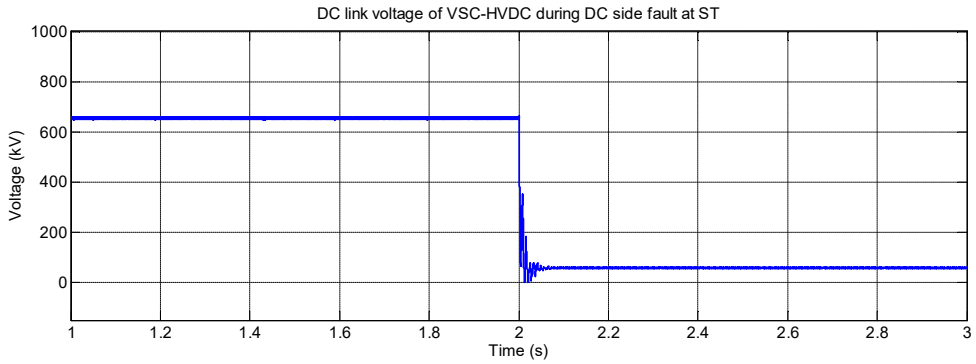

Figure 33: DC link voltage during fault t=2sec

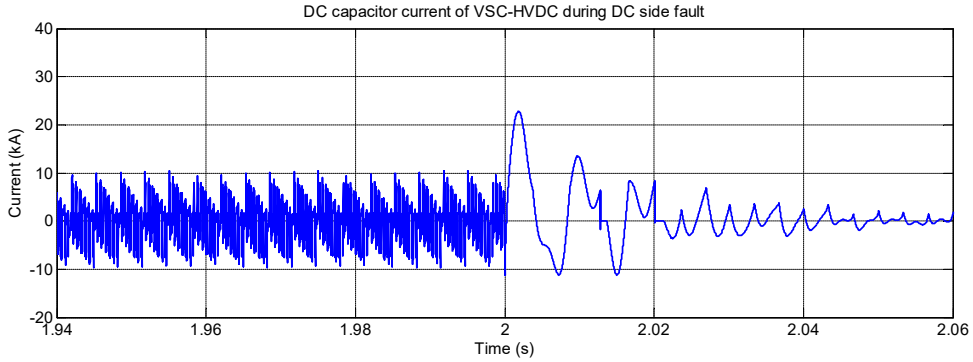

Figure 34: DC capacitor current at DC side fault at t=2 sec

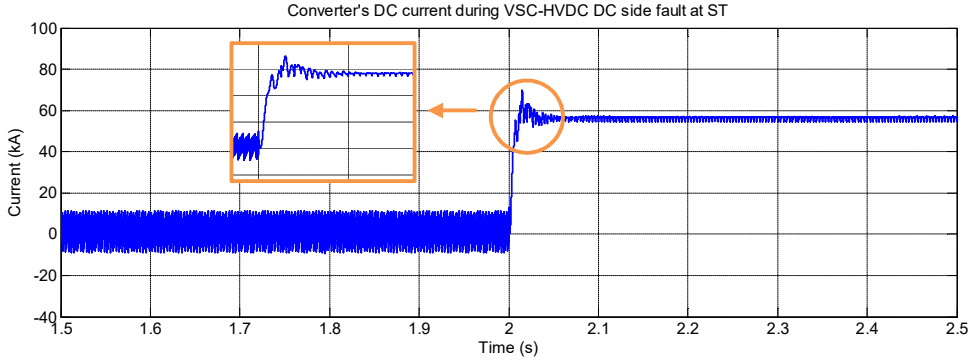

Figure 35: Inverter current during DC fault at t=2 sec

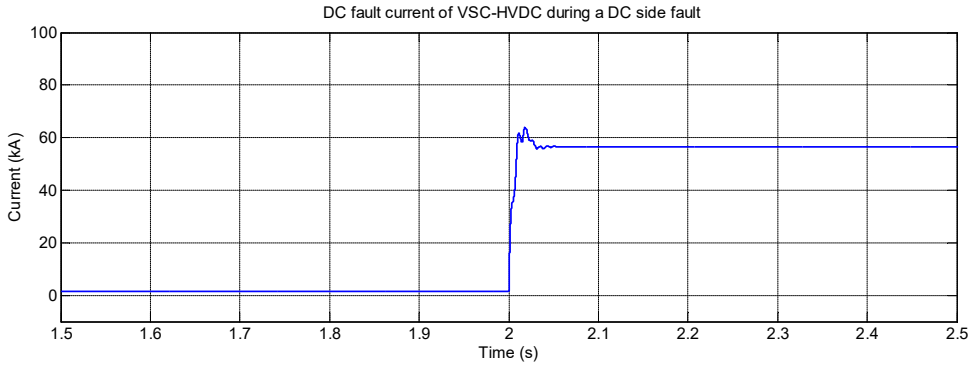

Figure 36: Fault current

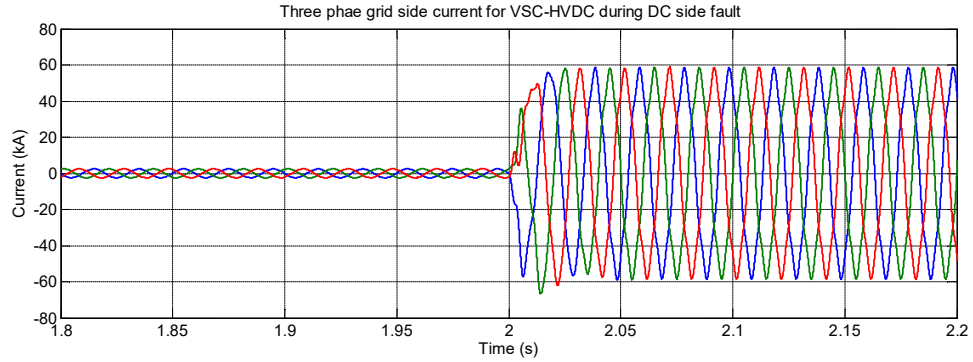

Figure 37: Three-phase grid side current during DC fault at t=2sec.

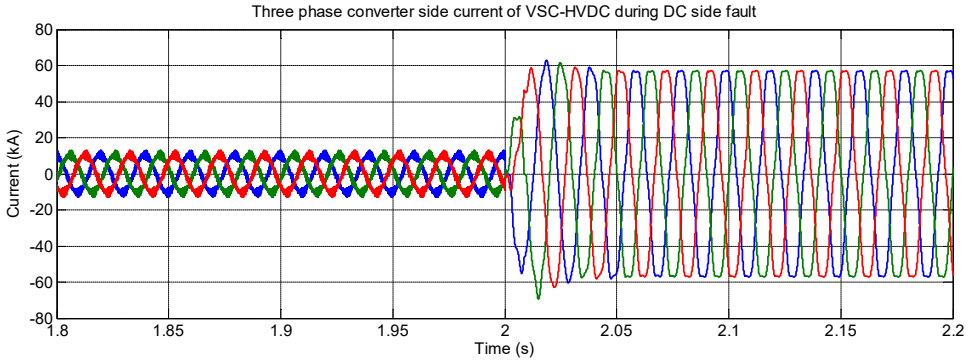

Figure 38: Three-phase converter side current of VSC-HVDC during DC side fault

3.4.2. Case 2: High Resistance Fault

In this case, the DC fault has been applied through R=5 Ω, where the DC link voltage of the ST drops to a value less than half of the DC link as shown in Figure 39 but not to zero. The DC capacitor starts to discharge high amplitude current as in Figure 40. However, in this case, the peak is lower when compared with case 1 because of the higher resistance. In addition, the high peak fault current shown in Figure 41 decays a bit slower when compared with case 1 because of the higher resistance. Nevertheless, the VSC is subjected to high amplitude current from the AC side passing through the freewheeling diodes as presented in Figure 42. It is also important to highlight the contribution of the AC side three-phase current at both grid and converter sides respectively as illustrated in Figure 43 and Figure 44. Based on this, high-performance protection devices are highly needed for the VSC-HVDC systems [66].

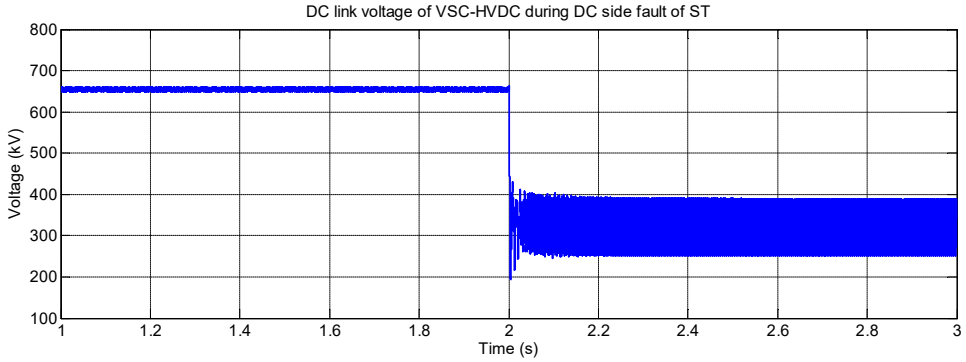

Figure 39: DC link voltage of ST under fault

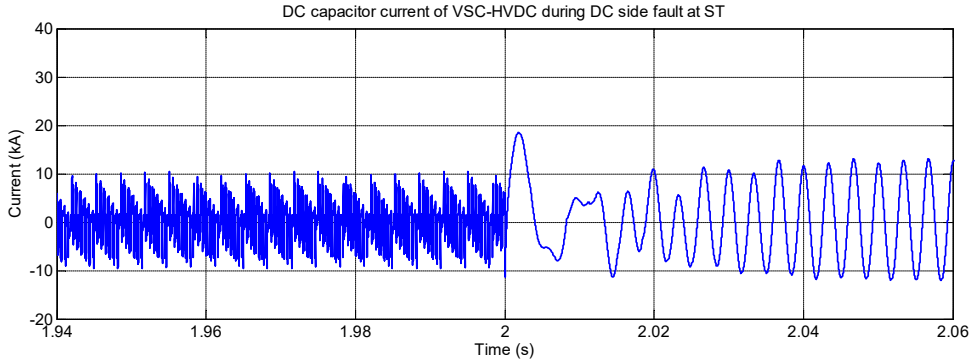

Figure 40: DC Capacitor current during DC side fault

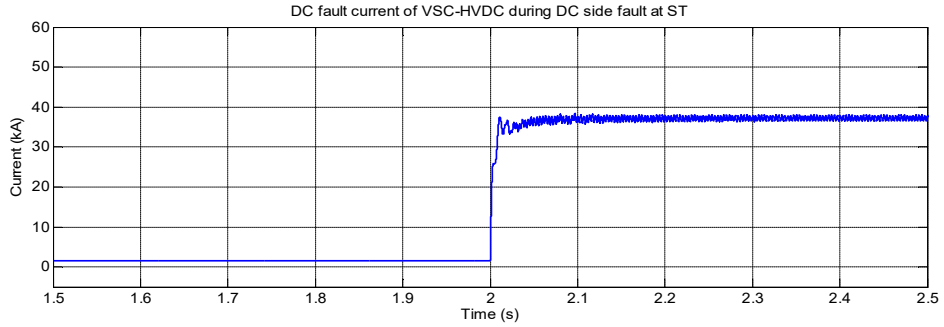

Figure 41: ST DC link fault current

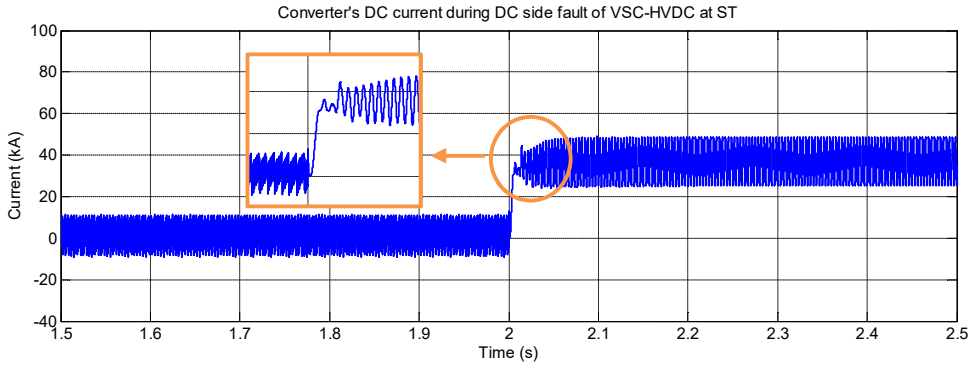

Figure 42: Converter current during the DC side fault

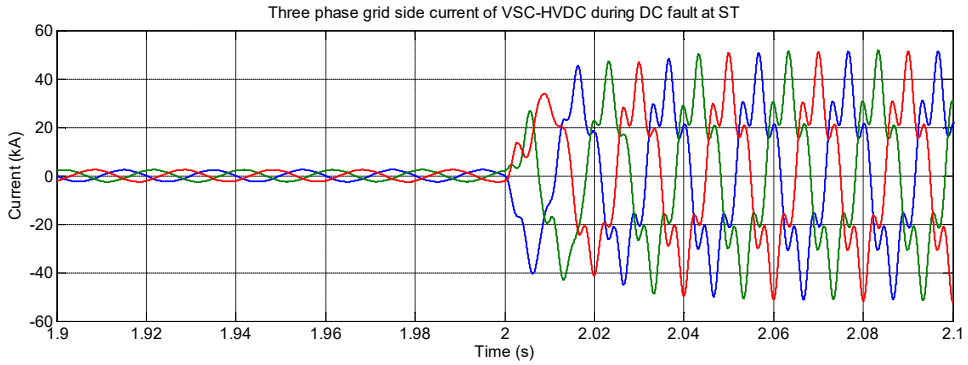

Figure 43: Three-phase current of the ST during DC side fault

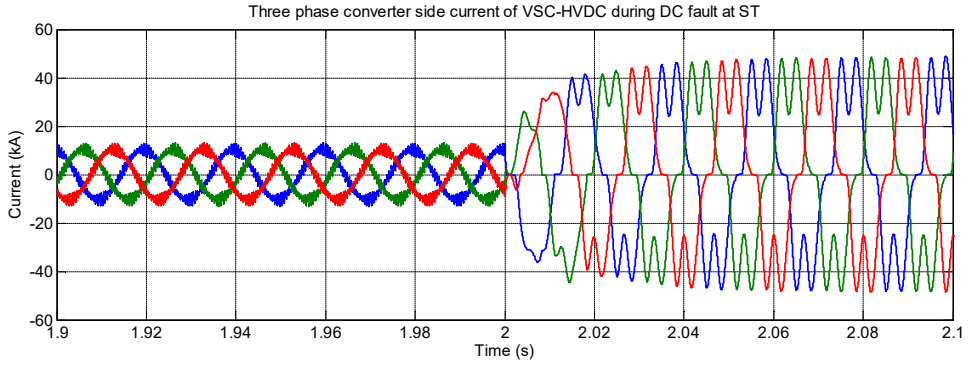

Figure 44: Three-phase converter side current during DC side fault at ST

3.4.3. Implementation of DCCB

Hybrid DCCB topology is implemented in this study to interrupt the fault current until normal operation of the VSC-HVDC transmission system is restored. In the previous section, a permanent fault has been subjected at t=2 sec, and the behavior of the system has been discussed during the fault. However, in this section, a temporary fault is applied where the CBs interrupt the fault current 5 milliseconds later and the fault is cleared at t=2.01 sec. The CBs reclose again at t=2.15 sec to restore normal operation as illustrated in Figure 45. A 20 mH DCCB limiting reactor is employed in this study as in [70].

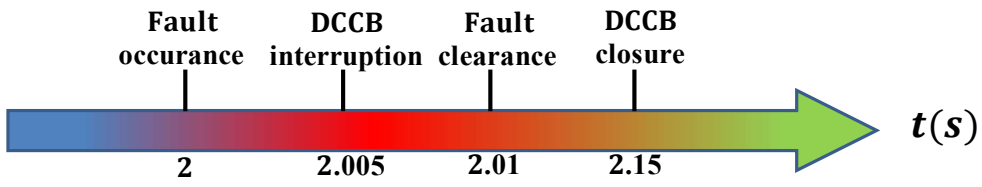

Figure 45: Fault scenario timeline

Figure 47 represents the DC link voltage before the fault, which maintains normal operation at 640 kV, then the voltage drops near to zero once the fault occurred. Five milliseconds later the CBs are triggered to interrupt the fault current while the fault is cleared at t=2.01 sec. The voltage then increases because of the open circuit operation until the CBs restore system's normal operation at t=2.15 to the pre-defined DC link voltage 640 kV. Similarly, Figure 47 presents the converter's DC side current. It shows the normal operation of the current before the fault occurrence. Once the fault occurs, a high peak current arises. When the CBs are triggered, the current drops to zero until the fault is cleared, and the CBs are back at t=2.15 sec. Figure 48 represents the DC link capacitor current. At t=2 sec, the capacitor discharges the current because of the fault until it reaches zero, then it starts to charge once the fault is cleared at t= 2.01 sec due to the effect of the AC side inductors. After that, it goes back to zero until the normal operation of the system is restored. The same scenario applies to ST DC link fault current shown in Figure 49; the high peak current occurred at the fault time starts to discharge till it reaches zero, however, once the CBs reclose at t=2.15 sec, normal operation is restored. Furthermore, the three-phase currents at grid and converter sides are presented in Figure 50 and Figure 51. During the fault, the grid side current has increased. Then the CB interrupts the fault. The normal operation is restored, after clearing the fault by closing the CB. Then the normal operation of the converter can be continued through normally ramping up of the power. It is important to indicate that the amplitude of the three-phase currents is higher after the system is restored when compared to the normal operation before the occurrence of the fault, and this is because the power transferred has increased as per the pre-defined reference power at t=2 sec from 800 MW to 2 GW. However, the converter side current presented in Figure

51 drops to zero during the fault period until the closure of the CBs.

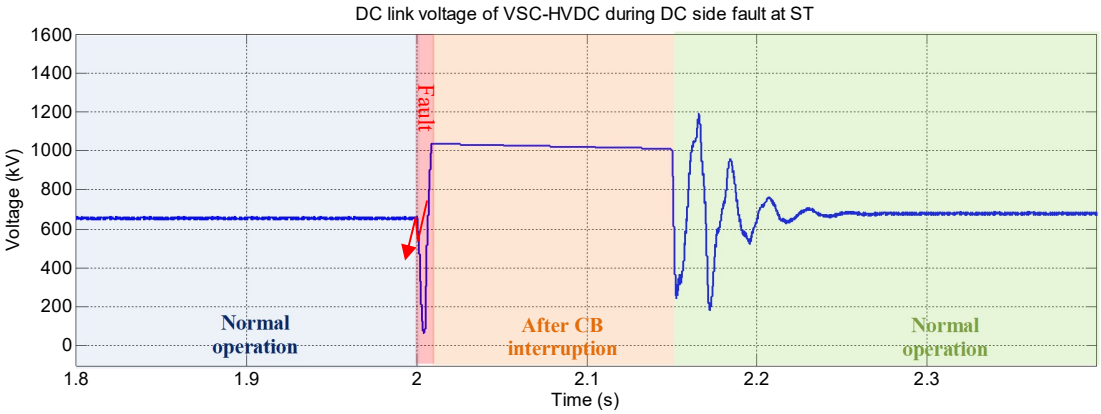

Figure 46: DC link voltage of the ST

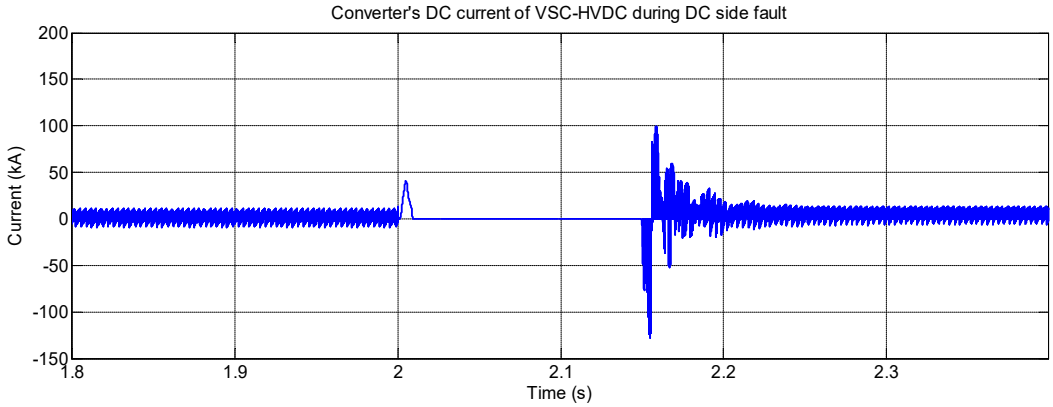

Figure 47: Converter's DC current

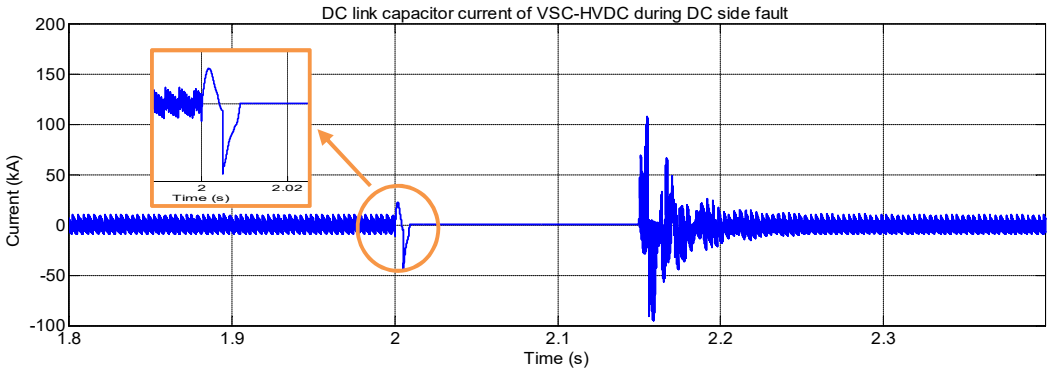

Figure 48: DC link Capacitor current

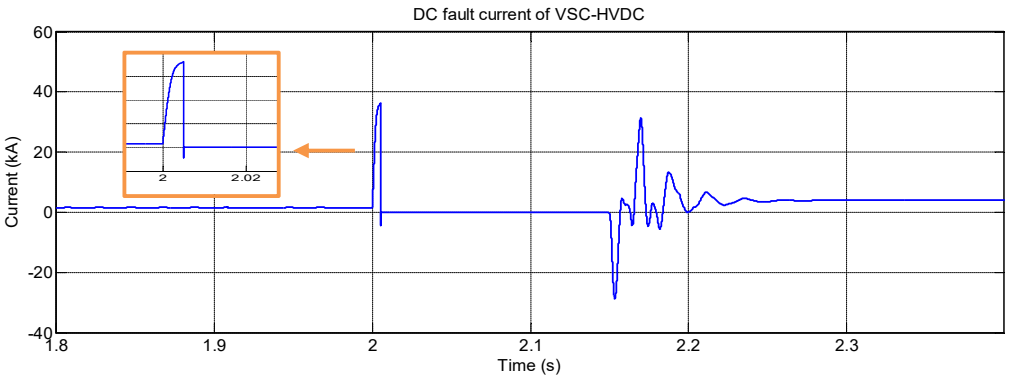

Figure 49: ST DC link fault current

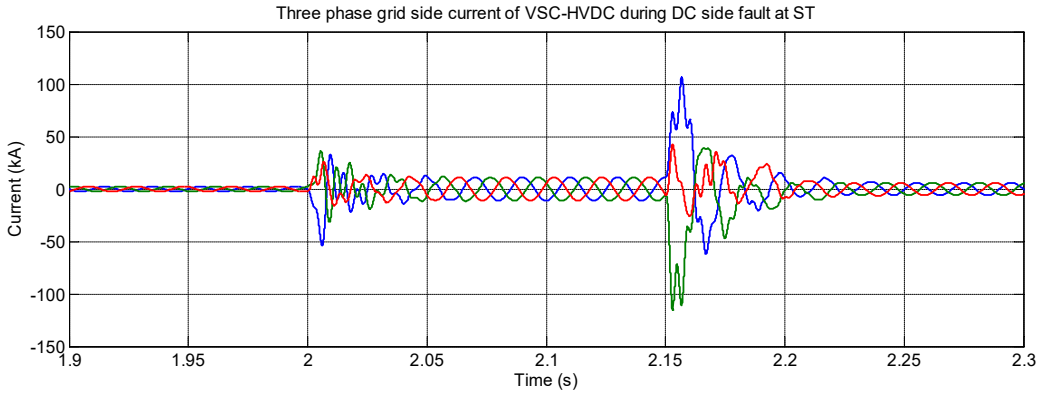

Figure 50: Three-phase current of the ST

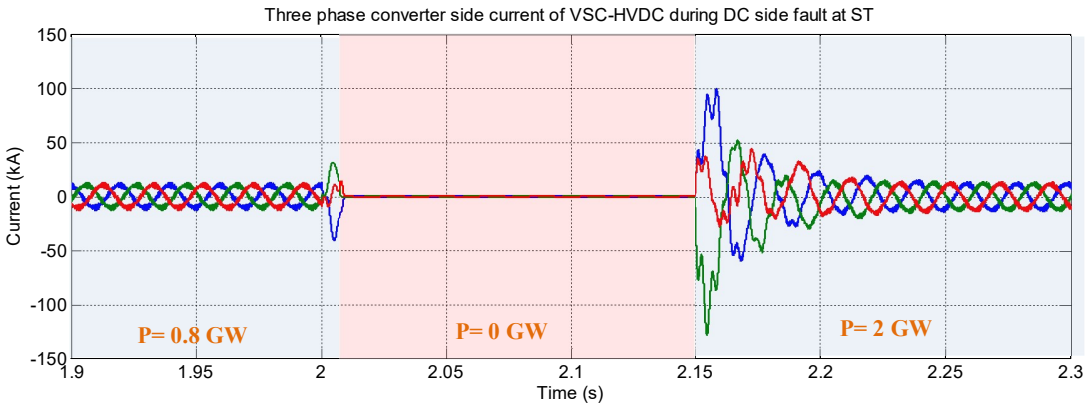

Figure 51: Three-phase converter side current during DC side fault

3.5. Conclusion

In conclusion, in this chapter, a two-terminal VSC-HVDC-based two-level converter has been modeled and simulated using MATLAB/Simulink. Studying this system initially is an important step to understand the behavior of the two-terminal VSC-HVDC transmission system. The results generated in this chapter have verified the functionality of the VSC-

HVDC systems. The powers were well controlled at the ST, and the DC link has been kept unchanged even during power change. Nevertheless, the harmonic profile could be enhanced by using multilevel converter topologies. Finally, DC side fault has been tested at the ST of the implemented system, to study the effect of it on VSC-HVDC systems. Different protection solutions are available. However, they suffer from slowness, and high conduction losses. Nevertheless, hybrid DCCB developed recently by ABB is a promising solution to DC faults problems as it is fast and has low conduction losses compared to regular DCCBs as discussed in this chapter.

CHAPTER 4: TWO-TERMINAL MMC-BASED HVDC SYSTEM

4.1. Modular Multilevel Converter (MMC)

4.1.1. MMC topology and operation

The MMC has attracted the attention of researchers to replace the two-level VSC in HVDC systems due to the introduced merits, e.g., modularity and scalability. The typical structure of an MMC is shown in Figure 9 earlier, where HB-SM is adopted in this study. The switching states of the SM are shown in Table 2 where every SM has two states ON and OFF, based on that the corresponding output voltage V_{SM} is V_c or 0 depending on the switches' status [73]. The charging and the discharging of the capacitor voltages basically depend on the direction of the current flowing in the SMs. If the current flows in the positive direction (into the SM), then the capacitors are charged, whereas the capacitors are discharged if the current flows in the inverse direction (out of the SM).

Table 2: Half-bridge SM working states

S1	**S2**	V_{SM}	I_{SM}	**SM state**	**Capacitor**
ON	OFF	V_c	> 0	ON	Charging
ON	OFF	V_c	< 0	ON	Discharging
OFF	ON	0	> 0	OFF	Unchanged
OFF	ON	0	< 0	OFF	Unchanged

4.1.2. MMC Mathematical Model

According to [74],[75] and Figure 52, the phase voltage in the MMC can be described as:

$$v_j = \frac{1}{2}\left[v_{jl} + L\frac{dI_{jl}}{dt}\right] - \frac{1}{2}\left[v_{ju} + L\frac{dI_{ju}}{dt}\right] \quad (14)$$

By assorting (14):

$$2v_j = (v_{jl} - v_{ju}) + L\frac{d(I_{jl} - I_{ju})}{dt} \quad (15)$$

Where the phase current can be represented as:

$$I_j = I_{ju} - I_{jl} \quad (16)$$

Substituting (16) into (15):

$$2v_j = (v_{jl} - v_{ju}) - L\frac{dI_j}{dt} \quad (17)$$

where v_{ju} and v_{jl} are the total upper and lower SMs voltages, v_j is the voltage of phase *j (j=a,b,c),* as well as I_{ju} and I_{jl} are the upper and lower arm currents of phase *j* respectively, and I_j is the current of phase j. Then, i_{ccj} is the circulating current of one leg where i_{ccj} can be expressed as:

$$i_{ccj} = \frac{I_{ju} + I_{jl}}{2} \quad (18)$$

Furthermore, the voltage relationship of the MMC based on the Kirchhoff's voltage law can be described as [74]:

$$v_{dc} = \left(v_{jl} + L\frac{dI_{jl}}{dt}\right) + \left(v_{ju} + L\frac{dI_{ju}}{dt}\right)$$

$$v_{dc} = \left(v_{jl} + v_{ju}\right) + L\frac{d(I_{ju} + I_{jl})}{dt}$$

$$v_{dc} = \left(v_{jl} + v_{ju} \right) + 2L\frac{di_{ccj}}{dt} \tag{19}$$

$$L\frac{di_{ccj}}{dt} = \frac{1}{2}(v_{dc} - v_{ju} - v_{jl}) \tag{20}$$

$$\mathrm{e} = \frac{1}{2}(v_{jl} - v_{ju}) \tag{21}$$

$$v_{ccj} = L\frac{di_{ccj}}{dt} = \frac{1}{2}(v_{dc} - v_{ju} - v_{jl}) \tag{22}$$

$$\begin{aligned} v_{ju} &= \frac{1}{2}v_{dc} - e - v_{ccj} \\ v_{jl} &= \frac{1}{2}v_{dc} + e - v_{ccj} \end{aligned} \tag{23}$$

Where v_{dc} is the input DC voltage.

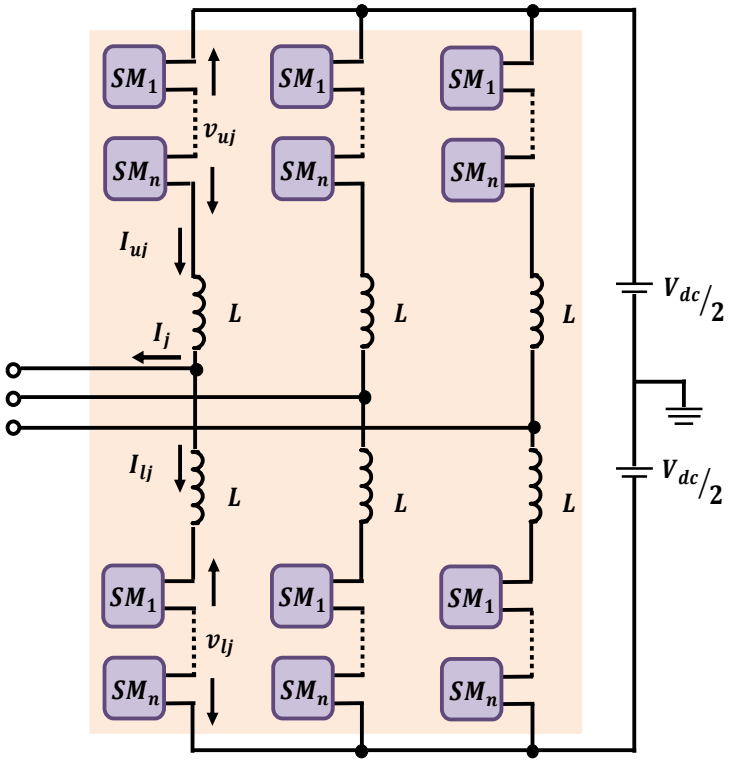

Figure 52: Simplified MMC configuration

4.1.3. Modulation Technique

MMCs can be controlled using several PWM switching schemes as carrier-based PWM [61], [75], space vector modulation [76], selective harmonic elimination [77], and Nearest Level Control (NLC) [78]. Carrier-based PWM can be classified according to the carrier type as Phase Disposition (PD) [75], Phase Opposition Disposition (POD) [75], Alternative Phase Opposition Disposition (APOD) [75], and Phase-Shifted Carriers PWM (PSC-PWM) [74]. One of the commonly used PWM techniques is the PD-PWM technique. Nevertheless, all PD-PWM techniques are not preferred for MMC as they cause uneven power distribution between the SMs [79]. However, PD techniques are used for HVDC applications as they allow the operation of MMCs at a low-frequency modulation. In contrast, PSC-PWM is a commonly used modulation technique in MMCs as the stresses on the switches and the power handled by each SM are evenly distributed [79]. Therefore, the balancing of the capacitor voltages can be easily achieved. PSC-PWM might not operate at a very low-frequency modulation frequency ratio as m_f= 2 because of the asymmetry of the carrier with the modulation signal. Nevertheless, it can operate at low m_f that would be equivalent to the PD-PWM. Nevertheless, both techniques allow the operation at high m_f for low voltage applications, where m_f is defined as.

$$m_f = \frac{f_{carrier}}{f_{fundamental}} \tag{24}$$

Hence, PD-PWM has been applied in this thesis for the MMC control. In an N-level MMC, each arm with (N-1) SMs requires (N-1) triangular carrier waves with a switching frequency of f_s. The basic concept of PD-PWM applied in this study is illustrated in Figure 53. A reference sinusoidal wave is compared with multiple levels shifted triangular carrier

in order to get the IGBTs' switching signals. The modulating signals in the upper and lower arms can be expressed as follows:

$$n_u = \frac{1}{2}(1 - m_a \sin(\omega t))$$
$$n_l = \frac{1}{2}(1 + m_a \sin(\omega t)) \quad (25)$$

where m_a is the modulation index.

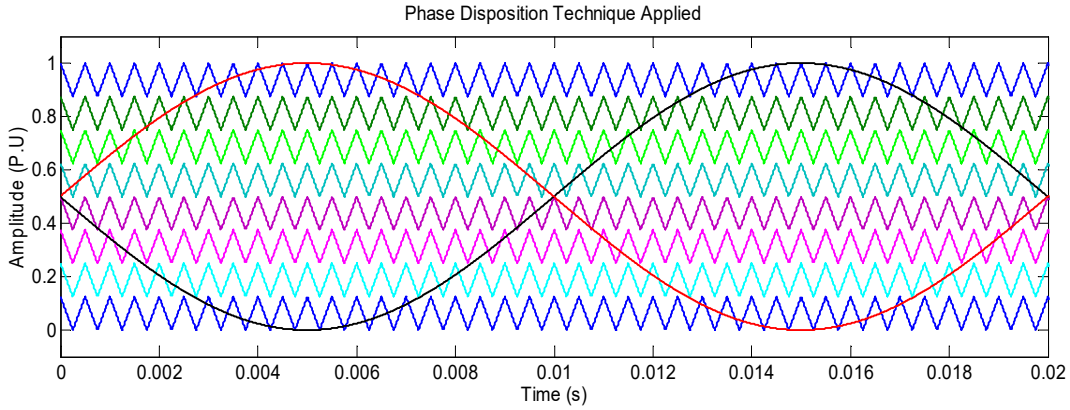

Figure 53: 9-Level PD-PWM technique with a modulation index of 1

4.2. Capacitor Voltage Balancing

One of the main technical challenges associated with the control of the MMC is to keep the SM capacitor voltages balanced at their nominal values. Typically, the complexity of capacitor voltage balancing increases as the number of levels increases. Hence, several balancing techniques have been developed in the literature [80-92]. In [80], a developed predictive algorithm for capacitor voltage balancing, which aims to combine a low

switching frequency with a low capacitor voltage ripple is presented. This algorithm evaluates the amount of charge that should be stored in each SM capacitor during the fundamental frequency period. Furthermore, in [81] a methodology of fast voltage balancing control based on average comparison and a fast numerical simulation model for MMC has been introduced. In [82], a new modulation method is based on selective virtual loop mapping in order to achieve dynamic capacitor voltage balance without the need for an external compensation signal. However, in [83] an improved phase disposition PWM for MMCs based on the selective loop bias mapping method is proposed for balancing the capacitor voltages. Furthermore, in [84] a stable voltage control method to realize both averaging and balancing controls of floating capacitors. A combination of averaging and balancing controls allows the MMC to achieve voltage balancing without external circuit, but using PI controllers, is presented in [85]. In addition, an internal and external voltage balancing method characterized for large-scale MMCs is proposed in [86]. This proposed technique is beneficial for large-scale MMC modeling as each arm is divided into Valve Groups (VGs) each of N SMs. The internal voltage balancing technique is responsible for balancing the SMs within each VG. However, the external voltage balancing is responsible for balancing the average SM voltages of each VG within the arm. In [87], the SMs of the MMC are modulated independently as they are controlled using PSC-PWM, hence, the voltage balancing of the capacitors can be attained by adjusting the reference signal of each SM. In [88], a sorting algorithm is presented in order to reduce the switching commutations of each SM also for voltage balancing control, in which a practical and effective mitigation measure is integrated to keep the energy balance while avoiding the undesired switching stresses. In [89], an analytical discussion of the voltage balancing control approach with

rotation of switching angles is presented. In [90], a novel modulation and capacitor voltage control method for the MMC. Using this approach, the SMs can be self-balanced by periodically swapping the pulse patterns. The study in [91] shows a model predictive control strategy that takes the advantage of a cost function minimization topology to eliminate the circulating currents and carry out the voltage balancing problem of the MMC. The study in [92] proposes a Model Predictive Control (MPC) that eliminates the circulating current and tackles the voltage balancing of the SM capacitors of an MMC-based back-to-back HVDC system. Another problem associated with MMCs is the circulating current that has been addressed widely as well. The circulating current is an inherent phenomenon that influences the performance of MMC, such as power losses, capacitor voltage ripples, and the current rating of the switches. The study in [93] presents a circulating current controller of the MMC that uses the available redundancies of the multilevel waveform, to adjust the circulating current to pre-defined reference. However, an improved steady state analysis that studies the circulating current control has been proposed in [94]. By considering the effect of the second-order harmonic component of the reference voltage, the influence of the circulating current control has been included [94]. The study in [95] presents a stable and balanced voltage and current control with reduced circulating current in different operational situations. This controller uses weighted model predictive control based on a normalized cost function to select the switching patterns of the inverter, to control the load current and minimizing the voltage variation and circulating current. However, the reduction of circulating current is out of the thesis scope, and the intuitive approach of properly sizing the arm inductor is considered in this thesis.

4.2.1. The applied Voltage Balancing Technique

In a similar manner of [88], a generalized voltage balancing technique for MMCs is modeled using Matlab/Simulink platform in this study [96]. The presented model can be simply extended to any number of levels. The modeled approach is tested for different switching frequencies (modulation frequency ratios) downward to $m_f = 2$ [96].

The presented balancing technique is mainly based on measuring the capacitor voltages and sorting them in either ascending or descending order. Then, based on the direction of the arm currents and the number of required state of the SMs within each control period, a number of SMs are inserted/bypassed [74]. The balancing technique consists of a sorting algorithm as shown in Figure 54 (a), de-multiplexer blocks to switch the modulation control signals between the HB-SMs cells in each arm and an adder block that links the chopper cells with the different de-mux outputs as shown in Figure 54 (b).

In this technique, the PD-PWM control signals are always in swapping mode to charge the less capacitor voltage in case of positive arm current ($I_{arm} > 0$), where in this case the capacitor voltages are sorted in ascending order. In contrast, PD-PWM control signals are used to discharge the capacitor with the higher voltage value in case of negative arm current ($I_{arm} < 0$). In this case, the capacitor voltages are sorted in descending order. Each de-mux used has one input, N outputs, and control signals depending on the number of levels. The input for each de-mux is the PD-PWM signals. The output is then decided based on control signals, which are the indices generated from the sorting block used in MATLAB/SIMULINK as shown in Appendix A. These indices (V_{index}) are numbers from 0-7 (in nine level MMC) that points out the voltage arrangement, however, this is then converted into binary in order to control the de-mux.

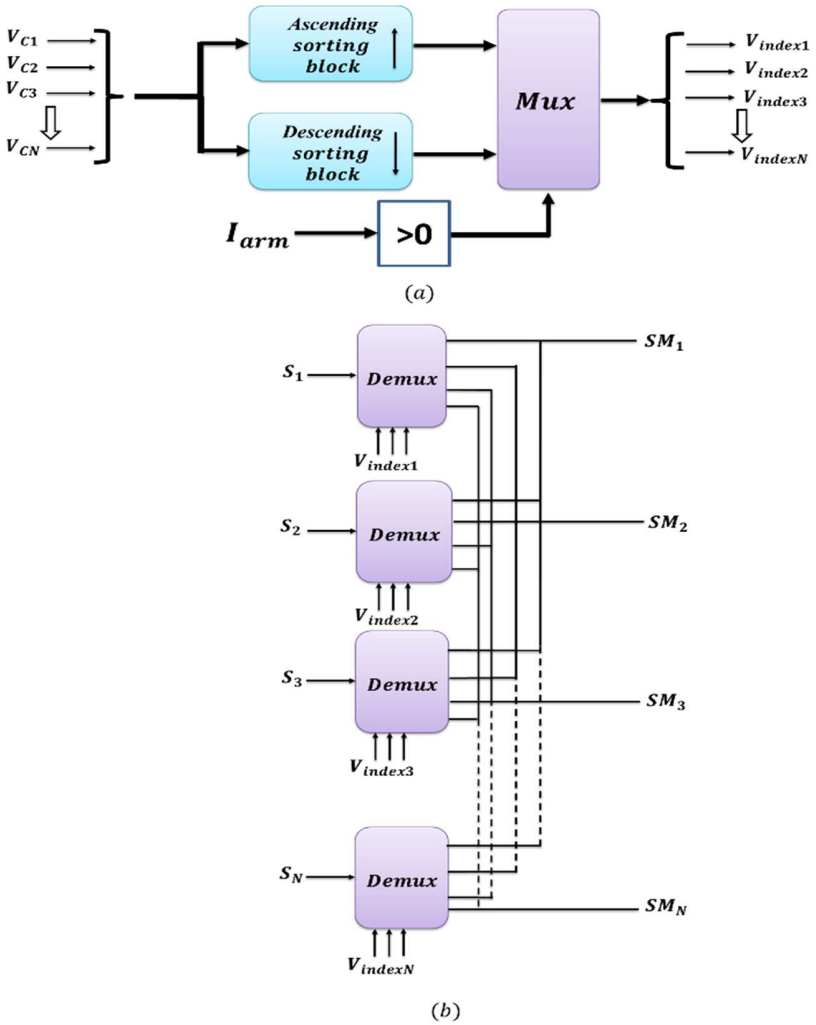

Figure 54: Applied balancing technique (a) sorting approach (b) modulation strategy

4.2.2. Capacitor Voltage Balanceng Simulation Results

The proposed general voltage balancing technique shown in Figure 54 is applied to a 9-level MMC. The modeled MMC consists of 8 SMs in each arm. So a total of 16 SMs per phase is used as shown in Appendix A. The simulation is conducted for m_f= 2, and for

m_f > 2 to validate the effectiveness of the modulation method used to control the MMC at a switching frequency equal to the 100 Hz and at 2 kHz.

For such converters that depend on charged capacitors in their cells to produce AC voltage, it is important to highlight that this energy storage element is a driving factor of the cost, and size of the SMs. Hence, it is better to keep the capacitance minimal while limiting the voltage fluctuation caused by the current. A detailed analysis for the passive elements in MMC such as SM capacitors and arm inductors that relates the power transfer capability to the stored energy in the converter KJ/MVA is presented in [97], [98]. The parameters used in the simulation are shown in Table 3 [44],[45].

Table 3: Nine-Level MMC transient model parameters

Parameter	**Value**
L	5 mH
C	20 mF
R (load)	10 Ω
L(load)	5 mH
f_s	2 kHz (case 1), 100 Hz (case 2)
V_{DC}	640 kV
n (number of SMs)	8 per arm
V_{SM}	80 kV
m_a	0.9

Starting with 2 kHz switching frequency, Figure 55 represents a zoomed-in scale of phase (a) capacitor voltages when balanced at their nominal value, which is 80 kV in this case as the DC link is 640 kV. The balancing technique is also tested when adding extra three-phase load to the system at t = 2.35s. The ripples in the SMs capacitor voltages are increased slightly but still balanced at the nominal value as shown in Figure 56. This indicates the effectiveness of the proposed general voltage balancing technique. Figure 57 represents the three-phase output voltage of the MMC, where it is not affected by the sudden change in load. However, the output current is increased by adding the extra load as illustrated in Figure 58.

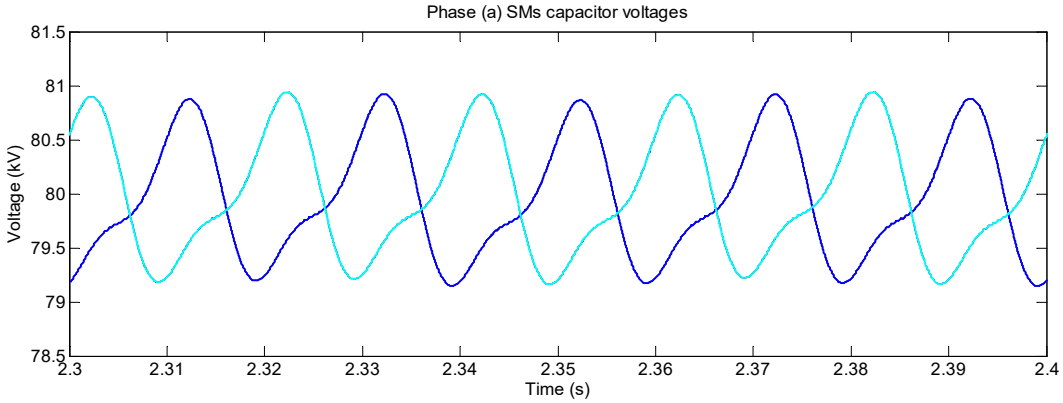

Figure 55: Zoomed-in scale of the capacitor voltages of phase (a) at $f_s = 2kHz$

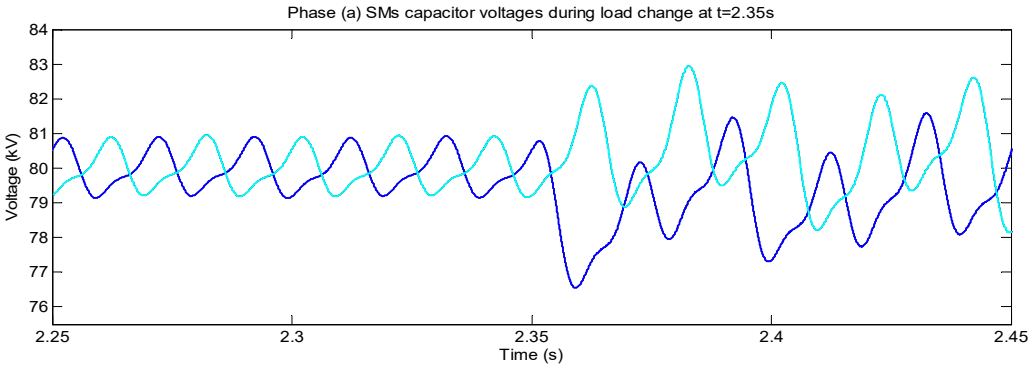

Figure 56: SMs capacitor voltages of phase (a) in case of load change at $f_s = 2kHz$.

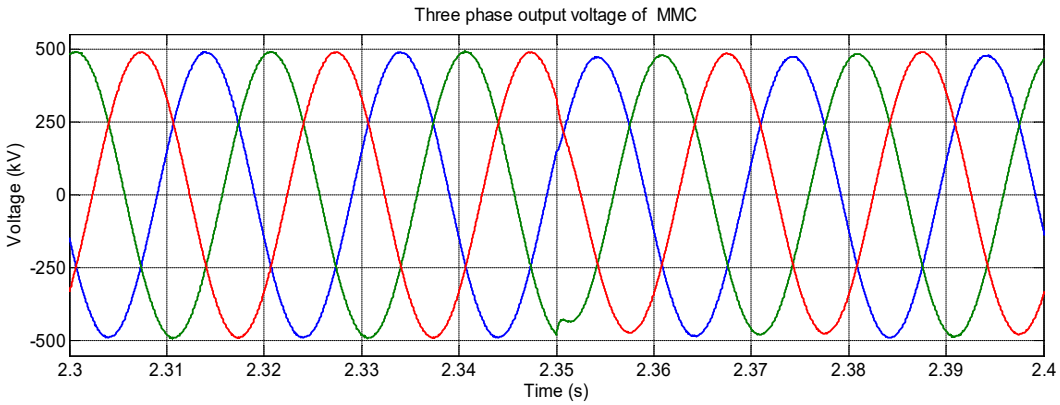

Figure 57: Three-phase output voltage of MMC operating at 2kHz

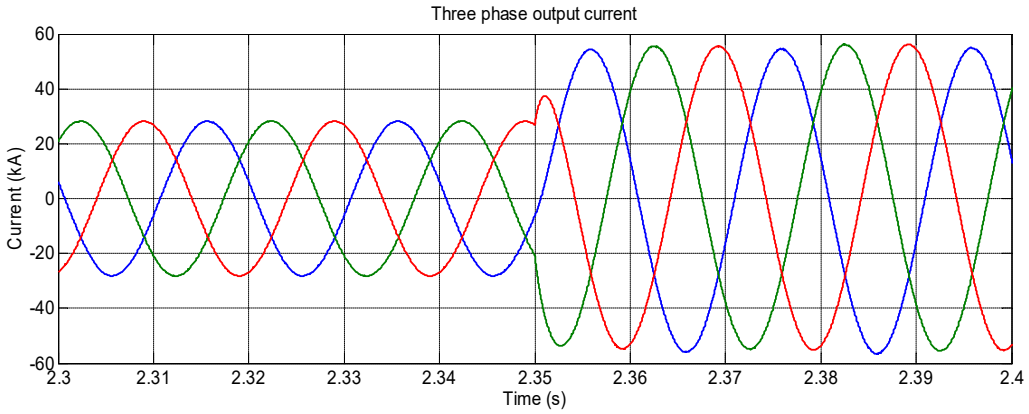

Figure 58: Three-phase output current operating at 2kHz

The same strategy is applied for $f_s = 100\ Hz$. As shown in Figure 59 that represents a zoomed-in scale of the capacitor voltages of phase a, when balanced at their nominal value which is also 80 kV. Again, an extra load is added to study the effect of a sudden increase in the load demand. The ripples in the SMs capacitor voltages have increased slightly also at this switching frequency, but still balanced at the nominal value as shown in Figure 60. Figure 61 represents the three-phase output voltage of the MMC. It is not affected by the sudden change in load. However, the output current is increased by adding the extra load as illustrated in Figure 62.

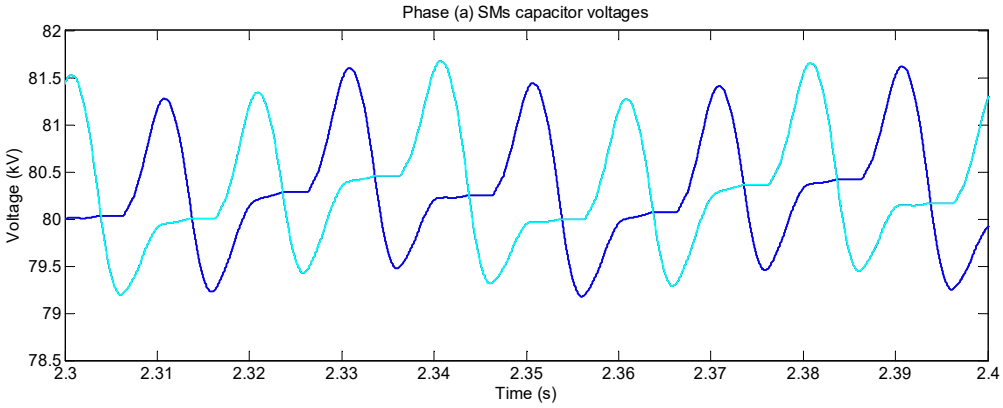

Figure 59: SMs capacitor voltages of phase (a) f_s=100 Hz

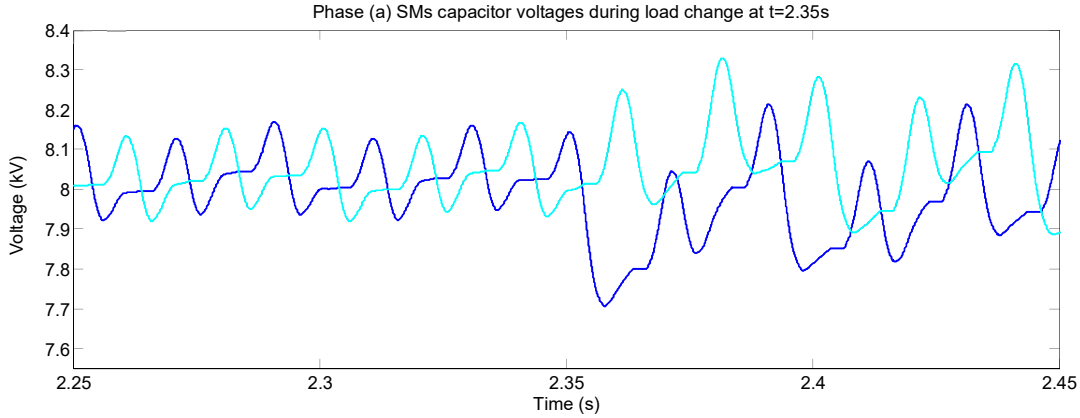

Figure 60: SMs capacitor voltages of phase (a) in case of load change at f_s=100 Hz

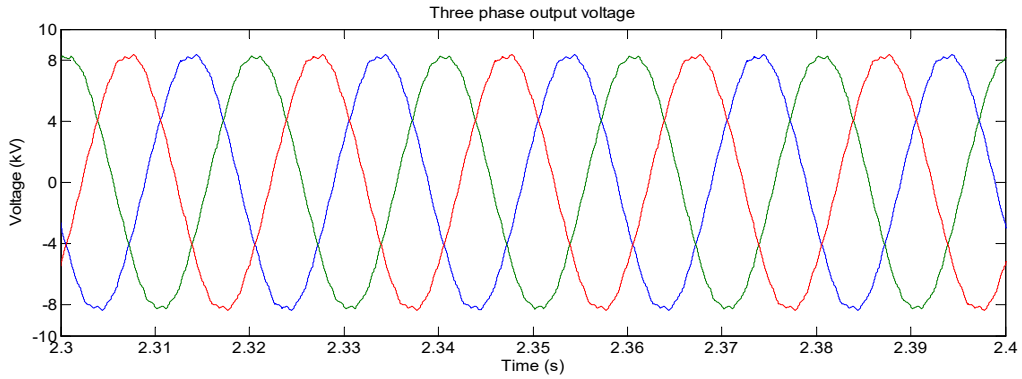

Figure 61: Three-phase output voltage of MMC at f_s=100 Hz

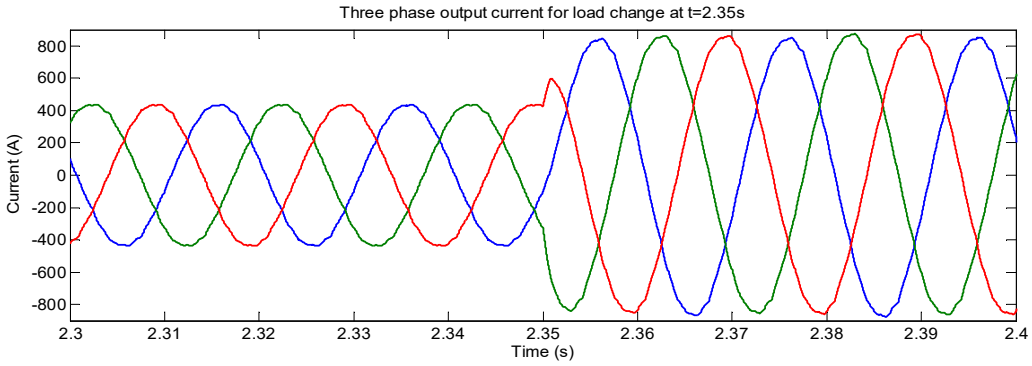

Figure 62: Three-phase output current of MMC operating at f_s=100 Hz

The results generated from the different switching frequencies prove the efficiency of the modulation technique used (PD-PWM) as it allows the operation of the MMC at different switching frequencies starting from $f_s = 100\,Hz$ and at several modulation indices. Finally, it is also important to highlight the behavior of the floating capacitors in MMCs

without balancing the SMs capacitors as shown in Figure 63.

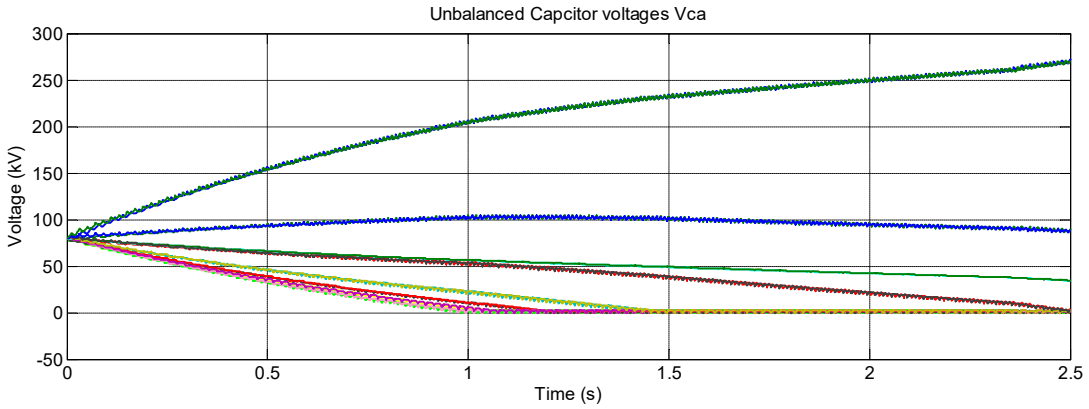

Figure 63: SMs capacitor voltages of phase (a) without balancing

4.3. Two-terminal MMC-Based HVDC System

The power transfer in the two-terminal MMC-based HVDC system is modeled and controlled in a similar way as conventional VSC-based HVDC transmission discussed earlier in details in chapter 2, section 2.2. Generally, VSC-HVDC consists of VSCs, phase reactors, AC filters, transformers, DC capacitors, and DC cables. However, with MMC-based HVDC the need for central DC link capacitor is eliminated because of the integration of the distributed capacitors in the SMs of the MMC [99]. Also, the filter requirements in MMC-HVDC is reduced because of the existence of the arm inductors and the SMs capacitors [99], which is clear in a higher number of levels models as in reality MMC-HVDC systems is expected to have a high number of levels. Similar to what has been implemented in chapter 2, power control is carried out at ST. Nevertheless DC link voltage

control is carried out at the RT. The schematic of a two-terminal MMC-HVDC system is illustrated in Figure 64.

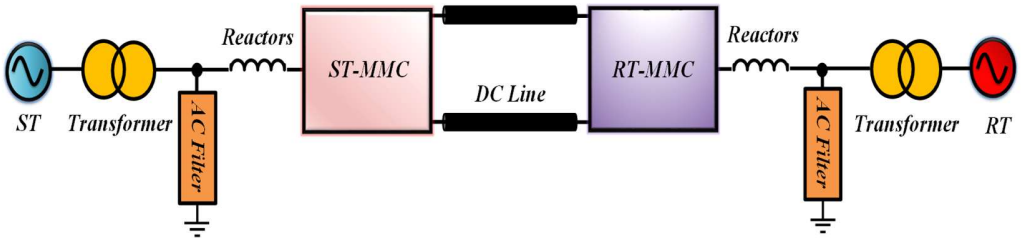

Figure 64: MMC-Based HVDC transmission system scheme

4.3.1. MMC-HVDC Simulation Results

The two-terminal MMC-HVDC system has been modeled and simulated using MATLAB-Simulink platform. The 9-level MMC transient model discussed earlier in this chapter is used to model the two-terminal transmission system and validate its efficiency compared to conventional VSC technologies. The same scenario is implemented in the simulation of MMC-HVDC system. The LCL filter used here have the same parameters defined for the two-terminal two-level converter transmission system. Although, the filter requirements should be reduced when using MMC, however, because the number of levels is not high, so it will not introduce a significant difference. For a higher number of levels, filter parameters will be reduced significantly. Each terminal is tested separately to validate the functionality of both terminals. The models of both terminals and the control methodology implemented using MATLAB/Simulink are shown in Appendix B. Based on this, the parameters used in this simulation are presented in Table 1 and Table 4.

Table 4: Nine-Level transient MMC-HVDC system parameters

Parameter	Value
Grid Voltage (line-line)	400 kV
Fundamental Frequency	50 Hz
Switching Frequency ($\boldsymbol{f_s}$)	2 kHz
DC Voltage	640 kV
AC Line Damping Resistance (R)	1 Ω
LCL Filter Inductance ($\boldsymbol{L_g, L_{inv}}$)	8 mH
LCL Filter Capacitance ($\boldsymbol{C_f}$)	100 μF
High pass Filter Resistance ($\boldsymbol{R_f}$)	0.01 Ω
High pass Filter Inductance ($\boldsymbol{L_f}$)	0.0634 mH
HCLC reactor $\boldsymbol{L_{CL}}$	18 mH
DCCB limiting reactor $\boldsymbol{L_{lim}}$	2 mH

4.3.2. ST Simulation Results

Figure 65 and Figure 66 present the ST terminal active and reactive powers respectively against their pre-determined reference value. At steady state, the active power of the ST becomes equivalent to the reference value P_{ST}^{*}. The reactive power is set to zero equivalent to the reference value. In addition, Figure 67 and Figure 68 show the dq currents,

respectively versus their reference value. In addition to, Figure 69 and Figure 70 show the three-phase current and voltage at ST.

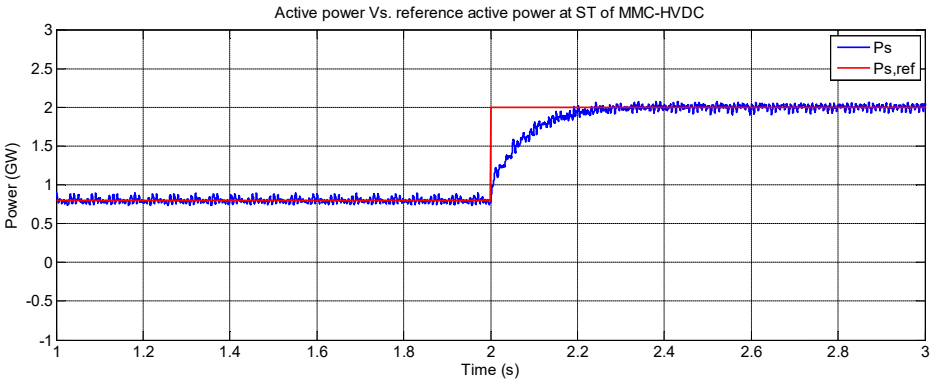

Figure 65: Active power response against reference active power

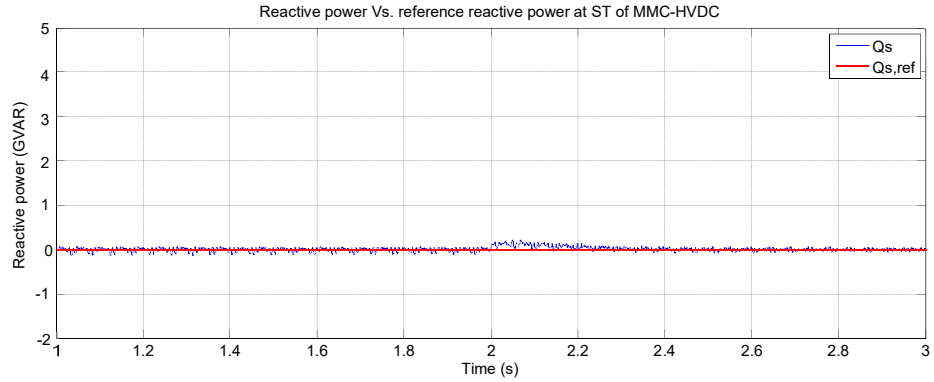

Figure 66: Reactive power response against reference reactive power

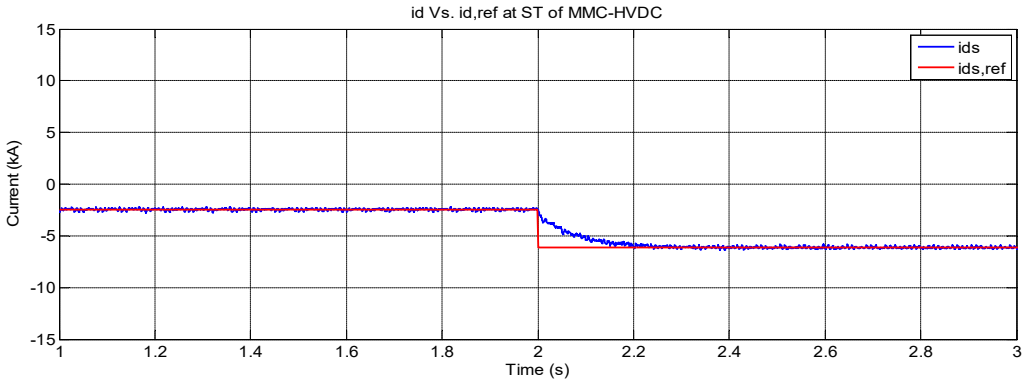

Figure 67: d-component current against its reference

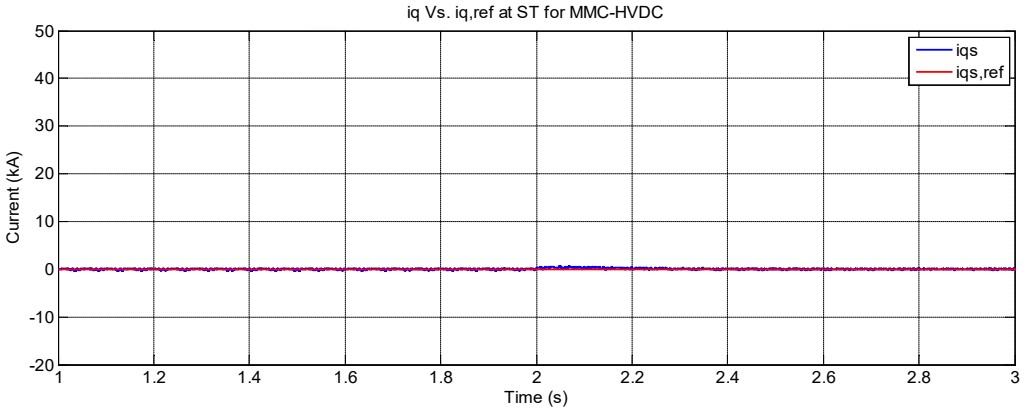

Figure 68: q-component current against its reference

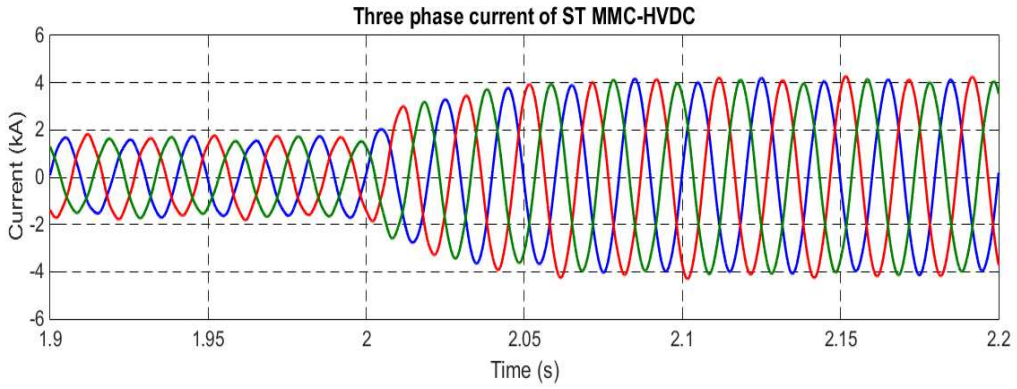

Figure 69: Nine-Level MMC three-phase grid side current of ST

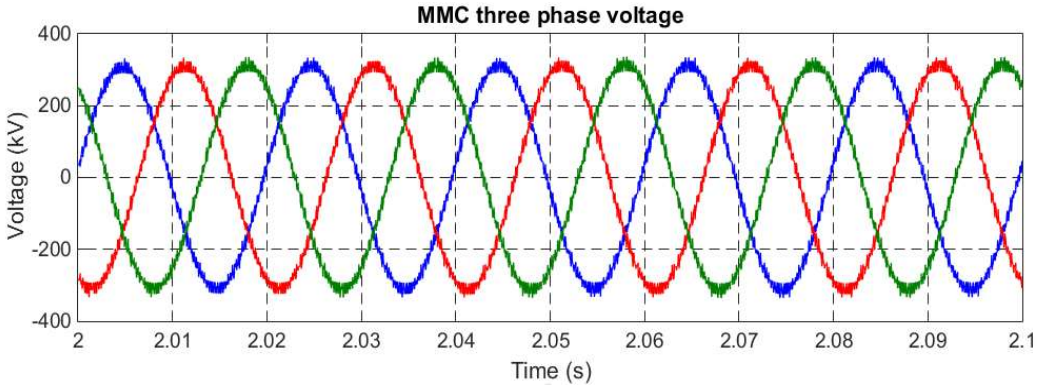

Figure 70: Nine-Level MMC Three-phase voltage at ST

The results presented for the ST shows clearly the controllability of active and reactive powers as they are following their pre-defined reference value.

4.3.3. RT Simulation Results

Similarly, RT is also tested separately to investigate its capability to control the DC link voltage at the reference value. Figure 71 illustrates the DC voltage at the RT versus its reference value. This shows the ability of the system to keep the DC voltage at the predetermined value, which is very important when the sending and receiving terminals are connected as the RT DC link should be kept unchanged, against any change in the active power at the ST. Furthermore, Figure 72 presents the RT terminal reactive power against its pre-determined reference value. At steady state, the reactive power of the RT becomes equivalent to the reference value Q_R^* which is zero. In addition, Figure 73 and Figure 74 show the dq currents respectively versus their reference value. In addition to, Figure 75 and Figure 76 show the three-phase current and voltage at RT.

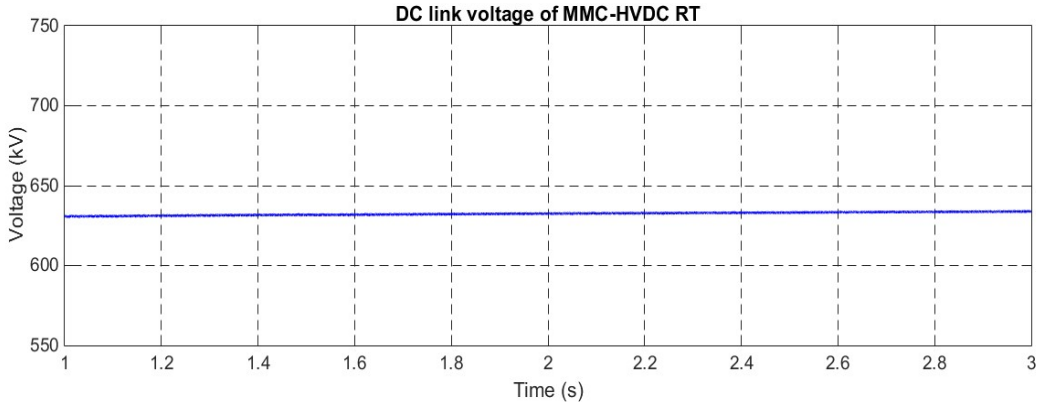

Figure 71: DC link voltage of MMC-HVDC RT

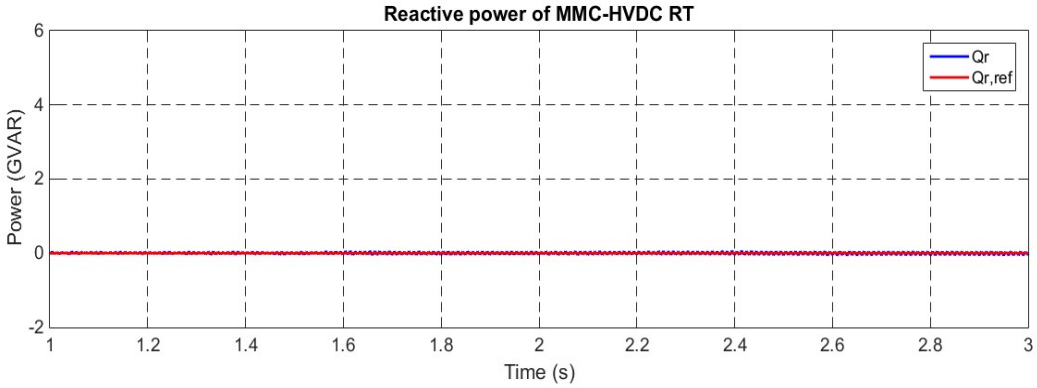

Figure 72: Reactive power and reference reactive power of MMC-HVDC RT

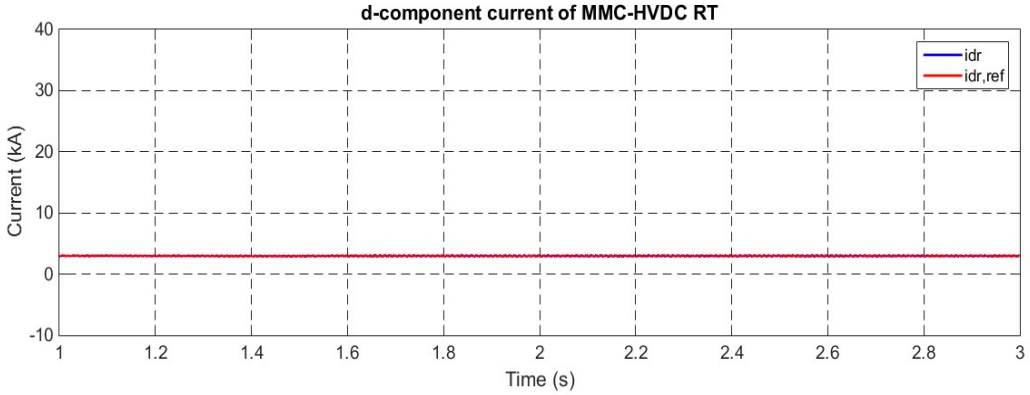

Figure 73: d-component current and reference d-component current of MMC-HVDC RT

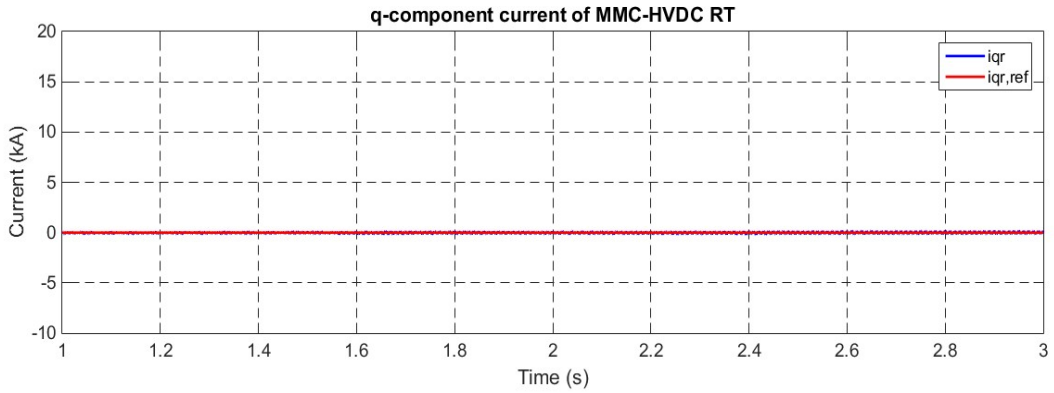

Figure 74: q-component current and reference q-component current of MMC-HVDC RT

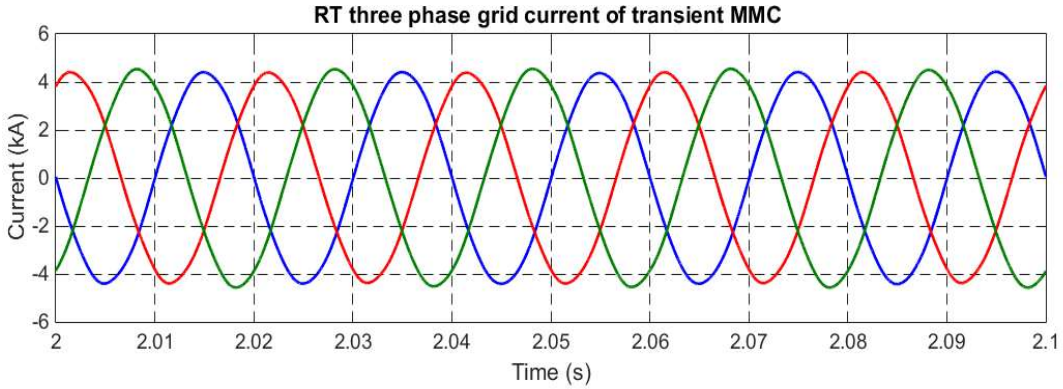

Figure 75: Nine-Level MMC three-phase grid side current of RT

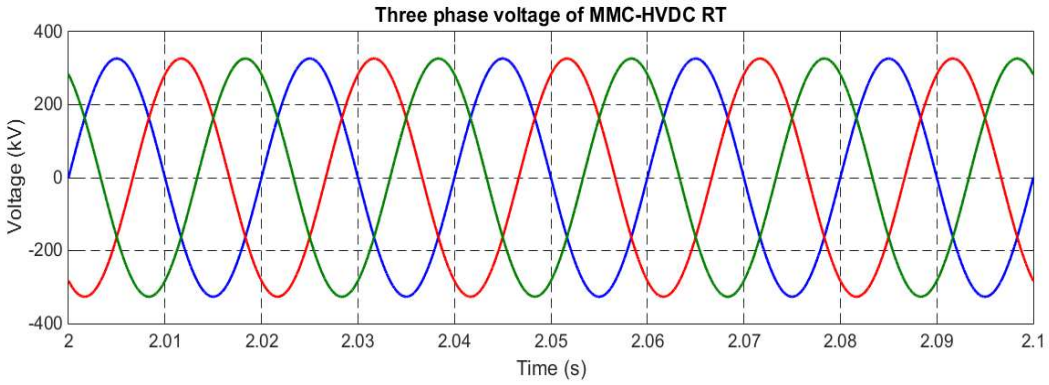

Figure 76: Nine-Level MMC three-phase voltage of RT

4.4. DC Side Fault

DC side faults in HVDC systems should be managed fast and safely regardless of the fault location. Also, the converter should have the ability to resume normal operation after a fault, within approximately one millisecond [73]. Thus, MMC has the privilege when compared to conventional VSCs in HVDC applications because of the following fault handling capabilities [73]:

- The arm inductors limit the AC current whenever the DC bus is short-circuited.
- Different SM topologies provide minimized losses as well as fault blocking capability.

Fault analysis for MMC-based HVDC system is similar to that of the VSC-HVDC system and can be summarized as follows:

- SMs normal operation stage: During this phase, the MMC is still operating normally where the SM is still in the on state, and the SM capacitors are discharging. Hence, the fault detection should be fast enough in order to block the SMs as the

semiconductor devices may be damaged because of the high current [73].

- Initial stage after blocking SMs: In this stage, the SMs are blocked, and the freewheeling diodes D2 are energized. This means that the SM capacitors are bypassed by the fault current, and hence the capacitor will not be discharged, but the arm inductors are discharged. In addition, the AC side source keeps feeding the fault current through the freewheeling diodes and the arm inductors acting as an uncontrolled rectifier as in Figure 77.

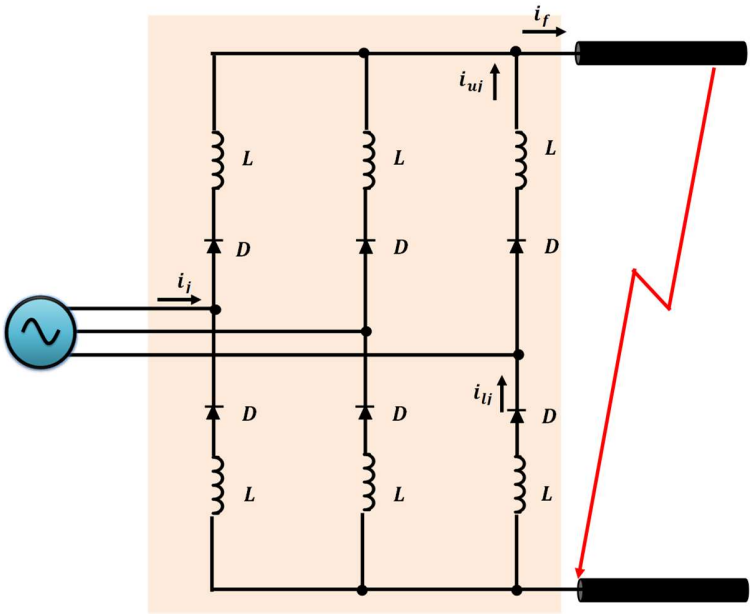

Figure 77: Equivalent fault circuit during blocked SMs

The behavior of the MMC-HVDC systems is studied for the same scenarios of the two-level VSC, where, the system has been subjected to a pole-to-pole fault at the ST side.

However, in MMC-HVDC the need for DC line limiting reactors is less compared to conventional VSC-HVDC because of the existence of the arm inductors. Nevertheless, large inductors are proposed for future HVDC grids as in [71]. However, using large inductors has several drawbacks as it introduces losses and changes the dynamics of the system. One solution to overcome the drawbacks of these large inductors is Hybrid Current Limiting Circuit (HCLC) that is proposed in [100] as shown in Figure 78. This HCLC operates only during fault conditions to limit the fault current, which reduces the requirements of the DCCBs capacity and breaking speed. Also, it improves the modeling of the system as it requires less time to simulate.

HCLC consists of a limiting reactor located at the ends of the DC lines. This limiting reactor L_{CL} is placed in parallel with an energy dissipation circuit compromised from absorption resistor R_{CL} in series with double thyristor switches T_1 and T_2. In this section, a 2 mH inductor is connected in series with L_{CL}= 18 mH to form 20 mH used earlier in this study. The purpose in the coming first two sections is to study the behaviour of the system during DC side fault through different resistances, but the purpose of section 4.4.3 is to understand the behaviour of the system during the implementation of DCCB and HCLC.

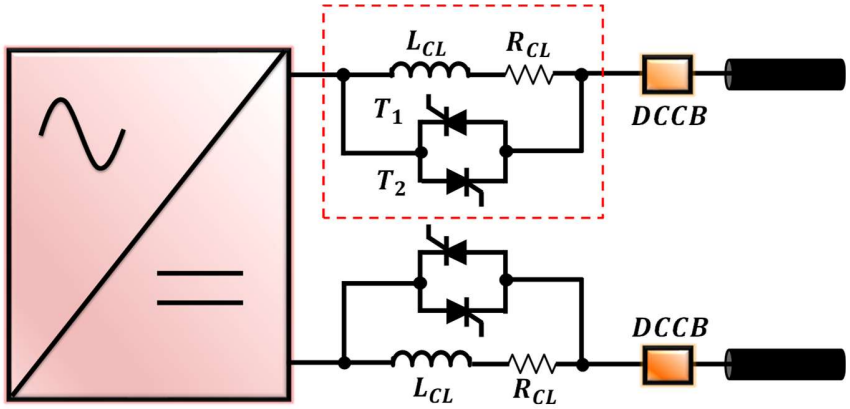

Figure 78: Hybrid current limiting circuit (HCLC)

4.4.1. Case 1: Low Resistance Fault

A pole-to-pole fault is applied at the DC side of ST through R=0.5 Ω at t= 2 sec, while the active power has step change from P =0.8 to 2 GW at the same time. The results generated show that the DC link voltage of the ST drops near to zero as shown in Figure 79. However, the SMs capacitor voltage maintain constant and smooth voltage during the fault at the SMs nominal voltage as in Figure 80. In addition to, the high amplitude DC fault current shown in Figure 81. Furthermore, the MMC is subjected to high amplitude current passing through the freewheeling diodes known as the arm currents of phase a,b, and c that contributes to the fault as the amplitude of that current is higher after the occurrence of the fault as illustrated in Figure 82. The arm currents are clipped, which explains the rectifier operation mode due to the grid current contribution during the fault. Figure 83 and Figure 84 present the three-phase currents of the ST at the grid and converter sides respectively, in which the system is subjected to high amplitude three-phase current.

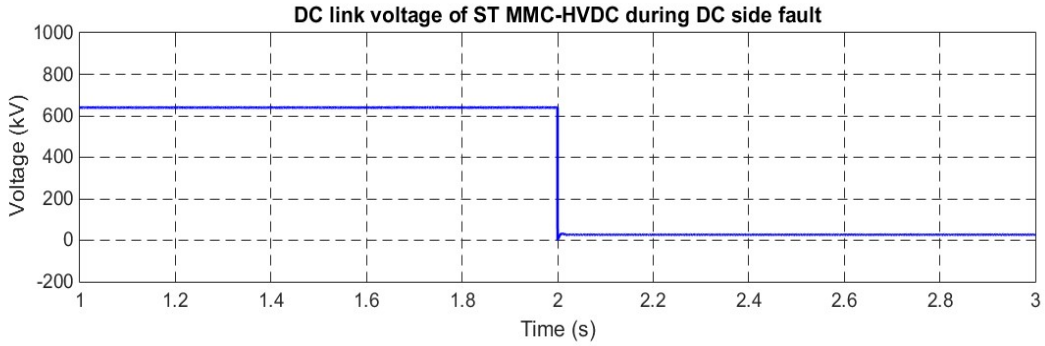

Figure 79: DC link voltage of Nine-Level transient MMC-HVDC system during fault at ST

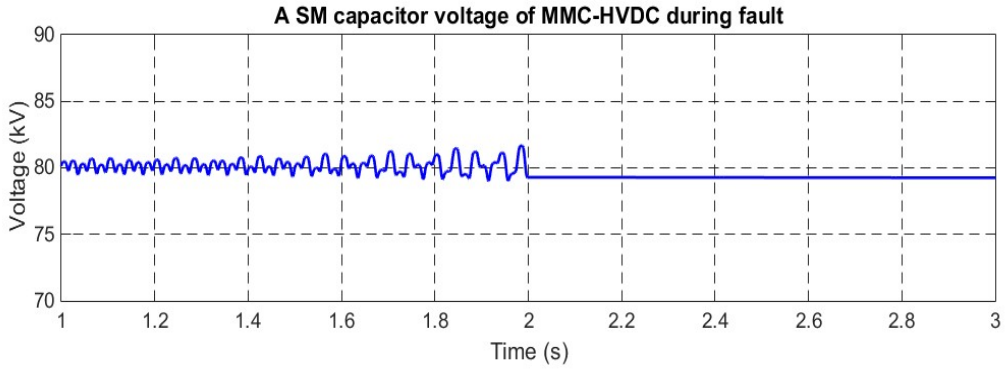

Figure 80: SM capacitor voltage of Nine-Level transient MMC-HVDC system during fault at ST

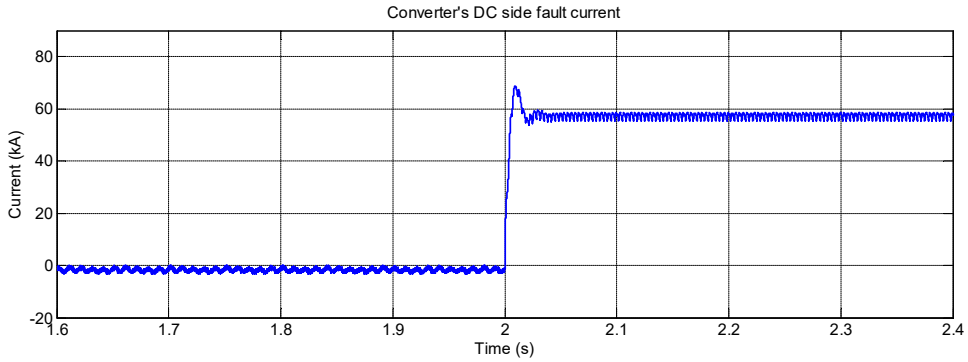

Figure 81: Fault current of the Nine-Level transient MMC-HVDC system during fault at ST

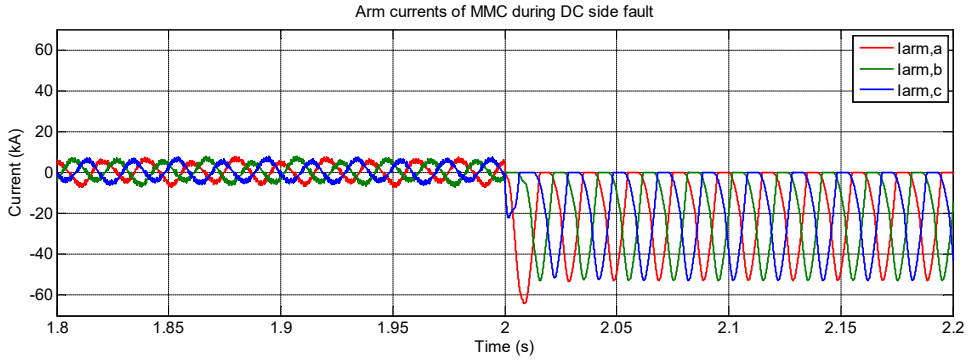

Figure 82: Currents passing through upper arms of Nine-Level MMC-HVDC during fault

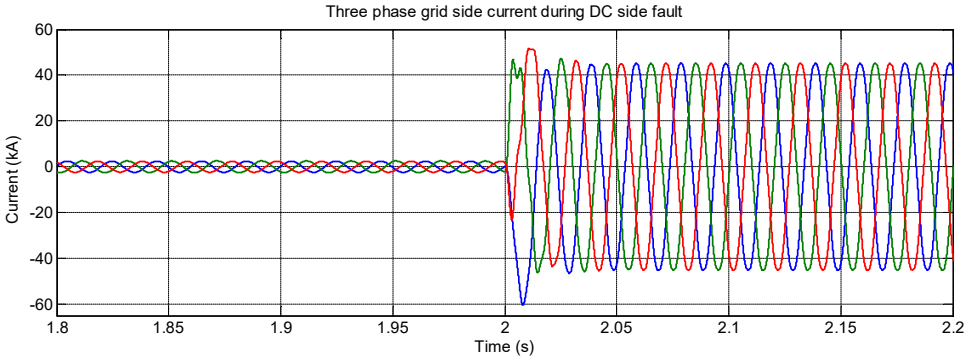

Figure 83: Three-phase grid side current of Nine-Level transient MMC-HVDC during fault at ST

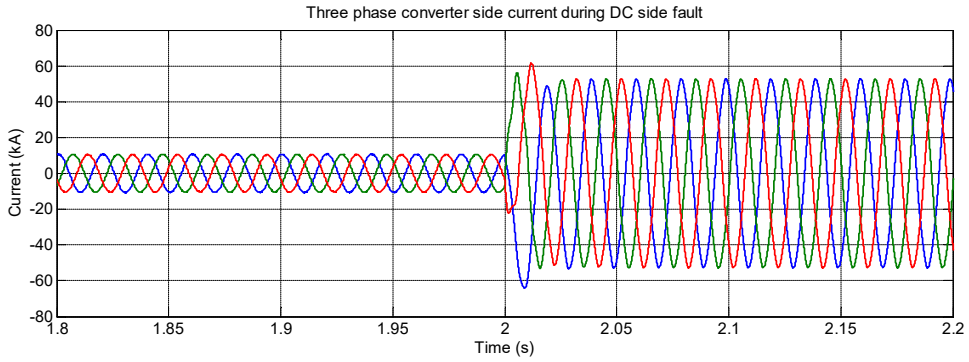

Figure 84: Three-phase converter side current of Nine-Level transient MMC-HVDC during fault at ST

4.4.2. Case 2: High Resistance Fault

A pole-to-pole fault is applied at the DC side of ST through R=5 Ω at t= 2 sec, while the active power has the same step change defined earlier in the previous section at the same time. The results generated show that the DC link voltage of the ST dropped significantly to 200 kV which is slightly higher than zero because of the higher resistance as shown in Figure 85. However, the SMs capacitor voltage maintain constant and smooth voltage during the fault at the SMs nominal voltage as in Figure 86. In addition to, the DC fault current that has a less amplitude compared to the low resistance case as shown in Figure 87. Furthermore, the high amplitude arm currents of phases a, b, and c of the MMC passing through the freewheeling diodes that contribute to the fault, although the amplitude of that current is less in comparison with section 4.4.1 as illustrated in Figure 88. Also, Figure 89 and Figure 90 present the three-phase current of the ST at the grid and converter sides respectively, in which the system is subjected to high amplitude three-phase current.

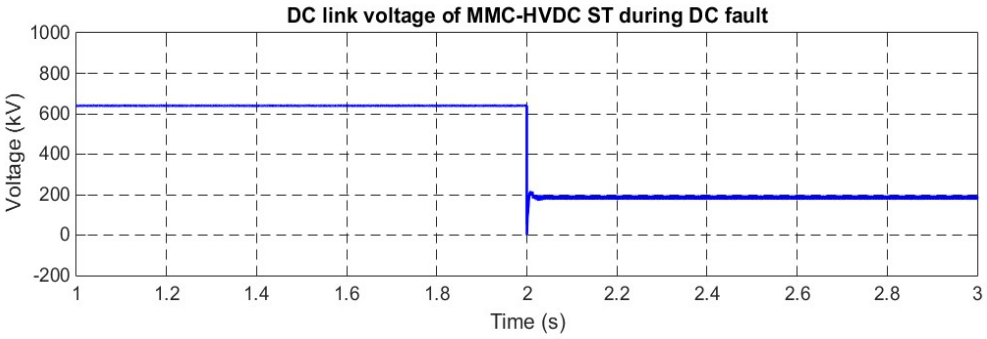

*Figure 85:*DC link voltage of Nine-Level MMC-HVDC system through high resistance fault

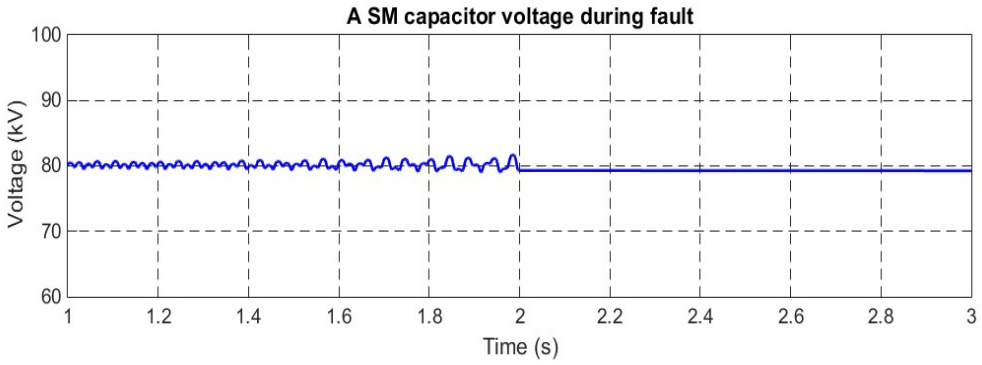

Figure 86: A SM capacitor voltage of Nine-Level MMC-HVDC through high resistance fault

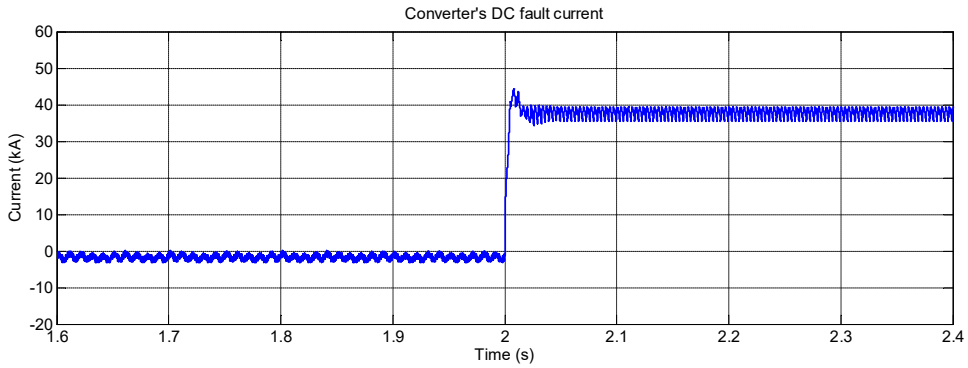

Figure 87: Fault current of Nine-Level MMC-HVDC through high resistance fault

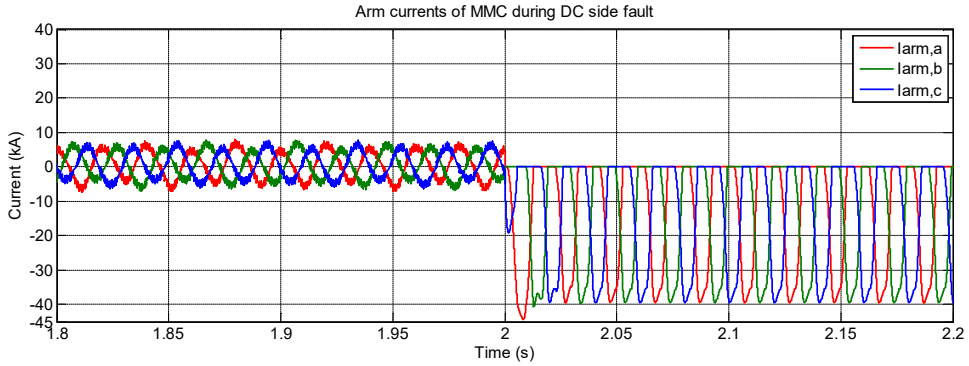

Figure 88: Currents passing through upper arms of Nine-Level MMC-HVDC at high resistance fault

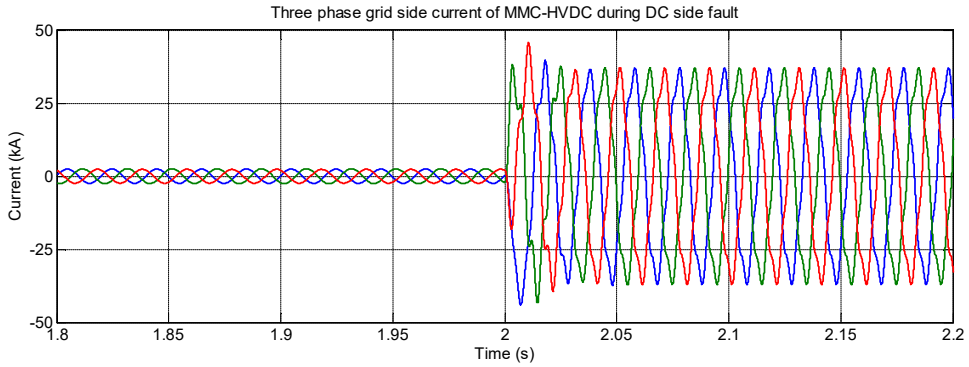

Figure 89: Three-phase grid current of Nine-Level MMC-HVDC at high resistance fault

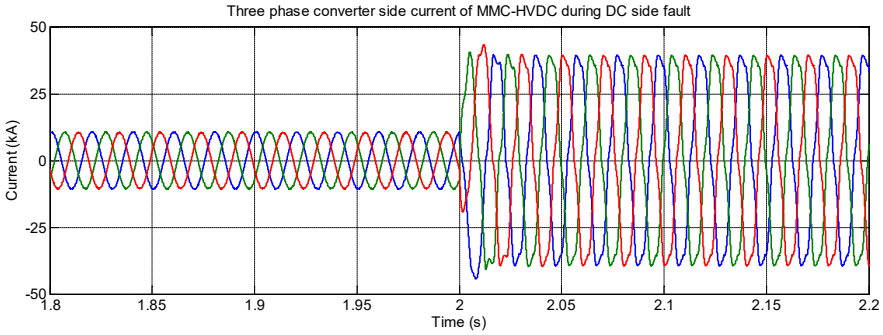

Figure 90: Three-phase converter side current of Nine-Level MMC-HVDC at high resistance fault

4.4.3. Implementation of DCCB

Earlier in section 4.4, a fault has been subjected at t=2 sec, and the behaviour of the system has been discussed during the fault, however in this part DCCB has been implemented to interrupt the fault current after 5 milliseconds while the fault is cleared at t=2.01 sec and the CBs reclose again at t=2.15 sec as presented in the following results. Figure 91 represents the DC link voltage before the fault maintains normal operation at 640 kV, then the voltage drops to zero once the fault occurred. Five milliseconds later the CBs are triggered to interrupt the fault current while the fault is cleared at t=2.01 sec. Therefore, the voltage increases to be slightly above 400 kV because of the open circuit operation, until the CBs are back on to restore the system's normal operation at t=2.15 sec, where the voltage then returns back to 640 kV. As well as, Figure 92 represents the SM capacitor voltage operating normally and balanced at 80 kV as the DC link voltage is 640 kV, however, the moment the fault occurred the SM capacitor keeps the energy stored until the fault is cleared and the CBs reclose again to restore normal operation. Similarly, Figure 93

presents the converter's DC side current; it shows the normal operation of the current before the fault occurs, once the fault occurred a high peak current arise. When the CBs are triggered, the current drops to zero until the fault is cleared and the CBs are back at t=2.15 sec. It is visible that rate of change of the fault current peak is slower in this case because of the existence of the limiting reactor of hybrid DCCBs. Furthermore, Figure 94 and Figure 95 represent grid and converter side three-phase currents for the same scenario. During the fault, the grid side current has increased until the CBs restore normal operation of the system after the fault is cleared. Then after restoring the system's normal operation, normally a ramp of the power is introduced. However, the converter side current drops to zero during the fault till the closure of the CBs at t= 2.15 sec. It is important to highlight that the predefined reference power is designed to increase at t=2 sec. Thus the current amplitude when the system is restored is higher than normal operation before the occurrence of the fault.

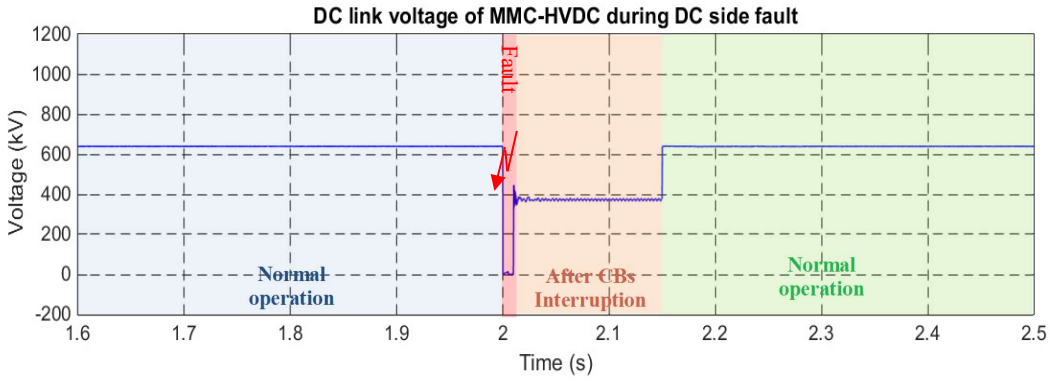

Figure 91: DC link voltage of Nine-Level transient MMC-HVDC during temporary fault

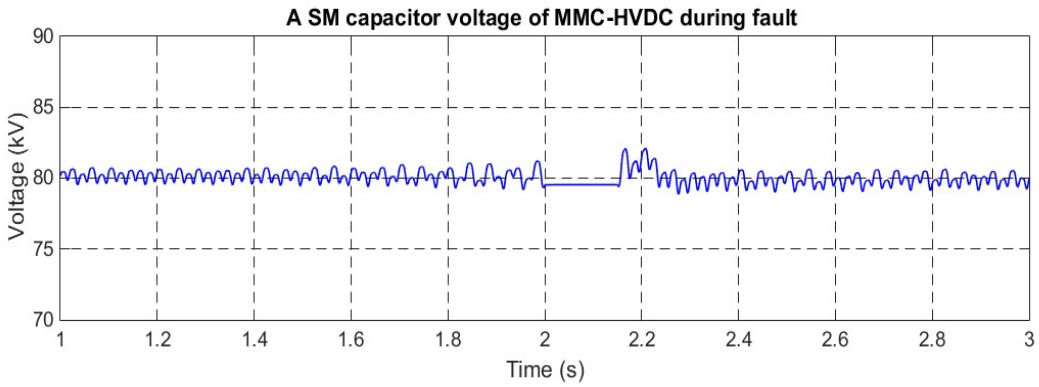

Figure 92: A SM capacitor voltage of Nine-Level transient MMC-HVDC during temporary fault

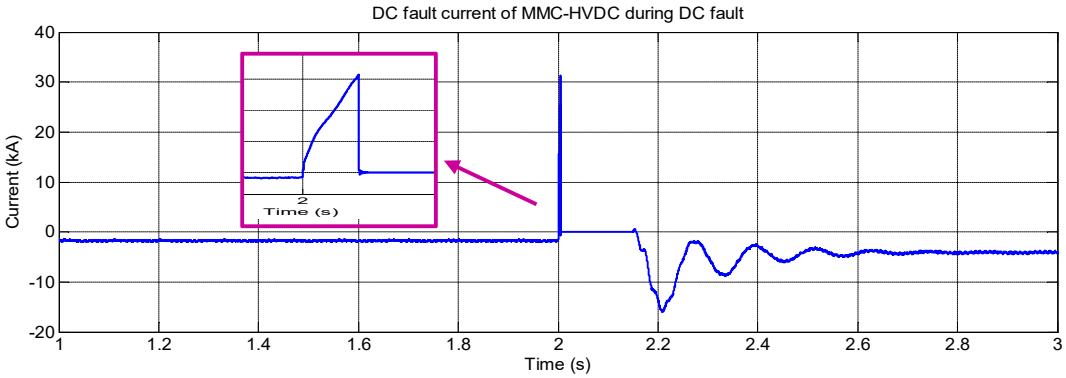

Figure 93: DC fault current of Nine-Level transient MMC-HVDC during temporary fault

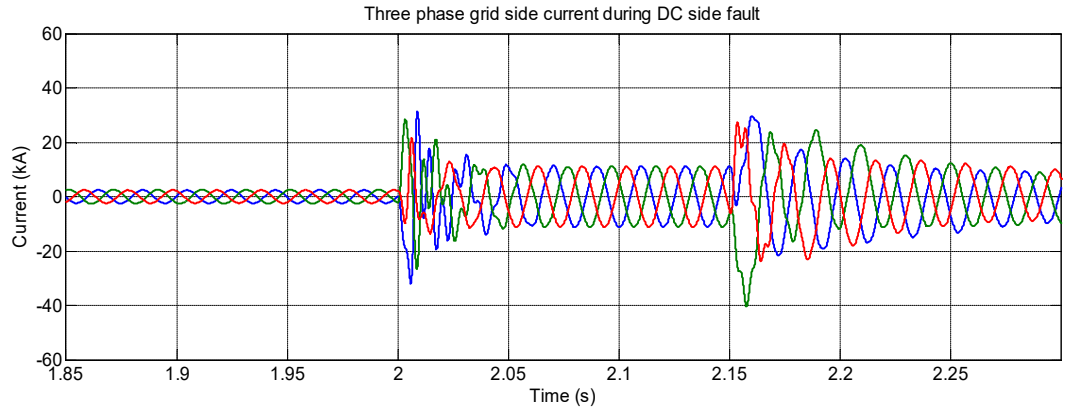

Figure 94: Three-phase grid side current of Nine-Level transient MMC-HVDC during temporary fault

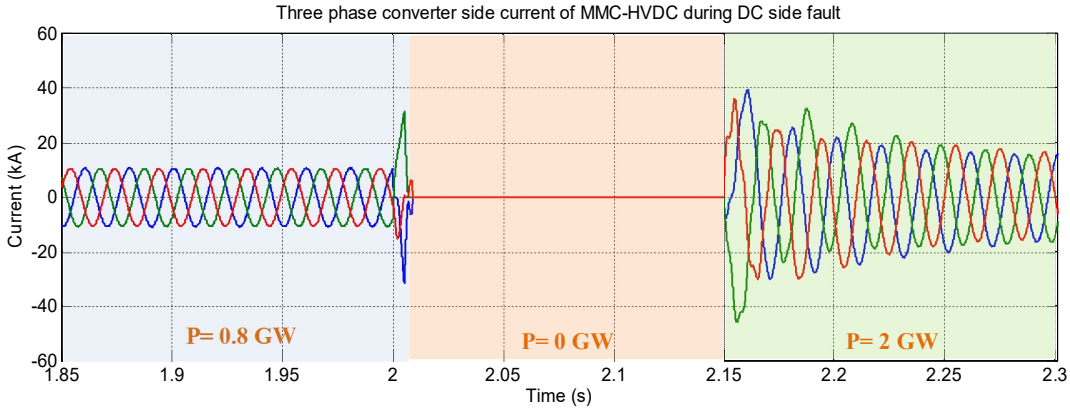

Figure 95: Three-phase converter side current of Nine-Level transient MMC-HVDC during temporary fault

4.5. Conclusion

Two-terminal HVDC transmission systems are used as a solution for saving cost and conversion losses, also for providing enhanced reliability and functionality of DC grids. Therefore, studying and modeling of two-terminal HVDC system based on MMC is extremely important in order to ensure safe and reliable operation of those large-scale interconnected networks. Especially, during DC network disturbances as discussed earlier in this chapter. Also, because studying the two-terminal HVDC system gives an idea about multi-terminal HVDC transmission systems. The results generated in this section for each of the sending and receiving terminals proves the effectiveness and the capability of the MMC-HVDC to generate enhanced harmonic profile. Furthermore, Hybrid HV DCCBs have proven its effectiveness in terms of speed and conduction losses to overcome the drawbacks of the existing CBs.

CHAPTER 5: TWO-TERMINAL MMC AVERAGED MODEL-BASED HVDC SYSTEM

5.1 MMC Averaged Model (AVM-MMC)

5.1.1 AVM-MMC: Topology and Operation

MMCs used for HVDC transmission systems consist of hundreds of cells per arm. Therefore, in order to model and simulate MMC for HVDC systems, it is computationally an intensive task that needs high computing capability and large memory machines. In addition, it requires a long time to simulate, as the detailed MMC model contains a considerable number of switches. Thus, in this case, an AVM-MMC that mimics the dynamic behavior of the detailed MMC is very useful, as it provides a fast performance of converter simulation, which is highly needed for large systems such as multi-terminal HVDC transmission systems [101], where multi-terminal HVDC systems contain several MMCs each of hundreds of levels. Therefore, MMC Averaged Model (AVM-MMC) has been addressed recently in the literature as it is highly needed. The study in [101], examines the applicability of AVM-MMC operating in VSC-HVDC transmission systems. Moreover, it presents and studies the AVM-MMC under DC fault conditions. The work in [102] introduces AVM-MMC and adapts the DC side AVM-MMC to present a simplified way of transient performance during DC side fault. In [104], AVM-MMCs considering SM capacitor voltage ripple is introduced. The effect of the SM capacitor voltage ripple on the dynamic behavior of MMC has been studied, and the equivalent impedance of the DC and AC sides of the converters are evaluated. Based on the equivalent impedances, an AVM-MMC, that comprises the equivalent capacitors reflecting the capacitor voltage ripple, has been presented. In [104], numerous modifications proposed on the existing models,

resulting in improved AVM-MMC, that is significantly more accurate and can be used for a wider range of studies such as DC faults. However, the study in [105] presents a novel AVM-MMC for efficient and accurate representation of a detailed MMC–HVDC system. It also conducts a 401-level detailed model MMC-HVDC to validate the AVM and study the performance of both models when employed in a 400 KV transmission system. Generally, the AVM-MMC model is based on the converter dynamic equations (26)-(37) [106] presented in the following section, using continuous arm voltages rather than switched voltages generated using SPWM. This means that the SMs in each arm will be represented by a controlled voltage source as illustrated in Figure 96 that shows a three-phase AVM-MMC.

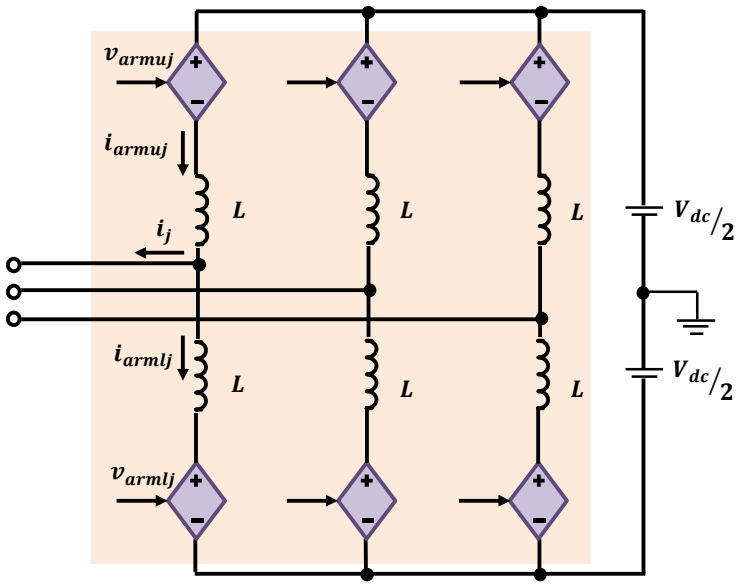

Figure 96: Three-phase MMC averaged model

5.1.2 AVM-MMC Mathematical Model

From the AVM-MMC shown in Figure 96, the following set of equations (26)-(37) can be written according to Kirchhoff voltage law as per [106]. The voltage in each loop can be written as:

$$\frac{V_{dc}}{2} = L_{uj}\frac{d}{dt}i_{armuj} + v_{armuj} \tag{26}$$

$$\frac{V_{dc}}{2} = L_{lj}\frac{d}{dt}i_{armlj} + v_{armlj} \tag{27}$$

Where $i_{arm,uj}$ and $i_{arm,lj}$ are the upper and the lower arm currents of phase *j (j=a,b,c)* respectively. Similarly, for $v_{arm,uj}$ and $v_{arm,lj}$.

$$\begin{aligned} i_{armuj} &= \frac{i_j}{2} + i_{ccj} \\ i_{armlj} &= -\frac{i_j}{2} + i_{ccj} \end{aligned} \tag{28}$$

Where i_j is the AC current of phase j and i_{ccj} is the circulating current of phase j.

The modulating signals in upper and lower arms are the same modulation signals expressed earlier in (25). The summation of *n* SM capacitor voltages shown in Figure 9, in upper and lower arm respectively can be given as:

$$v_{cuj} = \sum_{K=1}^{n} v_{cuKj}\ , \qquad v_{clj} = \sum_{K=1}^{n} v_{clKj} \tag{29}$$

Where *n* represents the number of SMs per arm (N-1). The arm voltages in the upper arm v_{armuj} and in lower the arm v_{armlj} can be obtained by:

$$v_{armuj} = n_u v_{cuj}\ , \qquad v_{armlj} = n_l\, v_{clj} \tag{30}$$

Furthermore, SM capacitor voltages depend, in turn, on its capacitance C_{SM} and currents

i_{CU} or i_{CL} as:

$$C_{SM}\ \frac{dv_{cuKj}}{dt} = n_u\ i_{armuj}$$
$$C_{SM}\ \frac{dv_{clKj}}{dt} = n_l\ i_{armlj} \tag{31}$$

Assuming that all capacitor voltages in the converter arm are balanced, which means that sums of capacitor voltages (29) are equal to $V_{cuj}= n_u V_{cuKj}$ and $V_{clj}= n_l V_{clKj}$ Therefore, equation (31) can be rewritten to

$$C_{arm}\ \frac{dv_{cuj}}{dt} = n_u\ i_{armuj}$$
$$C_{armj}\ \frac{dv_{clj}}{dt} = n_l\ i_{armlj} \tag{32}$$

Where C_{arm} is referred to as the arm capacitance that corresponds to an equivalent capacitance of the series connected capacitors of all SMs in the converter arm.

$$C_{armj} = C_{SM}/n \tag{33}$$

Due to the fact that both arms parameters are typically equal, then $L_{uj}= L_{lj} =L_j$.

Substitute by (28) & (30) in (26) & (27) gives:

$$\frac{V_{dc}}{2} = L_j \frac{d}{dt}\left(\frac{i_j}{2} + i_{ccj}\right) + n_u v_{cuj} \tag{34}$$

$$\frac{V_{dc}}{2} = L_j \frac{d}{dt}\left(-\frac{i_j}{2} + i_{ccj}\right) + n_l v_{clj} \tag{35}$$

By adding equations (34) & (35)

$$V_{dc} = 2L_j \frac{d}{dt}\left(i_{ccj}\right) + n_u v_{cuj} + n_l v_{clj} \tag{36}$$

From equations (26)-(36) the state space representation of the MMC averaged model is [106]:

$$\frac{d}{dt}\begin{bmatrix} i_{ccj} \\ V_{cuj} \\ V_{clj} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{n_u}{2L_j} & -\frac{n_l}{2L_j} \\ \frac{n_u}{C_{armj}} & 0 & 0 \\ \frac{n_l}{C_{armj}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{ccj} \\ V_{cuj} \\ V_{clj} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_j} \\ \frac{n_u i_j}{2C_{armj}} \\ -\frac{n_l i_j}{2C_{armj}} \end{bmatrix} \tag{37}$$

5.1.3 AVM-MMC Modulation

In the detailed model, for an N-level MMC, each arm with (N-1) SMs requires (N-1) triangular carrier waves with switching frequency of f_s. Similarly, for the AVM-MMC, where the control signal of the controlled voltage source plays the main role in this model, as the output of the MMC is generated according to this control signal. Also, the number of levels of the MMC is dependent on this control signal. PD-PWM is applied to control the AVM-MMC. The N-1 PD-PWM is compared with the sinusoidal signals (modulating signals) expressed in (25), in order to generate the N-level staircase waveform. The basic concept of the PD-PWM applied in this study is represented in Figure 97 (a) for f_s= 2 kHz of the upper arm, however, Figure 97 (b) shows the summation of the firing signals generated.

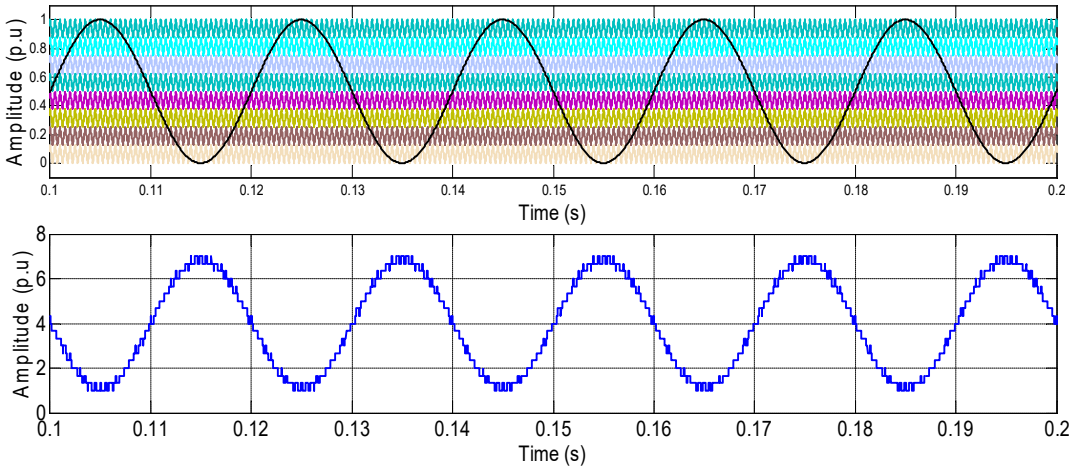

Figure 97: 9-Level AVM-MMC (a) PD-PWM technique applied (b) arm voltage of AVM-MMC

5.2 Two-terminal AVM-MMC-based HVDC System

In this section, the power transfer in the two-terminal AVM-MMC-based HVDC system is modeled and controlled in a similar way as transient MMC-based HVDC transmission discussed earlier in details in chapter 3, section 3.3. Similar to what has been implemented in chapter 3, power control is carried out at ST. Nevertheless, DC link voltage control is carried out at the RT. The schematic of a two-terminal MMC-HVDC system is illustrated in Figure 64. The AVM-MMC Simulink model is presented in Appendix C.

5.2.1 AVM-MMC Simulation Results

The two-terminal AVM-MMC-based HVDC system has been modeled and simulated using 25-level AVM-MMC discussed earlier in this chapter in order to validate its efficiency compared to MMC transient model technology. Same scenario has been implemented in this chapter, where each terminal has been tested separately as shown in the results. The simulation parameters of the AVM-MMC model are presented in Table 5. As the number of levels has increased, the values of SM capacitor C and the arm inductors L have changed to fit the requirements of the 25-level AVM-MMC.

Table 5: AVM-MMC model simulation parameters

Parameter	**Value**
L	15 mH
C	30 mF
f_s	2 kHz
V_{DC}	640 kV
m_a	0.9

5.2.1.1 ST Simulation Results

The results generated in this section present the ST terminal active and reactive powers respectively against their pre-determined reference value as in

Figure *98* and Figure 99. At steady state, the active power of the ST becomes equivalent to the reference value P_{ST}^{*}. The reactive power is set to zero equivalent to the reference value. In addition, Figure 100 and Figure 101 show the dq currents respectively and their reference value. In addition, Figure 102 and Figure 103 show the three-phase current and voltage at ST.

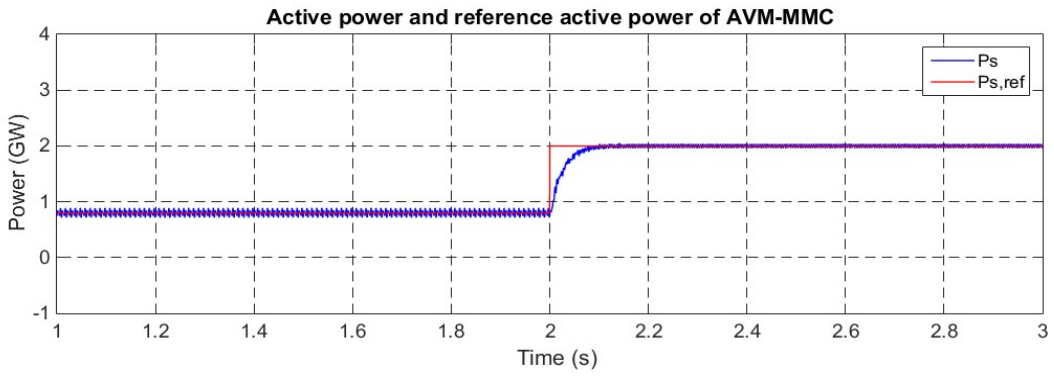

Figure 98: Active power and reference active power of 25-Level AVM-MMC of ST

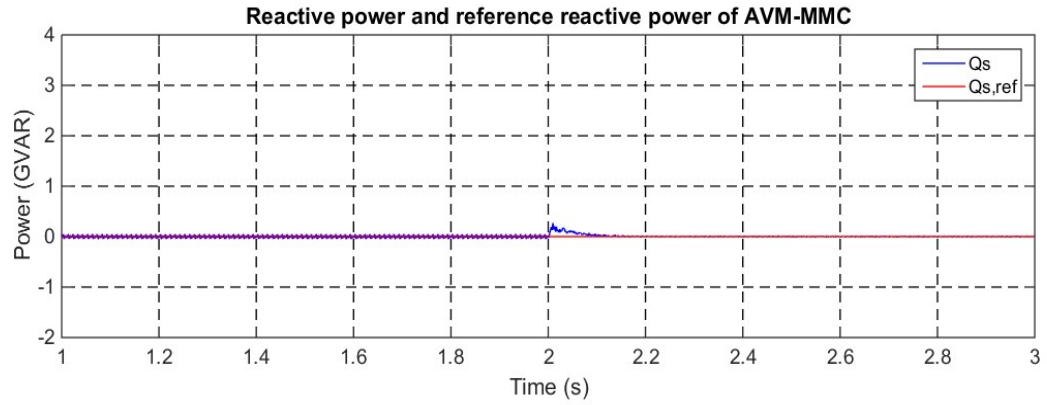

Figure 99: Reactive power response Qs against. Qs,ref of AVM-MMC of ST

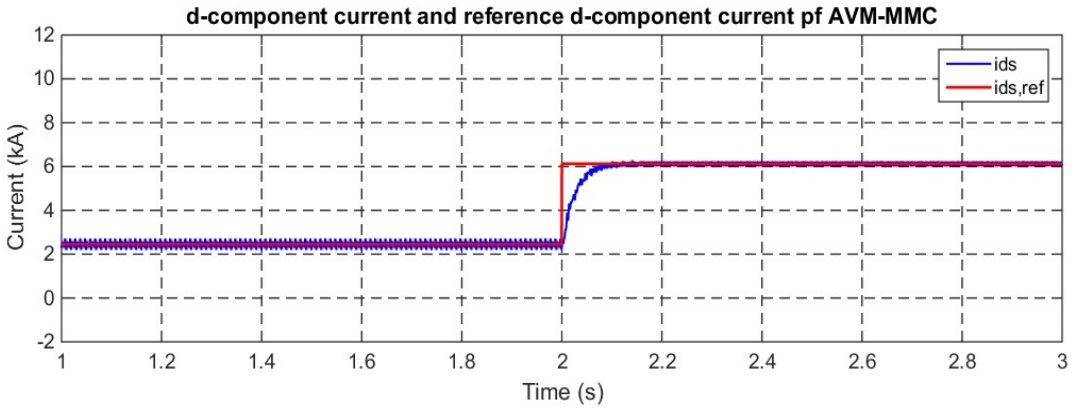

Figure 100: AVM-MMC d-component current against its reference of ST

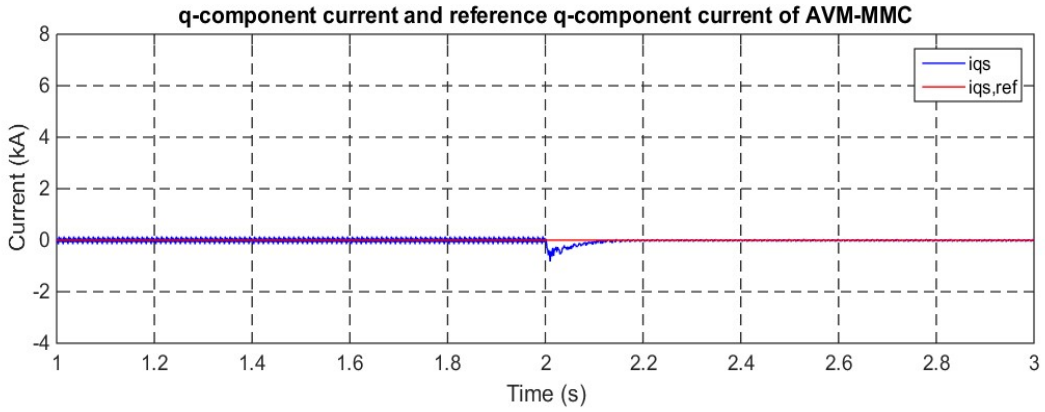

Figure 101: AVM-MMC q-component current against its reference of ST

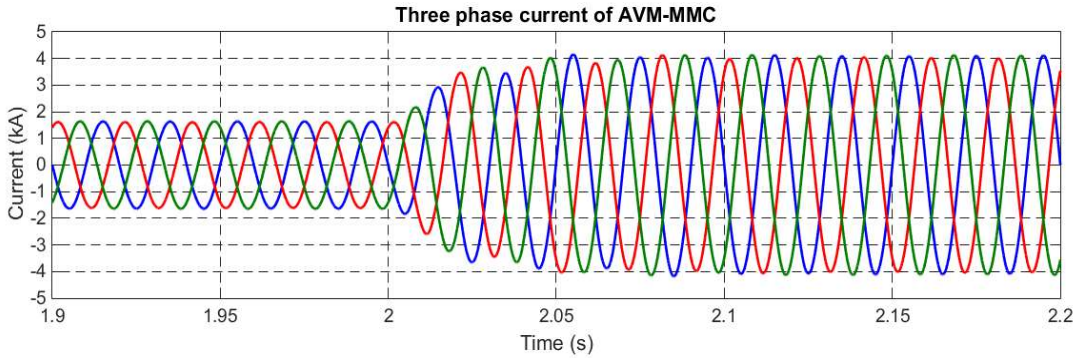

Figure 102: 25-Level AVM-MMC three-phase current at ST

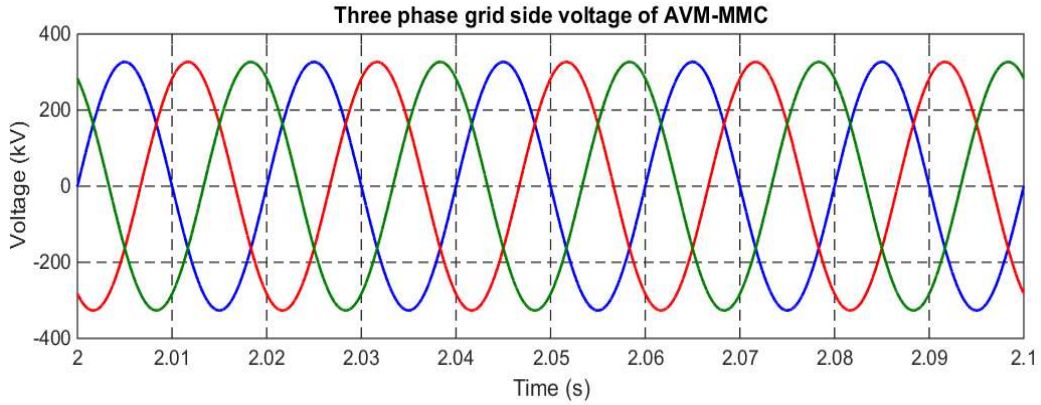

Figure 103: 25-Level AVM-MMC three-phase voltage at ST

The ST results generated in this chapter represents the same behavior of the ST using detailed model MMC. However it took less time to be generated which gives the ability to conduct higher MMC levels.

5.2.1.2 RT Simulation Results

Similarly, RT is also tested separately to investigate its capability to control the DC link voltage at the reference value. Figure 104 illustrates the DC voltage at the RT settled at the reference value 640 kV. This shows the ability of the system to keep the DC voltage at the predetermined value, which is very important when the sending and receiving terminals are connected as the RT DC link should be kept unchanged, against any change in the active power at the ST. Furthermore, Figure 105 presents the RT terminal reactive power against its pre-determined reference value. At steady state, the reactive power of the RT becomes equivalent to the reference value Q_R^* which is zero. In addition, Figure 106 and Figure 107 show the dq currents respectively against their reference. In addition to, Figure

108 and Figure 109 show the three-phase voltage and current at RT.

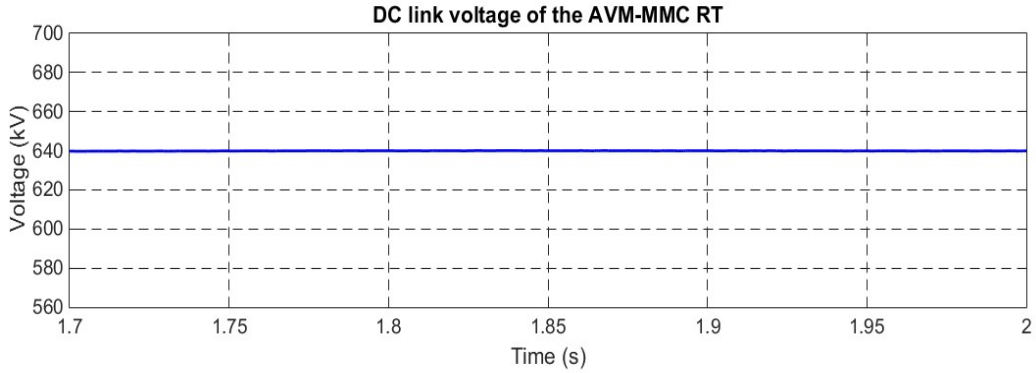

Figure 104: DC link voltage of AVM-MMC RT

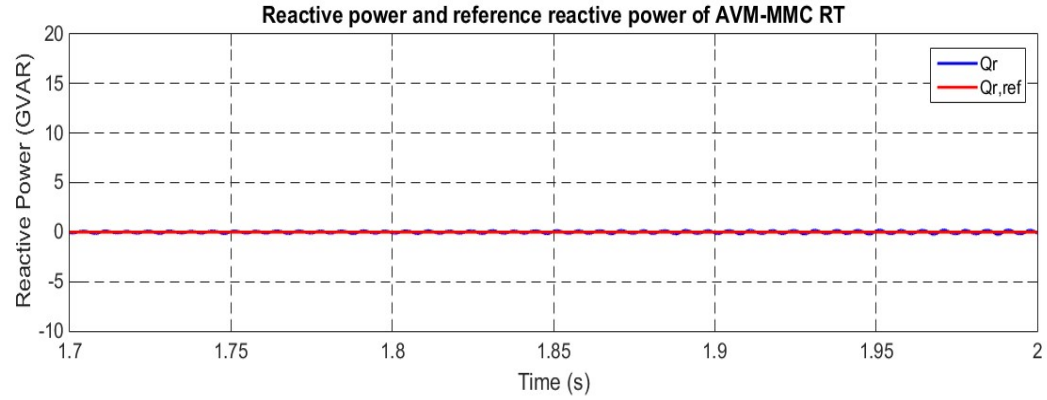

Figure 105: Reactive power and reference reactive power of AVM-MMC RT

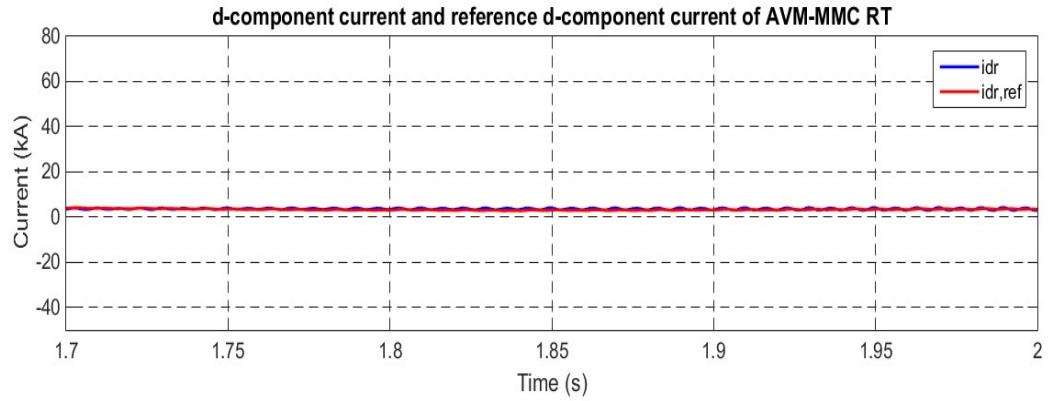

Figure 106: d-component current and its reference at AVM-MMC RT

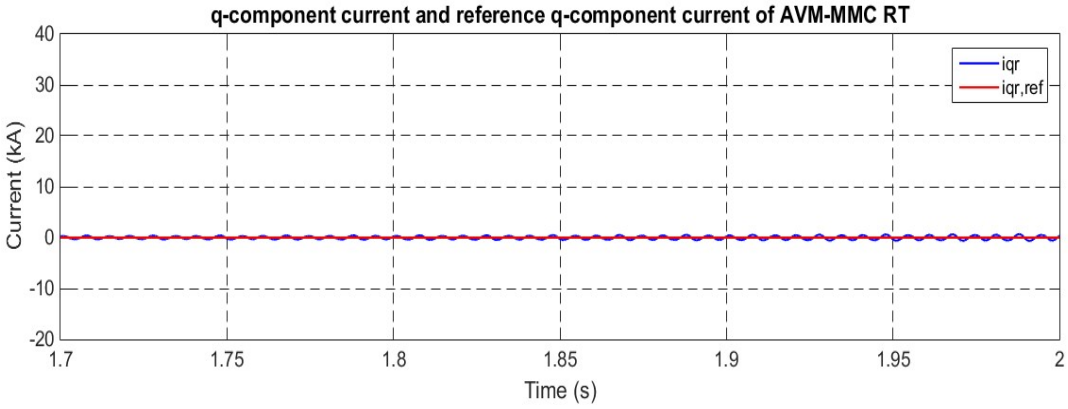

Figure 107: q-component current and its reference at AVM-MMC RT

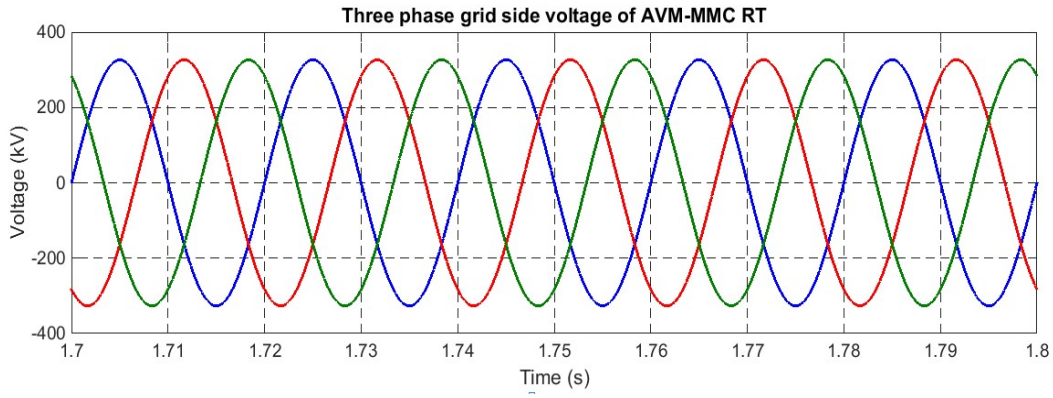

Figure 108: 25-Level AVM-MMC three-phase grid side voltage at RT

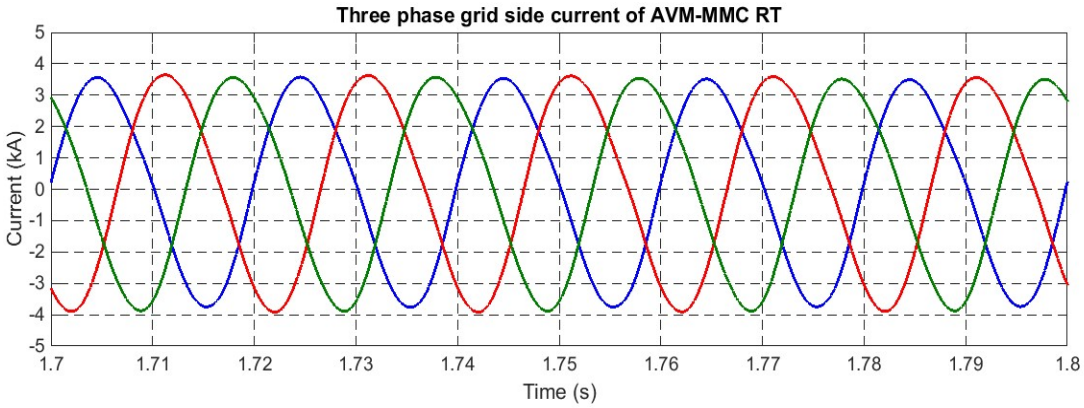

Figure 109: 25-Level AVM-MMC three-phase grid side current at RT

5.2.2 Two-terminal AVM-MMC Simulation Results

Earlier in this chapter, the results for both sending and receiving ends have been presented individually, in order to test each terminal aside as the simulation takes longer time when both terminals are connected. In this section, both sending and receiving terminals are

connected to form a point-to-point AVM-MMC connection as per Appendix C, where the Simulink model is presented. The results below verify the operation of the AVM-MMC HVDC system, in which the DC link voltage of RT is kept constant at the predetermined value which is 640 kV and that the ST voltage is slightly higher than the RT voltage as per Figure 110. In Figure 111, the DC link current is presented as a positive value current, which indicates that the power flow is from sending to receiving end of the AVM-MMC HVDC system.

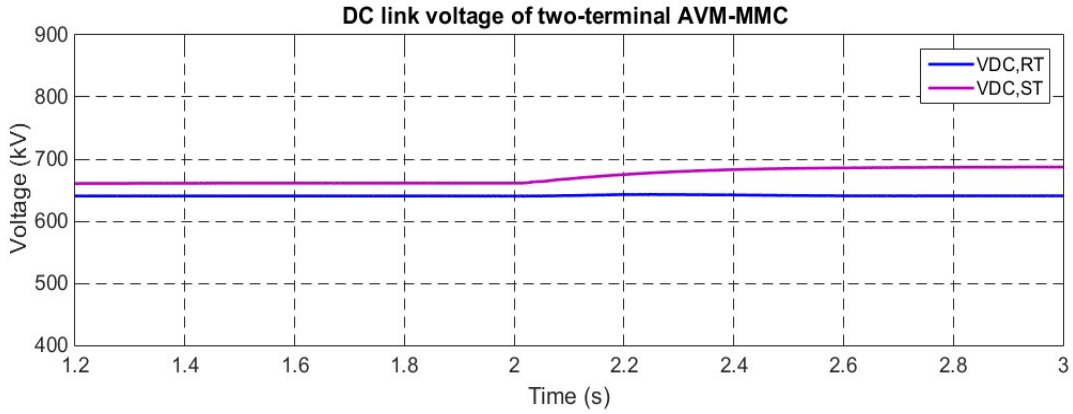

Figure 110: 25-Level AVM-MMC two-terminal DC link voltage

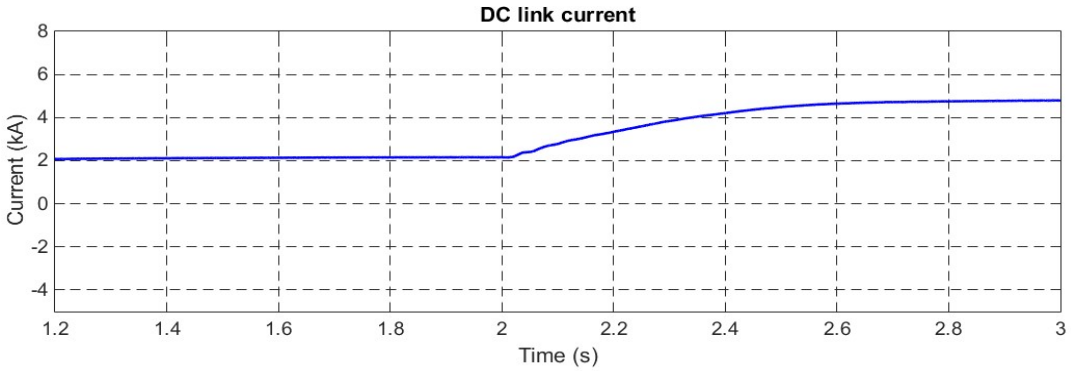

Figure 111: 25-Level AVM-MMC two-terminal DC link current

5.3 Conclusion

In conclusion, the purpose of AVM-MMC is to capture the dynamic behavior of the MMC transient model in which the switching actions of IGBTs are implicitly modeled using simplified functions and controlled sources. This facilitates the study of large MMC-based systems such as multi-terminal HVDC as it takes less computing time in comparison with detailed model MMC that take several minutes to run the simulation. A two-terminal AVM-MMC HVDC system using 25-level AVM-MMC has been modeled and implemented successfully. The modeled system accurately imitates the dynamic performance of the detailed model in less time.

CHAPTER 6: CONCLUSION & FUTURE WORK

6.1 Conclusion

Voltage Source Converter-based High-Voltage Direct Current (VSC-HVDC) transmission system is a promising solution to transmit large amounts of power over long distances using back-to-back or point-to-point configurations. This is obvious in various HVDC applications such as DC interconnections to provide higher reliability, multi-terminal direct current transmission, installation of offshore wind power generation such as Europe super DC grid and installation of other renewable energy sources into existing AC networks.

The development of semiconductor devices such as IGBTs has favored VSC-based HVDC systems over classical line-commutated Current Source Converter-based HVDC (CSC-HVDC) systems. Those advantages made VSC-HVDC a suitable solution for building Multi-Terminal HVDC (MT-HVDC) systems. However, protection of HVDC systems is a major concern especially for MT-HVDC systems, where fast protection algorithm is highly needed in comparison with conventional HVAC protections schemes that have been used for DC side protection. Hence, ABB has recently developed hybrid DCCBs as a solution for HVDC faults.

VSC is the main block for VSC-HVDC technology where, several VSC topologies have been developed for HVDC systems including the conventional two and three-level converters, multilevel converters, and recently Modular Multilevel Converter (MMC) that has the capability to meet HV levels at both AC and DC sides of HVDC converter station. This has accelerated the adoption of MMC in modern HVDC transmission market, due to its scalability, modularity, and fault ride through capability. MMC employs multiple SMs

connected in series from their AC side terminals in order to construct a multilevel. SMs can be constructed using Half-Bridge SM, Full-Bridge SM, Switched Capacitor SM, and other topologies. Thus, one main concern associated with MMC is SM capacitor voltage balancing.

Therefore, this thesis investigates and models a point-to-point VSC-based HVDC transmission system using nine-level MMC transient model, and 25-level AVM-MMC using MATLAB/Simulink platform to meet the requirements of HVDC systems such as HV requirements and fault ride through capability. Also, studying the conventional two-level converter system initially is an important step to understand the behavior of the two-terminal VSC-HVDC transmission system. The design of the MMC transient model in this study is based on Half-Bridge Sub-Modules (HB-SMs) because of its simple structure. However, other structures are discussed. Nevertheless, balancing of the SM floating capacitors, and its modeling are addressed. Then the average model of the MMC-based HVDC system is explored. Also, the behavior during DC side faults is investigated, and the employment of hybrid DC circuit breakers and hybrid current limiting circuit HCLC are introduced for protection and limiting the DC fault current, which introduces a platform for studying large MMC-based HVDC systems in normal operation and during faults.

The results generated using two-level converter have verified the functionality of the VSC-HVDC systems. The powers were well controlled at the ST, and the DC link has been kept unchanged even during power change. Nevertheless, the harmonic profile could be enhanced by using multilevel converter topologies. Similarly, the results generated using MMC-HVDC system for each of the sending and receiving terminals proves the effectiveness and the capability of the MMC-HVDC to generate enhanced harmonic

profile. Furthermore, a pole-to-pole DC side fault has been tested at the ST of the modeled MMC-HVDC and two-level VSC systems, and the behavior of the system during the fault has been studied, and the role of hybrid DCCB has been validated in terms of speed and conduction losses to overcome the drawbacks of the existing CBs. Also, HCLC has been employed to limit the fault current as it allows the use of large reactors during fault conditions only, in which it reduces the requirements of the DCCB's capacity and breaking speed. Finally, 25-level AVM-MMC HVDC is addressed to introduce a platform that facilitates the study of large MMC-based systems such as multi-terminal HVDC. The modeled system accurately imitates the dynamic performance of the detailed model in less time. Hence, both sending and receiving terminals were connected to form a two-terminal HVDC in which the operation of the system was verified.

6.2 Future work

The work presented in this thesis can be further expanded from, the modeling of the two-terminal MMC-based HVDC can be expanded to model a multi-terminal HVDC system using MMC transient and averaged models implemented in this thesis. Throughout this system, different types of DC side faults can be studied along with protection scheme. Also, adding wind farms can be considered to represent a real HVDC link with offshore wind farms instead of using ideal AC networks. In addition, MMC transient model can be further enhanced by the employment of other submodules that are capable of blocking AC side contribution to a fault on the DC side, such as FB-MMC. Moreover, this model can be used as a platform for studying optimal power flow of multi-terminal HVDC systems.

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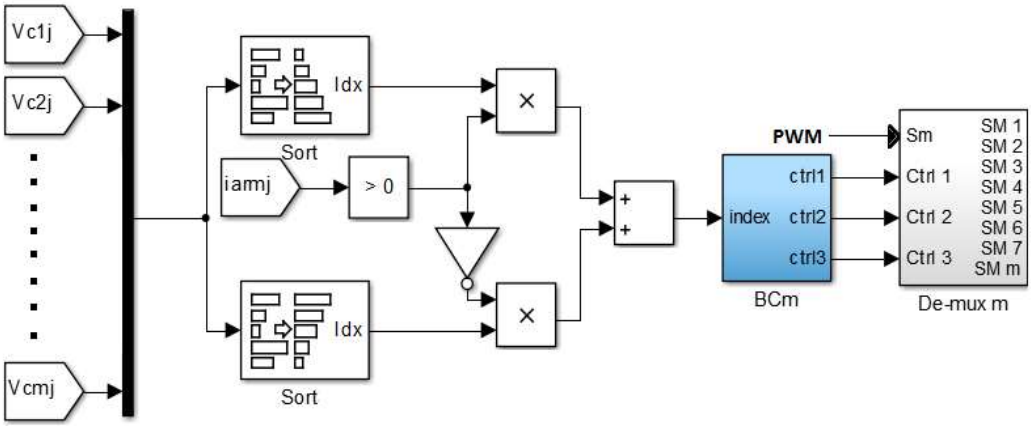
APPENDIX

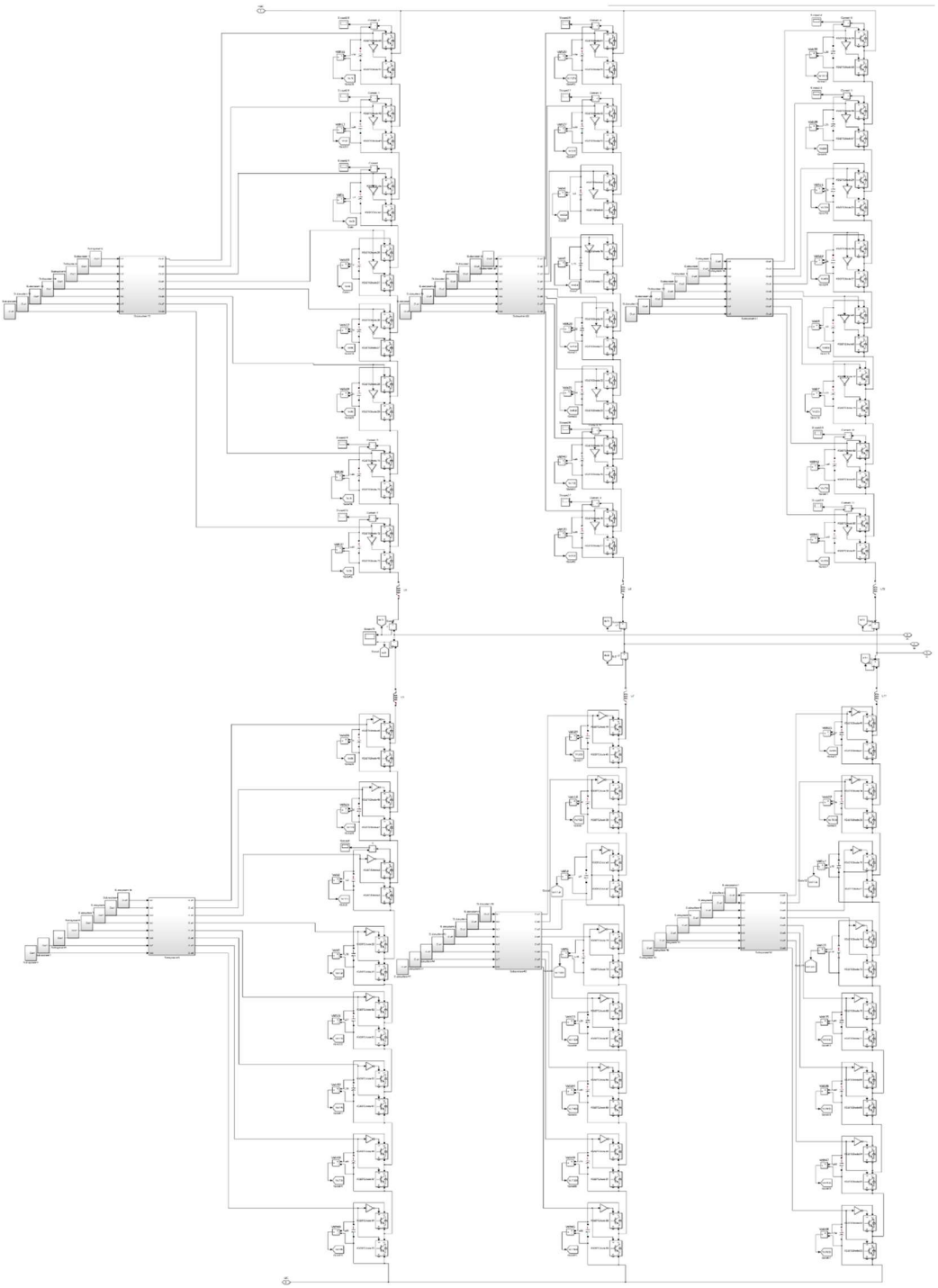
Appendix A.1 Voltage balancing technique & MMC SIMULINK MODEL

Voltage balancing technique



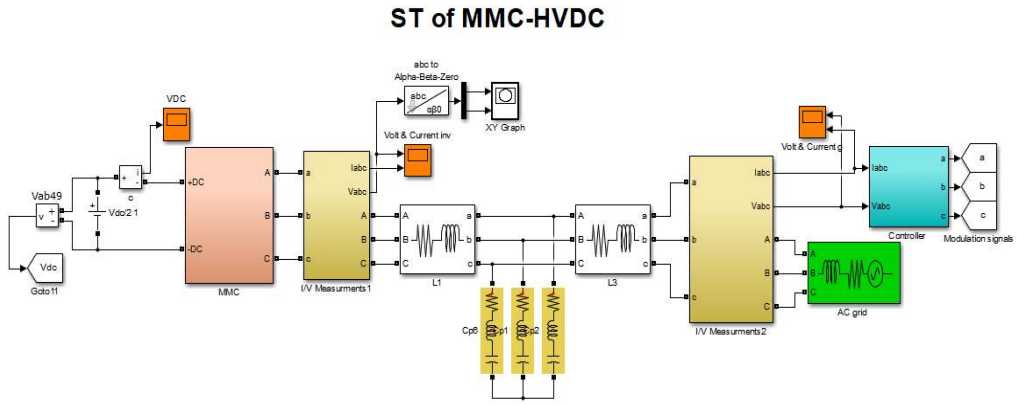
Where, m is the number of cells per arm and j is the phase (a,b, and c).

Nine-Level MMC transient model

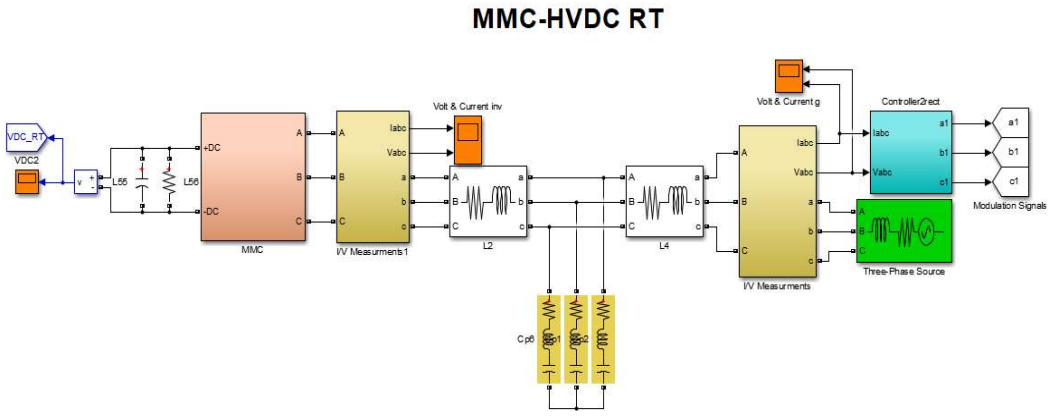


Appendix A.2 MMC-Based HVDC system model in simulink

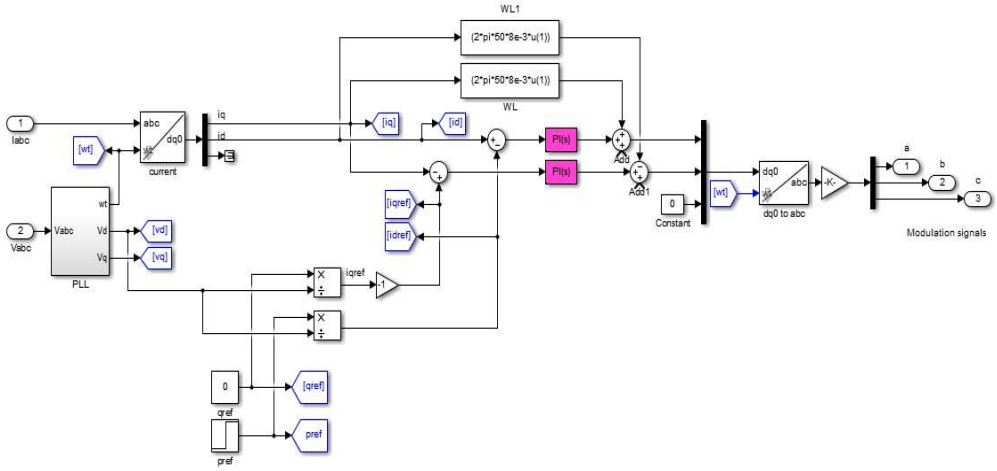
ST MMC-HVDC



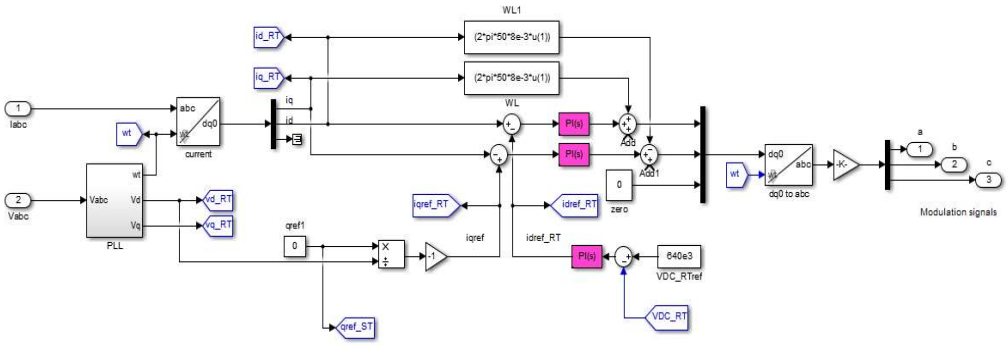
RT MMC-HVDC



Control of ST MMC-HVDC

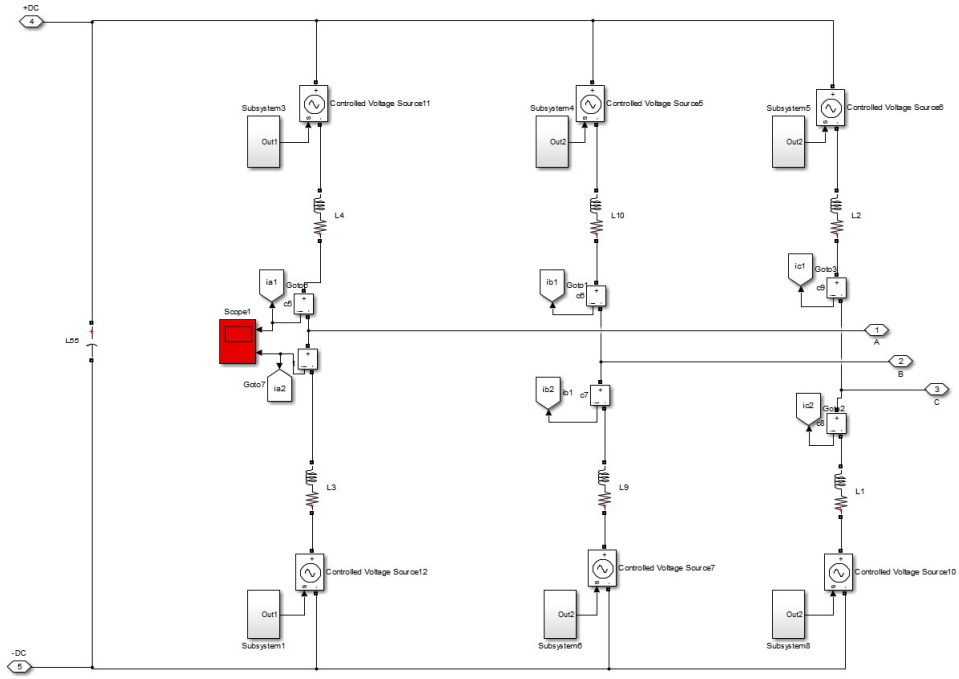


Control of RT MMC-HVDC

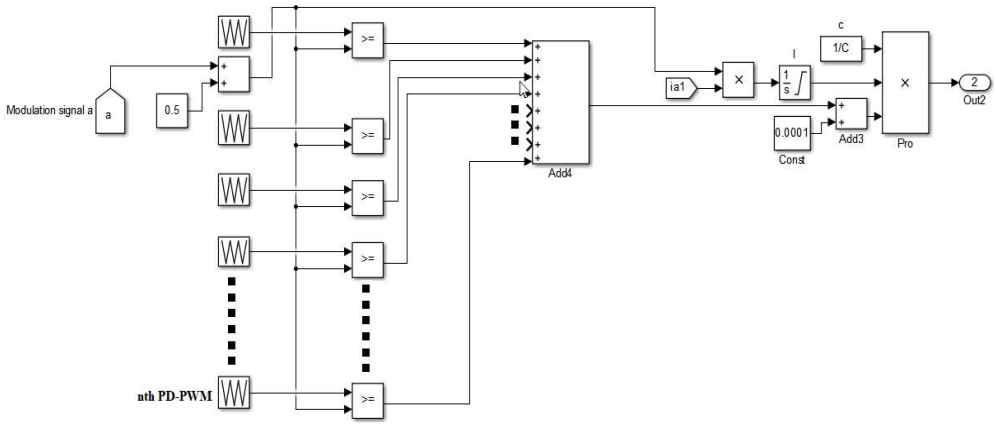


Appendix A.3 AVM-MMC Based HVDC model in simulink

MMC Averaged model using Simulink



AVM-MMC controlled voltage source control including capacitor effect in Simulink



Two-Terminal AVM-MMC Based HVDC system Simulink model