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Structure-based capacitance modeling and power loss analysis for the latest high-performance slant field-plate trench MOSFET

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Field-plate trench MOSFETs (FP-MOSFETs), with the features of ultralow on-resistance and very low gate-drain charge, are currently the mainstream of high-performance applications and their advancement is continuing as low-voltage silicon power devices. However, owing to their structure, their output capacitance (C_{oss}), which leads to main power loss, remains to be a problem, especially in megahertz switching. In this study, we propose a structure-based capacitance model of FP-MOSFETs for calculating power loss easily under various conditions. Appropriate equations were modeled for C_{oss} curves as three divided components. Output charge (Q_{oss}) and stored energy (E_{oss}) that were calculated using the model corresponded well to technology computer-aided design (TCAD) simulation, and we validated the accuracy of the model quantitatively. In the power loss analysis of FP-MOSFETs, turn-off loss was sufficiently suppressed, however, mainly Q_{oss} loss increased depending on switching frequency. This analysis reveals that Q_{oss} may become a significant issue in next-generation high-efficiency FP-MOSFETs.

1. Introduction

Power semiconductor devices are contributing to the reduction of energy consumption in many applications from very small mobile devices to very large power electronics systems. Among these, low-voltage power MOSFETs (LV-MOSFETs), which are generally classified into those with rated voltage in the range from 12 to 250 V, are applied in various circuits such as DC-DC converters of distributed power supply systems and three-phase inverters of motor drives. For LV-MOSFETs, historically, planar gate double-diffused MOSFETs (D-MOSFETs) and trench gate MOSFETs (U-MOSFETs) were developed in the 1970s and the 1980s, respectively,[1)] and they are currently used as matured low-cost devices. As great advancements of LV-MOSFET in terms of performance, field-plate trench MOSFETs (FP-MOSFETs)[2-10)] and superjunction trench MOSFETs (SJ-MOSFETs)[11-17)] were devised in the 1990s and commercialized in the 2000s. In both types of MOSFETs, specific on-resistance ($R_{ON}A$) could be drastically reduced with a high breakdown voltage (V_B) maintained. In particular, the FP-MOSFETs achieved not only ultralow $R_{ON}A$ but also very low reverse transfer capacitance (C_{rss}) and gate-drain charge (Q_{gd}) owing to the shielded-gate structure. Therefore, the FP-MOSFETs are currently the mainstream of high-performance applications and their advancements are continuing.

In general power conversion applications, power loss occurs during both conduction and switching operation. The power loss consists of the following components: gate drive loss (P_{GD}), conduction loss (P_{CON}), turn-on loss ($P_{SW(on)}$), turn-off loss ($P_{SW(off)}$), diode reverse recovery charge (Q_{rr}) loss (P_{Qrr}), and output charge (Q_{oss}) loss (P_{Qoss}).[18-20)] Among these, it is expected that P_{GD} can be reduced by circuit control and gate driver technologies such as very low impedance and very high current gate drive.[21-23)] Low-recovery-charge Shottky barrier diodes (SBD) can improve P_{Qrr}. Regarding FP-MOSFETs, it is obvious that there is a potential to reduce P_{CON}, $P_{SW(on)}$, and $P_{SW(off)}$ drastically, and several power loss analysis has been reported so far.[24-30)] However, owing to their structure, the output capacitance (C_{oss}) which leads to P_{Qoss} is a significant issue, especially in the case of megahertz switching.[31)]

In this paper, we describe a structure-based capacitance model of the FP-MOSFET, which was proposed in a related report,[32)] to estimate power loss under various conditions. In the modeling, we consider in detail the components of capacitance for both the conventional D-MOSFETs and the latest slant FP-MOSFETs, and provide additional more comprehensive explanations of the derivation of equations. The accuracy of the model is validated by comparing its results with those of technology computer-aided design (TCAD)

simulation. For more comprehensive validation data, we present not only C_{oss} curves and Q_{oss} curves but also C_{rss} curves and switching waveforms. By utilizing the proposed model, we expect that it is greatly useful for predicting the device performance of next-generation FP-MOSFETs.

2. Device structures, parameters, and basic characteristics

Figures 1(a) and 1(b) show schematic cross sections and representative structural parameters of a conventional D-MOSFET and a slant FP-MOSFET. Figure 1(c) shows comprehensive structural parameters of the FP-MOSFET to describe the capacitance model. The FP-MOSFET has a field plate inside a trench and the field plate is connected to a source electrode. In the off-state, an electric field in the drift region between trenches is reduced by the field-plate effect through a thick oxide. Therefore, despite the higher doping concentration in the drift layer than in the D-MOSFET, high V_B and low $R_{ON}A$ can be obtained at the same time. Moreover, as one of the latest FP-MOSFET, a slant field-plate structure has been devised and its superior $R_{ON}A$–V_B characteristics have been reported.[33-36] In the slant field-plate structure having a gradient thick oxide, the electric field is distributed more uniformly in the vertical direction, and the structure can achieve high MOSFET performance.

In this study, we chose a 100-V-class MOSFET as a motive device, which is applied to, e.g., high-efficiency switching-mode power supply and a high-current motor drive inverter circuit. The capacitance model can be described by structural parameters such as detailed cell structure dimensions and impurity doping concentrations, as shown in Table I. It does not require any measurement of electrical characteristics. Physical constants used in the modeling are shown in Table II. As shown in Table I, the unit cell width (W_{Cell}) of the FP-MOSFET is set to 2.6 μm, which is smaller than that of D-MOSFET (6.0 μm). Despite its smaller W_{Cell}, it has a drift layer concentration (N_D) that is ten times higher than that of a conventional one.

Before the capacitance modeling, we confirmed the basic characteristics of both MOSFETs using the TCAD simulator named Sentaurus Device.[37] As a result, the FP-MOSFET showed a sufficient V_B of 110.1 V and an ultralow $R_{ON}A$ of 32.8 mΩ·mm^2, which was approximately one-sixth of that of the D-MOSFET, as shown in Table III. Moreover, in the FP-MOSET, a very small $R_{ON}\cdot C_{rss}$, which approximately one-twentieth of that of the D-MOSFET, was confirmed. These indicate good features of the FP-MOSFET. However, $R_{ON}\cdot Q_{oss}$ is still high. Therefore, the capacitance modeling especially for C_{oss}, which requires the analysis P_{Qoss}, is important.

3. Description of capacitance modeling

Several analytical capacitance models for different vertical power device structures have been reported, e.g., those for silicon D-MOSFETs,[38] silicon U-MOSFETs,[39-41] and SiC D-MOSFETs.[42] In those reports, however, since the C_{oss} components of D-MOSFETs and U-MOSFETs are relatively simple, those modeling methods are not applied to complex-structured FP-MOSFETs.

3.1 D-MOSFET

Figure 2(a) shows the components of C_{oss} in the D-MOSFET. C_{oss} is simply expressed as

$$C_{oss\_DMOS} = C_{ds} + C_{gd}. \tag{1}$$

The drain–source capacitance C_{ds} is a pn-junction capacitance and it is varied by the drain–source voltage V_{ds}.

$$C_{ds} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{(W_B+2X_{JB\_l})}{W_{Cell}} \tag{2}$$

Here, q is the elementary charge, $\varepsilon_{Si}\varepsilon_0$ is the permittivity of Si, W_B is the p-base width, and X_{JB_l} is the lateral expansion length of the p-base junction. The built-in potential V_{bi} is given by

$$V_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{{n_i}^2}, \tag{3}$$

where k is Boltzmann's constant, T is the absolute temperature, n_i is the intrinsic carrier density of Si, and N_A is a p-base layer concentration.

The gate–drain capacitance C_{gd} is a series connection of a gate oxide capacitance (C_{gox}) and a depletion layer capacitance (C_{dep}). Since C_{rss} is equal to C_{gd}, C_{rss} is written as

$$C_{rss} = C_{gd} = \frac{C_{gox}C_{dep}}{C_{gox}+C_{dep}}. \tag{4}$$

Furthermore, C_{gox} and C_{dep} are expressed as

$$C_{gox} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{gox}} \cdot \frac{(W_G-2X_{JB\_l})}{W_{Cell}}, \tag{5}$$

$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_0}{W_{d\_mos}} \cdot \frac{(W_G-2X_{JB\_l})}{W_{Cell}}, \tag{6}$$

where $\varepsilon_{OX}\varepsilon_0$ is the permittivity of SiO_2, T_{gox} is the gate oxide thickness, and W_G is the gate width. W_{d_mos} is the depletion layer width beneath the gate electrode and is given by[43]

$$W_{d\_mos} = \frac{\varepsilon_{Si}T_{gox}}{\varepsilon_{OX}}\left(\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}{T_{gox}}^2}+1}-1\right). \tag{7}$$

By substituting Eqs. (5)–(7) into Eq. (4), the C_{rss} model can be obtained.

$$C_{rss\_DMOS} = C_{gd} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}\varepsilon_{OX}{}^2\varepsilon_0}{qN_D\varepsilon_{Si}}+T_{gox}{}^2}} \cdot \frac{W_G-2X_{JB\_l}}{W_{Cell}} \tag{8}$$

Finally, by substituting Eqs. (2), (3), and (8) into Eq. (1), the C_{oss} model can be obtained.

$$C_{oss\_DMOS} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2\left(V_{ds}+\frac{kT}{q}\ln\frac{N_AN_D}{n_i{}^2}\right)}} \cdot \frac{W_B+2X_{JB\_l}}{W_{Cell}} + \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}\varepsilon_{OX}{}^2\varepsilon_0}{qN_D\varepsilon_{Si}}+T_{gox}{}^2}} \cdot \frac{W_G-2X_{JB\_l}}{W_{Cell}} \tag{9}$$

3.2 FP-MOSFET

As an approach to capacitance modeling in the complex FP-MOSFET structure, we consider the four components of C_{oss}, as shown in Fig. 2(b). C_{oss} is simply expressed as

$$C_{oss\_FPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd}. \tag{10}$$

Here, C_{ds1} is the depletion layer capacitance of the pn-junction, C_{ds2} is a series connection of a field-plate oxide capacitance and a depletion layer capacitance along the trench side wall, and C_{ds3} is the trench bottom capacitance including the field-plate oxide and depletion layers. In the FP-MOSFET, however, C_{gd} is negligible in the case of C_{oss} calculation, because the area of the parallel-plate capacitor is usually very small for optimized cell design.

Figures 3(a)–3(c) show the TCAD-simulated FP-MOSFET half-cell structures, which show the V_{ds} dependence of equal-potential contours. The potential contours of 5 V intervals and the depletion layer boundaries are shown as black and white lines, respectively. In each figure, the dominant capacitance components are C_{ds1}, C_{ds2}, and C_{ds3}, respectively.

3.2.1 pn-Junction capacitance. In the region of C_{ds1} [Fig. 3(a)], the depletion layer of the pn-junction extends down to the vertical direction with increasing V_{ds}. However, the capacitance width in the lateral direction decreases because of the expansion of another depletion layer along the trench side wall caused by the field-plate effect. It is considered that this pn-junction capacitance C_j is divided into C_{j0} and C_{j1} according to the V_{ds} condition.

$$C_{ds1} = C_j = \begin{cases} C_{j0}, & V_{ds} < 1(V) \\ C_{j1}, & V_{ds} \geq 1(V) \end{cases}. \tag{11}$$

C_{j0} is the capacitance at an early voltage including the V_{bi}. C_{j0} is modeled similarly to Eq. (2) for the C_{ds} of the D-MOSFET.

$$C_{j0} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{W_{Mesa}}{W_{Cell}}, \tag{12}$$

where W_{Mesa} is the mesa width.

Before C_{j1} modeling, we additionally explain some parameters shown in Fig. 1(c). θ_2 is

the angle of the field plate and it given by

$$\theta_2 = \tan^{-1}\left(\frac{T_{FPOX\_b} - T_{FPOX\_t}}{D_T - X_{JB} - X - T_{FPOX\_c}}\right), \tag{13}$$

where T_{FPOX_t} and T_{FPOX_b} are the lateral field-plate oxide thicknesses at top and bottom positions, respectively, T_{FPOX_c} is the vertical field-plate oxide thickness of the center of the trench bottom, D_T is the trench depth, and X is the length between the p-base layer depth and the horizontal position of the top of the field plate.

θ_1 is the direction of the electric line of force and it is given by

$$\theta_1 = \tan^{-1}\left(\frac{\varepsilon_{Si}}{\varepsilon_{OX}}\tan\theta_2\right). \tag{14}$$

T(y) and *W(y)* are used to calculate the charge densities in the field-plate oxide and the silicon mesa region, respectively, and are given by

$$T(y) = T_{OX}(y)\cos\theta_2, \tag{15}$$

$$W(y) = \frac{W_{Si}(y)}{\cos\theta_1}, \tag{16}$$

where y is the depth from the top of the field plate, $T_{OX}(y)$ is the field-plate oxide thickness at the position y and $W_{Si}(y)$ is the depletion layer width of the mesa region along the slant field plate at the position y. $T_{OX}(y)$ is expressed as

$$T_{OX}(y) = \frac{T_{FPOX\_b} - T_{FPOX\_t}}{D_T - X_{JB} - X - T_{FPOX\_c}}y + T_{FPOX\_t}. \tag{17}$$

Although $W(y)$ varies with V_{ds}, it has to be considered that V_{ds} is shared by the voltage of the field-plate oxide (V_{OX}) and the voltage of the silicon mesa (V_{Si}). The relationship between V_{OX}, V_{Si}, $T(y)$, and $W(y)$ are expressed as

$$V_{ds} = V_{Si} + V_{OX}, \tag{18}$$

$$V_{Si} = \frac{1}{2}E_{Si}W(y), \tag{19}$$

$$V_{OX} = E_{OX}T(y), \tag{20}$$

$$\varepsilon_{Si}E_{Si}\cos\theta_1 = \varepsilon_{OX}E_{OX}\cos\theta_2, \tag{21}$$

$$E_{Si} = \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}W(y), \tag{22}$$

where E_{Si} and E_{OX} are the electric field strengths of the silicon mesa region and field-plate oxide region, respectively. $W(y)$ is derived by solving Eqs. (18)–(22). Since y varies with V_{ds}, $W(y)$ is exactly expressed as $W(V_{ds}, y)$ and can be described as

$$W(V_{ds}, y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}\cdot V_{ds}}. \tag{23}$$

C_{j1} includes the effect of capacitance width decrease by $W(V_{ds},y)$ and is described as

$$C_{j1} = \frac{\varepsilon_{Si}\varepsilon_0}{y_0 + X}\cdot\frac{W_{Mesa} - 2W(V_{ds},y)}{W_{Cell}}, \tag{24}$$

where y_0 is the depletion layer depth of the center of the mesa.

3.2.2 Oxide and depletion layer capacitance along field plate. In the region of C_{ds2} [Fig. 3(b)], the initial C_{ds2} is nearly equal to the field-plate oxide capacitance C_{OX}. With increasing V_{ds}, the mesa region is depleted linearly owing to the relation $y_0 \propto V_{ds}$ in the vertical direction, and the lateral depletion width under the position of y_0 expands gradually by $W(V_{ds},y)$. Thus, C_{ds2} is divided into two components according to the V_{ds} condition.

$$C_{ds2} = \begin{cases} C_{OX} & , V_{ds} < 1(V) \\ C_{FP}(V_{ds}), & V_{ds} \geq 1(V) \end{cases} \tag{25}$$

C_{OX} is provided by integrating field-plate oxide thickness in the depth direction.

$$C_{OX} = \frac{2(D_T - X_{JB} - X - T_{FPOX\_c})\varepsilon_{OX}\varepsilon_0}{W_{Cell}(T_{FPOX\_b} - T_{FPOX\_t})} \cdot ln\frac{T_{FPOX\_b}}{T_{FPOX\_t}} \tag{26}$$

At an arbitrary position y, the charge, which is across the field plate and the depletion layer in the mesa region, is defined as dQ. Differential equation of dQ expresses a voltage change of the drain–source electric charge and described as

$$\frac{dQ}{dV} = qN_D \frac{d}{dV} W(V_{ds}, y). \tag{27}$$

The voltage dependence capacitance $C_{FP}(V_{ds})$ is provided by integrating Eq. (27) from y_0 to y_b, which is the end of the depletion layer and is described as

$$C_{FP}(V_{ds}) = \frac{2 \cdot \int_{y_0}^{y_b} qN_D \frac{d}{dV}(W(V_{ds},y))dy}{W_{Cell}}. \tag{28}$$

Finally, by substituting Eqs. (15), (17), and (23) into Eq. (28), $C_{FP}(V_{ds})$ can be obtained.

$$C_{FP}(V_{ds}) = \frac{2}{W_{Cell}} \int_{y_0}^{y_b} \frac{\varepsilon_{Si}\varepsilon_0}{\sqrt{\frac{\varepsilon_{Si}{}^2 \cos^2\theta_1 \left[T_{FPOX\_t} + \frac{y(T_{FPOX\_t} - T_{FPOX\_b})}{X_{JB}+X+T_{FPOX\_b}-D_T}\right]^2}{\varepsilon_{OX}{}^2} + \frac{2\varepsilon_{Si}\varepsilon_0 V_{ds}}{qN_D}}} dy \tag{29}$$

3.2.3 Trench bottom capacitance. In the region of C_{ds3} [Fig. 3(c)], when V_{ds} increase, at last y_0 reaches almost the same depth as that of bottom of field plate. C_{ds2} decreases continuously in the model [Eqs. (25) and (29)]. Therefore, the trench bottom capacitance C_{ds3} has to be included as a component of total C_{oss}.

In the trench bottom region, the depletion layer $W_{btm}(V_{ds},l)$ begins to expand slightly when V_{ds} is greater than approximately 60 V. $W_{btm}(V_{ds},l)$ can be described similarly to Eq. (23).

$$W_{btm}(V_{ds}, l) = -\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}} \tag{30}$$

Here, l is the length from the center of the trench, $T(l)$ is the oxide thickness of the trench

bottom, and θ_4 and θ_3 are given by

$$\theta_4 = \tan^{-1}\left(\frac{l}{T_{FPOX\_c}}\right), \tag{31}$$

$$\theta_3 = \tan^{-1}\left(\frac{\varepsilon_{Si}}{\varepsilon_{OX}}\tan\theta_4\right). \tag{32}$$

Thus, C_{ds3} is provided by integrating $W_{btm}(V_{ds},l)$ in the direction of the trench width from 0 to T_{FPOX_b} and is described as

$$C_{ds3} = \frac{2\cdot\int_0^{T_{FPOX\_b}} qN_D\frac{d}{dV}(W_{btm}(V_{ds},l))dl}{W_{Cell}}. \tag{33}$$

3.2.4 Gate-drain capacitance. As mentioned above, in the FP-MOSFET, C_{gd} is negligible small, which is approximately two to three orders of magnitude lower than C_{oss}. However, to compare it with the D-MOSFET, we carry out simplified modeling for C_{gd}. As shown in Fig. 2(b), the C_{gd} of the FP-MOSFET is the series connection of C_{gox} and C_{dep}, which is the same as in the case of the D-MOSFET. In the FP-MOSFET, C_{gox} and C_{dep} are expressed as

$$C_{gox} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{gox}}\cdot\frac{2(D_G - X_{JB})}{W_{Cell}}, \tag{34}$$

$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_0}{W_{d\_mos}}\cdot\frac{2(D_G - X_{JB})}{W_{Cell}}. \tag{35}$$

By substituting Eqs. (7), (34), and (35) into Eq. (4), the initial capacitance C_{gd0} can be obtained as

$$C_{gd0} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}\varepsilon_{OX}{}^2\varepsilon_0}{qN_D\varepsilon_{Si}}+T_{gox}{}^2}}\cdot\frac{2(D_G - X_{JB})}{W_{Cell}}. \tag{36}$$

Unlike the D-MOSFET, in the FP-MOSFET, the capacitance width of C_{gd} is drastically reduced by the factor of $W(V_{ds},y)$, as shown in Eq. (23). Thus, finally, the C_{rss} model is described as

$$C_{rss\_FPMOS} = C_{gd0}\cdot\frac{W_{Mesa}-2W(V_{ds},y)}{W_{Mesa}} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}\varepsilon_{OX}{}^2\varepsilon_0}{qN_D\varepsilon_{Si}}+T_{gox}{}^2}}\cdot\frac{2(D_G - X_{JB})}{W_{Cell}}\cdot\frac{W_{Mesa}-2W(V_{ds},y)}{W_{Mesa}}. \tag{37}$$

The analytically derived C_{oss} and C_{rss} model equations for the D-MOSFET and FP-MOSFET are shown in Table IV.

4. Validation of proposed model

4.1 C_{oss}-V_{ds} and Q_{oss}-V_{ds} curves

To validate the accuracy of the proposed model, firstly, we compared the calculated C_{oss}–V_{ds} curves of the FP-MOSFET with those of TCAD simulation. Figure 4 shows the V_{ds} dependence of calculated C_{oss} and each component of the FP-MOSFET; C_j (= C_{j0} + C_{j1}), C_{OX}, $C_{FP}(V)$, and C_{ds3} are drawn as the capacitances of a unit device area (cm^2). In the low-voltage region of V_{ds} < 1 V, C_j and C_{OX} were the dominant components of total C_{oss}, and the sum of C_j and C_{OX} corresponded well to TCAD results. This initial capacitance region is very important for calculating Q_{oss} and E_{oss}. The total C_{oss} curves, which consist of all components, in the region of $V_{ds} \geq 1$ V, also showed good agreement with TCAD results.

Figures 5(a) and 5(b) show the calculated C_{oss} for the D-MOSFET and FP-MOSFET with TCAD simulation results, respectively. Here, each active area was designed to achieve the same R_{ON} = 10 mΩ; therefore, 22.1 mm^2 for the D-MOSFET and 3.67 mm^2 for the FP-MOSFET were defined. In both V_{ds} linear scale [Fig. 5(a)] and V_{ds} log scale [Fig. 5(b)], the C_{oss} curves of both MOSFETs corresponded well qualitatively to TCAD results. In the detailed comparison for the FP-MOSFET, errors of 14 and 10% were seen at approximately V_{ds} = 1 and 60 V, respectively, and another region showed less than 5%. These results indicate that the error occurred at the point where the V_{ds} condition changed, as shown in Eqs. (11), (25), and (33). In the D-MOSFET, a maximum error of 24% was seen at V_{ds} = 0.1 V; however, another region showed good results of less than 5%. The reason considered why the early voltage region has the error is that the spherical pn-junction of the p-base is not modeled very well.

By using the proposed model, the output charge Q_{oss} and the stored energy E_{oss} in the output capacitance are calculated as

$$Q_{oss} = \int C_{oss} dV, \tag{38}$$

$$E_{oss} = \int C_{oss} V_{ds} dV. \tag{39}$$

Figures 6(a) and 6(b) show the calculated Q_{oss}–V_{ds} and E_{oss}–V_{ds} curves compared with TCAD simulation results, for the D-MOSFET and FP-MOSFET, respectively. Each active area was designed for the same R_{ON} of 10 mΩ. These modeled curves corresponded well qualitatively to TCAD curves. In an application circuit for 100-V-rating device, an input voltage (V_{IN}) of 50 V is assumed generally. In the comparison between the modeled Q_{oss} and the TCAD results at V_{ds} = 50 V, only 6 and 7% errors were seen for the FP-MOSFET and D-MOSFET, respectively. In addition, in the case of the E_{oss}, there were 5 and 10% errors for the FP-MOSFET and D-MOSFET, respectively. Therefore, it is recognized that these results are

sufficient to use for power loss analysis.

As mentioned above, this study especially focuses on the P_{Qoss} of the FP-MOSFET. Figures 7(a) and 7(b) explain the switching operation concerning C_{oss}. When the MOSFET is turned-off, C_{oss} stores charges. Then, during the turn-on sequence, the on-current I_{ON} is consumed by discharging of Q_{oss}. This becomes the energy loss E_{oss}, which is the Q_{oss} loss of one switching cycle.

4.2 C_{rss}-V_{ds} curves and switching waveforms

As additional validation data, we describe the calculated C_{rss}–V_{ds} curves compared with TCAD simulation results for the D-MOSFET and FP-MOSFET, respectively, as shown in Figs. 8(a) and 8(b). Each active area was designed for the same R_{ON} of 10 mΩ. In both V_{ds} linear scale [Fig. 8(a)] and V_{ds} log scale [Fig. 8(b)], the C_{rss} curves of the D-MOSFET corresponded well qualitatively to TCAD results. However, there were relatively large errors with the maximum of 32% at approximately V_{ds} = 0.1 and 10 V. The reason was the same as in the case of C_{oss} modeling, as mentioned in Sect. 4.1. On the other hand, in the case of the C_{rss} curves of the FP-MOSFET, errors of less than 10% were seen at $V_{ds} \leq 1$ V, and errors of less than 35% were seen at 1 V < $V_{ds} \leq$ 10 V. However, larger errors occurred in the high-V_{ds} region because of the small value of C_{gd}, which is approximately two to three orders of magnitude lower than C_{oss}, as mentioned in Sect. 3.2.4.

Figures 9(a) and 9(b) are the simply calculated turn-off switching waveforms using the C_{rss} model for the D-MOSFET and FP-MOSFET, respectively, under the conditions of V_{IN} = 50 V, I_{ON} = 10 A, gate resistance R_g = 1.5 Ω, and gate current I_g = 0.83 A. Here, the turn-off time t_{off} is given by

$$t_{off} = \int_0^{V_{IN}} \frac{C_{gd}}{I_g} dV. \tag{40}$$

As a result, t_{off} = 18.5 ns for the D-MOSFET and t_{off} = 1.1 ns for the FP-MOSFET were calculated using the proposed model. In the calculation, gate–source charge (Q_{gs}), circuit resistance (R_c), and stray inductance (L_s) are not considered.

4.3 Power loss analysis

As a comprehensive evaluation of the proposed model, we estimated the power loss assuming a low-side MOSFET of a buck converter circuit for the D-MOSFET and FP-MOSFET. Each active area was designed for the same R_{ON} of 10 mΩ. The operation conditions were V_{IN} = 50 V, output current I_O = 10 A, duty ratio D = 80%, and switching

frequency f_{SW} = 100 kHz to 2 MHz. Here, the calculated conduction loss P_{CON}, turn-off loss $P_{SW(off)}$, and output charge loss P_{Qoss} are given by

$$P_{CON} = {I_O}^2 R_{ON} D, \tag{41}$$

$$P_{SW(off)} = I_O V_{IN} t_{off} f_{SW}, \tag{42}$$

$$P_{Qoss} = E_{oss} f_{SW} = f_{SW} \int_0^{V_{IN}} C_{oss} V_{ds} dV. \tag{43}$$

As shown in Figs. 10(a) and 10(b), all P_{CON} values were constant at 0.8 W in both MOSFETs because of the same R_{ON}. $P_{SW(off)}$ was greatly influenced by C_{rss}. Thus, in the D-MOSFET, $P_{SW(off)}$ was the most dominant component and increased to 7.56 W at 2 MHz, because of the large $R_{ON} \cdot C_{rss}$, as shown in Table III. On the other hand, in the FP-MOSFET, the total power loss was drastically suppressed by the low $R_{ON} \cdot C_{rss}$, and was mainly increased by P_{Qoss}, which depended on f_{SW}. This analysis reveals that P_{Qoss} may become a significant issue in the case of high-frequency operation, in not only the latest FP-MOSFETs but also next-generation FP-MOSFETs.

4.4 Application to other MOSFET structures

As mentioned above, we validated the proposed model for the D-MOSFET and FP-MOSFET. In the case of the U-MOSFET structure, the modeling method is similar that for the D-MOSFET, which uses C_{ds}, C_{gox}, and C_{dep}. However, additional C_{gox} and C_{dep} components of the trench side wall have to be considered, if the trench gate penetrates the pn-junction deeply. Besides, in the case of a conventional FP-MOSFET structure, which has a nearly uniform field-plate oxide thickness, the model may be applied. In particular, the results of calculation of Eqs. (17) and (26) change depending on both T_{FPOX_t} and T_{FPOX_b}. In our future work, we would like to investigate a wider application range of the proposed model.

5. Conclusions

We proposed the structure-based capacitance model for the latest 100 V FP-MOSFET. The calculated C_{oss}–V_{ds}, Q_{oss}–V_{ds}, and E_{oss}–V_{ds} curves corresponded very well to TCAD results. Although errors of 10-14% were seen at any points of the C_{oss} curves, other regions showed less than 5% errors. Moreover, the modeling curves of Q_{oss} and E_{oss} showed good accuracy, with errors of 6 and 5%, respectively. We analyzed the power loss depending on switching frequency using the model and found that the Q_{oss} loss may become a significant issue, even in the latest slant FP-MOSFET. Regarding next-generation and ultimately high-efficiency FP-MOSFETs, it is expected that the proposed model is useful for the prediction of device performance.

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Figure Captions

Fig. 1. Schematic cross sections and representative structural parameters of (a) conventional D-MOSFET and (b) slant FP-MOSFET. (c) Comprehensive structural parameters of FP-MOSFET (half-cell structure) to describe capacitance model.

Fig. 2. Components of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) for D-MOSFET and FP-MOSFET.

Fig. 3. TCAD simulated FP-MOSFET half-cell structures, which represent V_{ds} dependence of equal-potential contours. Potential contours and depletion layer boundaries are shown as black lines and white lines, respectively. Three capacitance components are shown as dominant regions; (a) main pn-junction, (b) field-plate oxide and depletion layer along trench side wall, (c) field-plate oxide and depletion layer of trench bottom.

Fig. 4. C_{oss} components of FP-MOSFET calculated using proposed model compared with TCAD simulation results.

Fig. 5. C_{oss}–V_{ds} curves calculated using proposed model compared with TCAD results for D-MOSFET and FP-MOSFET. (a) V_{ds} linear scale and (b) V_{ds} log scale in X-axis. Each active area is designed for the same R_{ON} of 10 mΩ.

Fig. 6. (a) Q_{oss}–V_{ds} and (b) E_{oss}–V_{ds} curves calculated using proposed model compared with TCAD results for D-MOSFET and FP-MOSFET. Each active area is designed for the same R_{ON} of 10 mΩ.

Fig. 7. Explanation of switching operation concerning C_{oss} and Q_{oss}.

Fig. 8. C_{rss}–V_{ds} curves calculated using proposed model compared with TCAD results for D-MOSFET and FP-MOSFET. (a) V_{ds} linear scale and (b) V_{ds} log scale in X-axis. Each active area is designed for the same R_{ON} of 10 mΩ.

Fig. 9. Switching waveforms calculated using proposed model for (a) D-MOSFET and (b) FP-MOSFET.

Fig. 10. Estimated power losses for D-MOSFET and FP-MOSFET, assuming 50 V input, 10 A output, 80% duty ratio, and 100 kHz-to-2 MHz switching operation. Each active area is designed for the same R_{ON} of 10 mΩ.

Table I. Structural parameters for 100-V-class D-MOSFET and FP-MOSFET.

Symbol	Parameters		D-MOSFET	FP-MOSFET	Unit
N_D	Drift layer concentration		2.8×10^{15}	3.0×10^{16}	atoms/cm^3
N_A	p-Base layer concentration		5.0×10^{16}	1.0×10^{17}	atoms/cm^3
W_{Cell}	Cell width		6.0	2.6	μm
W_G	Gate width		3.4	N/A	μm
W_B	p-Base width		2.6	N/A	μm
W_T	Trench width		N/A	1.5	μm
W_{Mesa}	Mesa width		N/A	1.1	μm
D_T	Trench depth		N/A	6.0	μm
D_G	Gate depth		N/A	1.0	μm
T_{GOX}	Gate oxide thickness		0.05	0.05	μm
T_{FPOX_t}	Field-plate oxide thickness	(top)	N/A	0.1	μm
T_{FPOX_b}		(bottom)	N/A	0.75	μm
T_{FPOX_c}		(center)	N/A	0.75	μm
X_{JB}	p-Base junction depth		0.75	0.9	μm
X_{JB_l}	p-Base junction lateral length		0.60	N/A	μm

Table II. Physical constants.

Symbol	Description	Property	Unit
q	Elementary charge	1.60×10^{19}	C
k	Boltzmann's constant	1.38×10^{-23}	J/K
T	Absolute temperature	300	K
n_i	Intrinsic carrier density	1.50×10^{10}	atoms/cm^3
ε_0	Permittivity in vacuum	8.854×10^{-14}	F/cm
ε_{Si}	Dielectric constant of Si	11.7	
ε_{OX}	Dielectric constant of SiO_2	3.9	

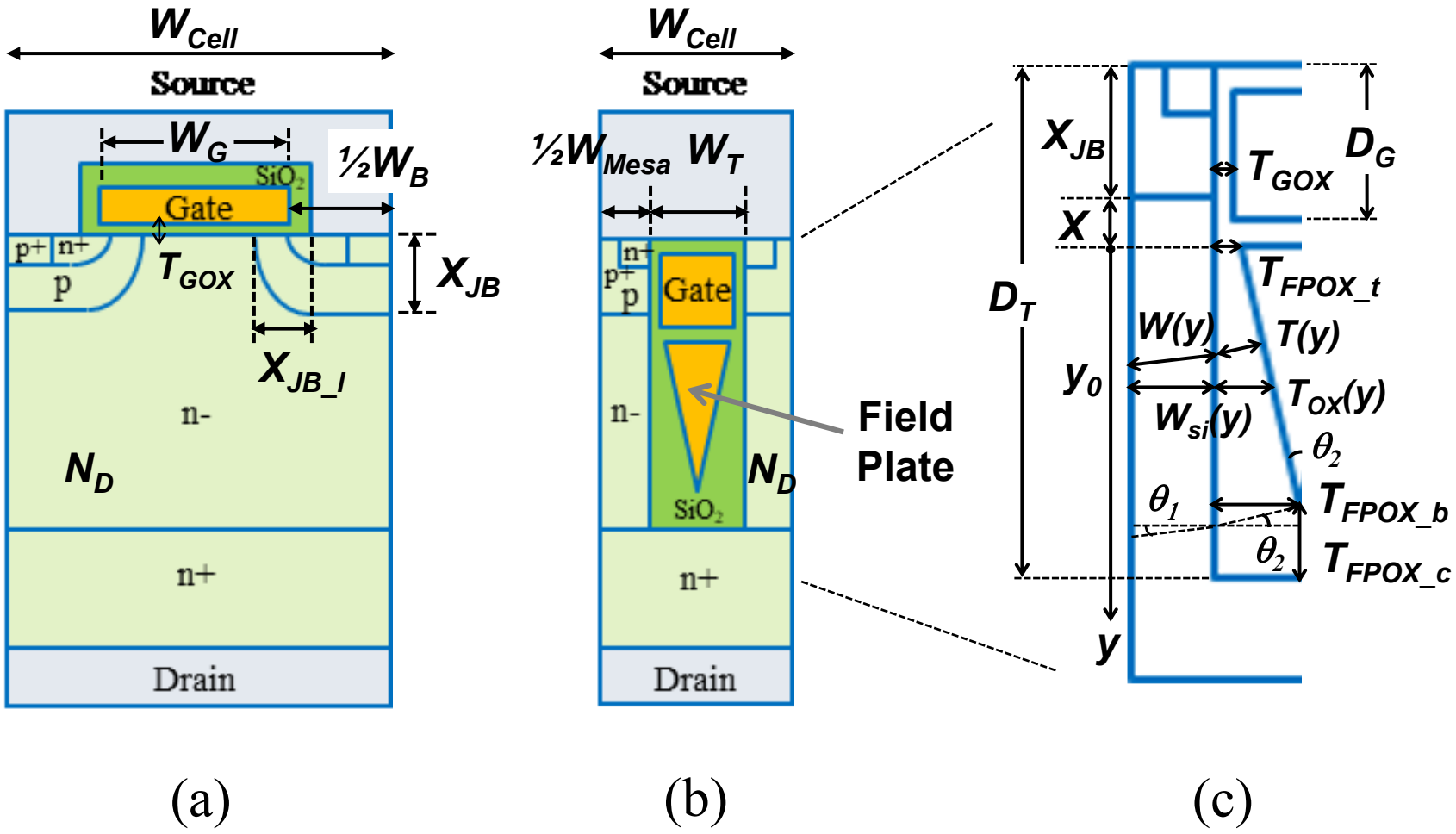
Table III. TCAD simulated basic characteristics for 100-V-class D-MOSFET and FP-MOSFET.

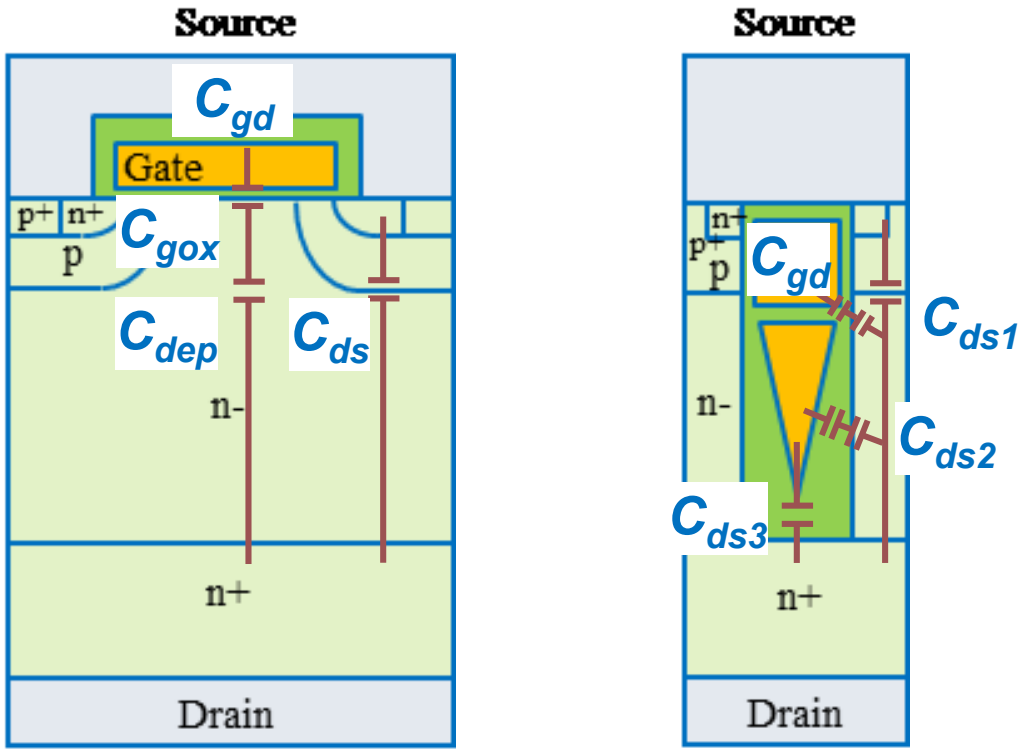
Symbol	Characteristics	Condition	D-MOSFET	FP-MOSFET	Unit
V_B	Breakdown voltage		111.3	110.1	V
V_{TH}	Threshold voltage	V_{ds}=10V	2.09	2.03	V
$R_{ON}A$	On-resistance	V_{gs}=10 V	199.1	32.8	mΩ·mm^2
R_{ON}·C_{rss}	FOM[a)]_1	V_{ds}=50 V	1364	5.7	mΩ·pF
R_{ON}·C_{oss}	FOM_2	V_{ds}=50 V	4205	2040	mΩ·pF
R_{ON}·Q_{oss}	FOM_3	V_{ds}=50 V	390	309	mΩ·nC

[a)] FOM, figure of merit.

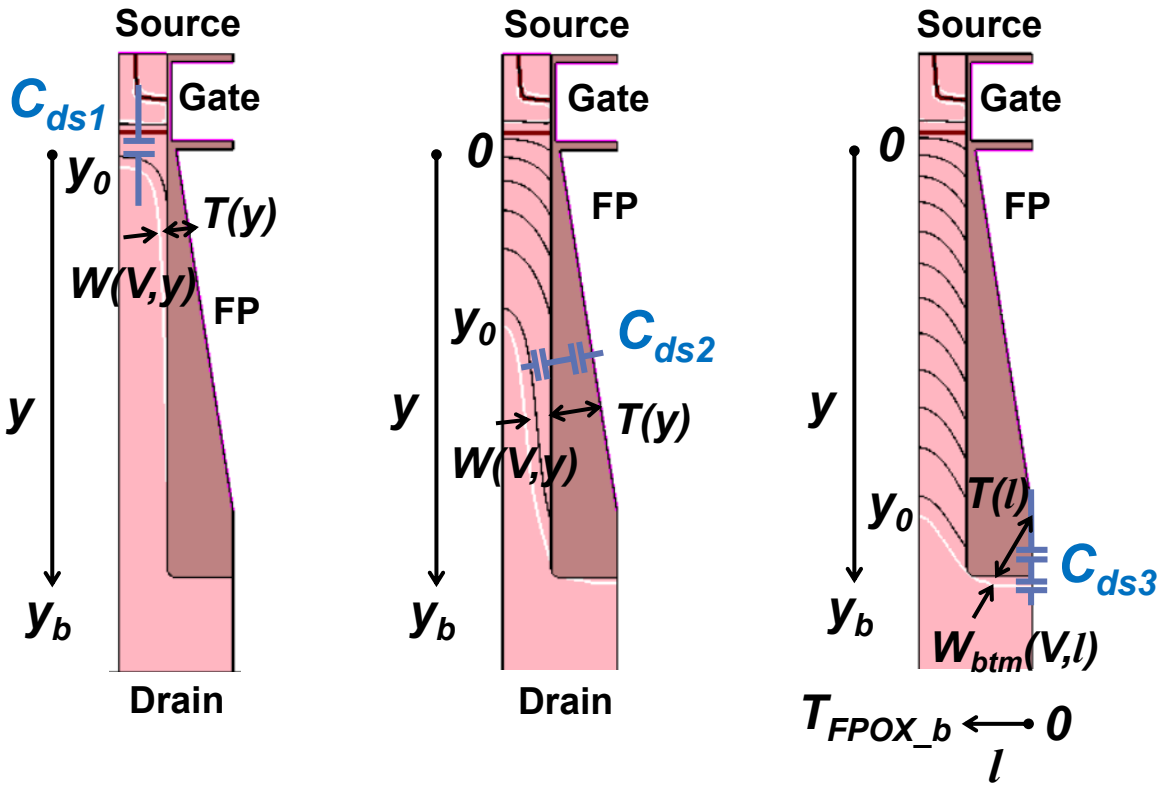
Table IV. List of C_{oss} and C_{rss} model equations for D-MOSFET and FP-MOSFET.

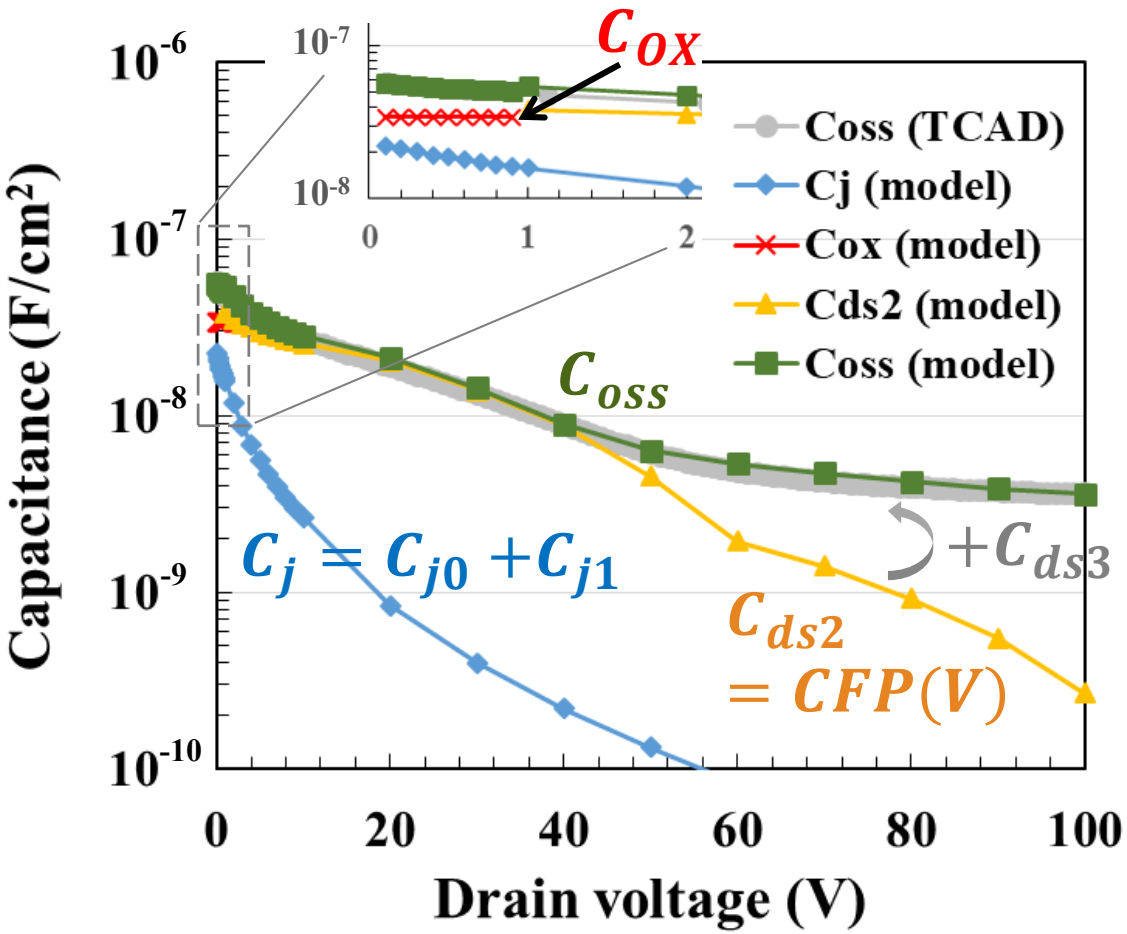
D-MOSFET	$C_{rss\_DMOS} = \dfrac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\dfrac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{gox}}^2}} \cdot \dfrac{W_G - 2X_{JB\_l}}{W_{Cell}}$
	$C_{oss\_DMOS} = \sqrt{\dfrac{qN_D\varepsilon_{Si}\varepsilon_0}{2\left(V_{ds} + \dfrac{kT}{q}\ln\dfrac{N_AN_D}{{n_i}^2}\right)}} \cdot \dfrac{W_B + 2X_{JB\_l}}{W_{Cell}} + C_{rss\_DMOS}$
FP-MOSFET	$C_{rss\_FPMOS} = \dfrac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\dfrac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{gox}}^2}} \cdot \dfrac{2\left(D_G - X_{JB}\right)}{W_{Cell}} \cdot \dfrac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Mesa}}$
	$W(V_{ds}, y) = -\dfrac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y) + \sqrt{\left(\dfrac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y)\right)^2 + \dfrac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$
	$C_{oss\_FPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd}$
	$C_{ds1} = \begin{cases} C_{j0} = \sqrt{\dfrac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \dfrac{W_{Mesa}}{W_{Cell}} & , \quad V_{ds} < 1(V) \\ C_{j1} = \dfrac{\varepsilon_{Si}\varepsilon_0}{y_0 + X} \cdot \dfrac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Cell}}, & V_{ds} \geq 1(V) \end{cases}$
	$C_{ds2} = \begin{cases} C_{OX} = \dfrac{2\left(D_T - X_{JB} - X - T_{FPOX\_c}\right)\varepsilon_{OX}\varepsilon_0}{W_{Cell}\left(T_{FPOX\_b} - T_{FPOX\_t}\right)} \cdot ln\dfrac{T_{FPOX\_b}}{T_{FPOX\_t}}, & V_{ds} < 1(V) \\ C_{FP}(V_{ds}) = \dfrac{2 \cdot \int_{y_0}^{y_b} qN_D \dfrac{d}{dV}\left(W(V_{ds}, y)\right)dy}{W_{Cell}} & , \quad V_{ds} \geq 1(V) \end{cases}$
	$W(V_{ds}, y) = -\dfrac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y) + \sqrt{\left(\dfrac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y)\right)^2 + \dfrac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$
	$C_{ds3} = \dfrac{2 \cdot \int_0^{T_{FPOX\_b}} qN_D \dfrac{d}{dV}(W_{btm}(V_{ds}, l))dl}{W_{Cell}}$
	$W_{btm}(V_{ds}, l) = -\dfrac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l) + \sqrt{\left(\dfrac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l)\right)^2 + \dfrac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$
	$C_{gd} \sim 0$

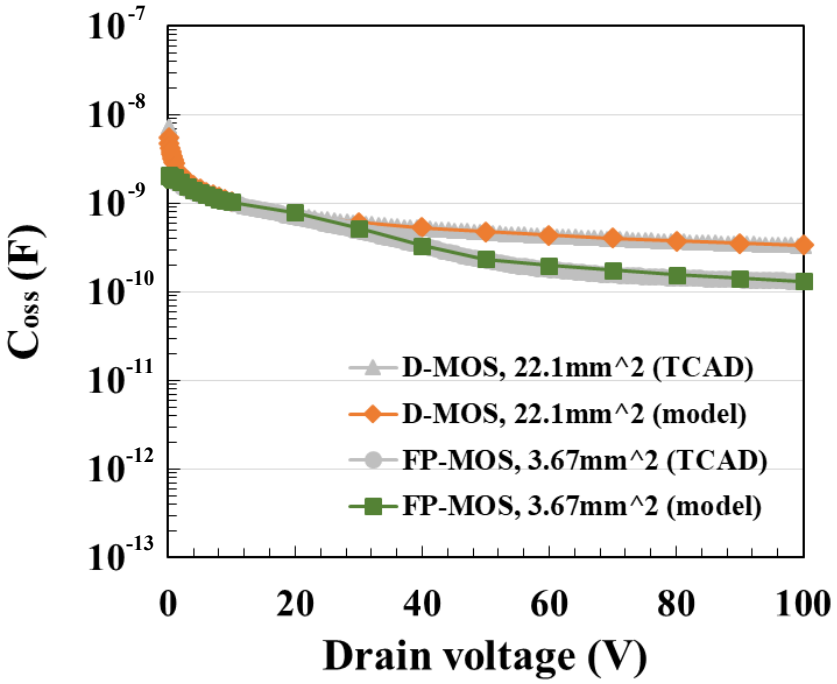

W_Cell
Source
W_G
½W_B
SiO2
Gate
p+
n+
p
T_GOX
X_JB
X_JB_I
n-
N_D
n+
Drain
W_Cell
Source
½W_Mesa
W_T
n+
p+
p
Gate
n-
N_D
SiO2
Field Plate
n+
Drain
X_JB
T_GOX
D_G
X
T_FPOX_t
D_T
W(y)
T(y)
y_0
T_OX(y)
W_si(y)
θ_2
θ_1
T_FPOX_b
θ_2
T_FPOX_c
y
(a)
(b)
(c)


Source
C_{gd}
Gate
p+
n+
p
C_{gox}
C_{dep}
C_{ds}
n-
n+
Drain
Source
n+
p+
p
C_{gd}
C_{ds1}
n-
C_{ds2}
C_{ds3}
n+
Drain

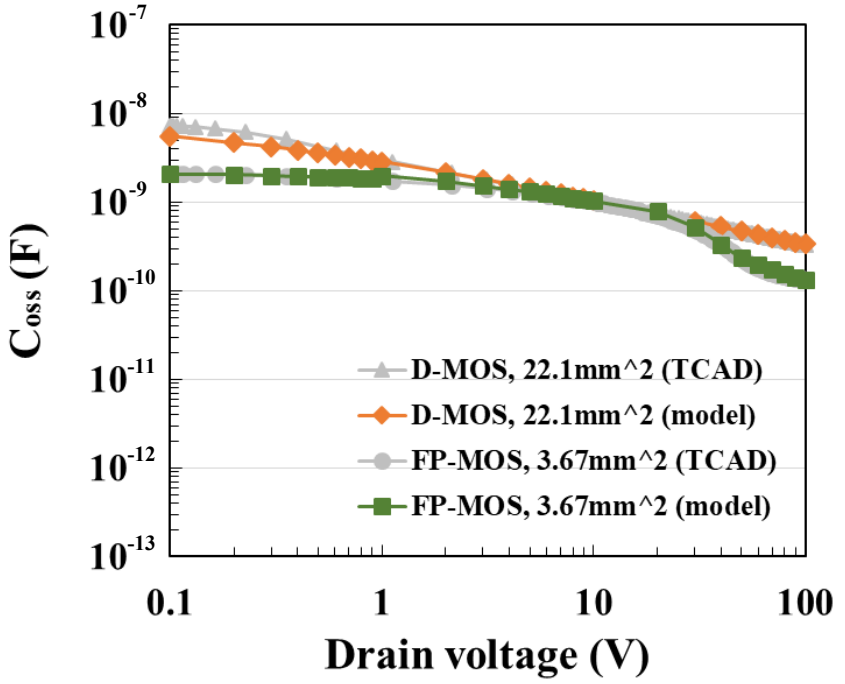
(a) (b)


Source
Gate
C_{ds1}
y_0
T(y)
W(V,y)
FP
y
y_b
Drain
(a)
Source
Gate
0
FP
y_0
C_{ds2}
y
T(y)
W(V,y)
y_b
Drain
(b)
Source
Gate
0
FP
y
y_0
T(l)
C_{ds3}
y_b
$W_{btm}(V,l)$
T_{FPOX_b}
0
l
(c)

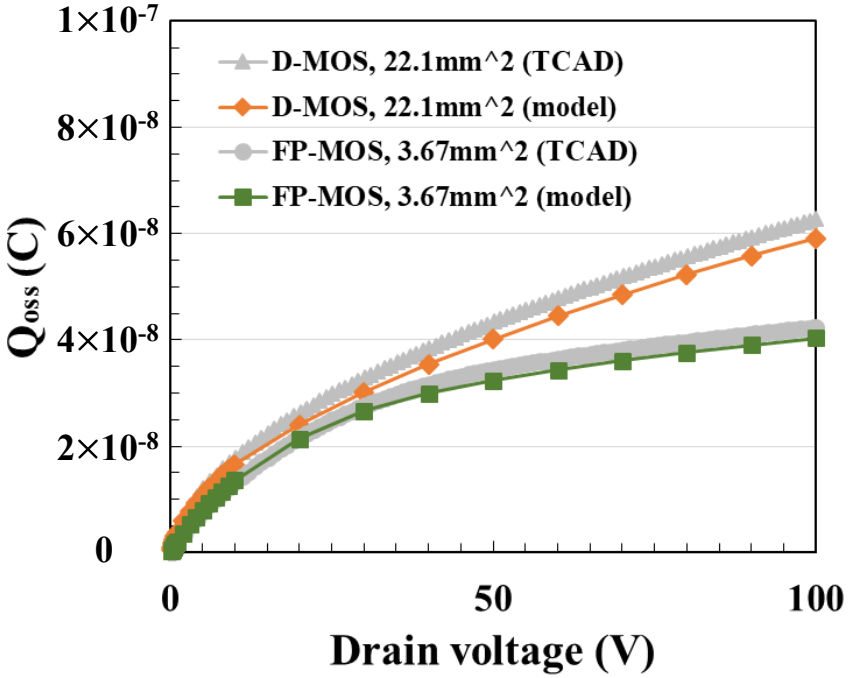

C_{ox}
10^{-7}
10^{-8}
0
1
2
Coss (TCAD)
Cj (model)
Cox (model)
Cds2 (model)
Coss (model)
C_{oss}
$C_j = C_{j0} + C_{j1}$
$+C_{ds3}$
C_{ds2}
$= CFP(V)$
Capacitance (F/cm²)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
0
20
40
60
80
100
Drain voltage (V)


10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
C_{oss} (F)
D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
0
20
40
60
80
100
Drain voltage (V)

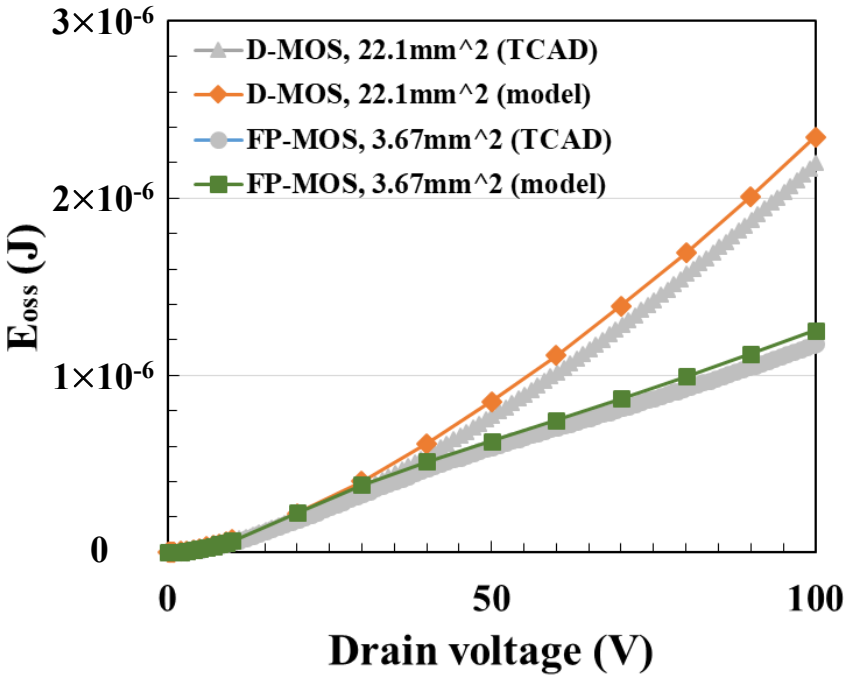
(a)


10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
C_{oss} (F)
D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
0.1
1
10
100
Drain voltage (V)

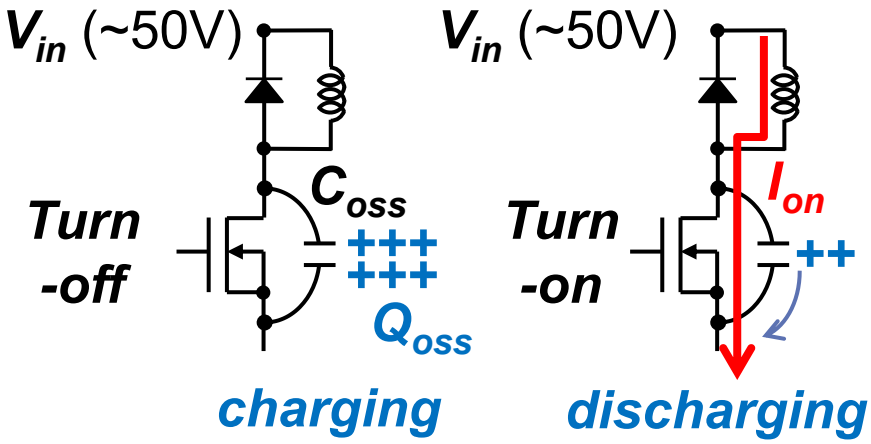
(b)

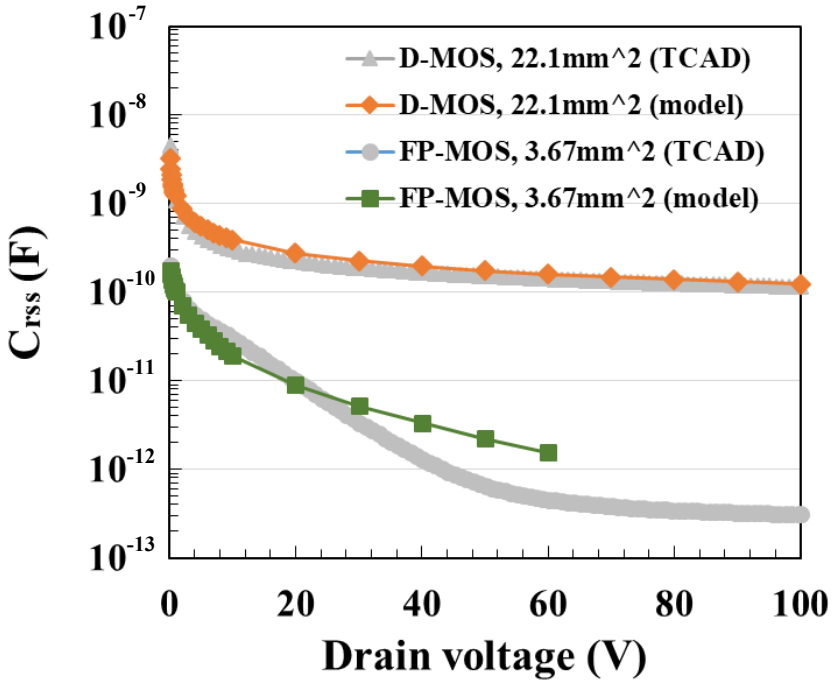

1×10-7
8×10-8
6×10-8
4×10-8
2×10-8
0
Qoss (C)
D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
0
50
100
Drain voltage (V)

(a)

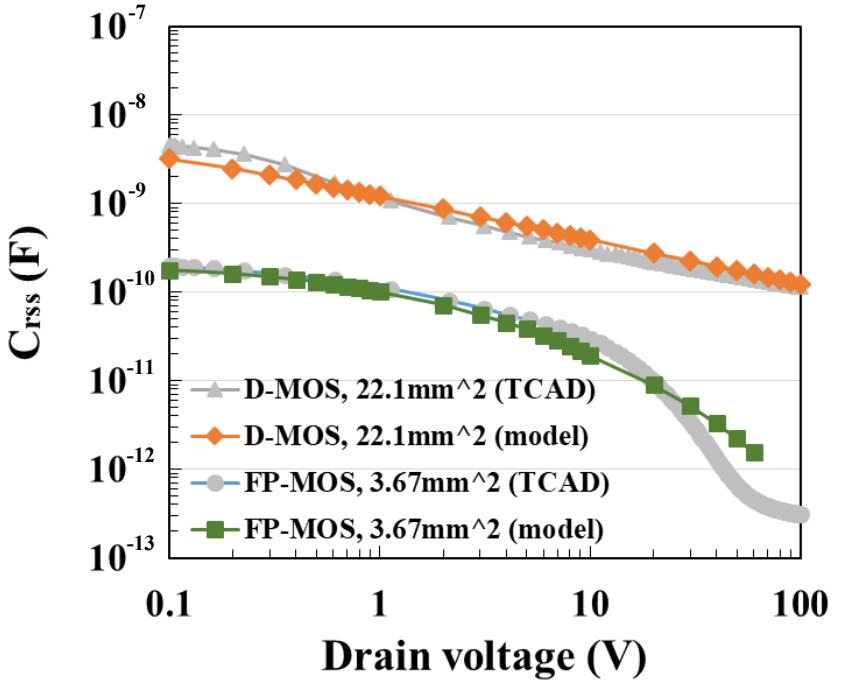

3×10-6
2×10-6
1×10-6
0
Eoss (J)
D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
0
50
100
Drain voltage (V)

(b)

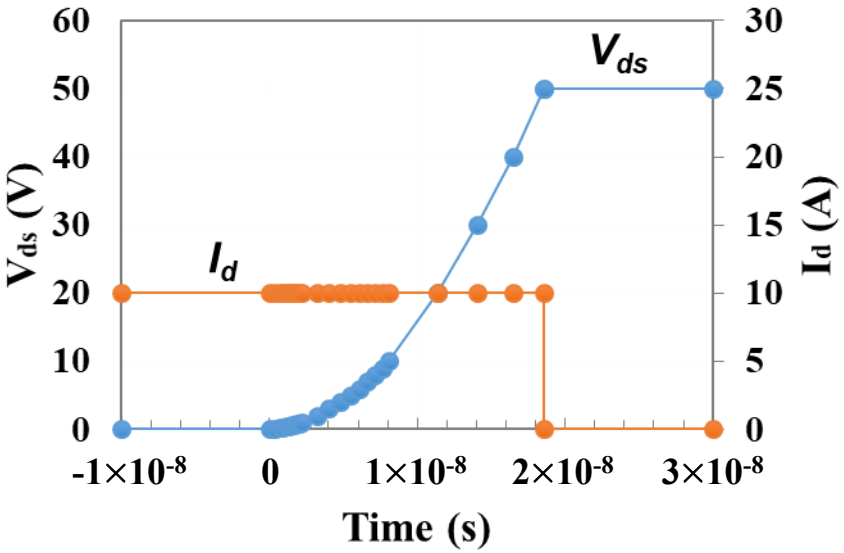

V_{in} (~50V)
Turn
-off
C_{oss}
+++
+++
Q_{oss}
charging
V_{in} (~50V)
Turn
-on
I_{on}
++
discharging


D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
C_{rss} (F)
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
0
20
40
60
80
100
Drain voltage (V)

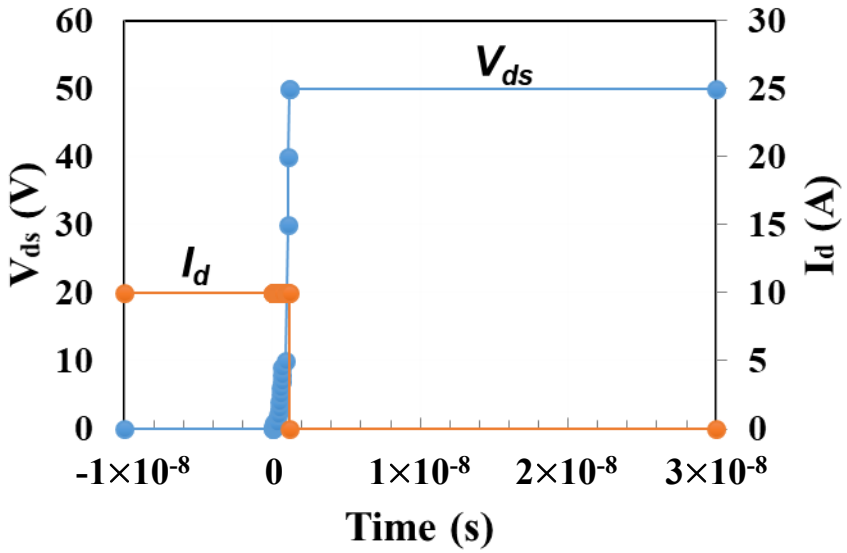
(a)


D-MOS, 22.1mm^2 (TCAD)
D-MOS, 22.1mm^2 (model)
FP-MOS, 3.67mm^2 (TCAD)
FP-MOS, 3.67mm^2 (model)
C_{rss} (F)
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
0.1
1
10
100
Drain voltage (V)

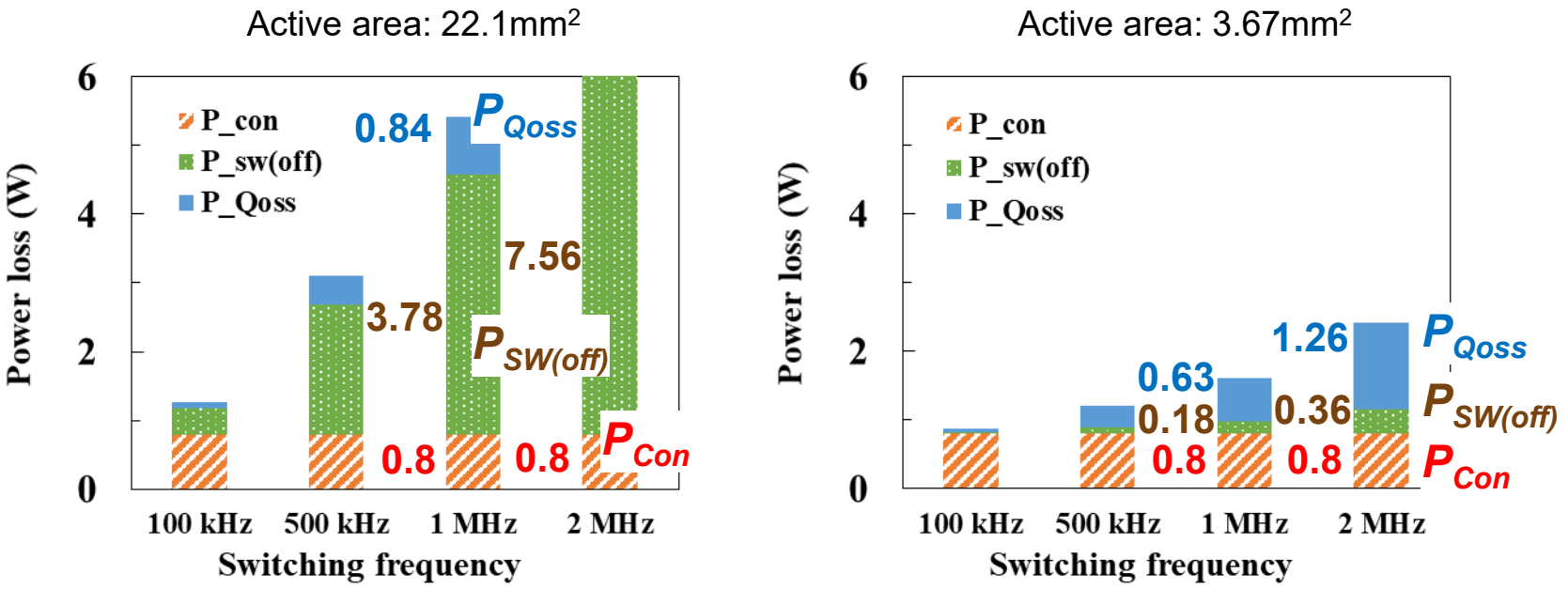
(b)


60
50
40
30
20
10
0
V_{ds} (V)
30
25
20
15
10
5
0
Id (A)
V_{ds}
I_d
-1×10-8
0
1×10-8
2×10-8
3×10-8
Time (s)

(a)


60
50
40
30
20
10
0
V_{ds} (V)
30
25
20
15
10
5
0
Id (A)
V_{ds}
I_d
-1×10-8
0
1×10-8
2×10-8
3×10-8
Time (s)

(b)


Active area: 22.1mm2
Power loss (W)
6
4
2
0
P_con
P_sw(off)
P_Qoss
0.84
P Qoss
7.56
3.78
P SW(off)
0.8
0.8
P Con
100 kHz
500 kHz
1 MHz
2 MHz
Switching frequency
Active area: 3.67mm2
Power loss (W)
6
4
2
0
P_con
P_sw(off)
P_Qoss
1.26
P Qoss
0.63
0.18
0.36
P SW(off)
0.8
0.8
P Con
100 kHz
500 kHz
1 MHz
2 MHz
Switching frequency

(a) (b)