Numerical predictions of a novel 3D stacked power-SoC structure based on hexagonal-BN

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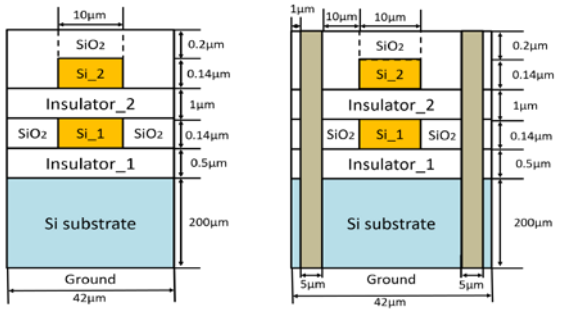
Abstract

Recently, power-SoC has been attracting attentions because it can realize ultimate miniaturization of power supply. The silicon-on-insulator (SOI) technology is one of the promising candidates for realizing power-SoC because this technology is suitable for high frequency switching, that is resulting from its smaller parasitic capacitance. However, the conventional SOI structure has a problem of self-heating because of low thermal conductivity of SiO_2. In such situations, hexagonal-BN(h-BN) is attractive for the buried insulator layer of SOI because it has higher thermal conductivity with atomically flat surface (Ra of h-BN < 0.25 nm). In this paper, we evaluate the thermal performance of a 3D stacked power SoC utilizing h-BN as an insulator and thermal interface material through numerical simulations. We also discuss the impact of the through-silicon-via (TSV) for heat dissipation.

Brief Description and Figures

The schematic cross sections of the 3D stacked power-SoC[1] with TSV and without TSV are shown in Figs.1 (a) and (b), respectively. Two insulator and silicon layers are stacked in this study. We use h-BN[2,3] and SiO_2 as *Insulator_1* and/or *Insulator_2*. The upper Si layer(*Si_2*) is covered with SiO_2. The materials constants and thermal conductivities of used in the simulations are listed in Table 1. Thickness of *Insulator_1* and *Insulator_2* are 0.5 μm and 1.0 μm, respectively. The relative permittivity of h-BN is almost the same as that of SiO_2. This means that breakdown voltage of the power device fabricated on h-BN is almost the same as that fabricated on SiO_2 because these devices are basically Silicon on Insulator(SOI) structure and breakdown voltage is determined by SOI Reduced Surface Field Principle[4]. We numerically estimate temperatures of the active Si layer at center using ANSYS Fluent[5]. In simulations, we consider only heat conduction. We give amount of heat which is correspond to keeping temperature of 473 K for *Si_1* layer (*Si_1* layer as a heat source) of the 3D stacked power-SoC when we use SiO_2 as I*nsulator_1* and *Insulator_2*. Temperature at center of *Si_1* are shown in Fig. 2 when we use *Si_1* layer as a heat source. Figs.2 shows that temperature of the heat source is about 70 K lower when h-BN is used for *Insulator_1* or *Insulator_2* because the thermal conductivity of h-BN is higher than that of SiO_2. The heat exhaust performance is

further improved when h-BN is used for both insulators. TSV can effectively suppress temperature increase by around 10-20 K in each insulator materials. Thermal conductivity of Cu used as TSV is 398 W/(m・K), which is the highest in this structure. Dependence of the temperature of the 3D power SoC on position of the heat source is shown in Figs. 3. TSVs are inserted. When *Si_2* layer is used as a heat source, temperature is higher because active *Si_2* layer is covered with SiO_2 (Fig.3). Therefore, we implement the heat source such as microprocessor at lower Si layer(*Si_1*).



(a) SOI structure model (b) TSV inserted model

Figs.1 Schematic cross sections of the 3D stacked power SoC.

Table 1. Material constants

Material	Density [kg/m³]	Thermal conductivity [W/(m・K)]		Specific heat [J/(kg・K)]	Relative permittivity (εr)
Si	2330	145		713	11.9
SiO_2	2650	1.38		760	3.9
h-BN	2100	Vertical	2	800	4.0
		Horizontal	390		

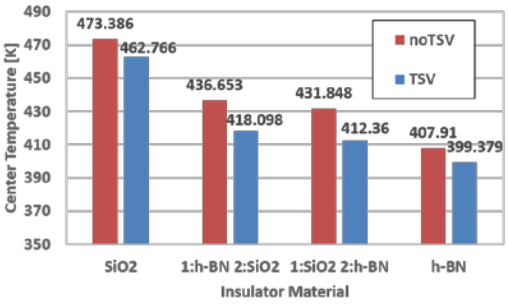
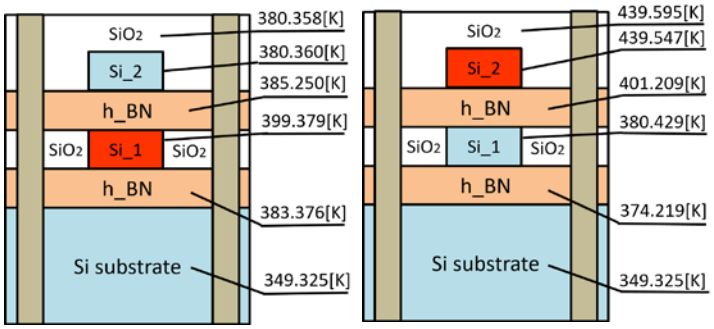


Fig. 2 Temperature of heat source (*Si 1*).



(a) heat source⋯*Si_1* (b) heat source⋯*Si_2*

Fig. 3 Dependence of the temperature of the 3D power SoC on position of the heat source

Key Contributions

The h-BN based 3D stacked power SoC shows better thermal exhaust performance compared with SiO_2 based one. Hexagonal-BN based 3D stacked power-SoC with TSV further improves heat exhaust performance. The simulation results also show that heat source should implement lower Si layer.

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