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Design of a Moderate-Resolution Dual-Slope ADC using Noise-Shaping Techniques and a Double Speed Quantizer

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Abstract

Being the slowest Analog-to-Digital Converter, the Dual-Slope quantizer is often used in sigma-delta ADC or SAR converter architectures, and in measurement instruments, due to its high accuracy. Despite the utility of the quantizer and the existent techniques to increase the accuracy and the conversion speed, the usability of this converter is still very limited by the its slow conversion rate.

The main interest of the Dual-Slope Quantizer lies in the high accuracy from the quantization technique used. To convert the input value, the value is integrated in the charge phase, by an integrator circuit, to be quantized, in the discharging phase using a digital block. Other benefits of the Dual-Slope Quantizers are the small size when implemented in a system on a chip (SOC) and the low power consumption.

By reducing the the conversion time of this ADC, while maintaining the high accuracy it will be possible to increase the converters utility, such as in IoT devices, or even mobile devices, benefiting all from the high accuracy and low power consumption of this circuit.

Nowadays, many techniques are being used in the Dual-Slope converters, such as, the addition of bi-directional capabilities, to increase the conversion speed, the addition of an half LSB compensation, to increase the accuracy, and the use of Noise-Shaping capabilities originated from the quantization error from each discharge phase. All of this techniques are presented and used in this research.

For the proposed solution, a Double-Speed Quantizer composed of two additional comparators will be added to grant the conversion speed increase, which will increase the power consumption and will lead to a redesigning of the digital block to receive more inputs.

As result the conversion speed will double in comparison to the existent 4 bit dual slope quantizer, being needed 8 clock cycles to quantize a input value, instead of 16.

Keywords: Analog-to-Digital Converter, Integrating Quantizer, Dual-Slope Quantizer, Noise-Shaping, 2-Bit Quantizer, Double-Speed Quantizer.

Resumo

Sendo o conversor Analógico-Digital mais lento, o quantizador dupla-rampa é geralmente usado em ADCs sigma-delta ou em arquiteturas de conversão do tipo SAR, e em instrumentos de medição, devido à sua alta precisão. Apesar da utilidade do quantizador e das técnicas existentes para aumentar a precisão e a velocidade de conversão, a usabilidade deste conversor é ainda muito limitada pela lenta taxa de conversão.

O principal interesse deste conversor dupla-rampa encontra-se na sua alta precisão proveniente da técnica de quantização usada. Para converter o valor de entrada, o valor é integrado na fase de carga, por um circuito integrador, para ser quantizado na fase de descarga usando um bloco digital. Outros beneficios do quantizador dupla-rampa são, o seu reduzido tamanho quando implementado num *System on a Chip (SOC)* e o baixo consumo.

Reduzindo tempo de conversão deste ADC, enquanto se mantém a alta precisão será possível aumentar a utilidade do mesmo, tal como em aparelhos IoT, dispositivos moveis, que irão beneficiar da sua alta precisão e o baixo consumo do circuito.

Atualmente, várias técnicas estão a ser usadas no conversores dupla-rampa, tais como, adição de capacidades bidirecionais, para aumentar a velocidade de conversão, a adição da compensação de meio LSB, para aumentar a precisão, e o uso de capacidades de modelação de ruido proveniente do erro de quantização a cada fase de descarga. Todas estas técnicas são apresentadas usadas na invertigação.

Para a solução proposta, um quantizador de dupla velocidade composto por dois comparadores adicionais vai ser adicionado para garantir o aumento da velocidade de conversão, que vai aumentar o consumo de energia e e levará à recriação de um bloco digital redesenhado para receber mais entradas.

Como resultado a taxa de conversão irá duplicar quando comparado com o conversor dupla-rampa existente, sendo necessários 8 ciclos de relógio para converter o valor de entrada, em vez de 16.

Palavras-chave: Conversor Analógico-Digital, Quantizador Integrador, Quantizador Dupla-Rampa, Modelação de Ruído, Quantizador de 2-Bits, Quantizador de Dupla-Velocidade.

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Acronyms

$\Sigma\Delta$	Sigma-Delta.
A/D	Analog-to-Digital.
ADC	Analog-to-Digital converter.
DAC	Analog-to-Digital converter.
DLL	delay-locked loop.
ENOB	efective number of bits.
FFT	fast fourier transform.
FIR	finite impulse response.
IC	Integrated Circuit.
IIR	infinite impulse response.
IoT	internet of things.
IQ	Integrator quantizer.
LSB	less significant bit.
MSB	most significant bit.
NSIQ	Noise Shapping Integrator quantizer.
NTF	Noise transfer function.
Op-Amp	Operational Amplifier.
OSR	oversampling ratio.
PSD	power spectral density.

SINAD	Signal to Noise and distortion.
SNDR	Signal-to-noise and Distortion Ratio.
SNR	Signal-to-Noise Ratio.
SoC	System-on-Chip.
SQNR	Signal-to-Quantization-Noise Ratio.
ZCB	zero-crossing-based.
ZCD	zero-crossing-detector.

Chapter 1

Introduction

1.1 Motivation and Background

Mobile devices System-on-Chip (SoC) and Internet of things (IoT) are the main subjects nowadays when the theme technologies are approached. With these subjects we must consider their implementation, one of the most important features is that almost all the systems used daily are digital, despite of we living in an analog world with continuous amplitude and time signals. Bearing this in mind, some of the most important components of these devices are the Analog-to-Digital converters (ADC) capable of converting analog signals to digital signals capable of being easily processed in the controller of the SoC.

Many developments were made to achieve faster Analog-to-Digital converters although not prioritizing the accuracy, that lead to a use of parallel (flash) and pipeline architectures in the Integrated Circuits (IC). As a result, single-slope and dual-slope tend to be only used in measurement instruments or as multi-bit quantizer on Sigma-Delta architectures, due to the low conversion speed and high accuracy.

This thesis will present another solution for IoT devices using double speed Dual-Slope A/D converters in the SoC presenting Matlab® simulations as well as Cadence® implementation and test of the circuit.

1.2 State-of-the-art

Taking advantage of the noise-shaping capabilities of the Dual-Slope quantizer, in IEEE 2009 Electronics Letter by N. Maghari, G.C.Themes and U. Moon [1] it is presented a Matlab® simulation of a Dual-Slope with the Noise-Shaping technique, being proposed as a suitable quantizer for delta-sigma modulators. The main goal of this work was to simulate through Matlab® the Sigma-Delta modulator studied in [2] using the presented Dual-Slope as the quantizer. The noise shaping quantizer was compared with a flash ADC and obtained a Signal-to-Quantization-Noise ratio (SQNR) of 75 dB was achieved revealing a good option when compared to a 65 dB SNDR with the flash quantizer, although the need of digital logic and a very fast clock.

Based on the previously referred work [1], N. Maghari and Un-Ku Moon [3] implemented a sigma-delta modulator using a noise-shaped Bi-directional Single-slope quantizer. A feature added to the previous work was the Bi-directional quantization, presented as a solution achieve better quantization speed, due to the slow conversion rate of the NSIQ, although leading to a quantization error that varies from 0 to $|V_{LSB}|$ originated from the polarity based offset of the comparators. To solve this problem, it was added a half LSB compensation, lowering the quantization error from 0 to $|V_{LSB}/2|$. In this implementation was also used a digital discharge logic and direction instead of a commonly used digital counter. This digital circuit uses a delay locked loop (DLL) to generate various clock signals used in the corresponding D-type flip-flop and the same flip-flop to obtain the signal direction, the solution was thought to achieve a lower power consumption. As a result of this implementation, using a 1.5V supply voltage and 24 of oversampling ratio (OSR), it was achieved 81 dB SNR peak and 72 dB SNDR peak.

In 2009, E. Prefasi, E. Pun, L. Hernández and S. Paton published a paper presenting a Second-Order Multi-Bit sigma-delta with a Pulse-Width Modulated DAC [4] to achieve a resolution of a multi bit design from a single bit DAC, and using a NSIQ. As a result, a signal to noise ratio (SNR) of 79 dB and a signal to noise distortion ratio (SNDR) of 76 dB as well as an effective number of bits (ENOB) of 13 bits, obtained through transient simulations.

With the addition of F. Cannillo, F. Yazicioglu, C. Van Hoof to the research team, the same architecture was used and implemented in a 0.18um CMOS technology, destined to Biopotential Signal Acquisitions [5]. The results were favorable, achieving 81 dB SNR and 72 dB SNDR with a power consumption of 13.3 μW and 1.2 V Supplied.

All the techniques simulated or implemented in the previously referred papers, were mathematically described and simulated in João Sousa's master thesis [6], with a bi-directional dual-slope, using a half low significant bit voltage (V_LSB) compensation, noise shaping techniques and a digital infinite pulse response (IIR) filter it was, achieved a 10.6 bits ENOB with a 65.75 dB SINAD.

Another addition to Analog-to-Digital converter (ADC) converters using Dual-Slope NSIQ as a quantizer, was in 2015 Symposium on VLSI Circuits Digest of Technical Papers, by T. Kim C. Han and N. Maghari in a Sigma Delta ($\Sigma\Delta$) modulator [7]. To achieve a better resolution without losing much speed from the 2.5-bit noise-shaped quantizer (NSIQ), with a Gm-C integrator, a delayed digital integrator was used, operating as a filter, to achieve a 4-bit output, in the back-end of the loop. With a supply voltage of 1.2 V and a 130 nm CMOS technology, a 75.3 dB SNDR, 75.5 dB SNR with a power consumption of 7.19 mW has been achieved.

Recently, in 2017, a Dual-Slope ADC was used as a programmable ADC for single-chip RFID sensor nodes, a research done by H. Shan, S. Rausch, Alice Jou, Nathan J. Conrad and S. Mohammadi [8]. This work presents the use of Dual-Slope ADC's in sensors that can easily be related to IoT and presents new approaches to a low power converter like the one presented. Being an ADC with good noise shaping properties and capable of being implemented in microscopic sizes, such as, 0.06 mm^2, with a low energy consumption, lower than 44 μW, and achieving moderate resolutions, with a ENOB of 7 bits achieved, the dual-slope continues to be a viable option in many areas.

1.3 Objectives

A dual-slope ADC using noise shaping techniques (NSIQ) is neither new nor differentiating implementation. This thesis main goal is to present and to simulate in Matlab® and Cadence® a new implementation of a dual-slope ADC with conversion time one half of a normal NSIQ and capable of achieving an almost identical ENOB. With the characteristics described, the goal of this implementation is to be capable of being implemented in IoT devices. Although not having the conversion rate of a SAR-ADC architecture, it can outperform this architectures in terms of accuracy while maintaining an acceptable conversion time, and, lower power consumption due to the use of passive components [1].

As stated before, the circuit presented in this thesis is based on the João Sousa's Master's Degree thesis [6]. With this, it was used some techniques described in João's work, like the digital filters implemented, the half LSB compensation and the bi-directional capabilities. In the proposed architecture, a 4-bit resolution NSIQ is used, like it has been achieved, while adding a 2-bit quantizer and a modified digital circuit to almost double the conversion-rate. Moreover, a secondary goal is to implement with advanced electronic circuits, the different building-blocks. In this context, a zero-crossing-detector (ZCB) based integrator has been studied and proposed.

1.4 Organization

The organization of this thesis is made in five chapters, being this one the Introduction which the objective is to present the subject and the work made in the area, followed by the Dual-Slope ADC fundamentals, presenting the state of the art and a mathematical introduction for this theme, the third chapter, entitled A Faster Noise-Shaping Dual-Slope Quantizer using a 2-bit Quantizer and Modeling, presents the mathematical simulation made and the results obtained for the noise-shaped Dual-Slope ADC with the 2-bit quantizer. The fourth chapter, entitled Dual-Slope ADC electric simulation, presents the simulation done with the presented circuit alongside the digital block and a new integrator approach for the Dual-Slope quantizer, and al te tests related to the circuits. In the last chapter, entitled Conclusions and Future Work, the overall conclusions will be discussed, as well, as some approaches to improve the presented topology.

CHAPTER 2

Dual-Slope Quantizer Fundamentals

2.1 Unidirectional Dual-Slope quantizer

Designed to achieve a high resolution, although having a slow conversion rate, the Dual Slope quantizers are widely used especially in measurement instruments. The dual slope quantizer is composed by an integrating circuit, a comparator, a digital controller with a counter and a phase controller. The schematic is presented in figure 2.1.

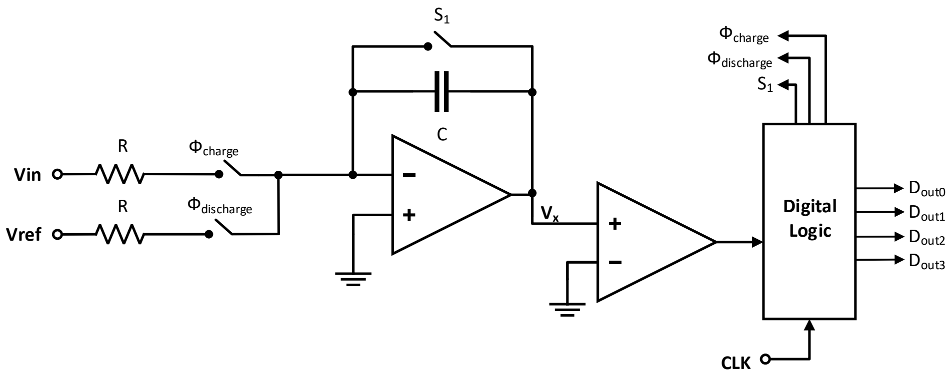


Figure 2.1: Schematic of a simple Dual-Slope A/D converter

The behavior of this quantizer can be described in two phases. The charging phase, ϕ_{charge}, where the input signal V_{in} is integrated during a fixed period T_1 leading to a charging of the capacitor C. In the discharge phase, $\phi_{discharge}$, a fixed reference voltage, V_{ref}, is integrated, discharging the energy accumulated previously in the capacitor, due to V_{ref} having an opposite polarity of V_{in}, until the integrator output, V_x, reaches zero. The zero crossing of V_x is detected with a comparator as shown in the figure 2.2. In this period, T_2, at the same time the capacitor is being discharged, the number of clock cycles are being counted in the digital circuit until V_x is nullified, this counting will be the digital output value of the quantizer.

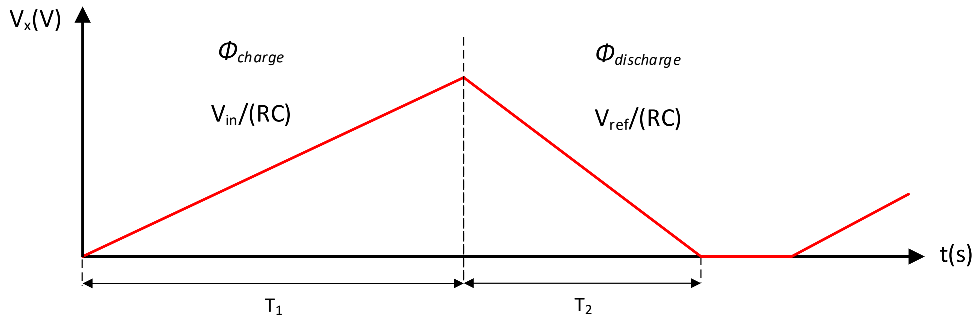


Figure 2.2: Temporal diagram of the integrators output, Unidirectional Dual-Slope Quantizer

The temporal diagram in figure 2.2 presents the V_x variation in each phase, this behavior can be mathematically described by 2.1, for the charging phase, and 2.2 for the discharging phase until the zero-cross.

$$V_x(\phi_{charge})(t) = \frac{V_{in}}{RC} \times t, \quad (t \leq T_1) \tag{2.1}$$

$$V_x(\phi_{discharge})(t) = V_x(\phi_{charge})(T_1) - \frac{V_{Ref}}{RC} \times (t - T_1), \quad (T_1 < t \leq T_2) \tag{2.2}$$

When analyzing in continuous-time periods, the behavior of each phase of the quantizer is represented in figure 2.2, the whole of the charging phase, with a T_1 period, is identical to the whole of the discharging phase with a T_2 period, assuming a V_{in} with the opposite polarity of V_{ref}, which can be described in 2.3.

$$\frac{1}{RC}\int_0^{T_1} V_{in}\mathrm{d}t + \frac{1}{RC}\int_0^{T_2} V_{ref}\mathrm{d}t = 0 \tag{2.3}$$

Resulting in a relation between the V_{in} e V_{ref} values:

$$V_{in} = -V_{ref}\frac{T_2}{T_1} \tag{2.4}$$

As an A/D converter, the dual slope quantizer will need to have a synchronous behavior in the digital circuit counter. Due to the measurement being done in a discrete-time operation, by clock counting, the time considered in the discharge phase will be the time, D_2, associated to the number clock-cycles of this phase, until the first clock ascend after the zero-cross.

Being T_1 a constant period defined, and when analyzing the discreet behavior of the quantizer, the value will be identical do the time of defined clock-cycles for the charging phase, D_1.

As can be seen in figure 2.3 the inequality between discrete time D_2 and zero crossing time T_2 originates a quantization error q_e presented in the output.

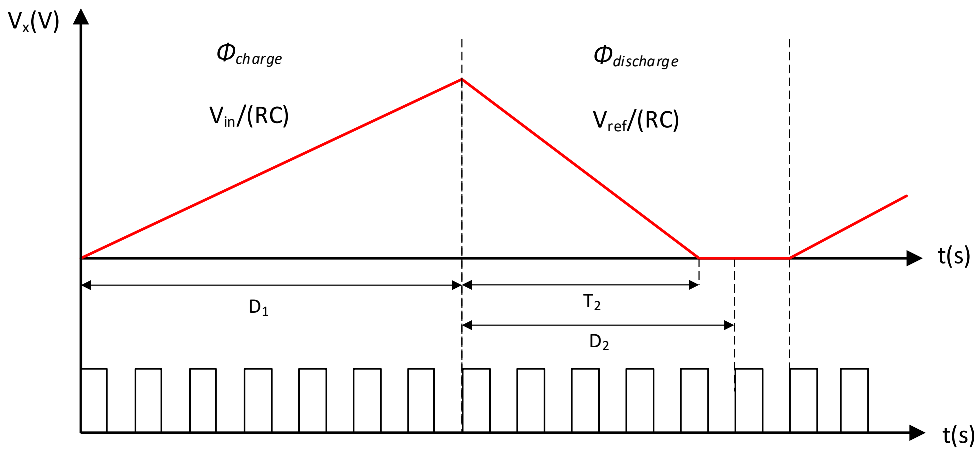


Figure 2.3: Temporal diagram of the integrators output with the clock presented bellow, Unidirectional Dual-Slope Quantizer

The minimum voltage step, V_{LSB}, is given by the integrated value of the reference voltage in a clock period, which can be described as the function 2.5.

$$V_{LSB} = V_{ref} \frac{T_{clk}}{D_1} \tag{2.5}$$

The switch, S_1, presented in schematic in the figure 2.1 is used to hold the integrator output value, V_x, at zero Volts, after the zero-crossing in the discharge phase. As a described in [6] the mathematical expression previously presented 2.3 cannot be applied when considering discrete time periods instead of a continuous. To mathematically describe the discrete time behavior of this circuit, presented in figure 2.3, the quantization error needs to be accounted, as is done on the equations 2.6 and 2.7.

$$\frac{1}{RC} \int_0^{D_1} V_{in} \mathrm{d}t + \frac{1}{RC} \int_0^{D_2} V_{ref} \mathrm{d}t = \frac{1}{RC} \int_{T_2}^{D_2} V_{ref} \mathrm{d}t \tag{2.6}$$

$$V_{in} = -V_{ref} \frac{D_2}{D_1} + q_e \tag{2.7}$$

With the expression shown and considering the variable quantization error period q_t the integrator equation can be simplified and the quantization error q_e can be obtained through the following expressions:

$$q_e = V_{ref} \frac{q_t}{D_1} \tag{2.8}$$

$$q_t = D_2 - T_2 \tag{2.9}$$

By the expression 2.7 it can be verified that the integrator quantizer, IQ, presents a noise transfer function, |NTF|=|1| as described in [6].

2.2 Noise-Shaped Dual-Slope Quantizer

A new approach to the Dual-Slope quantizers has been proposed in 2009, by N. Maghari, G.C. Themes and U. Moon using noise-shaping capabilities in the existent dual slope, NSIQ's. By removing the switch S_1 presented in the original Dual-Slope (figure 2.1) the quantization error q_v will appear in the output of the integrator, V_x, leading to discharging beyond the zero-crossing until the end of the clock cycle. This effect will create a new parameter correspondent to the residual quantization error coming from the previous discrete instant $q_e(n-1)$.

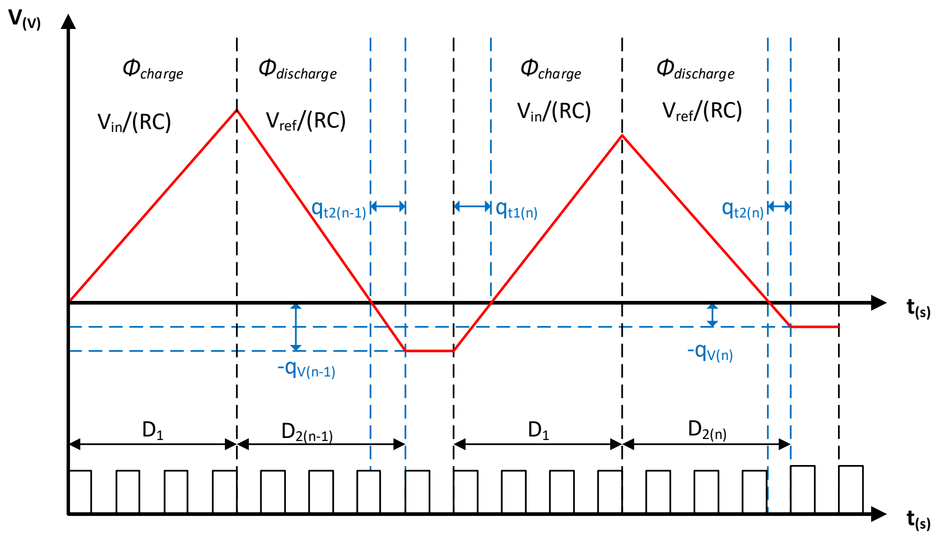


Figure 2.4: Temporal diagram of the Noise-Shaping Integrator Quantizer (based of the diagram presented in [6]).

The effect presented in the figure 2.4 will increase the converter accuracy and reduce the overall quantization error due to the residual effect mathematically previously described in [6], and presented on the expressions 2.10, 2.13, 2.14.

$$\int_0^{D_1(n)} V_{in}(n)\mathrm{d}t - \int_0^{q_{t_1}(n)} V_{in}(n)\mathrm{d}t = -\int_0^{D_2} V_{ref}\,\mathrm{d}t + \int_{T_2}^{q_{t_2}(n)} V_{ref}\,\mathrm{d}t \tag{2.10}$$

Being the quantization error period, q_t for the charging and discharging phase, D_1 and D_2 described by 2.11 and 2.12.

$$q_{t_1}(n) = D_1(n) - T_1(n) \tag{2.11}$$

$$q_{t_2}(n) = D_2(n) - T_2(n) \tag{2.12}$$

Being the quantization error, at the start of each charging phase, obtained from the previous discharging phase, the expressions 2.10 can be re-written to 2.13.

$$\int_0^{D_1(n)} V_{in}(n)\mathrm{d}t + \int_0^{q_{t_2}(n-1)} V_{ref}(n)\mathrm{d}t = -\int_0^{D_2} V_{ref}\mathrm{d}t + \int_{T_2}^{q_{t_2}(n)} V_{ref}\mathrm{d}t \tag{2.13}$$

By simplifying the expression in 2.13 the V_{in} value can be obtained presenting the noise factor of the actual (n) and previous $(n-1)$ conversion-cycle presented in te expressions 2.14 and 2.15.

$$V_{in}(n) = -V_{ref} \times \left(\frac{D_2(n)}{D_1} - \frac{q_{t_2}(n)}{D_1} + \frac{q_{t_2}(n-1)}{D_1}\right) \tag{2.14}$$

$$V_{in}(n) = -V_{ref} \times \left(\frac{D_2(n)}{D_1} - q_e(n) + q_e(n-1)\right) \tag{2.15}$$

With the Z-Transform of the expression presented previously, 2.15, it is obtained the expression 2.16. With this expression it can be concluded that the NSIQ has noise transfer function of, $|\mathrm{NTF}|=|1-z^{-1}|$, presenting better results when compared to a simple IQ.

$$V_{in}(n) = -V_{ref} \times \left(\frac{D_2(z)}{D_1} - (1-z^{-1}) \times q_e(z)\right) \tag{2.16}$$

2.3 Bi-directional Dual-Slope quantizer

In order increase the conversion rate of the dual-slope ADC a technique was also proposed by Maghari and Moon in [3], namely a bi-directional discharging scheme implemented in a Dual-Slope quantizer. The bi-directional implementation provides many advantages over the unidirectional quantizer, for example, the capability of converting directly an input value with positive or negative values due to the use of a directional bit, as the most significant bit (MSB), that indicates the polarity of the integrated input value in the charging phase, and doubling the conversion speed. On the other hand, the unidirectional ADC is only capable of converting inputs with a constant polarity, leading to a necessary circuitry implementation to convert a bi-directional input to a unidirectional one, capable of being converted.

To implement this concept, the reference voltage (V_{ref}) is integrated on the discharge phase, being the reference polarity dependent of the inputs polarity at the charging phase, in figure 2.5 is presented a simplified schematic of the Bi-directional Dual-Slope quantizer, compared to the one presented in [3].

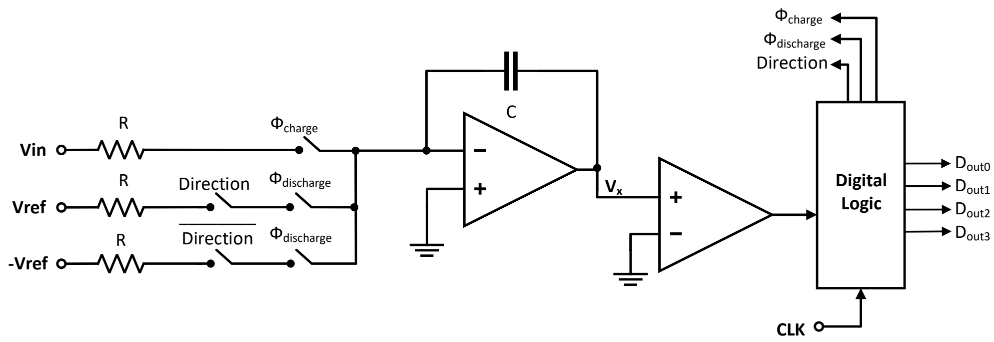


Figure 2.5: Schematic of a Bi-directional Dual-Slope A/D converter.

2.3.1 Achieving 4bits from a 3bit counter

Compared to a 4-bit unidirectional dual slope quantizer, the bi-directional uses a 3-bit counter with the bi-directional capabilities, by, in the discharge phase, integrating the reference value correspondent to the opposite polarity of the charging phase (V_{ref} for a negative value or $-V_{ref}$ for a positive value). In order to achieve the 4th bit from the 3rd bit quantizer, the most significant bit used corresponds to the directional bit, resulting in the 3 bit counter (counting from 0 to 7) quantizing the input value (positive or negative), instead of a 4bit counter (from 0 to 15), doubling the conversion ratio.

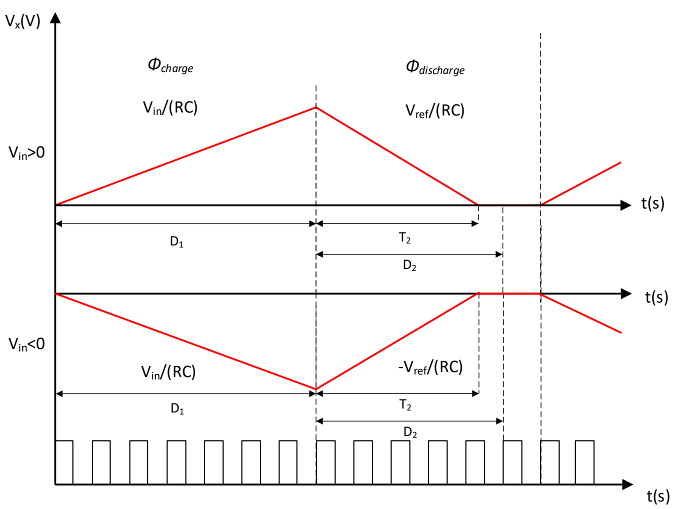
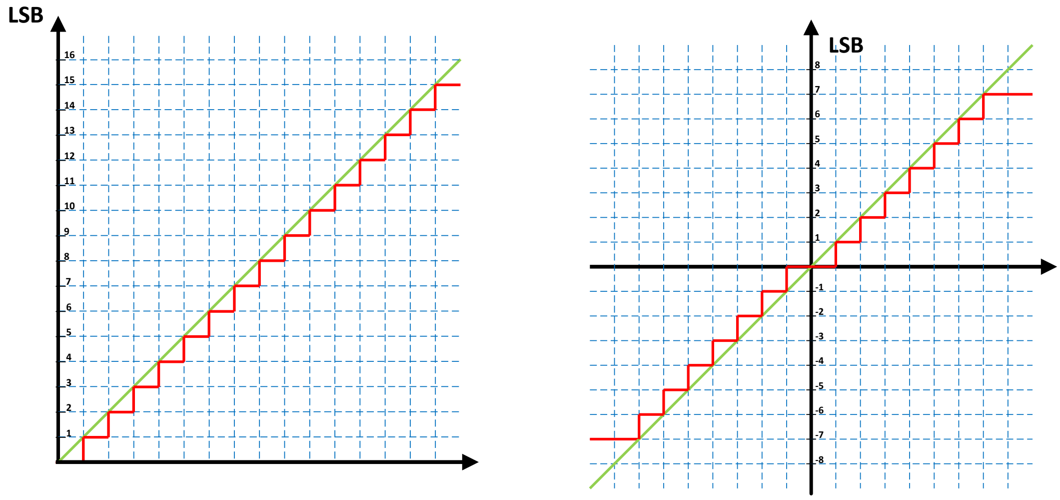


Figure 2.6: Temporal diagram of the Bi-directional Dual-Slope A/D converter integrator output (considering an none inverter integrator).

Having the same quantizing behavior for positive and negative values, from 0 to 7 or from 0 to -7, the output of a bi-directional quantizer with a 3-bit counter varies from -7 to 7 (15 values), losing a quantization value when compared to the unidirectional with a 4-bit counter, whose the quantization ranges from 0 to 15 (16 values) and resulting in a decrease of the resolution of the ADC, the comparison is presented in figure 2.7.



(a) Unidirectional Dual-Slop Quantizer

(b) Bi-directional Dual-Slop Quantizer

Figure 2.7: Comparison between a V_{in} slope (green), and the equivalent output value (red) for the 4-bit counter Unidirectional and the 3-bit counter Bi-directional Dual-Slope Quantizer.

2.4 Half LSB compensation

To reduce the maximum absolute error of the ADC from $|V_{LSB}|$, presented in the Bi-Directional Dual-Slope quantizer in section 2.3, to $|\frac{V_{LSB}}{2}|$ it is added additional circuit to operate in the charging phase, ϕ_{charge}, as presented in the schematic, figure (2.8).

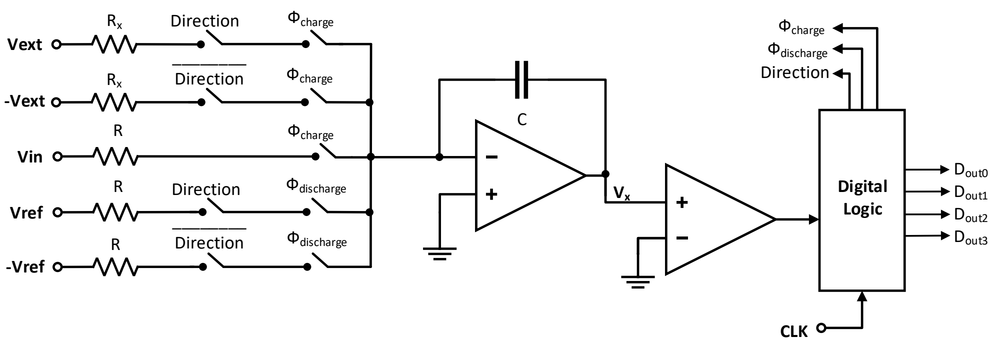


Figure 2.8: Schematic of a Bi-directional Dual-Slope A/D converter with noise shaping capabilities an the additional V_{ext} and R_x for the Half LSB compensation (as presented in [6])

This addition consists in increasing, or decreasing the final V_x value at the end of the charge phase by $\frac{V_{LSB}}{2}$ or -$\frac{V_{LSB}}{2}$ for a positive or negative input value $V_{in}(n)$.

Bearing in mind the added value in each charge phase, correspondent to a D_1 period, must be $\frac{V_{LSB}}{2}$ or -$\frac{V_{LSB}}{2}$, which respond to the variation of V_x in the discharge phase in $\frac{T_{clk}}{2}$, or the integrated value of V_{ref} in half a clock period. With the description made, and by adding an external voltage, V_{ext} and resistor R_x to obtain the half LSB addition, a mathematic relation is obtained as presented in the expressions (2.17) and (2.18).

$$\frac{1}{R_x C}\int_0^{D_1} V_{ext}\mathrm{d}t = -\frac{1}{RC}\int_0^{\frac{T_{clk}}{2}} V_{ref}\mathrm{d}t \tag{2.17}$$

$$R_x = 2\frac{D_1}{T_{clk}}\frac{V_{ext}}{V_{ref}}R \tag{2.18}$$

Comparing the output of the integrator of the original Dual-Slope presented on 2.1 with the half LSB ($\frac{V_{LSB}}{2}$) compensation addition, presented on figure 2.9, there can be seen a increase of half LSB ($\frac{V_{LSB}}{2}$) that will result in an increase of the discharging slope period (T_2) equivalent to half LSB discharge period.

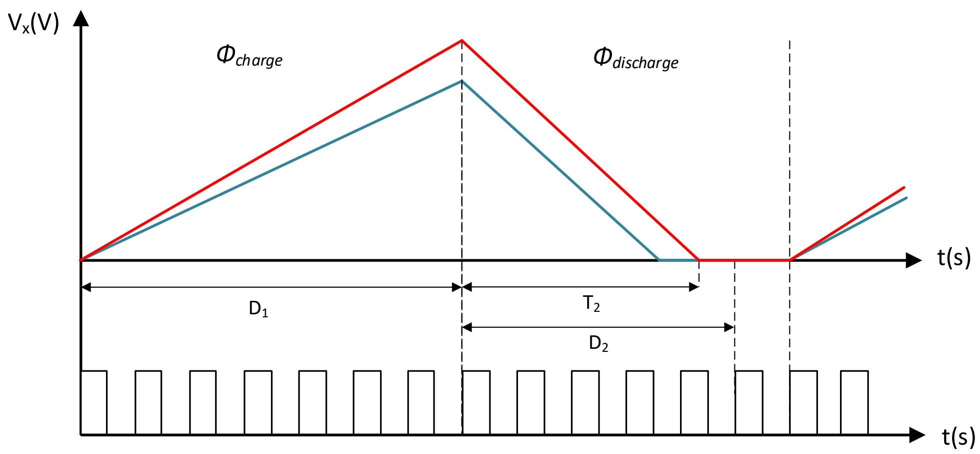
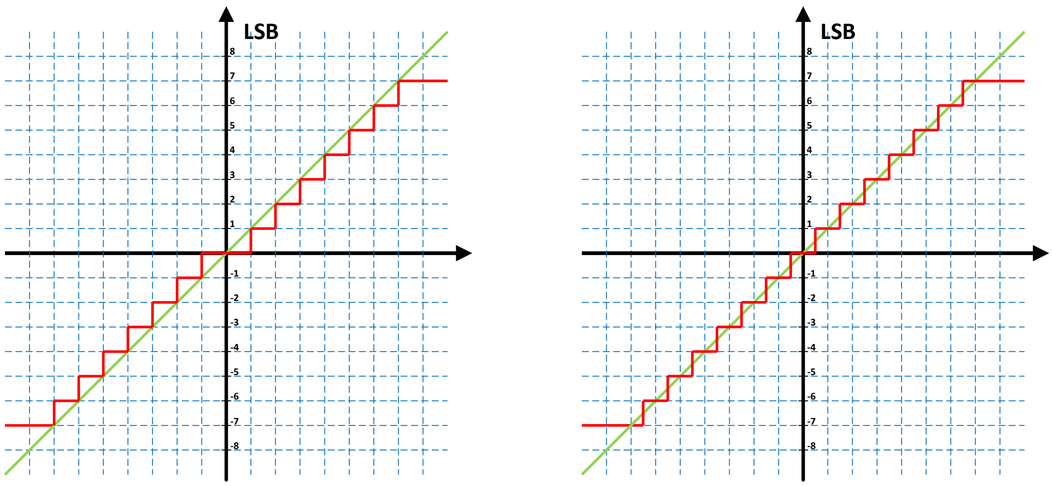


Figure 2.9: Temporal diagram comparing the Bi-directional Dual-Slope A/D converter standard (blue) with an half LSB compensation (red)

The comparison between the Bi-directional Dual-Slope Quantizer with and without the compensation is presented in the figures on 2.10, resulting in a absolute error reduction when the compensation is added, from each quantization being made for input values $|\frac{V_{LSB}}{2}|$ lower then simple Bi-directional implementation.



(a) Bi-directional Dual-Slop Quantizer

(b) Bi-directional Dual-Slop Quantizer with Compensation

Figure 2.10: Comparison between a V_{in} slope (green), and the equivalent output value (red) for each Dual-Slope Quantizer solution presented.

CHAPTER 3

A Faster Noise-Shaping Dual-Slope Quantizer using a 2-bit Quantizer and Modeling

The proposed approach consists in the use of a 2-bit quantizer, composed of three comparator circuits, the additional two comparators, to increase the conversion speed, and the zero detector, to the existent bi-directional NSIQ. In order to double the conversion ratio, a comparison is made between integrator output voltage excess, or quantization error (q_e), correspondent to the quantization error of the noise shaping technique eq.2.10, 2.11, 2.12, with with half LSB, further explained in 3.4, depending on the direction to obtain an additional bit value. The explained procedure is presented on the figure 3.1, as well and the added double-speed approach.

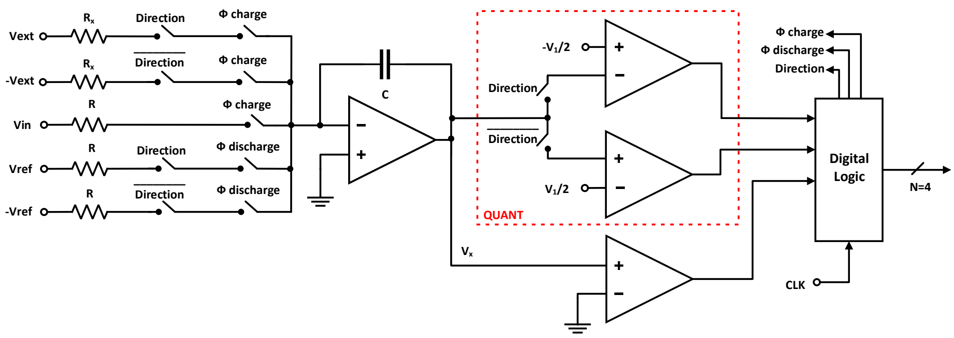


Figure 3.1: Schematic of the proposed bi-directional NSIQ using a Half LSB compensation, with the double-speed quantizer highlighted.

The approaches used in the circuit in 3.1 are further explained in sections 3.1, 3.2, 3.4, 3.5, 3.6, and the simulations, results with the associated analysis are presented in 3.7, 3.8

and 3.9.

3.1 Behavioral description and Quantization Error Technique

Based in the NSIQ, the addition of the 2-bit quantizer wont affect the behavior of the quantizer although needing a more complex digital logic circuit. Instead of using a 3-bit counter and the fourth bit being obtained by the direction of the integrated value, adding the 2-bit quantizer will need only, a 2-bit counter, being the most significant bit the directional, due to being a bi-directional circuit and the least significant bit obtained from the additional comparators.

By using a 2-bit counter (from 0 to 3, 4 clock-cycles) the conversion speed will double when comparing to a 3-bit counter (from 0 to 7, 8 clock-cycles). Being the goal of this thesis to obtain the results of a 4-bit bi-directional NSIQ, using a 3-bit counter, by using the same technology, although with a 2-bit counter there are many parameters to keep in mind, such as:

- Double-Speed Quantizer: The addition of two half LSB comparators to take advantage of the Noise shaping of the circuit obtaining the value of an additional bit at the output;

- Charging phase: Have a behavior equivalent to a 3-bit counter, the charging phase period as to be taken in mind, by using a 3.5clock-cycles representing half of the 7 clock-cycles from the 3-bit counter;

- Discharging phase: By using the 2-bit quantizer as the less significant bit (LSB) the 2-bit counter counting is made by doubling each counting value, resulting in a 3-bit counter.

Presented in figure 3.2 is the output of the integrator, with each sampling cycle having a total of 8 clock-cycles. The first 3.5 clock-cycles are destined to the charging phase, the ascending slope, and remaining 4.5 clock-cycles for the discharging correspondent to the descending slope and the sample phases the stable phase where the digital value can be sampled.

3.2 Parameters used for the behavioural modeling

The modeling of the circuit behavior was simulated using the software Matlab® running a Monte-Carlo method with 100 cycles with the simulated errors of the components, using the following parameters and values:

- Input frequency of f_{in} = 1 MHz

- Maximum input amplitude of 0.3 V

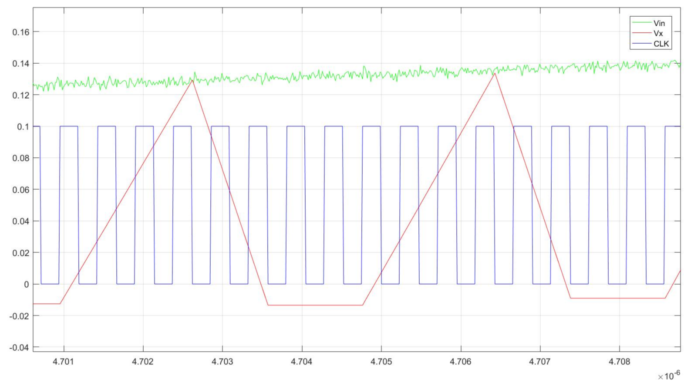


Figure 3.2: Dual-Slope Behavior with 3.5 clock-cycles in the charge phase

- Reference voltage $V_{ref} = 0.3$ V
- BW = 3 MHz
- $f_{clk} = 2.1$ GHz
- $R = 2\,\mathrm{k}\Omega \pm 0.1\%$
- $C = 1$ pF $\pm$ 0.1%

3.3 Frequency Parameters for Simulation

It was used a sine wave with a frequency of 1.001 kHz, as done in [6], with a clock frequency of 2.1 GHz, with 8 clock-cycles per sample phase, as explained previously in 3.1. With all this information the sampling frequency can be obtained using the equation 3.1

$$f_{sampling} = \frac{1}{8 \times \frac{1}{2} \times \frac{1}{f_{clk}}} = 525MHz \tag{3.1}$$

Oversampling is a technique used in Dual-Slope, SAR and Sigma Delta ($\Sigma\Delta$) architectures, and consists in having a sample rate higher than the Nyquist frequency ($2 \times BW$) increasing the resolution of the ADC based on the OSR through a binary scale.

The OSR corresponds to the scale between the ADC sampling frequency and the Nyquist frequency, as presented in the equation 3.2.

$$OSR = \frac{f_{sampling}}{2 \times BW} = 87.5 \tag{3.2}$$

3.4 The Double-Speed Quantizer

Highlighted in figure 3.1, as explained before, the double-speed quantizer consists in the comparison between the integrator output (V_x) and a half V_{LSB}, for each polarity. This half V_{LSB} value corresponds to the integrator output and must be calculated before the implementation of the circuit, due to the value being calculated from the clock frequency (f_{clk}), which the equation is presented in 3.3.

$$\frac{V_1}{2} = \frac{V_{x_{lsb}}}{2} = \frac{V_{ref}}{2 \times F_{clk} \times R \times C} \approx 36mV \tag{3.3}$$

3.4.1 Encoding

Considering the directional bit value is dependent of V_x (Dir_{V_x}), the variation of the comparison voltage $\pm\frac{V_{x_{lsb}}}{2}$ is dependent of this direction, with these values the encoding can be done as presented in the truth table 3.1.

Table 3.1: Truth table with the encoding of D_0, the less significant bit of the digital output (D_{out})

Dir_x	V_{CMP}	V_x	D_0
0	$\frac{V_{x_{lsb}}}{2}$	$\leq \frac{V_{x_{lsb}}}{2}$	1
0	$\frac{V_{x_{lsb}}}{2}$	$> \frac{V_{x_{lsb}}}{2}$	0
1	$-\frac{V_{x_{lsb}}}{2}$	$\leq \frac{V_{x_{lsb}}}{2}$	0
1	$-\frac{V_{x_{lsb}}}{2}$	$> \frac{V_{x_{lsb}}}{2}$	1

3.5 Error Evaluation

As stated on chapter 2.4, error range will decrease from $|V_{LSB}|$ to $|\frac{V_{LSB}}{2}|$ when the quantizer integrates an half LSB compensation. This behaviour is presented in figure 3.3, presents the relative LSB error of the integrator output (V_x) and input (V_{in}) described as follows:

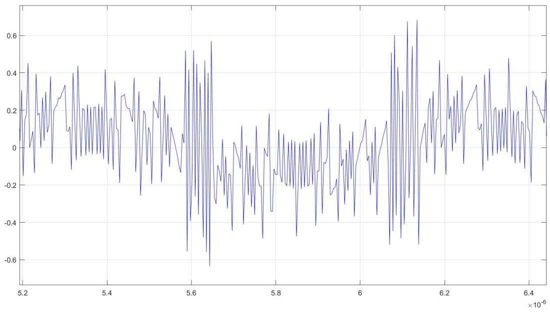
$$Error_{LSB} = \frac{V_x - V_{in}}{V_{lsb}} \tag{3.4}$$

3.6 IIR Filter

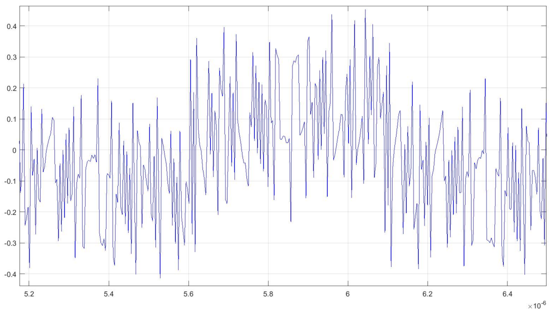
Following the study made in [6], which concluded the best approach to grant a higher resolution for the 4 bits NSIQ would be an IIR Filter, whose transfer function can be seen in 3.5.

$$F_{IIR}(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3.5}$$

Although granting a higher resolution compared to the "Finite Impulse Response"filter (FIR) the IIR filter delays the output 180 degrees when compared to the input as can be seen in the image 3.4.



(a) NSIQ with a 2-bit quantizer



(b) NSIQ with a 2-bit quantizer and Half LSB compensation

Figure 3.3: LSB_{error} between the integrator output (V_x) and input (V_{in}), being (a) the LSB_{error} of the NSIQ with a 2-bit quantizer; (b) the LSB_{error} of the NSIQ with a 2-bit quantizer and Half LSB compensation.

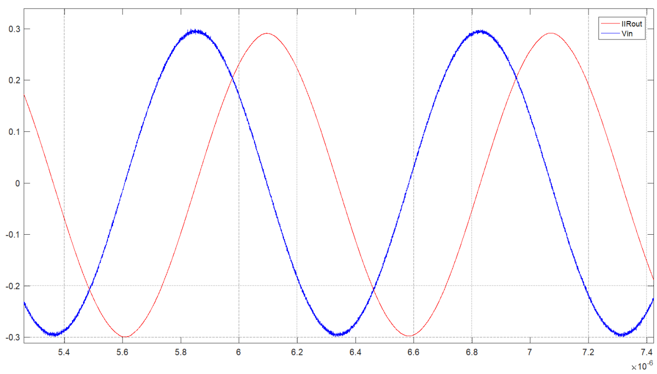


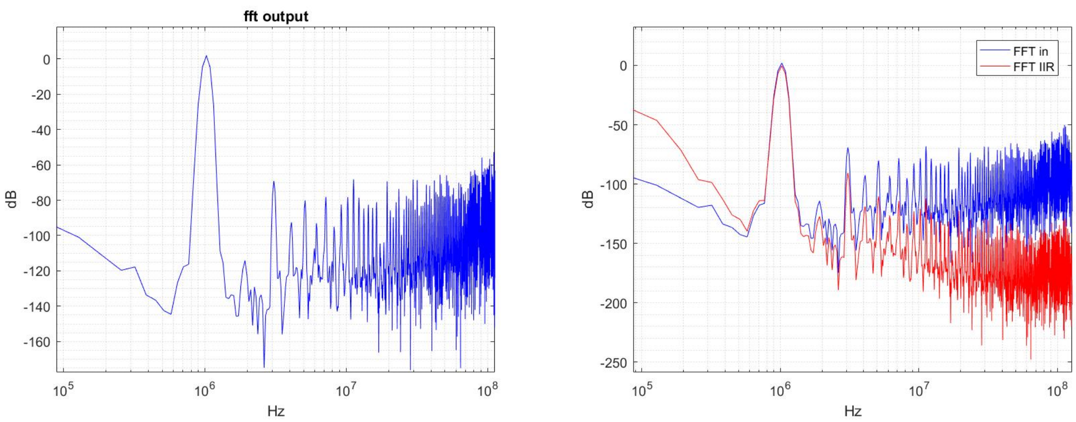
Figure 3.4: V_{in}(blue), compared to the IIR filter output(red).

3.7 NSIQ using a 2-bit quantizer Simulation

The simulation was made considering the first 16 input periods, using 4095 FFT points and white noise was added to the input, equal to the one used in [6], distributed by a Gaussian curve with the variance of 0.0054V obtained from the equation 3.6.

$$3\sigma_{VNT} = \frac{V_{scale}}{2^{N+1}\sqrt{12}} = \frac{V_{scale}}{2^{4+1}\sqrt{12}} = 0.0054V \tag{3.6}$$

Using all the parameters described previously in both this and in section 3.2, the power spectral density (PSD) of the quantizer output and IIR filter was generated and can be analyzed and compared in figure 3.5.



(a) D_{out}(blue)

(b) D_{out}(blue) and IIR_{out}(red)

Figure 3.5: FFT ouput of the quantizer for: 3.5a D_{out} with 8.6bits of ENOB and 3.5b D_{out} with 8.6 bits of ENOB and IIR_{out} with 9.7 bits.

By running a 100 cases of the Monte-Carlo method, varying the resistors, capacitor, and input, as described in section 3.2, it was possible to reach almost 10 bits ENOB in some cases, due to the ENOB increase from the IIR of more than a 1 bit of ENOB compared to the output of the quantizer, as presented in table 3.2.

Table 3.2: Results of 100 cases with a Monte-Carlo method simulation for the NSIQ using a 2-bit quantizer

	$ENOB_{AVG}$	$ENOB_{MAX}$	$SINAD_{AVG}$	$SINAD_{MAX}$
D_{out}	7.7 bits	8.6 bits	47.9 dB	53.8 dB
IIR_{out}	8.8 bits	9.7 bits	54.4 dB	59.9 dB

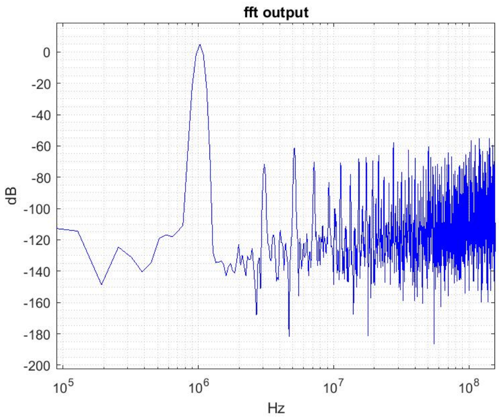
As stated in [6], the FIR filter will generate a -20 dB/dec FFT signal decrease, which will reduce the harmonics value as can been verified in 3.3.

Table 3.3: Analysis of the FFT spectrum for each harmonic

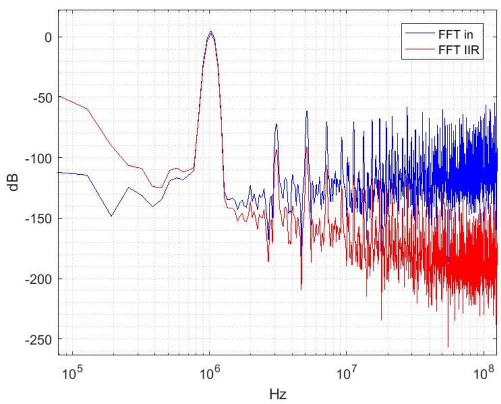
	2^{nd}	3^{rd}	4^{th}	5^{th}
D_{out}	-69.1 dB	-92.5 dB	-80.2 dB	-93 dB
IIR_{out}	-90.6 dB	-118.9 dB	-110.4 dB	-126.5 dB

3.8 NSIQ using a 2-bit quantizer and half LSB compensation Simulation

Following the results of the previous simulation, section, 3.7, the half LSB compensation stated on section 2.4 was added, which resulted on significantly better results as they can be compared between tables 3.4 and 3.5 when compared to the previous results, the tables 3.2 and 3.3.



(a) D_{out}(blue)



(b) D_{out}(blue) and IIR_{out}(red)

Figure 3.6: FFT ouput of the quantizer using a half LSB compensation for: 3.5a D_{out} with 9.1 bits ENOB and 3.5b D_{out} with 9.1 bits ENOB and IIR_{out} with 10.2 bit ENOB.

Table 3.4: Results of 100 cases with a Monte-Carlo method simulation for the NSIQ using a Half LSB compensation and a 2-bit quantizer

	$ENOB_{AVG}$	$ENOB_{MAX}$	$SINAD_{AVG}$	$SINAD_{MAX}$
D_{out}	8.1 bits	9.1 bits	50.4 dB	56.8 dB
IIR_{out}	9.2 bits	10.2 bits	56.9 dB	63.4 dB

Table 3.5: Analysis of the FFT spectrum for each harmonic

	2^{nd}	3^{rd}	4^{th}	5^{th}
D_{out}	-71.7 dB	-61 dB	-70.3 dB	-83.1 dB
IIR_{out}	-92.9 dB	-91.1 dB	-106.2 dB	-123.4 dB

3.9 Simulation analysis

As concluded previously in [3] and [6], the half LSB compensation will result in an increase of the ENOB, about 0.4 bits ENOB from the average values, as well a increase on the SINAD resulting in lower harmonics as can be compared between 3.3 and 3.5.

As described in section 3.6, the use of an IIR filter will result in a increase of the ENOB as presented in table 3.2 and 3.4 being achieved a increase of 1.1 bits ENOB when compared the average value, this approach will also increase the signal-to-noise and distortion ration (SINAD) and, as presented in table 3.3, lower the value of each harmonic except for the fundamental, effect created from the 180 degree delay of the output (V_{out}) when compared to the input (V_{in}).

Chapter 4

Dual-Slope ADC electric simulation

After the Matlab® simulation, a Cadence® electric simulation was prepared, using a CMOS 130nm technology, to create a more realistic circuit analysis, compared to the previously mentioned behavioral simulations.

The circuit has been separated in various parts, being the section 4.1 destined to explain the digital part, phase controller with flip-flops and logic gates are included; section 4.2 to present and study the comparator used; section 4.3, where a redesign of the Double-Speed Quantizer, explained in 3.4, is presented; section 4.4 presents the results of the simulation and the data used; and finally section 4.5 presenting a possible integrator solution for the circuit.

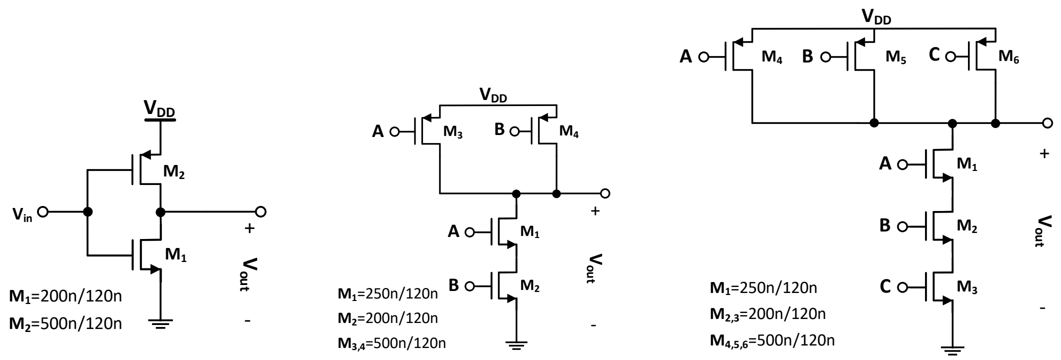
The integrator and switches used to control the input values of de Dual-Slope quantizer have been developed, taking into account ideal conditions with the modeling language, Verilog-A.

4.1 Digital Circuit

4.1.1 Elementary logic gate

Being response speed one of the most relevant factors in a digital circuit, the right elementary logic gates must be considered when designing more complex logical circuits such as, a flip-flip and a charge and discharge-phase generator.

To acquire a faster response speed, all the digital components, spanning the elementary logic gates such as AND, OR, XOR and XNOR to the more complex D flip-flops, were all designed using combinations of the NOT and the NAND logic gates, due to being the fastest logic gates, speed related to the number of PMOS transistors in, stacked in series, that separate the output from the source voltage (V_{DD}). The schematic and dimensions are presented on figure 4.1.



(a) (b) (c)

Figure 4.1: Schematic of the elementary logic gates used using a 130nm CMOS technology and dimensions. (a)NOT; (b)NAND (two inputs); (c)NAND (three inputs).

4.1.2 Flip-flop

To create a logic circuit capable of controlling and obtaining data from the integrator circuit it was required to have memory elements, which in this case, were used D flip-flops.

Two D flip-flop topologies have been studied, a faster and more simple, NOT gate based latch composed of transmission gate switches and NOT gates, with an internal feedback ensuring memory capabilities to the circuit, presented in figure 4.2a based on a topology presented in [9]. A slower but more consistent topology composed of NAND gates providing feedback between each other, having the advantage of using a reset input (RST) to clear the flip-flop memory at a clock transition, topology is presented in figure 4.2b.

The topology used in the 4.1.3 was the first one, figure 4.2a, due to the faster response speed compared to the NAND implementation.

The behavior of the flip-flops presented in figures 4.2a and 4.2b are described on table 4.1, having a special attention to the RST value only used on 4.2b.

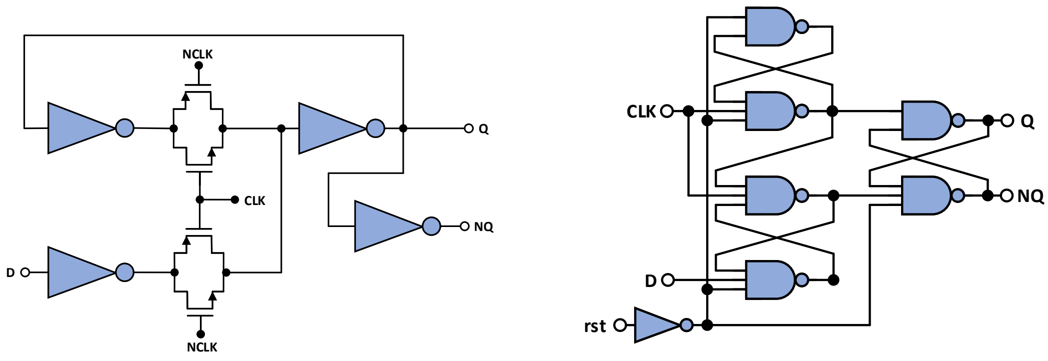
*Only applied to the circuit shown in fig.4.2b.

Table 4.1: Truth table of the flip-flop circuit.

RST*	CLK	Q	NQ
0	0	D(n-1)	$\bar{D}(n-1)$
0	1	D(n)	$\bar{D}(n)$
1	↑ or ↓	0	1

4.1.3 Phase Generator

To achieve the a half clock detection the circuit need a more complex phase generator, compared to the usual dual-slope ADC (2.1), bearing this in mind, a phase generator



(a) (b)

Figure 4.2: Schematic of two flip-flop circuits studied. (a)Faster NOT gate based latch; (b)NAND based flip-flop.

divided in two parts was designed for this implementation.

The first part, presented in figure 4.3, which controls and separates the charge from the discharge phase. This phase will be generated by a 3-bit counter, being the most signification bit, the one that separates the 8 clock-cycle counting into two parts. To achieve the half clock cycle, it was used a flip-flop with a inverted clock cycle, resulting in a delay of half a clock cycle after all the digital counter bits are at 1 (D_0, D_1, D_2=1), corresponding to the 7 value (111), value that is achieved at the end of the third clock cycle, corresponding to 3.5 clock-cycles.

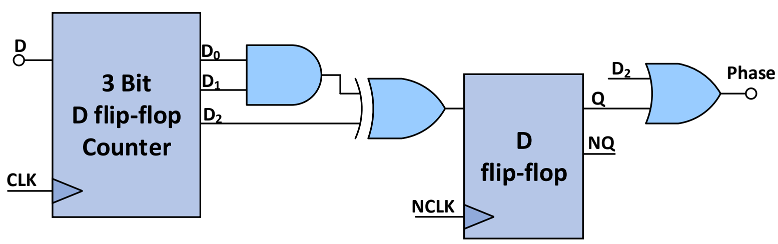


Figure 4.3: Phase Generator.

Although having the separation of charging as discharging phases is the main goal of the phase controller, there was also needed a way to control the discharging phase, a factor very relevant due to the use of the noise shaping capabilities from the circuit. It was designed and added a new controller presented in figure 4.4 only destined to separate the discharging slope phase and the sample phase.

Initially, the direction of the integrators output V_x from the start of the discharge phase is held in a flip-flop and compared to the current direction of V_x, if the two values differ, means that the discharging slope as crossed the central voltage, $\frac{V_{DD}}{2}$, entering the sample phase. Having the discharge phase synchronous with the inverted clock signal, a flip-flop was added do obtain the signal desired, namely $Phase_2$, as presented in figure 4.4. The synchronization with the inverted clock signal will ensure that the sample phase always exist in each conversion cycle and each one is performed in 8 clock-cycles.

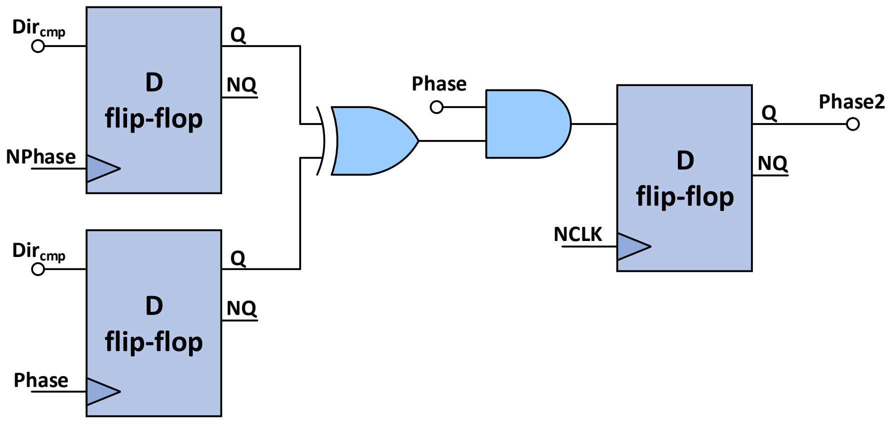


Figure 4.4: Discharge Phase Controller.

With the digital circuits presented in 4.3 and 4.4 it was possible to control the integrator phases, based on the output (V_x) as presented in figure 4.5.

Although presenting a separation between phases, as expected, each phase has a delay compared to the clock signal as a consequence of the propagation time of the logic circuits related to the technology used, as well as the inherent delay of the PMOS compared to the NMOS transistors and the comparator threshold. With these limitations resulted in less then 0.1 ns delay for the first phase and 0.4 ns for the second phase.

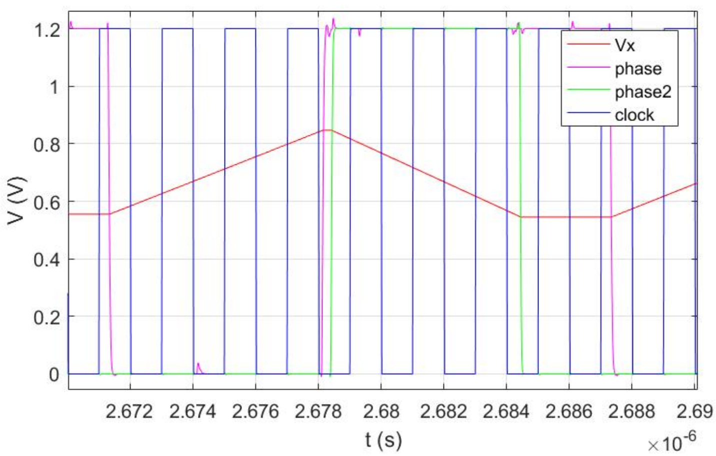


Figure 4.5: Phases generated based on the V_x value.

4.2 The StrongARM Latch Comparator

Following the StrongARM proposal reported in [10], by Yun-Ti Wang, used as the comparator, a further study was made in 2015 in [11], by Behazad Razavi, analysing the operation, offset and noise of the circuit, adding a buffer and a SR Latch.

Based on the Cadence® simulations of the StrongARM latch topology presented in [10], the sizing of PMOS and NMOS was dimensioned and is shown in figure 4.6, with the addition of a buffer and SR Latch to be used as a comparator presented in figure 4.7.

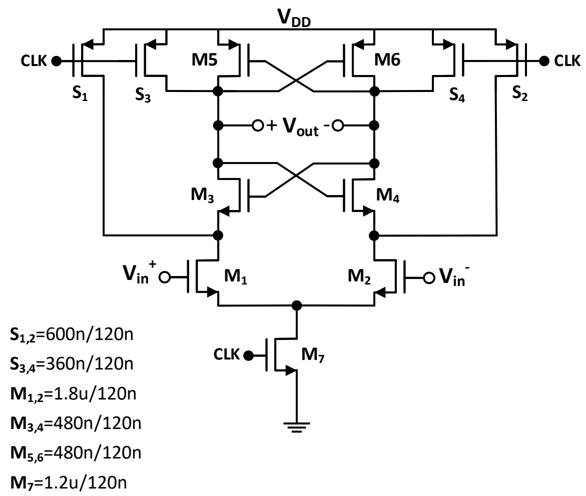


Figure 4.6: StrongARM latch (using a CMOS 130) with W/L dimensions shown.

The StrongARM latch presented in figure 4.6 works by comparing the input values, V_{in}^+ and V_{in}^-, when a CLK signal is received (↑CLK), resulting in V_{out}^+=V_{DD} when V_{in}^+>V_{in}^- and V_{out}^+=0 V for the remaining input values, maintaining output value while CLK=1. When CLK=0, output takes the positive digital value (V_{out}^+=V_{DD}), regardless of the input value, this state can be seen as an idle state, where the circuit is inactive, having the consumption almost nullified.

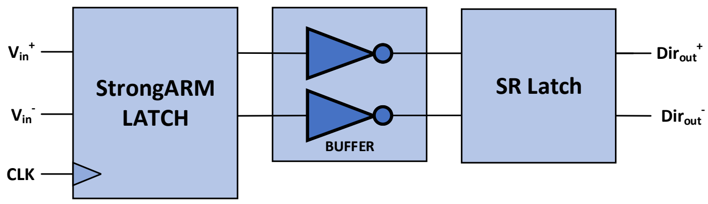


Figure 4.7: StrongARM latch using a SR latch and a buffer stage in the between.

The buffer and SR latch presented in figure 4.7 are responsible of maintaining the StrongARM comparison value during the inactive state, value that is the comparator output.

To test the behavior of the StrongArm latch, a Cadence® simulation was made using the circuits presented in figures 4.6 and 4.7, with the $V_{in}^{+}=\frac{V_{DD}}{2}$ and V_{in}^{-} being a variable input, as a result, the circuit presents a delay under 0.15 ns as presented in figure 4.8.

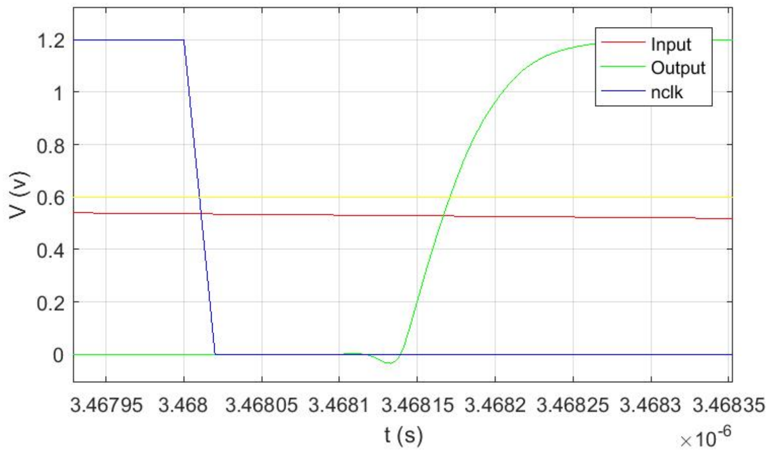


Figure 4.8: Response of the StrongARM latch using a SR latch and a buffer stage with a variable input, a $\frac{V_{DD}}{2}$ threshold voltage (0.6 V) and an inverted CLK signal.

4.3 The Double-Speed Quantizer circuit

Although the Double-Speed quantizer has been presented as a technique to improve the Dual-Slope quantizers speed, it also decreases the power efficiency of the circuit with the addition of two comparators. In order to improve the power efficiency of the proposed solution, without affecting the behavior presented in the table 3.1, it was used a StrongARM comparator with additional logic, as presented in figure 4.9, being the CLK signal of the StrongARM the sample phase of the quantizer.

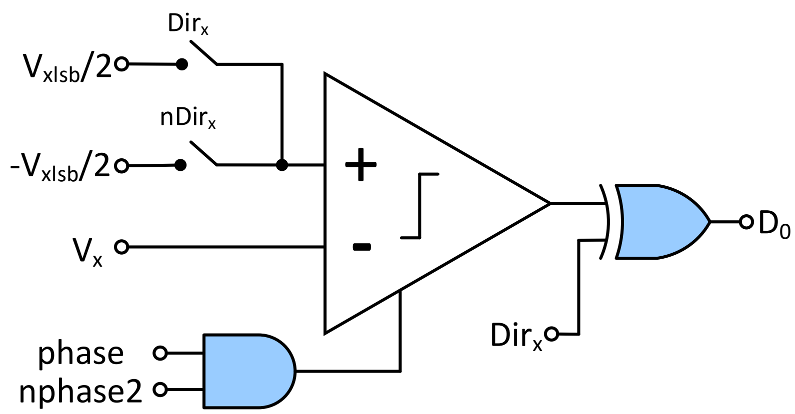


Figure 4.9: The Double-Speed quantizer solution.

4.4 Simulation Results

Due to the response time of the circuit not being capable of working properly at 2.1 GHz f_{clk}, the circuit has been dimensioned for a 0.5 GHz f_{clk}. The following parameters have been used in the electric simulations:

- Input frequency of f_{in} = 250 kHz;
- Maximum input amplitude of 0.295 V;
- Reference voltage V_{ref} = 0.3 V;
- BW = 3 MHz;
- f_{clk} = 0.5 GHz;
- $R = 6\,\text{k}\Omega$;
- $C = 1$ pF.

It was used a sine wave with a frequency of 0.25 kHz, with a clock frequency of 0.5 GHz, with 8 clock-cycles per sample phase, as explained previously in 3.1. With all this information the resulting maximum sampling frequency can be obtained using the equation 4.1.

$$f_{sampling} = \frac{1}{8 \times \frac{1}{2} \times \frac{1}{f_{clk}}} = 125MHz \tag{4.1}$$

Resulting in an OSR of 87.5 as a result of equation 4.2.

$$OSR = \frac{f_{sampling}}{2 \times BW} \approx 87.5 \tag{4.2}$$

In order to achieve twice the conversion-rate, with the 2-bit quantizer, the LSB voltage value ($V_{x_{lsv}}$) correspondent to the integrator output and scale (V_x) must be obtained again, due to the use of different parameters RC when compared to the chapter 3 values. The value can be obtained through the expression 4.3.

$$\frac{V_1}{2} = \frac{V_{x_{lsv}}}{2} = \frac{V_{ref}}{2 \times F_{clk} \times R \times C} = 50mV \tag{4.3}$$

As a result of the simulation presented in figure 4.10 the conversion presents quantization problems when the input values are near the central value, $V_{in} \approx 0V$, problems represented as a variation of the direction as well as a bad quantization.

$$|q_e(n-1)| > |V_{x_{lsv}} \times t_{charge}| \tag{4.4}$$

As presented in expression 4.4, a bad quantization occurs when the quantization error (q_e) of the previous conversion ($n-1$) is higher than the total input integrated value of the charging phase, resulting in a deviation of the direction of V_x which will result in the expected crossing of the central value ($\frac{V_{DD}}{2}$) not happening and counting being done until the end of the discharging phase as presented in figure 4.10.

As a solution for this problem the half LSB can be considered, raising the charging output value, but couldn't be implemented due to problems and limitations while conceiving the integrator.

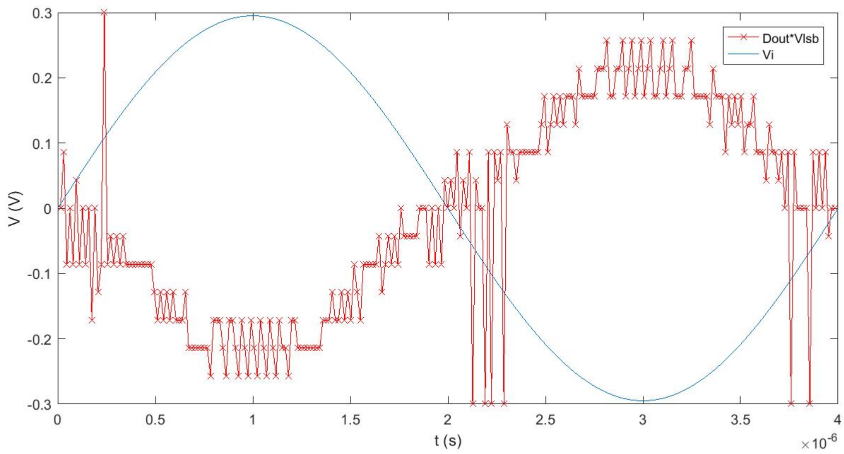


Figure 4.10: NSIQ Double-Speed input compared to the output $V_{out}(D_{out} \times V_{x_{lsb}})$.

4.5 Zero-Crossing-Based (ZCB) integrator

For the integrator, although the results presented below were not acceptable for the clock frequency used, this configuration was considered and tested to be used as integrator in the implemented NSIQ circuit.

The circuit designed relies on a single input ZCD based on one of the architectures studied by Matthew C. Guyton [12] in his PhD thesis in Electrical Engineering and Computer Science. In his work, it was simulated in Simulink a Sigma-Delta modulator ($\Sigma\Delta$), using a differential implementation of the ZCB integrator reaching a 14 bit ENOB with a 5 kHz input.

Some examples of use of this integrator is in the pipeline ADC architecture presented in [12], previously mentioned, as well as, in [13], by Lane Gearle Brooks, which also uses a fully differential version of the circuit in each stage of the ADC reaching near 10 bit ENOB at 50 MHz sampling frequency.

For this example was simulated a version of this integrator dimensioned for some of the specifications of the NSIQ presented in figure 4.11.

This concept consists on a sampled integrator which the output values are only gathered at the sample phase, once per clock-cycle, a factor well suited to discrete time circuits whose values are only gathered at certain instants, circuits such as, ADCs.

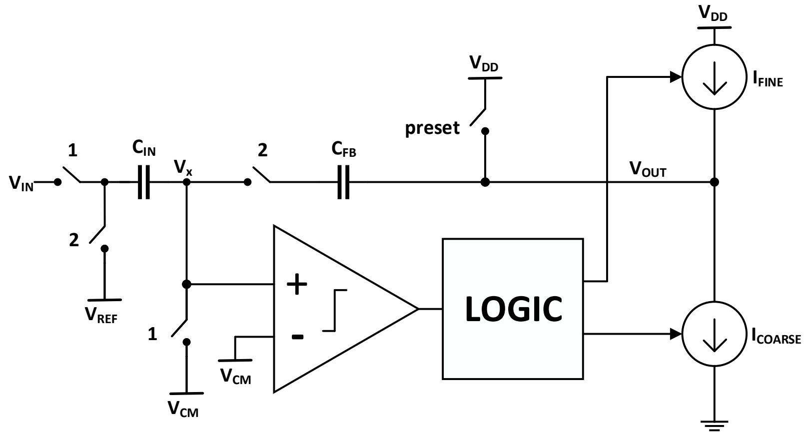


Figure 4.11: Schematic of the Zero-Crossing-Based Integrator presented in [12].

The behavior of the circuit is described in figure 4.12, and it is divided between two main phases, the input sample phase (phase 1), where the input value (V_{in}) is charged in the capacitor C_{in} and the compared value (V_x) set to V_{CM}, and phase 2 where the input value, proportional to the charge on C_{in} is integrated.

The second phase is divided in four phase in four phases, being the first one, the preset phase (P) where the output value (V_{out}) is set to V_{DD} and the capacitor C_{FB} charged with a value dependent of the input, V_{CM}, from phase 1 charge, and V_{DD}, also increasing the V_x value. In the coarse phase the capacitor is discharged based on the coarse current I_{coarse} until V_x reaches the V_{CM} value creating an overshoot due too the circuit response delay. To compensate this overshoot the capacitor C_{FB} is charged with a current (I_{fine}) in the fine phase. Having the V_{out} value set, the circuit enters in the samples phase (S) where the value can be sampled in a register.

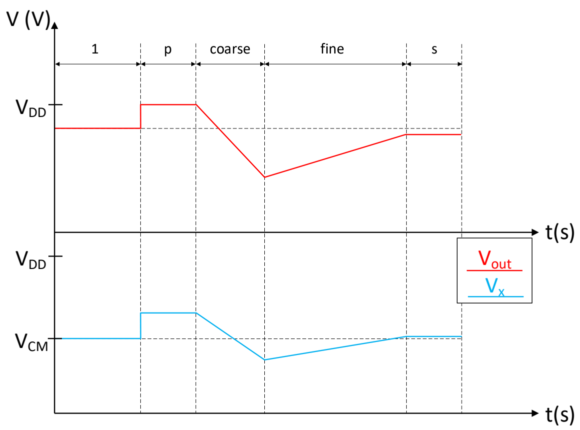


Figure 4.12: ZCD integrator behavior V_{out} (above) and V_x (below) for each phase.

4.5.1 Integrator Simulation Results

The simulation has been performed using a V_{in} sine wave with 1MHz f_{in} centered in $\frac{V_{DD}}{2}$ with 200 mV of amplitude an the parameters presented:

- f_{clk}=100 MHz;
- V_{CM}=350 mV
- V_{ref}=600 mV;
- C_{in}=1 pF;
- C_{FB}=2.5 pF;
- $I_{coarse} = I_{fine} \times 8$=80 μA.

All the values presented previously where obtained from expressions presented in the document [12], to get the V_{CM}, C_{in} and C_{FB} values, and the slope equations following the ones used in the document [14] written by Sadegh Biabanifard, Toktam Aghaee and Shahrouz Asadi, as a guide to design a ZCB integrator.

Presented in figure 4.13 the output has a sinusoidal pattern similar to a cosine wave, as can be seen in the sampled results which represents the discrete-time domain integral of a sine wave signal, V_{in}, although with a increase in amplitude.

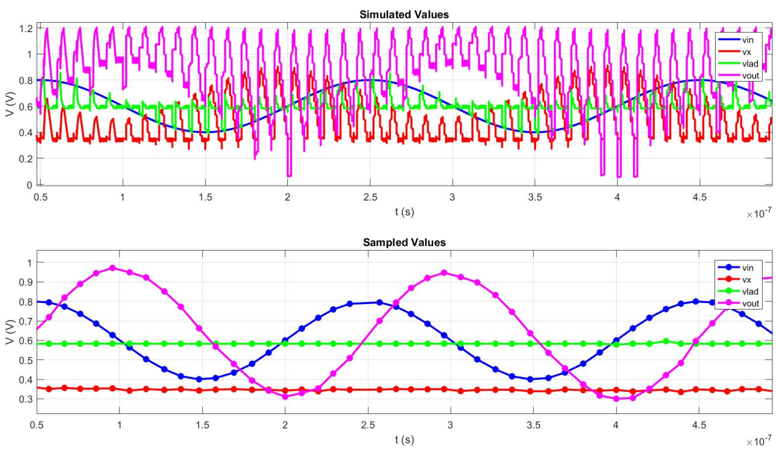


Figure 4.13: ZCD integrator input (V_{in}), output (V_{out}) and node voltages (V_x and V_{lad}) simulation (above) and the sampled values ou each voltages (below)

4.5.2 Zero-Crossing-Based (ZCB) integrator analysis

Following the research done for this thesis in the ZCB topologies including the ZCD architectures, and with the integrator simulation results presented previously in figure 4.10, the architecture, appears to be very acceptable for the input parameters it was designed to work, having an amplification value near ideal ($\frac{V_{out}(Max)}{V_{in}(Max)}$=1) and the result being centered in 0.6 V (output threshold = 0).

Despite of these results, the bigger problems dimensioning the circuit occurred when the clock speed was increased, presenting a saturation of the output due to an added output threshold not accounted for in the performed calculations, a bigger amplification than expected has been noted, and the stability of the output value being very related to each phase active time. Further investigation should be done to implement this integrator in the Dual-Slope quantizer.

As a discrete integrator circuit, when designing the ZCB integrator, the Nyquist Sampling Theorem [15] as to be taken into account, which states that a continuous-time signal can be sampled and reconstructed if $f_{sampling} > 2 \times f_{in}(max)$. Following Nyquist Sampling Theorem [15], the Dual-Slope ADC presented is also a discrete-time circuit, which, considering a sampling period taking 8 clock-cycles, the CLK rate would be $f_{clk_{ADC}} > 2 \times f_{in}$, and the sample rate of the integrator $f_{clk_{int}} > 2 \times f_{clk_{ADC}}$, and considering that in section 4.5 the presented circuit has been dimensioned to $f_{clk_{ADC}} = 0.5GHz$, the integrator would need to work at, at least 1 GHz, in ideal condition, but a more reasonable value would be at least 2 GHz not being an ideal circuit. The integrator dimensioned presents reliable results for with a 100 Mhz sample-rate, it is a ratio of at least 20 between the wanted rate and the obtained one which prevented the use of this integrator.

Chapter 5

Conclusions and Future Work

The initial goal of this thesis was to create noise shaping integrator quantizer using a Double-Speed quantizer, by analyzing the quantization error, coming from noise shaping properties of the circuit in order to double the conversion rate of this dual slope ADC. To achieve this goal it was planned to divide the work in many phases, the initial being, to modulate the circuit in Matlab® with a 0.3 V reference voltage and $V_{in_{max}}$, to obtain a 10 bit ENOB, from a 4-bit the Dual-Slope A/D proposed, lead to a Cadence® design and simulation as well as the creation of a layout and, eventually, a physical product, but some problems occurred during the thesis. First, some delays on the proposed schedule due problems in the access of the software followed by problems and delays designing the circuit and an overall misdirection on the project which led to the accomplishment of part of the goals.

The second chapter presented the existent topologies for the Dual-Slope, all the formulation associated, the detailed explanation of each topology, as well as, the added features to improve the performance of the ADC, the associated calculation, all the schematics and the expected results.

In the third chapter the new concept was presented, explained and the results of the Matlab® modeling obtained. Many techniques where used to further increase the resolution of the ADC, such as the noise shaping in the Dual-Slope ADC which is the major technique used in this study. This because, of the Double-Speed quantizer requiring this technique to be used, alongside the 3.5 clock-cycle period of the charging phase to simulates the behavior of a 7 clock-cycle. The half LSB compensation was also used to further increase the resolution (ENOB in particular) of the quantizer, while decreasing the output (V_{out}) when compared to the input (V_{in}). The use of a bi-directional circuit previously explained in the second chapter and the addition of a IIR filter were also techniques used to further increase the conversion rate and the ENOB, respectively, resulting in the modeling reaching 9.7 bit ENOB while not using the half LSB compensation, and 10.2 bits of ENOB when the compensation was added. A spectral analysis of the power spectral density was made for each case which provided an harmonic value decrease when the filter was applied. This modeling can be considered a success.

The fourth chapter was destined perform a circuit design as well as an electric simulation in the software Cadence®, using the CMOS 130nm technology, with different input parameters, when compared to the third chapter. The digital circuit was presented in detail as well as the schematic of the logic gates used, being presented afterwards, the simulation results and the problems detected. The power consumption of the circuit was taken into account when designing the Double-Speed quantizer, leading to a redesign of this circuit. The ZCB integrator, although not achieving the results needed for the implementation, still presents many advantages over the remaining integrator implementations, being the power consumption and the size some of them, with further research the circuit could certainly be implemented on a Dual-Slope quantizer.

Although not achieving the best results due to numerous problems it was possible to research new approaches to this topology and create new techniques.

5.1 Future Work

This concept brings a great improvement to the A/D converters topologies, in particular the NSIQ, but many more studies should be made in this regard. As a suggestion, he directional bit of the circuit should be obtained from the input value (Dir_{in}), instead of the integrators output direction (Dir_x), this implementation although leading to the use of an additional comparator to identify the input polarity, affecting the power efficiency, and will possibly correct the quantization problems verified in the simulations. Further research should be made in the zero-crossing-based integrator, being a discrete, low power integrator when compared to an Op-Amp base integrator, being capable of reaching tinier and faster implementations than the Op-Amp without stability issues, with high accuracy as well.

After having this concept matured, the best path to follow for a future work is the use of tinier CMOS technologies, the use and circuit adaptation for faster clock signals, and the study of the power efficiency of the circuit as well as techniques to increase it.

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Appendix A

Matlab® modeling code

The code presented is based of the João Sousa Marters thesis [6].

A.1 NSIQ double speed

```
  function [integ_vref, integ_out, integr_pos_array, i_Dout ,Dir, Dout_dec] =
=NSIQvx2(VLSB2_adding,Vin,pulse,np,clk_integ,Aref,fsampling,Rin,C,Req,C2,R2)
      Ts=1/(fsampling);
      fsampling;
      Vref=Aref*ones(1,np);
      integ_out=zeros(1,np);
      Integr_pos=1;
      clk_count=0;
      k=1;
      Rdis=Rin;
      endphicharge=1;
      Dir(1)=3;
      integ_vref=zeros(1,np); %Vref integration
      countmax=0;
      count=0;
      count_aux=0;

      for i=2:np
       clk_changed=0;
       switch Integr_pos
        case 0
```

```
  integ_out(i)=integ_out(i-1);
 case 1 %charging
  if(VLSB2_adding==0) %without compentation
   integ_out(i)=integ_out(i-1)+Ts*Vin(i)*(1/(Rin*C));
  else %with compentation
   if(Dir(endphicharge)==1) %positive vin
    integ_out(i)=integ_out(i-1)+Ts*Vin(i)*(1/(Rin*C))-Ts*Vref(i)*(1/(Req*C));
   else %negative vin
    integ_out(i)=integ_out(i-1)+Ts*Vin(i)*(1/(Rin*C))+Ts*Vref(i)*(1/(Req*C));
   end
  end
 case 2 %discharging
  if(Dir(endphicharge)==1) %positive vin
   integ_out(i)=integ_out(i-1)+Ts*Vref(i)*(1/(Rdis*C));
  else %negative vin
   integ_out(i)=integ_out(i-1)+Ts*-Vref(i)*(1/(Rdis*C));
  end
end
integr_pos_array(i)=Integr_pos;
Dir_array(i)=Dir(endphicharge);

if(pulse(i)~=pulse(i-1))
 clk_changed=1;
 clk_count=clk_count+0.5;
end

if(clk_count==clk_integ && Integr_pos==1)
 Integr_pos=2;
 clk_count=0;
 endphicharge=endphicharge+1;

 if (integ_out(i)<0)
  Dir(endphicharge)=0;
 else
  Dir(endphicharge)=1;
 end
 count=0;
 continue
end

if(Integr_pos==2 && clk_changed==1)
```

```
    count_aux=count_aux+1;
   end

   aux=(integ_out(i)<=0 && Dir(endphicharge)==1)||(integ_out(i)>=0
   && Dir(endphicharge)==0);

   if(clk_changed==1 && Integr_pos==0 && clk_count==4.5)
    Integr_pos=1;
    Dout_dec(k)=Dout_count;
    i_Dout(k)=i;
    k=k+1;
    clk_count=0;
    continue
   end

   if(aux && Integr_pos==2 && clk_changed==1 && count_aux==2)
    Integr_pos=0;
    count_aux=0;
    clk_count;

    if((integ_out(i)<=64*Ts*Vref(i)*(1/(C2*R2)) && Dir(endphicharge)==1)||
    (integ_out(i)>=-64*Ts*Vref(i)*(1/(C2*R2)) && Dir(endphicharge)==0))
     Dout_count=clk_count*2-1;
    else
     Dout_count=clk_count*2;
    end
    continue
   end

   if(count_aux==2)
    count_aux=0;
   end

   if(count>countmax)
    countmax=count;
   end
  end

  clear Dir
  Dir=Dir_array;
 end
```

Annex I

Cadence® Circuit

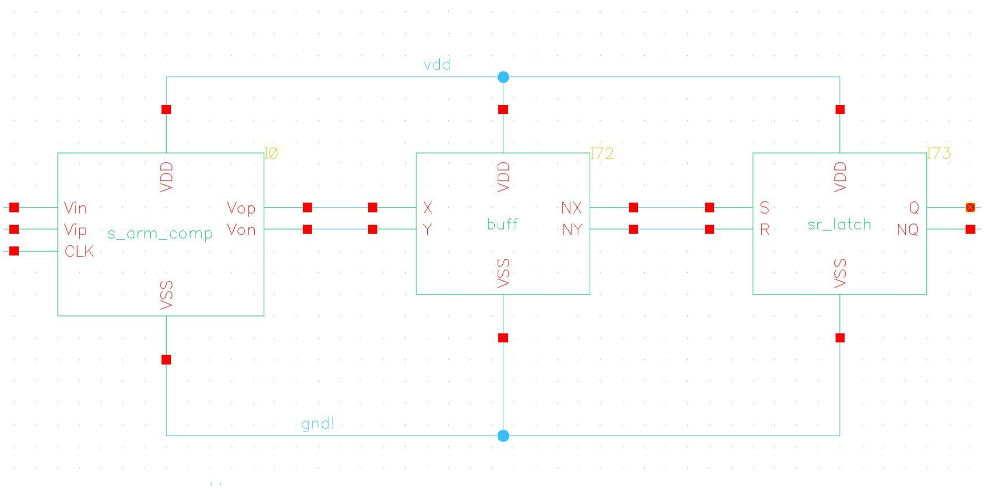

Figure I.1: Strong Arm Cadence

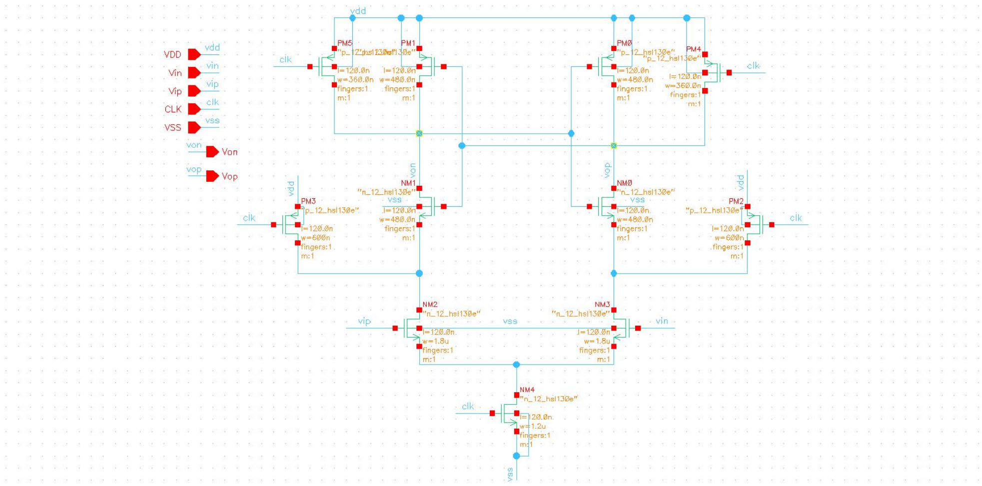

Figure I.2: Strong Arm Circuit Cadence

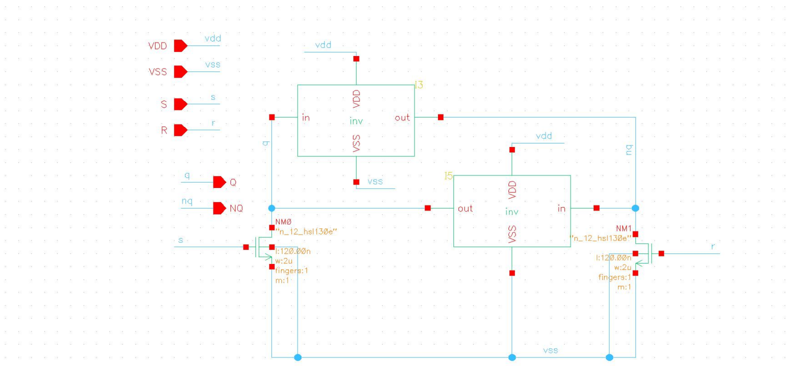

Figure I.3: Strong Arm Cadence

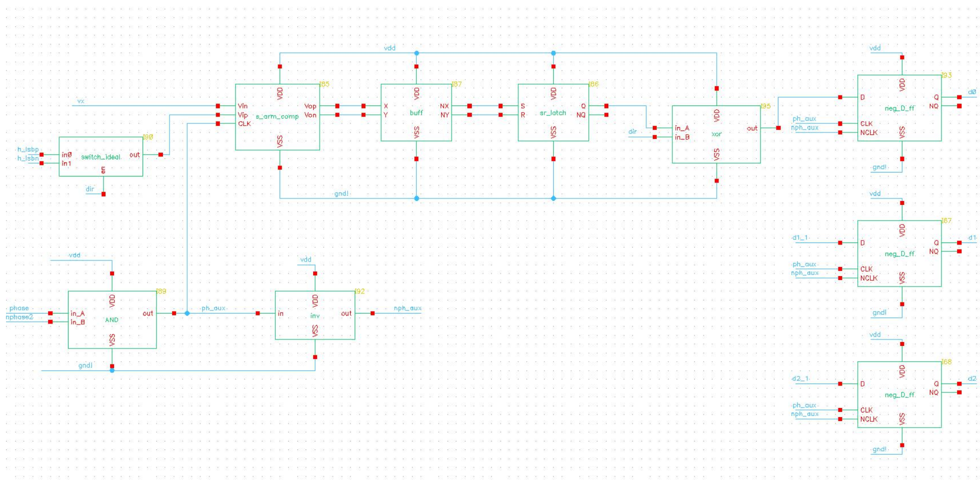

Figure I.4: double speed quantizer Cadence

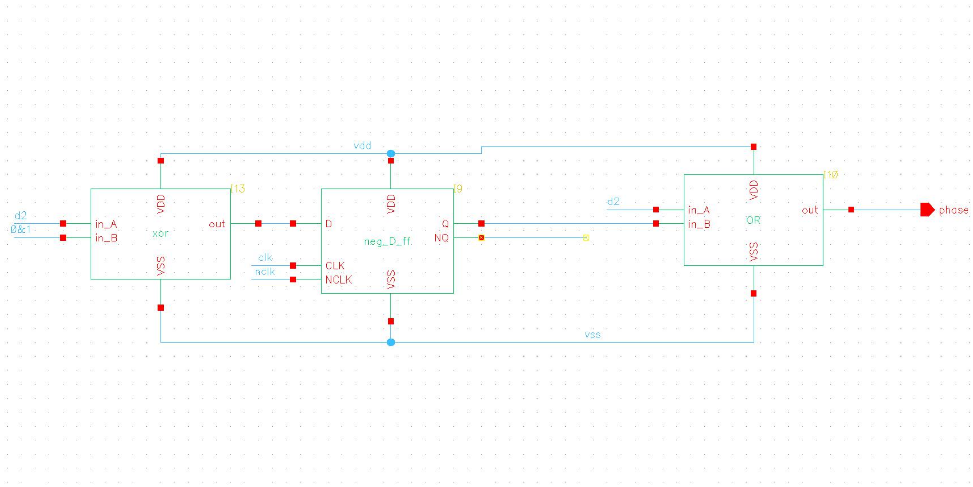

Figure I.5: phase generator Cadence

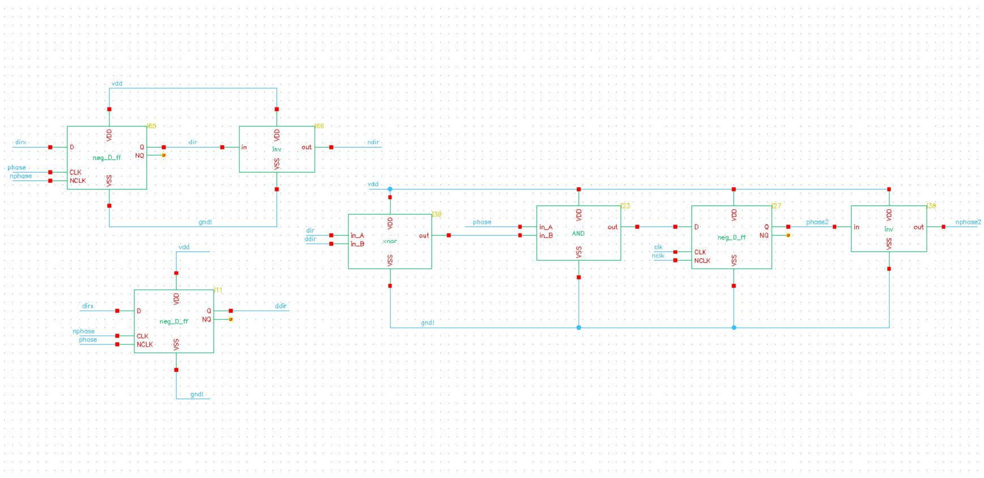

Figure I.6: phase2 generator Cadence

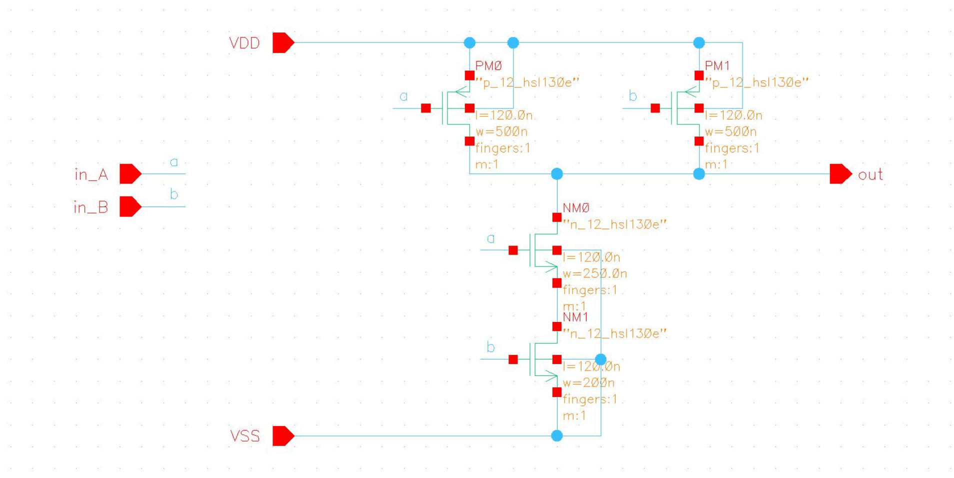

Figure I.7: Nand logic gate Cadence

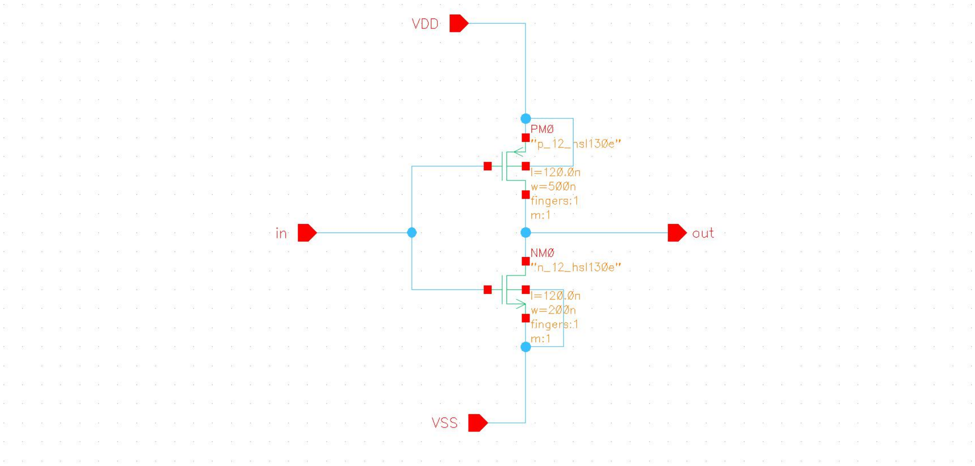

Figure I.8: Not logic gate Cadence

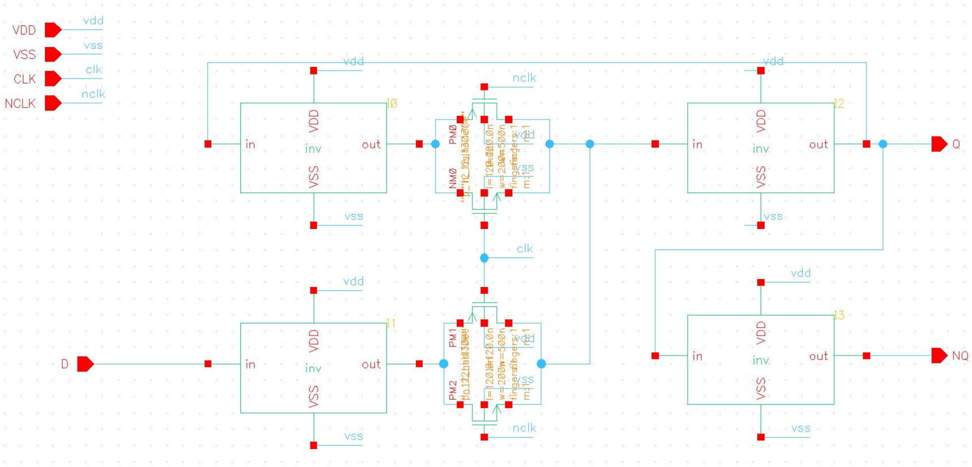

Figure I.9: D flip-flop Cadence

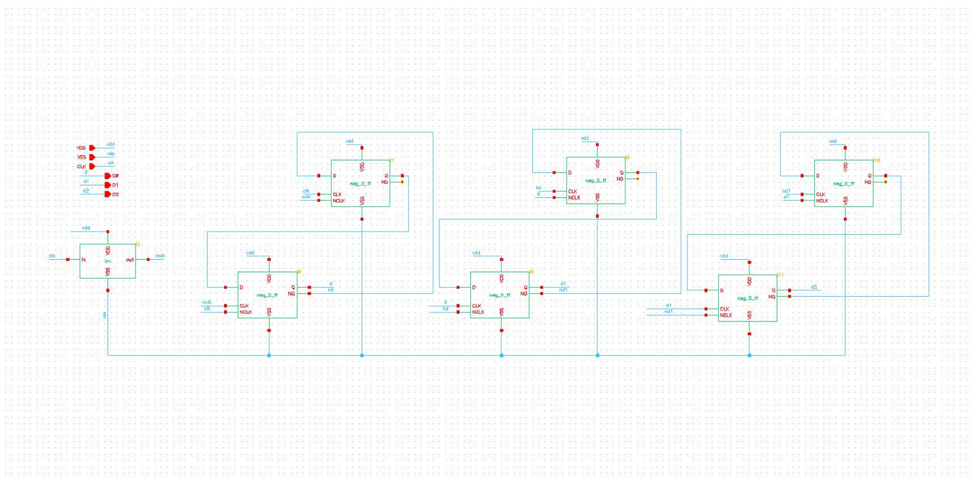

Figure I.10: D flip-flop counter Cadence

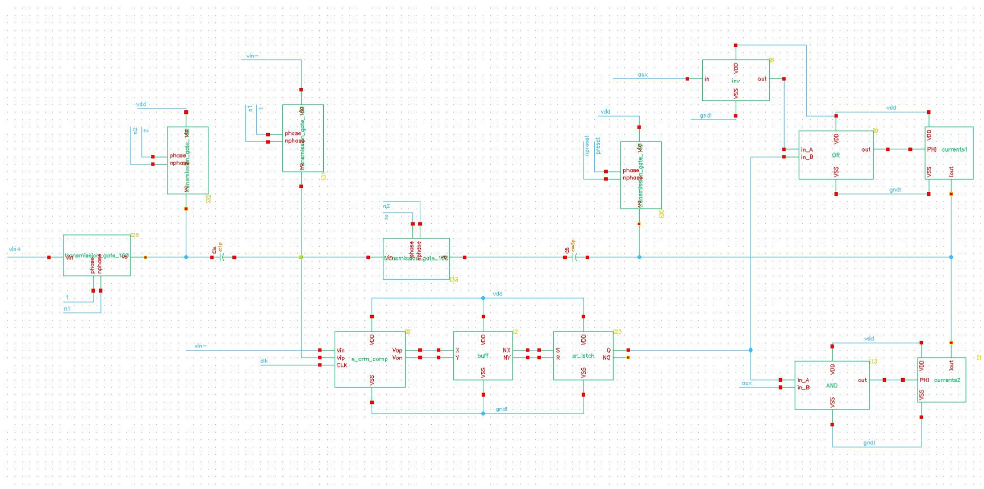

Figure I.11: ZCD base integrator Cadence

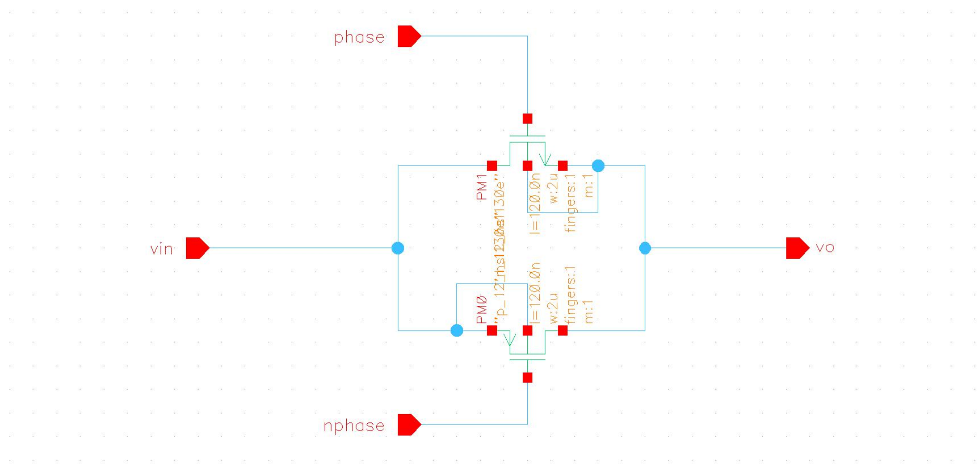

Figure I.12: Switch implementation Cadence