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3D Interconnection by FIB Assisted Pt Deposition and Electroless Nickel Deposition on the Sides and Edges of an I-Seed

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Abstract

This paper reports on the development of a 3D interconnection process leading to the successful assembly of a five-layer 3-D 1mm cube module. This proof of concept module demonstrates the capability for successful integration and interconnection of commercial off the shelf components to fabricate functional modules in 1mm cube dimensions. It also demonstrates that use of established volume scale technologies like Flip-chip, dicing and patterning techniques are viable for fabricating these 1mm modules. The demonstrator consists of LED's bonded to the six sides of the 1mm cube, interconnected and powered up. The work will particularly report on two different processes to fabricate the interconnection pattern using direct Focused Ion Beam (FIB) assisted Pt deposition and electroless metal deposition, which again patterned by FIB. Uniform thickness of the deposit and excellent coverage on all six sides is achieved by electroless nickel deposition. Voltage current characterisation of the deposited Pt shows a resistivity value of 1864 ± 100 μΩ cm, whereas electroless Ni film shows a resistivity of 25 μΩ cm due to boron inclusion. 100 nm Au layer is deposited by chemical displacement reaction to enhance the conductivity and solderability of the film.

Introduction

This proof of concept module demonstrates the capability to provide interconnection solutions for 1mm functional intelligent seed (I-Seed) [1-3]. The I-Seed is Tyndall National Institute's specification for future autonomous transducer nodes in the ubiquitous computational networks that will drive the vision of Ambient Intelligence. 3D interconnection and integration of functional bare die devices is a key target in achieving the I-Seed.

In the first phase, we have successfully developed 3D integration technologies including processes, which includes techniques to enable free stacking of thinned bare die silicon in 1mm cube form factor. We have also investigated the 3D integration and assembly sequences through test vehicle development, primarily (in this phase) using daisy chain patterns to interconnect stacked bare die silicon. The interconnection for the five-layer stacked silicon is completed using Focused Ion Beam assisted Pt deposition technique. In the second phase, we have connected light emitting diode (LED) to the patterned cube, which would prove the concept of 3D functional integration of five layer stacked bare silicon die. The outcome of these investigations paves the way for new 3D integration techniques that can be adopted for the fabrication of I-seed using various bare die devices, including sensors.

Experimental

We have developed two different processes to fabricate the 1mm cube module. For both the processes the initial work on the development of 1mm cube is same. Initially, five 10 × 10 mm^2 square die are diced from an oxide coated silicon wafer of standard thickness and then thinned to 180 μms each. A composite five-stack block is then formed by flip-chip alignment and joining of each layer with a thermally cured layer of non-conductive adhesive fill. The 10 × 10 × 1 mm^3 composite cube is then diced into 1 × 1 × 1 mm^3 cubes.

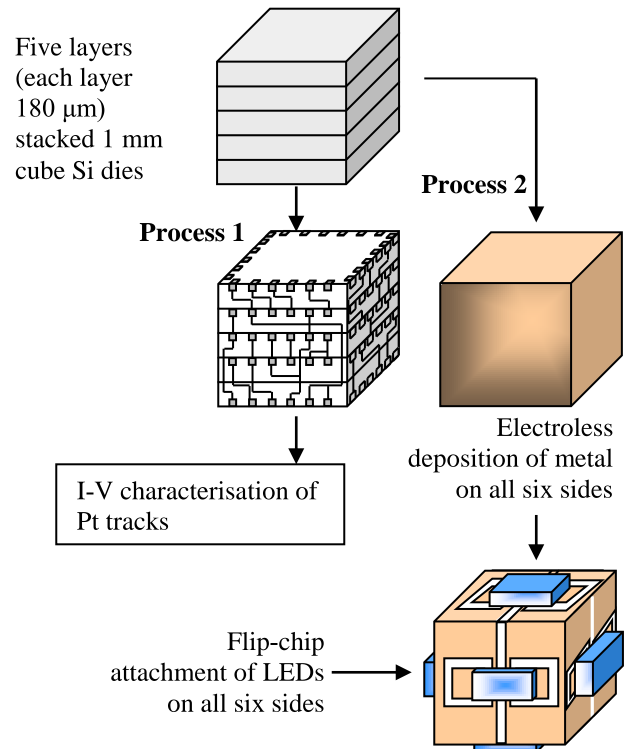

Fig. 1. Different Fabrication process flows of 1mm cube module

Process 1

Arrays of 20 × 20 μm^2 pads have been deposited to a thickness of 0.1 μm using FIB assisted Pt deposition technique on all six sides of 1 mm cube module as shown in Figure 1. Tracks are deposited to connect the pads, which have a dimension of L × 20 × 0.1 μm^3, where the tracks have variable lengths. FEI Vectra 200DE, 30keV Ga ions, 10 nm nominal spot diameter FIB system is employed for imaging, and direct-writing of electrical tracks between the pads as

shown in the schematic of Figure 1. All tracks are fabricated under the same experimental conditions.

Process 2

In the process 2 development phase, the cubes are oxide coated using Plasma Enhanced Chemical Vapour Deposition Techniques (PECVD) with the deposition thickness in the range of 500 to 1500 nm. Next the cubes are electrolessly plated first with nickel, then with a gold finish. Electroless nickel deposition is based on the reduction and deposition of nickel ions from a solution to a surface in the absence of an external electric source. The process is autocatalytic and requires the immersion of a catalytically activated surface into a plating bath containing a reducing agent and complexed nickel ions. A significant advantage of electroless nickel deposition is its ability to produce deposits with uniform thickness on substrates with complex geometries and shapes. Given that this reaction is chemical in nature, any catalytic surface exposed to the plating solution will plate uniformly. The current density effects typically associated with electroplating do not arise, therefore sharp edges readily plate to uniform thickness. Since its inception by Sullivan et al [7], electroless deposition of nickel at silicon surfaces has gained increasing application in the silicon industry for contact metallisation, via-hole filling of ICs and fabrication of metal microstructures in MEMs [8]. In the present work, we have demonstrated the electroless deposition of a nickel film at all six faces and edges of a PECVD coated, 5 layers stacked, 1 mm^3 silicon cube. The film is deposited from a commercial nickel plating bath Niposit 468 using dimethylamine borane as a reducing agent. The electroless nickel boron alloy (Ni-B) deposited is harder as plated and exhibits superior wear and corrosion resistance over those deposited from nickel phosphorous baths. In addition, the low B content incorporated in the nickel film (ca. 0.3 %) provides a low resistivity coating. The specific resistivity of the Ni-B film is 25 μΩ cm, while that of pure Ni is 6.84 μΩ cm.

The PECVD coated silicon cube was firstly pre-treated in four steps in order to render its surface catalytically active for deposition:

Solvent degreasing

Etch in 1:1 H_2SO_4: H_2O_2

Etch in 20% (v/v) HF

Sensitisation and activation with acidified solutions of $SnCl_2$ and $PdCl_2$

The activated cube is then immersed in the Niposit 468 bath for 8 minutes at pH 7 at 65°C.

To optimize solderability of the nickel film and prevent its oxidation a thin layer of immersion gold (ca. 100 nm) is deposited at its surface using an Ormex gold bath operating at 90 °C at pH 5.2 for 10 minutes. The chemical displacement reaction involved is driven by the electrochemical potential difference between gold and nickel and ceases when all the surface nickel has been replaced with gold. After the deposition process, N and P contact poles and pads are subtractively pattern generated using a Focused Ion Beam (FIB) tool.

LEDs are used to demonstrate functionality of 1mm cube module. The N and P contact pads of a 95 μm thick and 375 × 325 μm^2 square LED have solder dispensed using an Ink Jet tool. Two 40 mm high and 80 mm diameter solder bumps are printed onto the LED's by the Jetlab II printing system. The LEDs are flip chip aligned and reflowed onto the cube faces, and probe power tested to illuminate. A working demonstrator has been successfully assembled. The interface layers between two bare die were investigated using Scanning Acoustic Microscope (SAM) and Optical microscope. The pattern and the uniformity of the nickel film and gold finish was further investigated using Scanning Electron Microscope (SEM). The current-voltage (I-V) characteristics of FIB assisted Pt tracks and gold finished tracks are investigated using HP precession semiconductor parameter analyzer model 4156A.

Results and Discussion

Initial characterisation of these cubes using optical microscopy and SEM shows that the thicknesses of the layers vary between 6-10 μm and as a result the overall dimension of the module varies. Scanning Acoustic Microscope shows that the adhesion quality between layers is very good. There are small voids present (white regions marked with red cross) as can be observed from the SAM image analysis of Figure 2. These voids are eliminated using a higher pressure during flip-chip process and by curing the epoxy with a curing temperature of 180 °C for 1 minute.

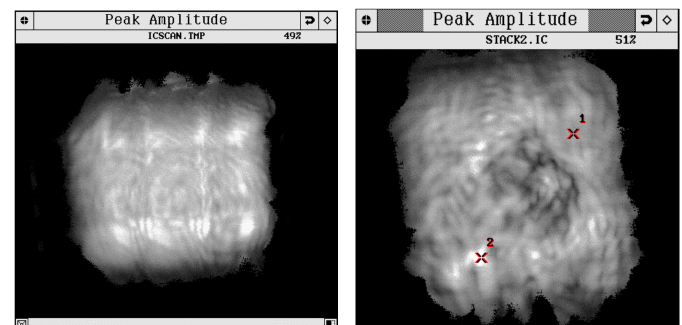

Fig. 2. Scanning Acoustic Microscope image showing voids present in the interface layer.

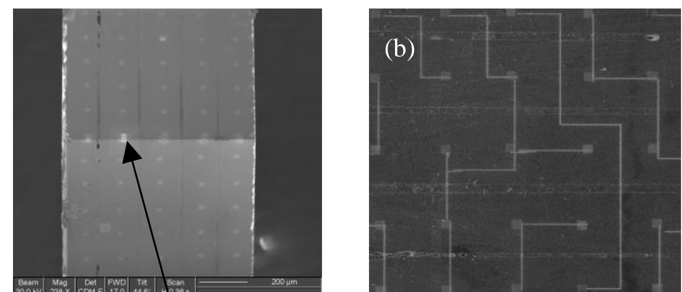

Fig. 3. (a) FIB image showing edge after pattering with platinum where platinum also deposited on the edge; (b) Daisy chain structures connecting pads on different layers.

Figure 3 shows the five layers stacked cube that is patterned with FIB assisted Pt deposition and the layers are connected with Pt tracks. Each of the layers in the cube may be considered as a functional bare die device that needs to be

connected with each other, that is with another layer as shown in the process 1 of Figure 1. Focused Ion Beam image of the edge shows patterned pads on the edges as in Figure 3(a). Figure 3(b) shows daisy chain pattern connecting the pads on the side walls of 5 layers stacked bar die silicon.

The current voltage properties of FIB patterned Pt metal tracks that make the daisy chain pattern to connect the stacked Si layers are characterised. The resistance of the different tracks are measured and plotted in Fig. 4, where the inset of Fig. 4 shows the room temperature current-voltage characteristic of a 326.7μm long FIB patterned track, with a cross-sectional area of 2μm^2 is presented. The resistivity of FIB-written Pt wire is extracted from the slope of the linear fit of Fig. 4. . The linear fit demonstrates ohmic behavior

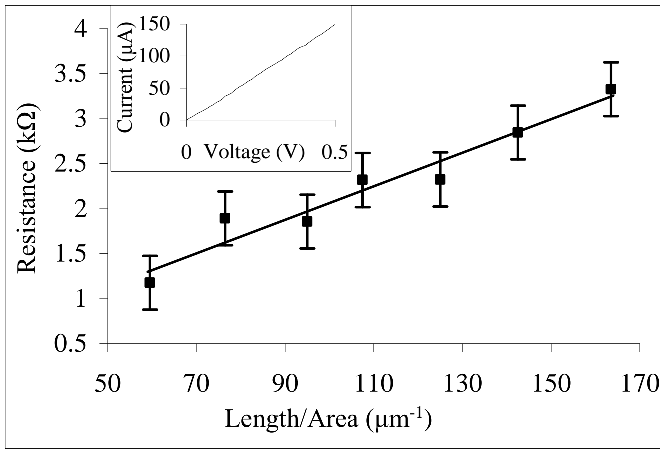

Fig. 4. Length/cross sectional area ratio (L/A) vs. measured resistance values of FIB deposited Pt tracks bridging pads of Si devices plotted

The value of FIB-written Pt track resistivity (ρ) is obtained from the slope of the linear fit of Fig. 4. Resistivity value of 1864 ± 100 μΩ cm is achieved, which is comparable to literature reports [4, 5]. FIB deposition method normally results in the deposition of disordered metallic compound containing Pt and C from the precursor gas ($C_9H_{16}Pt$), which is contaminated with Ga from the ion beam and O from the chamber and therefore this high resistivity value is expected [6].

In order to investigate the quality of the nickel and Au film deposited on all sides of 1mm cube module fabricated in Process 2 SEM analysis was performed. SEM inspection on the electroless nickel deposited surface indicated a relatively smooth film of thickness 650 nm as shown in Figure 5. Figures 6 and 7 show the energy dispersive x-ray analysis of Ni layer and Au layer. Figure 6 confirmed the pure Ni deposition without boron. The bath is operated at its lower practical temperature limit in order to minimize stress in the resulting film. Inset of Figure 7 shows SEM image of the relatively smooth Au film. In this sample nickel was totally replaced by gold as confirmed by the energy dispersive X-ray analysis, where Ni peak is absent.

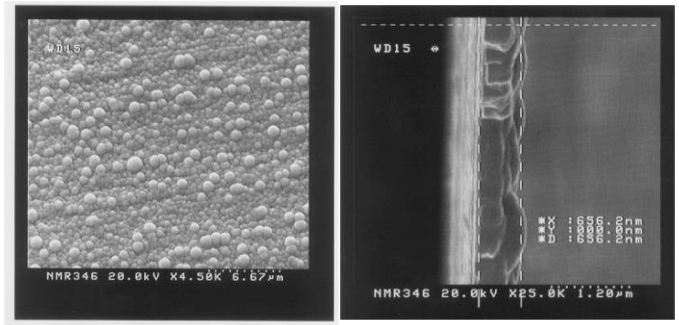

Fig. 5. Scanning electron micrograph of (a) nickel layer and (b) nickel layer deliberately detached from the cube.

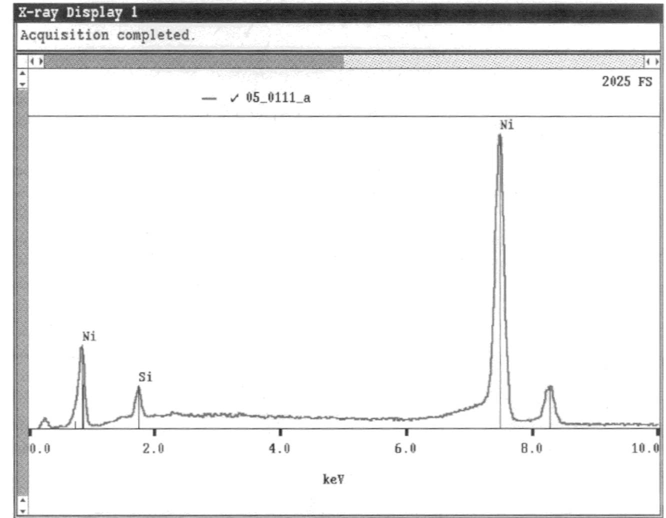

Fig. 6. Energy dispersive X-ray analysis of nickel layer.

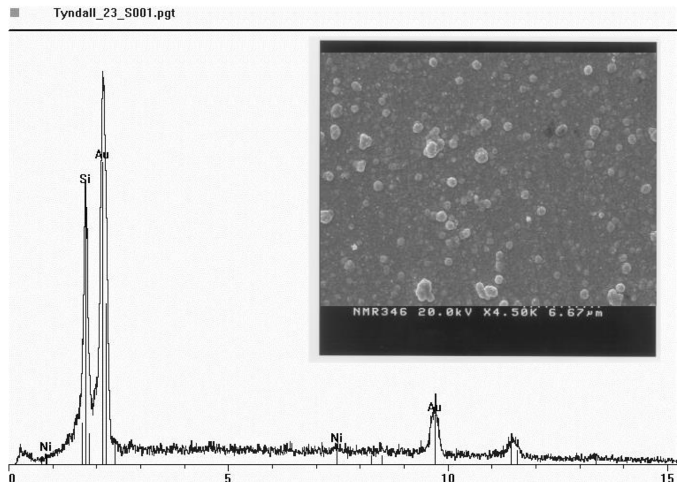

Fig. 7. Energy dispersive X-ray analysis of Au layer; Inset shows the scanning electron micrograph of the Au layer.

Figure 8(a) shows the silicon cubes after nickel deposition followed by gold flash layer to provide corrosion-resistant solderable contact layer and 8(b) shows the flip-chipped LED on one side of the patterned 1mm cube that has been turned on.

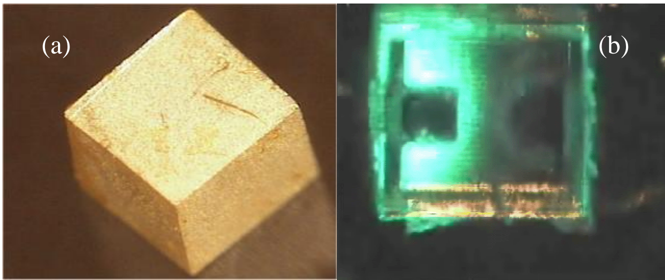

Fig. 8. (a) Optical micrographs of the final gold plated 1mm cube module; (b) Flip-chipped LED turned on.

Conclusions

The 3-D interconnected assembly process of 5 layers stacked silicon demonstrated a route towards the fabrication of micro modules at 1mm cube level. This module allowed us to use it as a proof of concept of novel 3D integration process; the next phases of development will focus in research towards a detailed understanding of the thermal and electrical properties of 1mm cube functional modules. It also demonstrates that use of established volume scale technologies like Flip-chip and dicing techniques are viable for fabricating these 1mm modules.

Acknowledgments

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