Packaging technology for high power blue-green LEDs

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ABSTRACT

High brightness LEDs (HBLEDs) have been fabricated on GaN semiconductor material grown on sapphire substrate. These devices provide an optical output power in excess of 50 mW at a driving current of 1 amp. For this high current application, large size (1.8 mm × 0.6 mm) GaN LEDs are flip-chip mounted onto a heat sink to provide a low thermal resistance path from the junction to the ambient. For the flip-chip mounting, a Au/Sn/Au solder and a Au/Au thermal compression bonding process have been optimized. The bond strength of the Au/Sn solder joints and the Au-Au bonds is measured through shear testing. Good bond strength results of 224 g/f for the Au/Sn/Au solder and 288 g/f for the solid Au bonds have been achieved. The thermal modeling of the assembly is done with a finite element analysis and the optimum design has been adopted for this high current application. At present these assemblies are under lifetime test and so far nearly 6000 hours of continuous operation has been achieved.

Key words: HBLED, Flip-chip mounting, Solder, Thermal compression bonding.

1. INTRODUCTION

There is a large demand for HBLEDs in the market due to the ever-increasing applications of these devices. According to Bob Steele of Strategies Unlimited, the LED market grew 37% to reach $3.7 billion in 2004[1]. For the last few years LEDs have been used extensively in small signal (traffic lights, mobile phones, interior and architecture lighting etc.) and medium signal applications (large area displays or billboards, exterior signaling functions for many types of vehicle such as brake lights and turn indicators etc.) whereas the largest application for LEDs will be the large signal application or otherwise referred to "solid state lighting". Two things, that need to improve for LEDs to be used in general lighting are the amount of light output from a single device and the conversion efficiency of the LEDs. The general target for HB LEDs for solid-state lighting is to increase the number of lumens per watt by increasing the internal quantum efficiency and improving the extraction of photons by clever design and packaging. The flip-chip design is a way to achieve higher light output. The flip-chip assemblies allow much higher drive currents, thus obtaining a much higher light output from a single device. However, a few issues need to be addressed before the LEDs can be driven with 1 amp or such higher current (typical driving current for a GaN LED is 20 mA). Firstly, the high drive current generates an amount of heat which needs to be dissipated through a proper heat sink. Also, as the GaN LED structure is grown on foreign sapphire substrate, the defect density is much higher ($10^{10}/cm^2$) compared to other semiconductor materials. At a high current density device failure will be rapid though metal migration along the defects[2]. Also at high current density there is increased voltage drop across the p-contact, which in turn reduces the power conversion efficiency of the LEDs. Also there will be carrier overshoot at higher operating currents which will result in a lower internal quantum efficiency.

In this paper we present the results on large area flip-chip mounted HB-LEDs that employ electroplated Au/Sn/Au solder layers on silicon substrate and Au-Au thermal compression bonding. The lead-free solder is bonded without the use of flux and has the potential of reliable operation over thousands of hours. The electrical and optical test results are presented. These devices will be suitable for applications where a large amount of light is required from a single device or a cluster of devices.

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2. THERMAL MODELING OF THE HB LEDS

An optimum design was made for high current application using Computational Fluid Dynamics (CFD) thermal analysis software. A 3-D geometry close to the actual device structure was considered for the simulation. A thick copper block was considered as the heat sink where the bottom of the block was assumed to be at the room temperature. It was considered in the simulation that all the heat was generated at the active region. The simulations showed that the main thermal path is through the p-metal, solder and the sub mount towards the heat sink and the result is shown in Figure 1. Two main conclusions from the thermal modeling were i) Good current spreading is necessary for low thermal resistance and ii) Overlap of solder is advantageous from a thermal point of view (intimate solder contact with the full chip surface). The detailed result of the thermal modeling can be found in the reference [3].

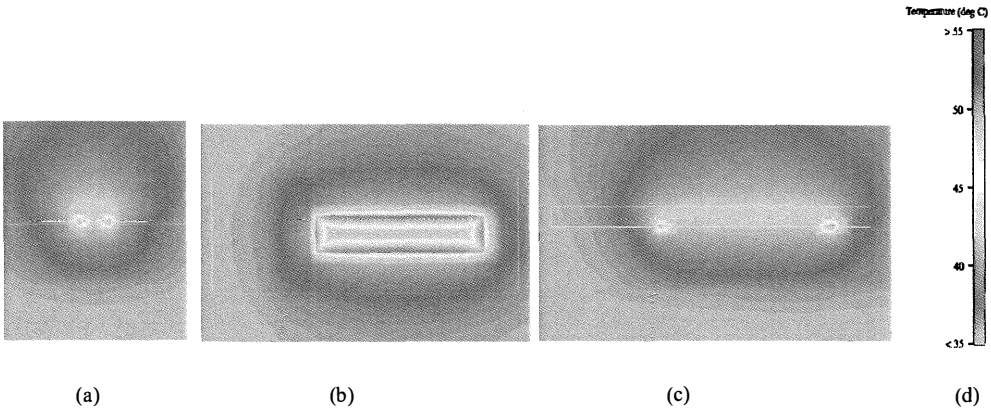
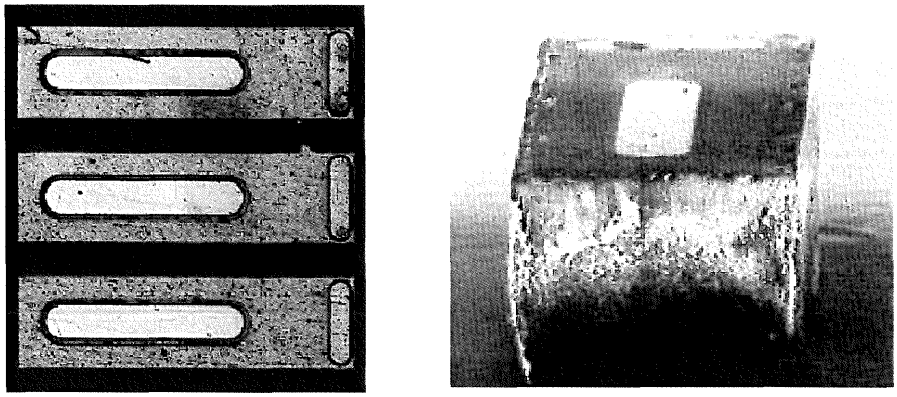


Figure 1: (a) Thermal simulation results for a heat dissipation that is concentrated along the p-contact perimeter (side view). The white rectangle shows the outline of the LED chip. b) top view. c) side view. d) Temperature scale (colour coding).

3. EXPERIMENTAL

3.1 Device Fabrication

Figure 2(a) shows the top view of a cluster of three HBLEDs fabricated in house. The fabrication process consists of four levels of lithography, wet and dry chemical etching of the metal and the semiconductor, two metal evaporations (p and n contacts) and a dielectric layer deposition for electrical insulation. Good adhesion of the p metal with the semiconductor is critical as this is the main path of the heat dissipation to the heat sink. Also, the p contact is stretched out to distribute the generated heat during the high current applications. An optimized multilevel metal, Pd-Ag-Ni-Au (3-50-30-500 nm) is evaporated as the p contact where the palladium layer makes good ohmic contact with the semiconductor surface and the silver layer works as a optical reflector for light extraction though the sapphire substrate. The p-contacts are cigar-shaped and measures 1 mm x 200 μm whereas the n contact, made of Ti-Al-Pt-Au (50-100-30-500 nm) fully surrounds the p contact area. This helps the uniform current spreading across the p- mesa. In general, both p and n contacts are ohmic as deposited. On top of the LED surface a 500 nm thick lowly stressed PECVD SiNx layer was deposited and contact windows were opened above both p and n contact (400 μm x 100 μm) areas. This dielectric layer provides the electrical isolation between the LED and the solder plated silicon submount after the flip-chip mounting.



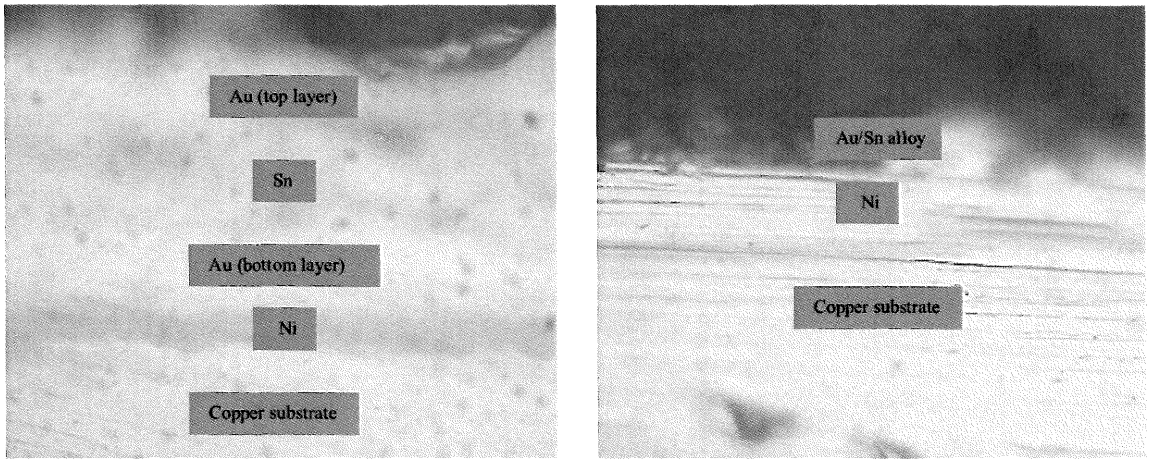
(a) (b)

Figure 2: (a) Top view of a cluster of three HBLEDs, where the dimension of the elongated p contact area is 1 mm x 200 μm and the dimension of the n pad is 400μm x 200 μm b) SEM image of a single HBLED.

The final step in the fabrication process is to thin down the sapphire substrate from 0.5 mm to 0.1 mm thickness and to dice the sapphire to separate the individual LED chips. The traditional grinding procedure is lapping down the sapphire by sub mm sized grit. This is a time consuming process and it is difficult to control the thinning rate. After thinning it is also possible to separate the individual devices by scribing. This scribing process using a Kurl-Suss diamond scriber gives higher yield than dicing. It is also possible to separate the individual LEDs or a cluster of LEDs by laser scribing[4]. The laser scribing provides very high yield and is a very fast process which circumvents the need for grinding and dicing/scribing. The single LED shown in Figure 1(b) has been laser scribed across the full sapphire thickness of 500 μm.

3.2 Substrate Preparation

The solder electroplating was done on patterned Si substrates. The solder was deposited in windows in a photoresist layer. A thin sputtered Ti/Cu metal layer served as the seed layer for electroplating. On top the sputtered metal a thin Ni layer was plated first. This acts as a barrier layer that prevents the diffusion of gold to the device areas. The total thickness of the Au/Sn/Au solder was 10 μm (Au 4μm, Sn 4μm, Au 2μm). In case of the bulk Au samples to be used for thermal compression bonding the thickness of the Au layer was 7 to 8 micron. All the plating was done at a low current density to obtain good plated thickness uniformity. Different compositions of Au-Sn in the plated layer will yield different thermal resistance values. From the thermal conductivity point of view, it is best to have as much gold as possible in the Au-Sn layer as gold has very high thermal conductivity (320 W/m-K). The picture of an Au-Sn solder before and after reflow where tin and gold alloyed over the Ni is shown in Figure 3 The total thickness of the plated metal is 12 microns.



(a) (b)

Figure 3: (a) Image showing 2 microns of Ni on copper substrate, with 4, 4 and 2 microns of gold tin gold layers respectively plated over it. This is prior to reflow, (b) Image after reflow as can be seen, the tin and gold alloyed over the Nickel after reflow.

3.3 Flip-chip mounting

The fabricated device is then flip-chip bonded to a solder plated substrate with matching contact pads. The Schematic view of a flip-chip assembly (side view) is shown in Figure 4. The flip-chip bonding was done on a Fineplacer System from FINETECH Electronics, Berlin. The machine has two separate heaters to heat up the substrate holder and the chip holder. Once the chip is placed on the chip holder, and held down by vacuum, the chip can be aligned to the solder bumps on the substrate. Once the alignment is done, the chip holder arm is pulled down and the chip is brought in contact with the substrate. The reflow of the solder is done by turning on the heat on both the substrate holders and the chip holder for the desired time. There is also a feature on the machine to apply pressure during the reflow process. As expected, thermal compression bonding (Au/Au bonding) both higher pressure and higher temperature than Au/Sn solder bonding for optimum results.

The bonding temperature and pressure were varied over a narrow range in order to find the optimum conditions for both Au/Sn/Au solder bonding and the Au/Au thermal compression bonding. The bond strengths of both types of bonds were measured by flip-chip mounting some test LEDs with p and n contact pads that measured 100 μm × 100 μm. The shear testing was done according to MIL-STD-883E (method 2019.5). The thickness of the final gold layer on the bond pads was about 750 nm. A summary of the test results on both types of bonds is given in the Table 1.

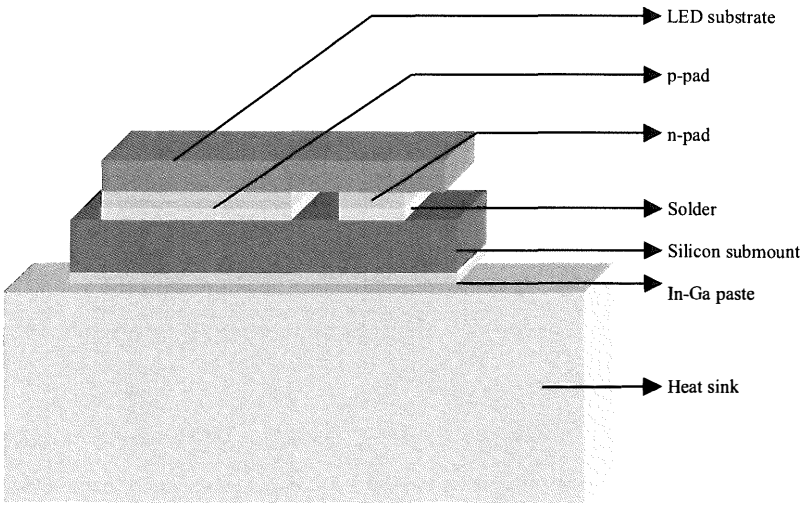


Figure 4: Schematic diagram of the flip-chip assembly.

Sample No	Temperature (°C)	Shear Strength (g)
1	265	164.5
2	270	167.5
3	**275**	**224.5**
4	280	208
5	285	19

(a)

Sample No	Temperature (°C)	Shear Strength (g)
1	310	223
2	315	246
3	320	-
4	**330**	**288.5**
5	335	275.5

(b)

Table 1: Bond strength test results (a) Au/Sn/Au solder bonding (b) Au to Au thermal compression bonding.

We see from the two tables that high values for the shear strength are obtained with both types of bonding. We have also observed that minimum pressure gives the better bonding strength for Au/Sn solder samples. Au to Au thermal compression bonding shows highest shear strength at the higher temperatures. Also the whole assembly after mounting the chip was tested in ultrasonic agitation for one minute. In most of the cases, the flip-chip assemblies survived the full strength ultrasonic agitation. Some devices were mounted with conducting solver epoxy. These devices showed higher thermal resistance than the metal bonded devices. We observed that the Au/Sn/Au remained in good condition, even when there was a delay of several weeks between the electroplating and the flip-chip bonding.

4. ELECTRICAL AND OPTICAL TEST RESULTS

The whole flip-chip assembly was mounted on the heat sink with liquid In-Ga paste and electrical and optical measurements were taken. The highest output power measured inside an integrating sphere was measured 54 mW @ 1 amp. The Light–current (L-I) and the forward I-V curve for this assembly is shown in Figure 5, where the LED was mounted using thermal compression bonding. The forward voltage was 4.9 V @ 500 mA and at high current, I>500 mA, the series resistance of the total assembly is about 2 Ω. The forward voltage value is as expected for a large area device. The emission wavelength is 460 nm and the wall plug efficiency is 2.0% at 400 mA bias, dropping to 0.8% at 1 amp

bias. This drop in wall plug efficiency may be due to carrier overshoot at the high current density. The wall plug efficiency could be improved with better wafer material and enhanced light extraction efficiency. Also encapsulating the assembly with a lower refractive index material will provide higher optical output, thus raising the wall plug efficiency. The thermal resistance (junction to copper) assembly was estimated to be about 15°C/W. Several flip-chip mounted HBLEDs on copper heat sink are in lifetime test for nearly a year. Initially some of them failed, but the remaining HBLEDs are still operating well.

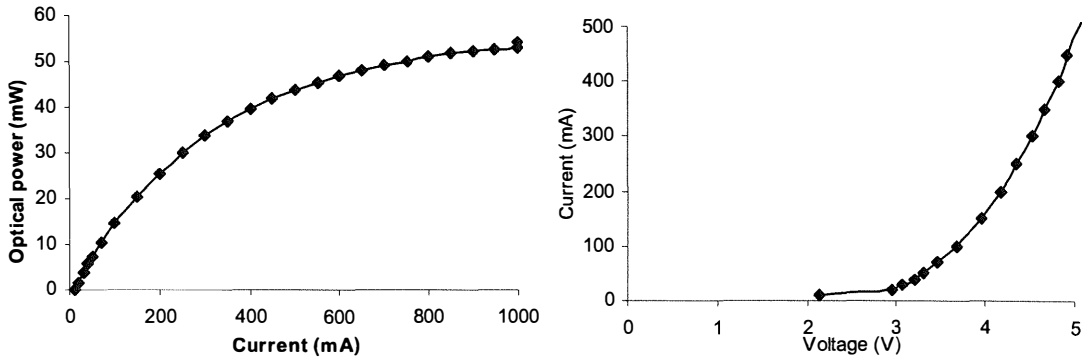


Figure 5: (a). L-I measurement on a flip-chip assembly (Au/Au) on a copper heat sink, (b) Forward I-V measurement for the same assembly.

5. CONCLUSIONS

We have fabricated HBLEDs with an optical power of more than 50 mW @ 1 amp. Electroplated Au/Sn/Au solder and a solid Au/Au bonding process have been optimized for flip-chip mounting of these devices. Good bond strength results have been achieved with both types of bonding. These devices are showing good lifetime (>6000 hours) under continuous high current operation. The optical output can be further improved by solving the carrier overshoot problem at higher bias.

6. ACKNOWLEDGEMENT

We gratefully acknowledge the financial support from Enterprise Ireland (grant IF/2002/025). We also thank NCLA, Galway for laser scribing of our LEDs.

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