High Frequency dc-dc Converter with Co-packaged Planar Inductor and Power IC

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Abstract

The paper introduces the trend of integration and miniaturization of power converters with potential for enhanced efficiency, form factor reduction and cost reduction. To demonstrate the concept of highly integrated switched mode power supply with integrated magnetic, a system-in-package DC-DC converter using a stacked co-packaging approach is developed. A system approach was taken to the design, and functional integration, using 3-D packaging for realizing a power supply in package solution (PwrSiP). The target integrated converter is capable of handling an input voltage of 5V and frequencies up to 40MHz. A DC-DC converter IC on a 0.35µm CMOS process was designed to meet this goal. In parallel with the IC design, technology development for on-silicon integrated micro-inductors was completed to achieve small-form factor and extremely low profile. A maximum measured efficiency of 83% and 78% was achieved on the stacked converter operating at 20MHz and 40MHz, respectively. The stacked approach showed a 30% area reduction compared to side-by-side implementation with external discrete inductor.

Integration and Miniaturization of DC-DC Power Converters

DC-DC power converters are power supplies that accept a wide range of input voltage and produce a DC output voltage regulated to a particular value. Electronic system performance requirements of current and emerging applications demand ever greater integration and miniaturization of power converters with potential for enhanced efficiency and cost reduction. For most of the switched mode power converters, the magnetic components are necessary to provide temporary energy storage, which is considered as the most difficult part to integrate applying conventional silicon processes.

Increasing DC-DC converter switching frequency is a key to miniaturization and functional integration, as this leads to lower values of the energy storage components (input/output capacitors, output inductors) and hence reduced passive component footprint. All of today's low power converter products operate at a frequency lower than 10 MHz. However, recent research has presented converters with frequencies up to 100sMHz [1][2]. At such frequencies the values of inductance required are small and integration of the inductor on to the IC or into the package may become practical. But this integration of power passives still presents significant challenges in microsystems processing and advanced packaging techniques [3].

Currently a major drive in the power semiconductor industry is to develop new miniaturised product formats that can be referred to as power supply-in-package (PwrSiP) and power supply-on-chip (PwrSoC). While PwrSoC offers potential of a fully monolithic solution, 3-D packaging technologies offer an intermediate solution by stacking individual passive components or a passive 'LC' interposer on a power train IC.

In this work we have taken an overall system approach to the design, and functional integration, using 3-D packaging for realizing a PwrSiP solution.

A miniaturized, DC-DC power converter, operating in the 30-40 MHz range and rated up to 1 W, is presented, which has been specifically co-designed with an inductor component fabricated using standard CMOS compatible processing technology. The co-design approach enables the DC-DC converter to meet specific challenges in footprint area, efficiency and 3-D packaging.

The paper will present the power IC design, fabrication process for the micro-inductors on silicon and its functional integration with the power train IC, using planar and 3-D assembly. For comparison, a different demonstrator using the same IC but with discrete wire-wound ferrite inductor was also prepared and tested. A performance comparison of the conventional planar and newly proposed 3-D stacked DC-DC converter will also be presented. Finally, a technology roadmap is proposed to achieve the ultimate goal of PwrSoC, which features 3-D/TSV/Interposer technology as an intermediate solution.

High Switching Frequency Power IC Design

The design specifications of the target power IC are summarized in the table below.

Input Voltage	2.7~5V
Output Voltage	0.5~4.5V
Switching Frequency	30~50MHz
Output Current	1 A
Si CMOS Process	AMS 0.35µm

The converter is shown in figure 1.The main elements to the converter are the pulse width modulation (PWM), dead time circuitry, drivers and switches.

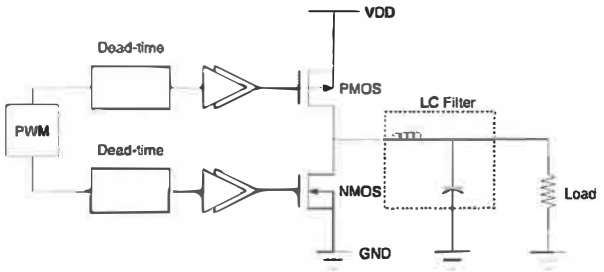

Figure1. Converter architecture

A digital block was implemented for the control, PWM and dead time. Figure 2 shows the block diagram for the digital block. There are 7 inputs and 5 outputs. The inputs consist of a clock signal clk (to clock the serial control data in); clk2 which is a clock signal to clock the data from a shift register to a working register; force HS which can switch the high-side switches off; force LS which can switch the low-side device off and Kick which is for enabling the PWM to oscillate.

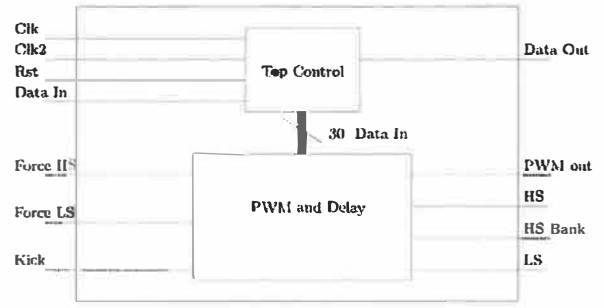

Figure2. A digital block for the control, PWM and dead time

The top control circuit consists of three main blocks as shown in Figure 3. They are a state machine, shift register and work register. The state machine works over 32 clock cycles to load in the control data. It has an active high synchronous reset, the state machine on the first clock signal resets the count to 0 and also goes into an idle state setting the shift register and working register enables to a logic 0 and hence disabling them. On the next clock cycle the state machine enters the load shift register stage, which enables the shift register. For the next 30 clock cycles the shift register is enabled with the control data shifted into it. On clock cycle 32 the state machine enters the load work register state, disabling the shift register enable while enabling the working register enable. On clk2 the data from the shift register is then shifted to the work register.

The analog core is made up of the buffers and the power switches. The design point for this application was for up to 1A of current. The optimization of the switches therefore resulted in picking a segmented switch size, which would give a high efficiency across the load line. The optimization was carried out with the target frequency of 30 MHz. The goal of the optimisation was that, for under 500 mA, it would be more efficient to use one of the top switches. For load currents greater than 500 mA, the use of two top switches will give a higher efficiency. Figure 4 shows an example of optimizing the sizing (the MOSFET channel widths) of the upper (PMOS) and lower (NMOS) power devices on the converter IC for 400mA at a switching frequency of 30MHz. Here it is seen that, for a given switching frequency, a plateau is reached where further increases in size (area) of the power devices, do not deliver any significant improvement in converter efficiency.

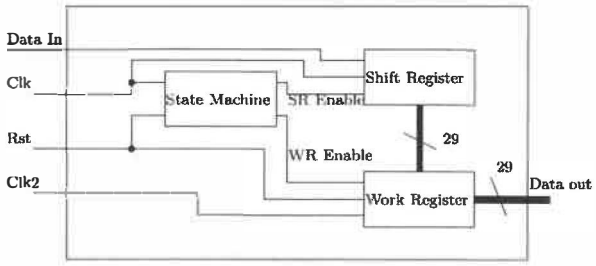

Figure 3. Top control circuit

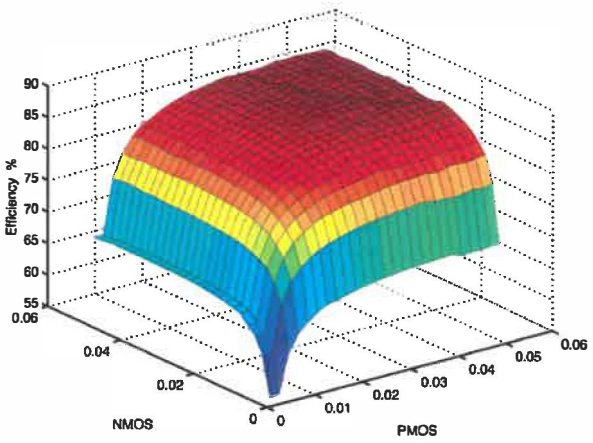

Figure 4. Efficiency optimized by varying switch size.

The gate drives consist of a tapered buffer arrangement, with the use of the minimum number of stages in order to reduce the power consumption. To verify the analog core the switch sizes where picked with the gate drivers sized accordingly and a SPICE level simulation carried out. Figure 5 shows the efficiency plot across the current range for both top segmented switches. This demonstrates the optimized switches. As can be seen for currents below 500 mA, the use of one top switch is more optimal and for greater than 500 mA the use of two switches results in a greater efficiency.

Figure 6 shows the top level layout of the designed IC. The die is 3.8mm long and 2.3mm wide. The digital layout was imported into Cadence Virtuoso and a DRC and LVS have been carried out and passed before prototyping. These top level verifications contained the full IC layouts up to top

metallization as far as the IC pads. This IC was fabricated using AMS 0.35µm process.

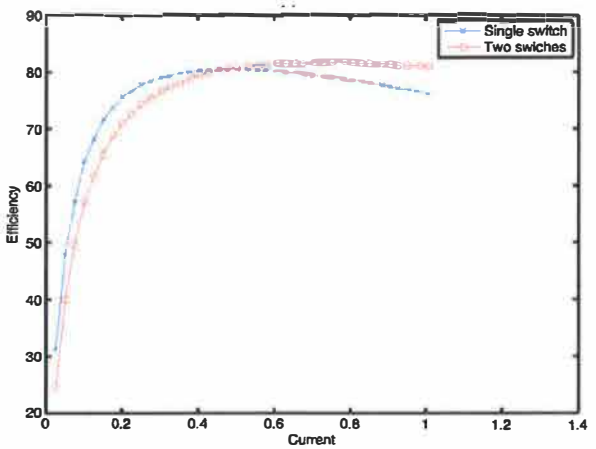

Figure 5. Efficiency plot across the current range (Amps) for both Top segmented switches.

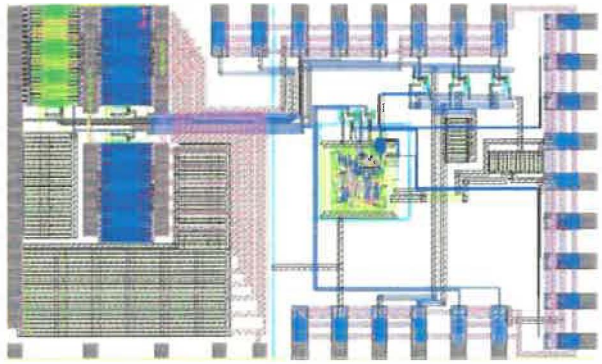

Figure 6. Final IC layout.

Micro-inductor Design and Fabrication

One of the key elements enabling miniaturisation of power supply and ultimate monolithic solution is on-silicon integrated magnetics technology. The integrated magnetics technology is based on processing, on a silicon substrate or on a post-CMOS wafer, of electroplated materials to form the coil/windings and magnetic core of a micro-inductor. Figure7 shows a race-track shape inductor integrated on silicon.

Figure 7. a micro-magnetic inductor integrated on silicon. The inductor consists of a racetrack shaped copper coil, which is surrounded by a layer of magnetic material.

Compared to the round shape spiral inductors, the race-track shaped inductors have the advantage of having anisotropy property in the magnetic core. The core material is deposited in the presence of a magnetic field which induces anisotropy, i.e. a hard and easy axis of magnetization in the material. The easy axis is induced parallel with the core long axis, so that during inductor operation the flux travel is along the hard axis, i.e. perpendicular to the easy axis. In the hard axis, magnetization takes place by domain rotation as opposed to domain growth. Domain rotation is a low loss mechanism, so that exploiting material anisotropy is an important technique for reduction of core loss for high frequency operation.

A detailed description of the integrated magnetics on-silicon technology used to fabricate the inductors has been given previously [4][5][6]. The essential details which are required in order to understand the design process are briefly described here. The substrate is a silicon wafer with a layer of insulation (SiO_2, approximately 1µm thick). A seed layer of Ti/Cu is deposited by sputtering on the insulation. A layer of magnetic material (Ni45Fe55) is electroplated and patterned (layer 1) on top of the seed layer. This layer is further insulated by a patterned layer of BCB (layer 2). The Cu-windings are then deposited using electroplated copper on top of a Ti/Cu seed layer (layer 3). These windings are covered by a layer of SU8 (epoxy type photoresist) to isolate them from the top magnetic layer (layer 4). Finally, the top magnetic layer is electroplated (layer 5) to obtain a closed magnetic path.

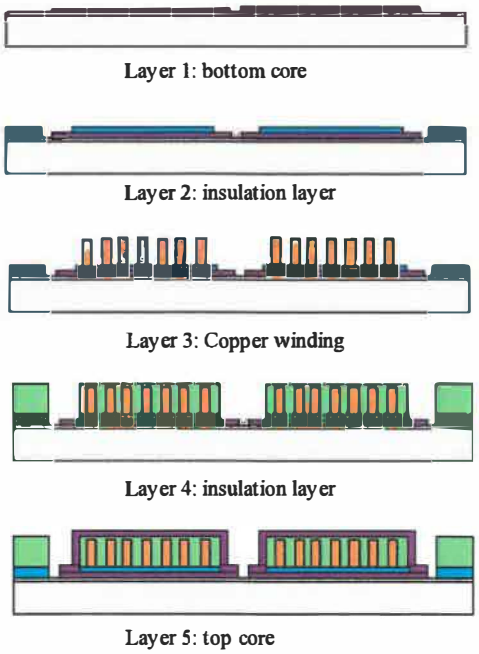

Figure 8. Micro-inductor process flow

A range of inductors were fabricated in this work, with the area from 3mm^2 to 6mm^2. The inductance value varies from 50nH to 70nH. Figure 9 shows the measured inductance of four different inductors at various frequencies. All the inductors show flat inductance up to 20MHz at least.

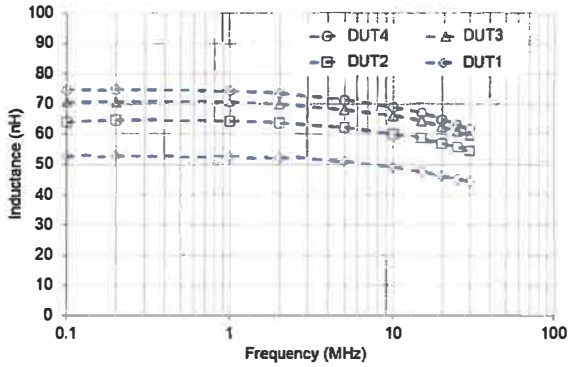

Figure 9. Measured inductance at various frequencies.

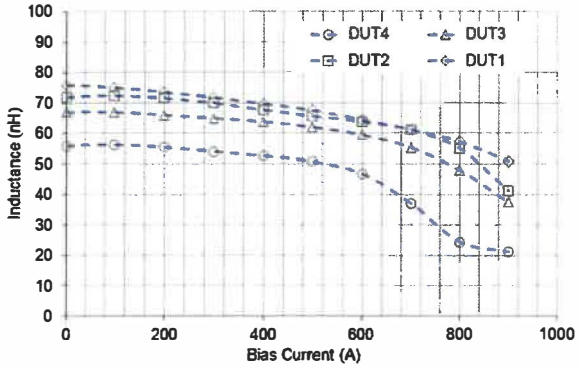

Figure 10. Measured inductance at various bias current.

DUT3 was selected to be co-packaged with a DC-DC converter active die to demonstrate the electrical performance due to its footprint became more comparable to the active IC. The inductor specifications are given in Table 1.

Table 1. Inductor's specifications

Parameters	
Core thickness, t_c (μm)	3.5
Conductor width, W_w(μm)	62
Conductor spacing, W_s (μm)	15
Number of Turns, N_r	3
Core Length, L_c (μm)	2370
Footprint Area (mm^2)	5.4
Inductance at low freq. (μH)	0.07
DC resistance, R_{DC} (Ω)	0.12
Inductor Width, (mm)	1.34
Inductor Length, (mm)	4.04

Packaging and Assembly

Two demonstrators have been prepared in this work. For the first demonstrator converter, the buck converter IC die was mounted in a ceramic QFN package using Ablestik 84-LMI-SR4 silver filled epoxy which is then temperature cured. 25 micron aluminium wire wedge/wedge bonding was used to connect the bond pads of the IC to the package bond pads. The QFN package was then mounted on to the test PCB (daughter board) by soldering. A discrete inductor 0402AF-780 is directly soldered to the daughter board. The inductance of this wire-wound ferrite inductor is 78nH and the DC resistance is 0.13Ω. the size of the wire-wound ferrite inductor is 1.12 mmx0.66 mm, and the profile is 0.66mm. All other components, such as input and output decoupling capacitors are also directly soldered on to the test PCB.

The prototype DC-DC converter was first demonstrated on a PCB board by mounting all components directly on the test PCB, as shown in Figure 11.

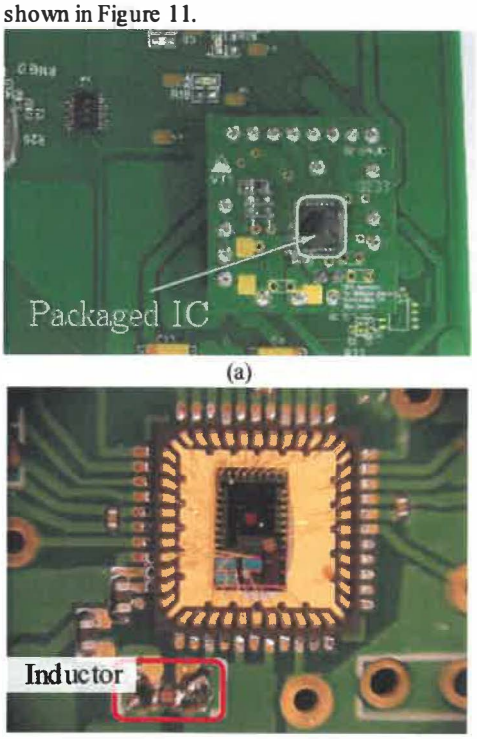

Figure 11. (a) Converter power IC and passive components are directly mounted on test PCB daughter board. (b) zoom-in image of daughter board.

In the second demonstrator converter, the buck converter IC was stacked on top of the micro-inductor because some of the IC pins, including the input voltage pins and the switching node are located in the middle of the IC. Access to the pins will become impossible if the micro-inductor was stacked on top of the IC. Figure 12 shows the buck converter IC stacked on a micro-inductor using a snap cure thermoset epoxy. The die size of the inductor is 4.5mmx2mm. 25 micron gold wire ball/wedge bonding was used to connect the copper inductor bond pads to both the relevant aluminium bond pads on the IC and the gold bond pads on the package. The 25um Au wire bond has a resistance of 46mΩ/mm. In order to reduce the parasitic resistance introduced by the wire bonds, two parallel wires were bonded to each inductor pad. The two pairs of 2mm long 25μm gold wires introduced approximately 92mΩ resistance.

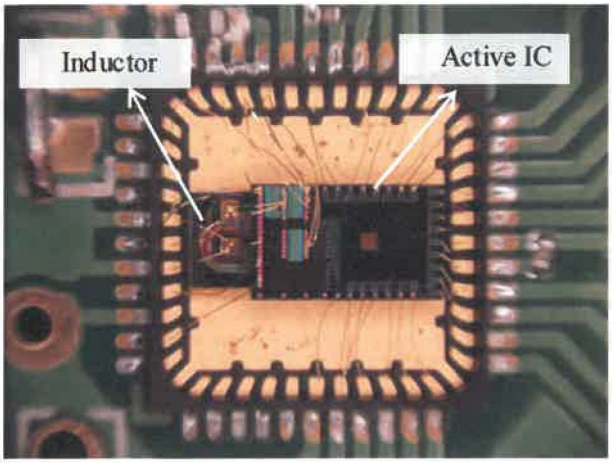

Figure 12. Image of the packaged IC and the integrated micro-inductor. The buck converter active IC is stacked on a micro-inductor and co-packaged in a QFN package using wire bonding.

The active IC and micro-inductor haven't been pre-thinned The functioning part of the inductor is 90µm thick and the silicon substrate on which the inductor was fabricated is 525µm thick. This gives an overall thickness of the stacked configuration of approximately 1mm. This overall thickness can be potentially reduced to 500µm or less by thinning the inductor and power active IC substrate. In this stacked co-package approach, the resulting total footprint area is 11mm^2, which is slightly bigger than the active die area due to the need for exposing the micro-inductor's pads for wire-bonding.

Converter Performance

The electrical characterisation of both DC-DC converter demonstrators using both assembly approaches, i.e. stacked co-packaging using a micro-inductor and side-by-side assembly using a discrete wire-wound ferrite inductor, has been carried out. Figure 13 shows the measured efficiency of the first demonstrator converter using a discrete inductor on board at varied load current levels at 20MHz and 40MHz respectively. The power consumption of the buffer stages are not included in the efficiency calculation. The current drawn by the digital logic, the level shifter and buffers is approx. 7mA at 3V. In all tests, the converter input voltage is 3.0 V and output voltage is 1.5 V. It can be seen from Figure 13 that the peak efficiency of the first demonstrator converter is 83% at 190mA load current for 20MHz and 78.2% at 320mA load current for 40MHz. It is more obvious at 20MHz switching frequency that switching off one top switch can improve the light load efficiency due to the lower switching losses.

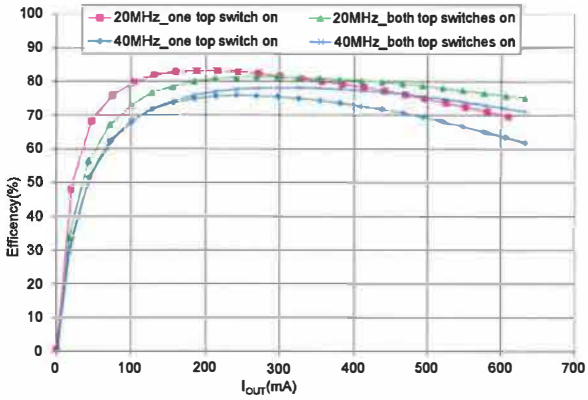

Figure 13. Efficiency of the first demonstrator at various load conditions with a single or two top switches on.

Figure 14 shows the measured efficiency of the second demonstrator converter using stacked co-packaged micro-inductor at varied load current levels at 20MHz and 40MHz respectively. It can be seen from Figure 14 that the peak efficiency of the first demo converter is 74.2% at 300mA load current for 20MHz and 70.9% at 300mA load current for 40MHz.

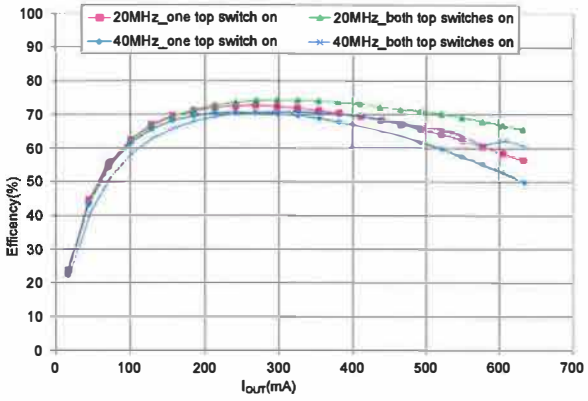

Figure 14. Efficiency of the second demonstrator at various load conditions with a single or two top switches on.

The footprint area has been reduced by stacking the active IC on the inductor while the efficiency of the DC-DC converter using the stacked approach is lower than using the discrete wire wound inductor. The difference in converter overall efficiency is due to two factors. The first one is the different parasitic resistance introduced by different wire bonding scheme. There is higher parasitic resistance introduced by wire bonds in the stacked approach. In stacked co-package approach, the switching node of IC is connected to one of the inductor terminations by a pair of 25µm gold wire bonds with a length of approximately 2mm. The second termination of the inductor is connected by a pair of 2mm long 25µm gold wire bonds to two pins in the QFN package, which is directly soldered to the test PCB. Hence, the two connections by wire bonds on inductors introduced 92 milliohm parasitic resistance while in previous approach

(using discrete inductor) the wire bonds connecting switch node on IC and micro-inductor is less than 46 mΩ. The problem with wire bonds is that they can typically contribute as much resistance as the inductor coils and hence degrade the converter efficiency. The total parasitic resistance introduced into the converter circuit by wire bonds was estimated to be 165mΩ in the stacked approach, which results in 6.6mW DC conduction loss at 200mA load current, corresponding to 6.3% of the overall converter loss at 20MHz.

The second factor is the higher micro-inductor losses. The micro-inductor has a resistance value of 1.48Ω at 20MHz while the wire-wound inductor's resistance is 0.81Ω at 20MHz. The higher resistance value indicates higher inductor losses which could be caused by higher eddy current losses and higher hysteresis loss in the magnetic core, or higher winding AC conduction losses, or a combination of both.

The parasitics introduced by wire bonding can be eliminated by using a flip-chip technique. The resistance and inductance introduced by solder balls are negligible. Because the active IC was not specially laid out to facilitate flip chipping with the micro-inductor on top, this approach was not pursued within this work.

Future Packaging Challenges

There are a number of challenges to be addressed in the future in providing a power component packaging solution which provides miniaturisation while at the same time ensuring good thermal and thermo-mechanical performance.

One of the challenges is to minimize the parastics. It is becoming more critical when the DC resistance of micro-inductor becomes comparable to introduced parasitic resistance for high switching frequency due to lower required inductance. The introduced parasitic inductance can also stimulate resonance and cause the power converter to exhibit "ringing", with the result that the output voltage will be unstable. The wire bond technology is not compatible with achieving the low parasitic inductance required. Flip-chipping or embedded approach can potentially achieve very low parasitics. The embedded approach utilises a build up process to both embed the die and to provide plated interconnection within a module.

For both demonstrators, the input and output capacitors are still mounted on the test PCB as external components, which inevitably introduced significant parasitics in the circuit. The conventional discrete capacitor is not suited for flip-chipping. The embedding approach can potentially allow placement of input capacitors as close as possible to the IC. However, this is still constrained to side by side assembly which may not be the optimum from miniaturisation point of view.

With the increase of the switching frequency of Buck converter, the values of input and output capacitance and inductance required are becoming smaller and smaller. The required capacitor and inductor may become small enough that integration of the inductor along with the capacitor on to the IC or into the package may become practical. In spite of the fact that discrete, commercial ceramic chip capacitors are at least an order of magnitude cheaper than chip capacitors, a number of academic and industry researchers have reported significant progress in delivering high-density, 3-dimensional, on-chip, trench capacitor technologies with capacitances per unit area in the range 100 to 440 nF/mm^2 [7]. The availability of high density capacitors raises the possibility to consider a passive, LC, interposer, comprising the input and output capacitors and the output inductor for a switched mode DC-DC converter. This passive interposer could then be stacked with a power management IC to deliver a complete PwrSiP platform. Alternatively, an LC interposer, consisting of an array of multiple LC combinations could be stacked on a large SoC chip or multi-core processor, thereby achieving a high granularity power supply delivering multiple, isolated voltage rails for digital, analog, I/O and RF functions. To deliver such an integrated solution would potentially require the application of wafer-level bonding and through-silicon vias (TSV).

Conclusions

This paper has presented a 20 to 40 MHz DC-DC converter with stacked co-packaged IC and micro-inductor. The micro-inductor was fabricated on silicon substrate using semiconductor compatible electrochemical deposition and photolithography. The power IC features an on-chip decoupling capacitor and configurable top switches. Two demonstrators have been built. For the first demonstrator, the power IC was wire-bonded to a QFN package, which is then soldered to a PCB test board. A discrete wire-wound ferrite inductor was assembled on board. For the second demonstrator, the power IC was stacked on micro-inductor and co-packaged in a QFN package. A maximum measured efficiency of 83% and 78.2 was achieved at a switching frequency of 20 MHz and 40MHz, respectively, for the first demo. A maximum measured efficiency of 74.2% and 70.9% was achieved at a switching frequency of 20 MHz and 40MHz, respectively, for the second demonstrator. This technology can be further developed to allow integration of magnetic components with deep trench capacitors to realise an integrated LC interposer. By stacking the LC interposer on the active IC, the footprint area of the buck converter can be significantly reduced.

Acknowledgments

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