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Drift-diffusion model for single layer transition metal dichalcogenide field-effect transistors

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A physics-based model for the surface potential and drain current for monolayer transition metal dichalcogenide (TMD) field-effect transistor is presented. Taking into account the two-dimensional (2D) density-of-states of the atomic layer thick TMD and its impact on the quantum capacitance, a model for the surface potential is presented. Next, considering a drift-diffusion mechanism for the carrier transport along the monolayer TMD, an explicit expression for the drain current has been derived. The model has been benchmarked with a measured prototype transistor. Based on the proposed model, the device design window targeting low-power applications is discussed. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4770313]

A great deal of interest in two-dimensional materials analogues of graphene has appeared among the scientific community since the demonstration of isolated 2D atomic plane crystals from bulk crystals.[1] Dimensionality is key for the definition of material properties and the same chemical compound can exhibit dramatically different properties depending on whether it is arranged in dots (0D), wires (1D), sheets (2D), or bulk (3D) crystal structure. Notably, experimental studies of 2D atomic crystals were lacking until recently because of the difficulty in their identification.[1] Representative of this class are the 2D monolayer of transition metal dichalcogenides (TMDs) with a chemical formula MX_2, where M stands for a transition metal and X for Se, S, or Te. The potential of this family of layered materials for flexible electronics was proposed by Podzorov *et al.*, who demonstrate an ambipolar WSe_2 p-field-effect transistor (FET) with a hole mobility comparable to silicon ($\sim$500 cm^2/Vs).[2] The electronic properties of TMDs vary from semiconducting (e.g., WSe_2) to superconducting (e.g., $NbSe_2$). The semiconducting monolayer TMDs, like MoS_2, $MoSe_2$, $MoTe_2$, WS_2, and WSe_2 are predicted to exhibit a direct gap in the range of 1–2 eV.[3] The wide gap together with a promising ability to scale to short gate lengths because of the optimum electrostatic control of the channel, by virtue of its thinness, make monolayer TMDs very promising for low power switching and optoelectronics applications. The first 2D crystal based FET relying on a semiconducting analogue of graphene was demonstrated using a monolayer MoS2 as the active channel.[4] Low power switching with an $I_{ON}/I_{OFF} \sim 10^8$ and subthreshold swing (SS) of 74 mV/decade at room temperature was experimentally measured. More recently, a monolayer p-type WSe_2 FET with an optimum SS $\sim$ 60 mV/decade and $I_{ON}/I_{OFF} > 10^6$ was demonstrated.[5]

To boost the development of 2D-material based transistor technology, modeling of the electrical characteristics is essential to cover aspects as device design optimization, projection of performances, and exploration of low-power switching circuits.[6–9] Some models aimed to explore the performance limits of monolayer TMD transistors have been reported assuming ballistic transport.[10,11] However, the behavior of state-of-the art devices is far from ballistic and a drift-diffusion transport regime seems more appropriate for channel lengths well above the carrier mean free path (see Refs. 12 and 13 as an illustrative example of carrier transport studies, where the case of graphene is discussed). In this context, I propose a model for the current-voltage (I-V) characteristics of monolayer TMD FETs, based on the drift-diffusion theory. As a previous step a surface potential model, accounting for the 2D density-of-states (DOS_{2D}) of monolayer TMDs, is proposed. I will consider that carriers are free to move parallel to the TMD sheet. However, their motion is restricted in the perpendicular direction because the strong quantum confinement. The DOS_{2D} has a profound impact on the quantum capacitance, which is essentially different from that of a nanowire (1D) or a bulk (3D) material. Analytical expressions are derived for both the surface potential and drain current covering both subthreshold and above threshold operation regions.

Let us consider a dual-gate monolayer TMD FET with the cross-section depicted in the inset of Fig. 1. It consists of

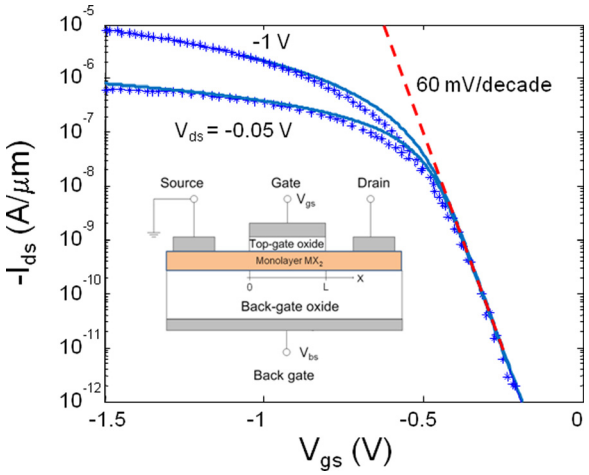

FIG. 1. Transfer characteristics obtained from the analytical model (solid lines) compared with experimental results from Ref. 5 (symbols). Inset: cross section of the dual-gate monolayer TMD transistor.

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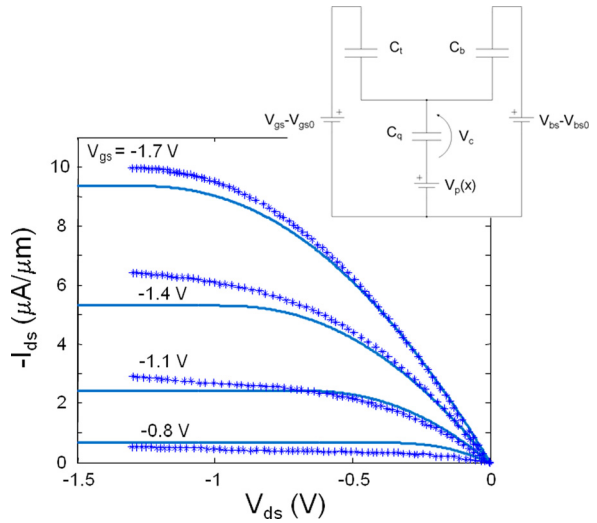

FIG. 2. Output characteristics obtained from the analytical model (solid lines) compared with experimental results from Ref. 5 (symbols). Inset: equivalent capacitive circuit.

one atomic layer thick TMD playing the role of the active channel. The source and drain electrodes contact the monolayer TMD and are assumed to be ohmic. The electrostatic modulation of the carrier concentration in the 2D sheet is achieved via a double-gate stack consisting of top and bottom gate dielectric and the corresponding metal gate. The source is grounded and considered the reference potential in the device. The electrostatics of this device can be understood using the equivalent capacitive circuit depicted in the inset of Fig. 2. Here, C_t and C_b are the top and bottom oxide capacitances and C_q represents the quantum capacitance of the 2D sheet. The charge density (per unit area) is calculated by integrating the DOS_{2D} over all the energies and can be expressed as

$$Q_c = Q_p + Q_n = q\int_{-\infty}^{0} DOS_{2D}(E)f(E_F - E)dE - q\int_{0}^{\infty} DOS_{2D}(E)f(E - E_F)dE, \quad (1)$$

where Q_p and Q_n refer to the positive (holes) and negative (electrons) charge contributions, respectively; f(E) is the Fermi-Dirac function, and $E_F = qV_c$ is the Fermi level, where the reference level is the semiconductor mid-gap. The parameter V_c represents the voltage drop across C_q or surface potential. For the sake of getting a simple model, $f(E) \sim 1$ for $E < E_F$ and $f(E) \sim \exp((E_F\text{-}E)/kT)$ for $E \geq E_F$ have been assumed. Noting that $DOS_{2D}(E) = D_0 \sum_n H(E - E_n)$, with $D_0 = \frac{m^*}{\pi\hbar^2}$, where m* is the effective mass, E_n represents the energy of the n^{th}-subband, H(E) is the Heaviside function, and considering that the ground state ($n = 0$) is the more relevant in determining the carrier density, then Eq. (1) can be written as

$$\begin{aligned}
&Q_p = -q^2 D_0 V_c - qD_0(E_0 - kT); \quad Q_n = -qD_0 kT e^{\frac{qV_c - E_0}{kT}}, \quad qV_c \leq -E_0,\\
&Q_p = qD_0 kT e^{\frac{-qV_c - E_0}{kT}}; \quad Q_n = -qD_0 kT e^{\frac{qV_c - E_0}{kT}}, \quad q|V_c| < E_0,\\
&Q_p = qD_0 kT e^{\frac{-qV_c - E_0}{kT}}; \quad Q_n = -q^2 D_0 V_c + qD_0(E_0 - kT), \quad qV_c \geq E_0,
\end{aligned} \quad (2)$$

where $E_0 = E_g/2$ and E_g is the band gap of the monolayer TMD. From Eq. (2), the quantum capacitance defined as $C_q = -dQ_c/dV_c$, results in

$$\begin{aligned}
&C_q = C_{q,p} + C_{q,n} = q^2 D_0 + q^2 D_0 e^{\frac{qV_c - E_0}{kT}}, \quad qV_c \leq -E_0,\\
&C_q = C_{q,p} + C_{q,n} = q^2 D_0 e^{\frac{-qV_c - E_0}{kT}} + q^2 D_0 e^{\frac{qV_c - E_0}{kT}}, \quad q|V_c| < E_0,\\
&C_q = C_{q,p} + C_{q,n} = q^2 D_0 e^{\frac{-qV_c - E_0}{kT}} + q^2 D_0, \quad qV_c \geq E_0.
\end{aligned} \quad (3)$$

Under nonequilibrium conditions ($V_{ds} \neq 0$), a single Fermi level cannot be assumed. Instead, two distinct quasi-Fermi levels for computing the electron $V_n(x)$ and hole $V_p(x)$ concentrations and currents have to be considered. Here x denotes the transport direction. In this work, I consider the modeling of unipolar p-FETs. Extension to unipolar n-FETs is straightforward. Coming back to the inset of Fig. 2, $V_p(x)$ is zero at the source end ($x = 0$) and V_{ds} at the drain end ($x = L$). Applying basic circuit laws to the equivalent capacitive network, the following relation can be obtained:

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$$V_c(x) = \frac{Q_p(V_c)}{C_t + C_b} + \left(V_{gs} - V_{gs0} - V_p(x)\right)\frac{C_t}{C_t + C_b} + \left(V_{bs} - V_{bs0} - V_p(x)\right)\frac{C_b}{C_t + C_b}, \quad (4)$$

where V_{gs}-V_{gs0} and V_{bs}-V_{bs0} are the top and back gate-source voltage overdrive, respectively. These quantities comprise work-function differences between the gates and the TMD monolayer, eventual charged interface states at the TMD monolayer/oxide interfaces, and intentional or unintentional doping of the TMD monolayer.

To model the drain current of a monolayer TMD p-FET, a drift-diffusion transport is assumed under the form $I_{ds} = -WQ_p(x)v(x)$, where W is the gate width, and v(x) the hole drift velocity $v = \mu F$, where F is the electric field and μ is the hole effective mobility assumed independent of field, carrier density, or temperature. This model applies as long as the channel length is well above the hole mean free path. As a reference, a mean free path (for electrons) of ~20 nm was estimated in Ref. 10 for MoS_2 monolayers. Applying $F = -dV_p(x)/dx$, inserting the above expression for v, and integrating the resulting equation over the device length, the drain current becomes $I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_p dV_p$. In order to get an explicit expression for the drain current, the integral is solved using V_c as the integration variable consistently expressing Q_p as a function of V_c,

$$I_{ds} = \mu\frac{W}{L}\int_{V_{cs}}^{V_{cd}} Q_p \frac{dV_p}{dV_c} dV_c, \quad (5)$$

where V_{cs} is obtained from Eq. (4) as $V_c(V_p = 0)$. Similarly, V_{cd} is determined as $V_c(V_p = V_{ds})$. Moreover, Eq. (4) provides the relation $\frac{dV_p}{dV_c} = -\left(1 + \frac{C_{q,p}}{C_t + C_b}\right)$, where $C_{q,p} = -dQ_p/dV_c$. Inserting this expression into Eq. (5), the following explicit drain current expression can be finally obtained

$$\begin{aligned} I_{ds} &= \mu\frac{W}{L}\{g(V_c)\}_{V_{cs}}^{V_{cd}} \\ g(V_c) &= \left(1 + \frac{q^2 D_0}{C_t + C_b}\right)\left(\frac{q^2 D_0}{2}V_c^2 + qD_0(E_0 - kT)V_c\right), \quad qV_c < -E_0, \\ g(V_c) &= D_0(kT)^2\left(e^{\frac{-qV_c - E_0}{kT}} + \frac{q^2 D_0}{C_t + C_b}\frac{1}{2}e^{\frac{-2(qV_c + E_0)}{kT}}\right), \; qV_c \geq -E_0, \end{aligned} \quad (6)$$

where $g(V_c)$ takes different forms whether $qV_c < -E_0$ (above threshold region) or $qV_c \geq -E_0$ (subthreshold region). To take into account eventual saturation velocity effects, the physical channel length should be replaced by an effective length $L_{eff} = L + \mu\frac{|V_{ds}|}{v_{sat}}$, where v_{sat} is the hole saturation velocity.

To test the model, I have benchmarked the resulting I-V characteristics with experimental results reported in Ref. 5, which are unipolar p-type FETs with a channel consisting of a monolayer WSe_2. The channel was contacted with Pd contacts acting as source and drain electrodes. P-type conduction was experimentally observed and this is presumably due to the small barrier height for hole injection at the Pd-WSe_2 interface. The energy band gap of the monolayer WSe_2 is $E_g \sim 1.68$ eV and the valence band effective mass along the transport direction is calculated to be $m^* = 0.64m_0$ ($K \rightarrow \Gamma$), m_0 being the free electron mass, estimated from the dispersion relations.[3] The device under test has $L = 9.4\,\mu$m, $W = 1\,\mu$m, top dielectric is ZrO_2 of 17.5 nm and relative permittivity ~12.5, and the bottom dielectric is silicon oxide of 270 nm. The backgate voltage was −40 V. The flat-band voltages V_{gs0} and V_{bs0} were tuned to −0.5 V and 0 V, respectively, to provide an appropriate shift of the transfer characteristics according to the experiment. A constant hole effective mobility of 250 cm^2/Vs was assumed, consistent with measurements. A source/drain resistance of 300 Ω provides a good fit with the experiment. Around the threshold voltage (~− 0.5 V), a slight disagreement is observed because the approximation made for the Fermi-Dirac distribution. The resulting I-V transfer and output characteristics are shown in Figs. 1 and 2. In accordance with the experiment, a SS ~ 60 mV/decade at room temperature and $I_{ON}/I_{Off} \sim 10^6$ is predicted by the model (Fig. 1). Note that no interface trap capacitance (C_{it}) was needed to be included in the model to match the experiment because the near ideal subthreshold slope suggests that $C_{it} \ll C_{ox}$. The output characteristics show saturation-like behavior at high V_{ds} (Fig. 2). Saturation velocity effects are not expected to be relevant for this transistor because $\frac{\mu}{v_{sat}} \sim 2.5$ nm/V, giving $L_{eff} \approx L$. At low V_{ds}, the model nicely reproduces the observed linear behavior, indicative of ohmic metal contacts. The agreement between the proposed model (solid lines) and the experiment (symbols) is pretty good. More accuracy could be expected by adding to the model a field dependent mobility and self-heating effects. Next, by using the model, the tradeoff between I_{ON} and I_{ON}/I_{Off} is calculated (Fig. 3). Ten orders of magnitude between switching states could be achieved, although at the expense of the I_{ON}. For the reported transistor, an $I_{ON}/I_{Off} \sim 10^6$ with $I_{ON} \sim 1\,\mu$A/μm at power supply voltage $V_{DD} = 0.6$ V could be achieved. Nevertheless, a huge improvement of the I_{ON} may be possible via channel length scaling. A simulation of an hypothetical transistor of L = 100 nm assuming the same hole mobility as the reference transistor gives a factor ×100 of ON-current

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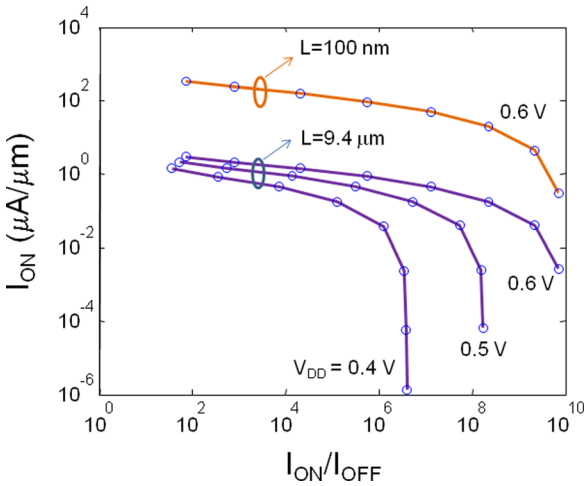

FIG. 3. Tradeoff between ON-current and ON-OFF current ratio.

improvement for a fixed I_{ON}/I_{Off}. Note that short-channel effects (SCEs) have not been included in the model, but due to the extreme immunity of 2D materials to SCE the 100 nm transistor considered here is expected to behave as a well tempered long-channel transistor. For short-channel length devices (sub 100-nm), the calculations should be done by solving the full Poisson's equation in both vertical and lateral dimensions, which is beyond the scope of this work.

In conclusion, a surface potential and drain current model for monolayer TMD transistors has been proposed, taking into account the 2D semiconducting nature of monolayer TMDs. The drain current is formulated assuming a drift-diffusion theory, which seems appropriate for explaining the experimental results of reported devices till date. These transistors hold promise for low-power switching applications. The proposed model should be valid for other transistors relying on 2D atomic layer thick channels.

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[1]K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, Proc. Natl. Acad. Sci. **102**(30), 10451–10453 (2005).
[2]V. Podzorov, M. E. Gershenson, C. Kloc, R. Zeis, and E. Bucher, Appl. Phys. Lett. **84**(17), 3301–3303 (2004).
[3]W. S. Yun, S. W. Han, S. C. Hong, I. G. Kim, and J. D. Lee, Phys. Rev. B **85**, 033305 (2012).
[4]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**, 147–150 (2011).
[5]H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, Nano Lett. **12**, 3788–3792 (2012).
[6]S. A. Thiele, J. A. Schaefer, and F. Schwierz, J. Appl. Phys. **107**, 094505 (2010).
[7]S. Thiele and F. Schwierz, J. Appl. Phys. **110**, 034506 (2011).
[8]D. Jiménez and O. Moldovan, IEEE Trans. Electron Devices **58**(11), 4049–4052 (2011).
[9]D. Jiménez, IEEE Trans. Electron Devices **58**(12), 4377–4383 (2011).
[10]Y. Yoon, K. Ganapathi, and S. Salahuddin, Nano Lett. **11**, 3768–3773 (2011).
[11]L. Liu, S. B. Kumar, Y. Ouyang, and J. Guo, IEEE Trans. Electron Devices **58**(9), 3042–3047 (2011).
[12]M.-H. Bae, S. Islam, V. E. Dorgan, and E. Pop, ACS Nano **5**, 7936–7944 (2011).
[13]M.-H. Bae, Z.-Y. Ong, D. Estrada, and E. Pop, Nano Lett. **10**, 4787–4793 (2010).

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