Investigation of degradation mechanisms in low-voltage p-channel power MOSFETs under High Temperature Gate Bias stress

Investigation of Degradation Mechanisms in Low-Voltage p-Channel Power MOSFETs Under High Temperature Gate Bias Stress

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Abstract

In this work we investigate the degradation mechanisms occurring in a p-channel trench-gate power MOSFET under High Temperature Gate Bias (HTGB) stress. The impact of negative bias temperature stress is analysed by evaluating relevant figures of merit for the considered device: threshold voltage, transconductance and on-resistance. Temperatures and gate voltages as large as 175°C and -24V, respectively, are adopted to accelerate the degradation in the device. Moreover, in order to investigate the origin of degradation mechanisms we analyse the interface states generation and the charge trapping processes, the impact of a switching gate voltage during the stress phase and the recovery phase after HTGB stress.

1. Introduction

Si-based power MOSFETs are typically used in low voltage applications. In this field, trench-gate architecture is usually adopted to achieve high integration and hence to improve the trade-off between breakdown voltage and on-resistance. Furthermore, p-channel devices can be easily adopted as high-side switches, without requiring complex driving solutions.

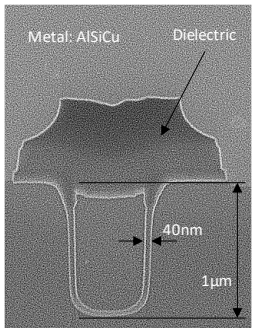
Several studies in the literature [1-8] reported that p-channel power MOSFETs are subjected to degradation under High Temperature Gate Bias (HTGB) stress. Such a phenomenon, known as bias temperature instability [9], leads to the degradation of threshold voltage, which has been ascribed to both build-up of oxide charges and interface states activation [2-7]. The present work extends the previous analyses, by focusing also on the on-resistance degradation and by stressing the device at temperatures as large as 175°C (which is a relevant condition for automotive-qualified devices). In order to better understand the origin of degradation mechanisms, this work also investigates the build-up of charges and the defects generation during the stress phase. Besides that, the recovery phase and the temperature dependence of relevant figures of merit are analysed. Finally, the degradation of on-resistance and the evolution of defects are analysed in the case of gate switching conditions.

The reminder of the work is organized as follows: in section 2 the details of the experimental setup and of the adopted characterization methodology are reported; in section 3 we discuss experimental results by focusing on the degradation of electrical parameters, on the investigation of defects, on the influence of temperature during the stress phase, on the effect of non-constant gate voltage, and on the analysis of the recovery phase; finally, in section 4 we summarize the main conclusions of the paper.

2. Experimental

The device under investigation is a low voltage trench-gate logic-level p-channel power MOSFET, with a breakdown voltage of above 40V and a rated drain current of 36A (at room temperature). Further details are reported in Fig. 1.

Measurements are performed on packaged devices, placed in a thermal chamber and biased by means of SMUs (Keithely 2450 and 2651A). The



Technological steps:
- p-Epy type (100) silicon surface
- Trench formation by dry ecth
- Gate oxide formation (40nm)
- Polysilicon deposition
- Body implantation and diffusion
- Source implantation and activation
- Intermediate dielectric deposition
- Contacts opening and metal deposition

Fig. 1. FIB cross section and technological steps of the power MOSFET under investigation.

devices are subjected to HTGB stress with a gate voltage ($V_{GS,stress}$) ranging from -16V up to -24V, while keeping the drain voltage to 0V. The stress phase is periodically interrupted in order to measure an I_D-V_{GS} curve (sense phase) in linear region. In order to minimize the recovery occurring during the sense phase, IV measurements (lasting only a few seconds) are carried out at the stress temperature. An example of IV curves acquired after different stress times is reported in Fig. 2. The sense phase allows to monitor the degradation of relevant figures of merit: threshold voltage (V_T), maximum transconductance (g_m) and on-resistance (R_{on}). The threshold voltage is estimated according to maximum-transconductance method. The on-resistance is evaluated as the ratio $V_{DS,sense}/I_D$, with the device operating in linear region. In order to study the degradation of both channel and drift components of the on-resistance, R_{on} is evaluated at different values of the gate voltage ($V_{GS,sense}$): between -3V and -20V.

3. Results and discussion

3.1. Degradation of electrical parameters under HTGB stress.

The threshold voltage shift under different gate bias stress conditions is reported in Fig. 3. As expected an increase of degradation is observed with the stress time and the gate voltage. The curves reported in Fig. 3 can be modelled with a power law only for limited stress time. Hence, a power law with saturation is considered in order to fit experimental data (similarly to [10]):

$$\Delta V_T = \beta / [1 + (t/\tau)^{-\alpha}] \quad (1)$$

where t is the stress time, and β, τ and α are fitting parameters representing a proportional constant in V,

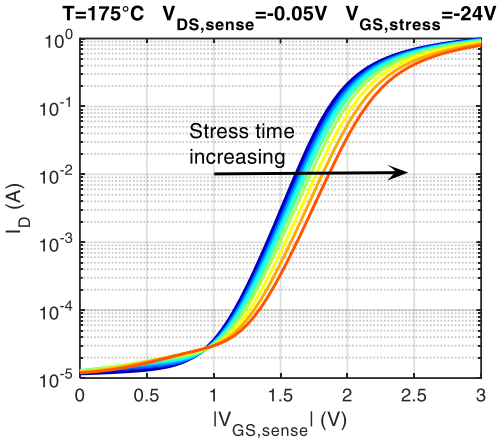


Fig. 2. IV curves measured after HTGB stress for T=175°C and $V_{GS,stress}$=-24V. A stress time up to 80000s (about 22hours) is considered.

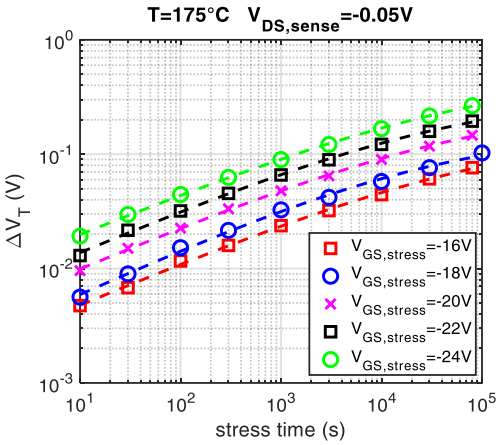


Fig. 3. Threshold voltage shift as a function of the stress time, for T=175°C and $V_{GS,stress}$ ranging from -16V to -24V. Experimental data are fitted with the saturated power law reported in Eq. 1. A similar power exponent α, ranging from 0.37 to 0.4, is found among the different experiments.

the time constant in s and the power exponent, respectively. The change of threshold voltage can be ascribed to both build-up of oxide charge and depassivation of interface states at the Si/SiO2 interface. To better distinguish between these two phenomena, we also analyse the transconductance degradation, which can be mainly ascribed to the creation of defects at the abovementioned interface (see Fig. 4). A reduction of transconductance, up to 10% is observed, meaning that the mobility in the channel region is significantly degraded.

As reported in Fig. 5, the HTGB stress significantly affects the on-resistance evaluated at low gate voltage (-3V). A degradation larger than 20% is

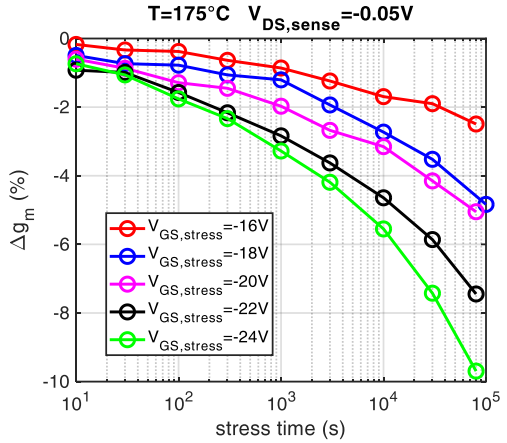


Fig. 4. Transconductance change as a function of the stress time, for T=175°C and $V_{GS,stress}$ ranging from -16V to -24V. A relative reduction of transconductance, up to 10%, is observed.

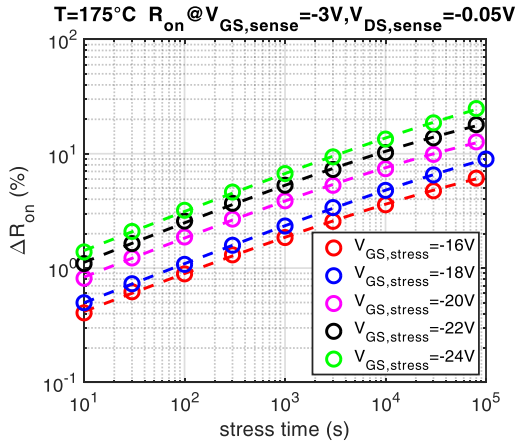


Fig. 5. On-resistance as a function of the stress time, for T=175°C and $V_{GS,stress}$ ranging from -16V to -24V. On-resistance is evaluated at a gate voltage of -3V.

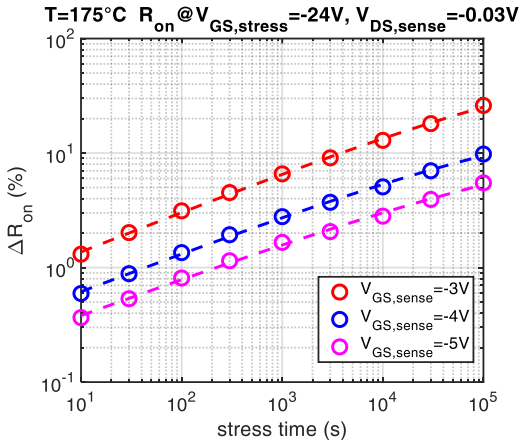


Fig. 6. On-resistance as a function of the stress time, for T=175°C and $V_{GS,stress}$=-24V. Different $V_{GS,sense}$ values are considered for the on-resistance evaluation.

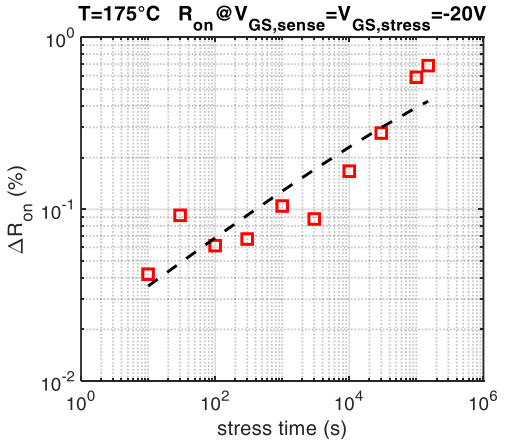


Fig. 7. On-resistance as a function of the stress time, for T=175°C and $V_{GS,stress}$ -20V. By sensing R_{on} at $V_{GS,sense}$=-20V and $V_{DS,sense}$=-0.01V, a much lower degradation (<1%) is observed with respect to Fig. 5.

observed in some stress conditions. As in the case of threshold voltage, the percentage increase of R_{on} can be modelled with a saturated power law. It is well known that for low values of V_{GS}, R_{on} is strongly dependent on the channel component. Hence, the increase of this parameter can be considered as a combined effect of both threshold voltage increase and transconductance reduction. As reported in Fig. 6, as long as the gate voltage is increased in the sense phase, R_{on} degradation reduces, being the channel component less relevant compared to the drift component.

R_{on} is also evaluated at $V_{GS,sense}$ as large as -20V. At this large gate voltage, we expect R_{on} to be significantly influenced by drift resistance. The results, reported in Fig. 7, reveal a R_{on} increase of less than 1%. This change is significantly smaller with respect to the degradation of more than 10% observed in Fig. 5 for the same stress conditions. It is worth noting that, since $V_{GS,stress}$ and $V_{GS,sense}$ are chosen to be the same and a single current value is measured during the sense phase, no recovery occurs in this test.

3.2. Temperature dependence and lifetime estimation

In order to accelerate the degradation mechanism occurring during HTGB stress, a large temperature (175°C) was adopted in the previous analysis. Fig. 8 illustrates the dependence of R_{on} degradation on the stress temperature. The increase of temperature leads to a time shift of ΔR_{on}, without significantly changing the evolution with the stress time. Hence, we can assume that the degradation mechanism is unchanged.

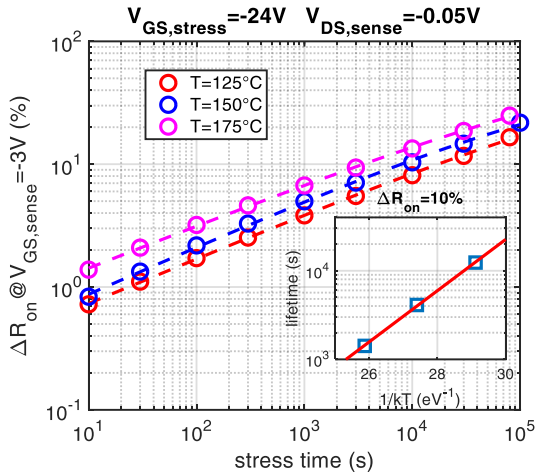


Fig. 8. On-resistance as a function of the stress time for different temperatures. The inset reports the Arrhenius plot of the lifetime calculated considering a failure criterion ΔR_{on}=10%.

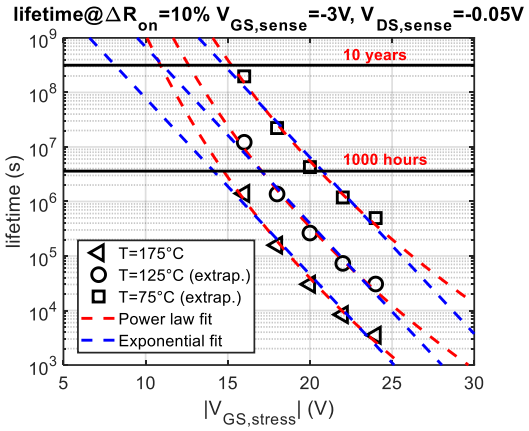


Fig. 9. Lifetime calculated considering a failure criterion ΔR_{on}=10%. R_{on} is evaluated at $V_{GS,sense}$=-3V and considering experimental data at T=175°C and extrapolated data at T=125°C and T=75°C with Eq. 2.

The lifetime is estimated by considering a failure criterion of ΔR_{on}=10%. According to the inset of Fig. 8, the lifetime can be modelled as:

$$lifetime = a \cdot e^{b\,/\,(k \cdot T)} \tag{2}$$

where a and b are two fitting parameters, and k is the Boltzmann constant.

By considering the data reported in Fig. 5, a lifetime plot for a temperature of 175°C is reported in Fig. 9. Moreover, considering the temperature dependence reported in Fig. 8 and the fitting model of Eq. 2, the lifetime is also extrapolated for temperatures of 125°C and 75°C. Depending on the considered extrapolation law, power or exponential law, the maximum operating gate voltage can be estimated allowing to achieve 1000 hours or 10 years of operation.

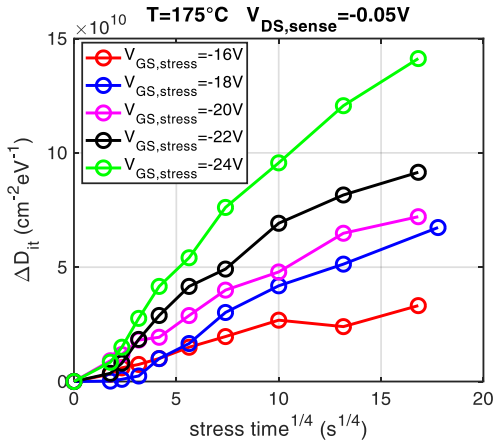


Fig. 10. Density of states ΔD_{it} as function of the stress time, for T=175°C and $V_{GS,stress}$ ranging from -16V to -24V. ΔD_{it} is evaluated from experimental subthreshold slope variations, according to Eq. 4.

3.3. Investigation of defects

As discussed in section 3.1, the degradation of electrical parameters is due to both build-up of charges in the gate dielectric and interface states generation at the Si/SiO_2 surface. In order to further analyse the defects generation process, the increase of density of charges ΔN_{ot} (cm^{-2}) and of the density of states ΔD_{it} ($cm^{-2}eV^{-1}$) is calculated according to Eq. 3 and Eq. 4, respectively [11]:

$$\Delta N_{ot} = C_{ox} \cdot \Delta V_T / q \tag{3}$$

$$\Delta D_{it} = C_{ox} \cdot \Delta S / (2.3 \cdot k \cdot T) \tag{4}$$

where C_{ox} is the oxide capacitance and ΔS is the change of subthreshold slope (evaluated in the range 10^{-3} A – 10^{-2} A). In Fig. 10 the evolution of ΔD_{it} with the stress time is reported. The amount of interface states increases with the stress time and the gate voltage. An increase of interface states larger than 10^{11} $cm^{-2}eV^{-1}$ is observed in some stress conditions. It is also important to analyse in Fig. 10 the dependence of ΔD_{it} on $t^{1/4}$. In the first part of the degradation, this dependence can be approximated as linear. According to the reaction-diffusion model [12], this kind of dependence is expected when hydrogen diffusion controls the trap generation process and it is typically observed in the case of thick oxides.

The evolution of defects is also compared to the case of switching gate voltage during the stress phase,

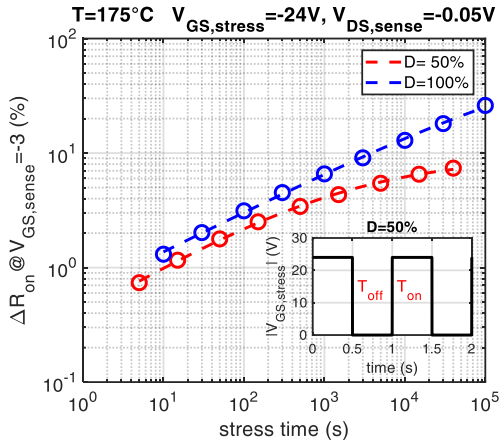


Fig. 11. On-resistance evaluated for different gate switching conditions: constant gate voltage; switching gate voltage at a frequency of 1Hz and D=50%. The effective stress time (time·D/100) is considered.

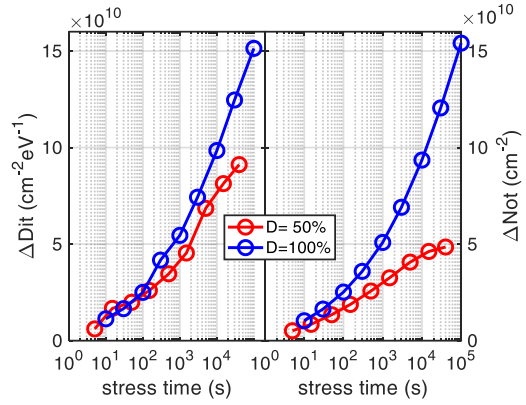


Fig. 12. ΔD_{it} and ΔN_{ot} for different gate switching conditions: constant gate voltage; switching gate voltage at a frequency of 1Hz and D=50%. The effective stress time (time·D/100) is considered.

with a frequency of 1Hz and a duty cycle D of 50%, i.e. on-time T_{on} and off-time T_{off} of 0.5 s. It is evident from fig. 11 that the gate switching has a significant impact on the R_{on} degradation. In particular, by reducing the duty cycle down to 50% we observe a lower ΔR_{on} with a clear saturation effect. Fig. 12 is useful to explain such a phenomenon. ΔN_{ot} shows a similar saturation effect and the number of charges at the end of the stress is less than half with respect to the case of constant gate voltage stress. On the other hand, ΔD_{it} is less influenced by the switching conditions, especially for a stress time lower than 100s, where the two curves are overlapped. These results demonstrate that: i) ΔR_{on}, evaluated at $V_{GS,sense}$=-3V is more affected by build-up of charges rather than interface states generation; ii) there are oxide defects with a

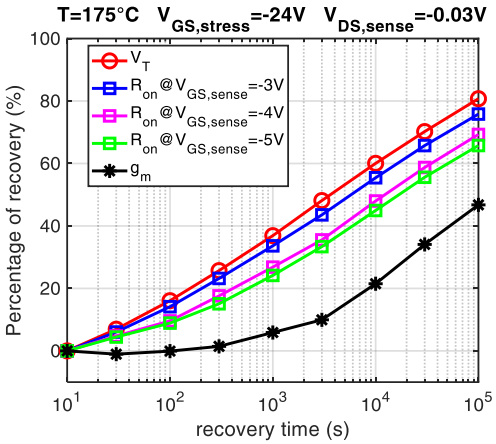


Fig. 13. Percentage of recovery as a function of the recovery time for V_T, R_{on} and g_m. after 10^5 s of HTGB stress. Percentage of recovery of a generic parameter P is calculated as $(1-\Delta P/\Delta P_{max})\cdot 100$, with ΔP_{max} being the shift at the end of the stress phase.

detrapping time comparable to T_{off} (0.5 s) iii) interface states generated during the stress phase are slowly recovered.

3.4. Analysis of recovery phase

At the end of the stress phase ($V_{GS,stress}$=-24V, T=175°C and stress time of 10^5 s), some of the devices are also tested under recovery conditions (V_{GS} = V_{DS} = 0V). The results of this analysis are reported in Fig. 13. Threshold voltage is significantly recovered (above 80%), while a lower recovery is observed for the transconductance (below 50%). An intermediate percentage of recovery is found for the on-resistance, depending of the considered $V_{GS,sense}$ value. According to the observations of section 3.3, we can assume that a significant component of V_T and R_{on} degradation is ascribed to the build-up of oxide charges (more easily recovered), while the g_m reduction is strongly related to interface states generation.

4. Conclusions

In this work we have analyzed the influence of HTGB on V_T, R_{on} and g_m in the case of p-channel trench-gate power MOSFETs. Experimental results reveal that the channel component of R_{on} is strongly influenced by HTGB, with a degradation larger than 20% under the considered stress conditions. On the other hand, the drift component is only slightly affected by HTGB. Hence, depending on the gate driving of the power MOSFET, HTGB could be a relevant issue. The analysis of defects shows that during the stress phase two phenomena are occurring: build-up of oxide

charges and interface states generation. Their evolutions with the stress is different, especially when considering switching stress conditions.

We also observed that V_T and R_{on} can be recovered faster with respect to g_m. This difference can be explained by the different impact of build-up of oxide charges and interface states generation. On the one hand, V_T and R_{on} (evaluated at low gate voltage) are strongly affected by build-up of charge. On the other hand, g_m is significantly influenced by interface states, which are slowly recovered.

Acknowledgements

This project has received funding from University of Padova, PRAT 2015 no. CPDA159190.

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