(19)

(11) **EP 2 555 242 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
23.07.2014 Bulletin 2014/30

(51) Int Cl.:
H01L 27/088 (2006.01) ***H01L 27/06*** (2006.01)
H01L 21/8252 (2006.01)

(21) Application number: **12178617.2**

(22) Date of filing: **31.07.2012**

(54) **Enhancement-/depletion-PHEMT device and manufacturing method thereof**

Verstärkungs-/Verarmungs-PHEMT-Vorrichtung und Herstellungsverfahren dafür

Dispositif PHEMT à enrichissement et appauvrissement et procédé pour sa fabrication

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **01.08.2011 IT TO20110713**

(43) Date of publication of application:
06.02.2013 Bulletin 2013/06

(73) Proprietor: **SELEX ES S.p.A.**
00131 Roma (IT)

(72) Inventors:
- **Chini, Alessandro**
  00131 ROMA (IT)
- **Lanzieri, Claudio**
  00131 ROMA (IT)

(74) Representative: **Bergadano, Mirko et al**
Studio Torta S.p.A.
Via Viotti, 9
10121 Torino (IT)

(56) References cited:

EP-A1- 0 371 686	**WO-A2-2006/083587**
JP-A- 63 222 462	**JP-A- 2009 032 729**
US-A1- 2006 208 279	**US-A1- 2008 251 837**
US-A1- 2010 001 318	**US-A1- 2011 049 526**

- **HURM V ET AL: "10 Gbit/s monolithic integrated optoelectronic receiver using an MSM photodiode and AlGaAs/GaAs HEMTs", MICROELECTRONIC ENGINEERING, ELSEVIER PUBLISHERS BV., AMSTERDAM, NL, vol. 15, no. 1-4, 1 October 1991 (1991-10-01), pages 275-278, XP024484431, ISSN: 0167-9317, DOI: 10.1016/0167-9317(91)90228-6 [retrieved on 1991-10-01]**
- **HSIEN-CHIN CHIU ET AL: "High uniformity enhancement and depletion-mode InGaP/InGaAs pHEMTs using a selective succinic acid gate recess process; High uniformity enhancement and depletion-mode InGaP/InGaAs pHEMTs", SEMICONDUCTOR SCIENCE AND TECHNOLOGY, IOP PUBLISHING LTD, GB, vol. 21, no. 1, 1 January 2006 (2006-01-01), pages 55-59, XP020098204, ISSN: 0268-1242, DOI: 10.1088/0268-1242/21/1/010**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 2 555 242 B1

Description

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates, in general, to enhancement/depletion Pseudomorphic High Electron Mobility Transistors (PHEMTs) and, in particular, to an enhancement/depletion PHEMT device and a method for manufacturing enhancement/depletion PHEMT devices that finds advantageous, but not exclusive, application in the production of integrated circuits operating at millimetre-wave and microwave frequencies.

STATE OF THE ART

[0002] As is known, Pseudomorphic High Electron Mobility Transistors (PHEMTs) are widely used in integrated circuits operating at millimetre-wave and microwave frequencies, such as the so-called Monolithic Microwave Integrated Circuits (MMICs).
[0003] In particular, PHEMTs are widely exploited in various types of system, such as radio communication systems and radar systems.
[0004] In detail, PHEMTs have found wide utilization over the years because they provide high Radio Frequency gain (RF gain), high Power Added Efficiency (PAE) and a low Noise Figure (NF).

OBJECT AND SUMMARY OF THE INVENTION

[0005] The applicant, in consideration of the excellent properties of PHEMTs that, as previously mentioned, have given rise to extensive usage thereof in various types of systems over the years, has carried out an in-depth study on currently-known enhancement/depletion PHEMT devices.
[0006] In particular, the applicant has carried out an exhaustive analysis regarding the characteristics of the enhancement/depletion PHEMT devices described in United States patent applications US 2006/0027840 and US 2006/0208279, in European patent application EP 0371686 and in United States patents US 6,670,652, US 6,703,638 and US 7,361,536.
[0007] On the basis of the results of said analysis, the applicant felt, thence, the need to develop:

- an innovative enhancement/depletion PHEMT device having superior properties than currently known enhancement/depletion PHEMT devices, in particular the enhancement/depletion PHEMT devices described in United States patent applications US 2006/0027840 and US 2006/0208279, in European patent application EP 0371686 and in United States patents US 6,670,652, US 6,703,638 and US 7,361,536; and
- an innovative method for manufacturing enhancement/depletion PHEMT devices.

[0008] Therefore, the object of the present invention is that of providing an enhancement/depletion PHEMT device and a method of manufacturing an enhancement/depletion PHEMT device.
[0009] This object is achieved by the present invention in that the latter relates to a layered epitaxial structure for enhancement/depletion PHEMT devices, to an enhancement/depletion PHEMT device and to a method for manufacturing an enhancement/depletion PHEMT device, according to that defined in the appended claims.
[0010] In particular, the layered epitaxial structure for PHEMT devices comprises:

- a superlattice and buffer layer;
- an undoped back-barrier layer formed on the superlattice and buffer layer and made of aluminium gallium arsenide (AlGaAs);
- a doped back delta doping layer formed on the back-barrier layer;
- an undoped back-spacer layer formed on the back delta doping layer and made of aluminium gallium arsenide (AlGaAs);
- an undoped channel layer formed on the back-spacer layer and made of indium gallium arsenide (InGaAs);
- an undoped spacer layer formed on the channel layer and made of aluminium gallium arsenide (AlGaAs);
- a delta doping layer formed on the spacer layer;
- an undoped enhancement barrier layer formed on the delta doping layer;
- a doped first etch stopper layer formed on the enhancement barrier layer and made of aluminium arsenide (AlAs);
- a doped first depletion barrier layer formed on the first etch stopper layer;
- an undoped second depletion barrier layer formed on the first depletion barrier layer;
- a doped second etch stopper layer formed on the second depletion barrier layer and made of aluminium arsenide (AlAs);
- a first cap layer doped with n-type doping, formed on the second etch stopper layer and made of gallium arsenide (GaAs);
- an undoped second cap layer formed on the first cap layer and made of gallium arsenide (GaAs);
- a third etch stopper layer doped with n-type doping, formed on the second cap layer and made of aluminium arsenide (AlAs); and
- an ohmic layer doped with n-type doping, formed on the third etch stopper layer and made of gallium arsenide (GaAs).

[0011] Furthermore, the enhancement/depletion PHEMT device according to the present invention comprises:

- the above-stated layered epitaxial structure;

- a first region comprising
  - a first recess vertically formed through the ohmic layer and the third etch stopper layer so as to expose a first upper surface of the second cap layer,
  - a second recess that is narrower than the first recess and which vertically extends from the first recess through the second cap layer, the first cap layer and the second etch stopper layer so as to expose a first upper surface of the second depletion barrier layer, and
  - a third recess that is narrower than the second recess and which vertically extends from the second recess through the second depletion barrier layer, the first depletion barrier layer and the first etch stopper layer so as to expose an upper surface of the enhancement barrier layer defining a first Schottky contact region;
- a second region laterally spaced apart, and electrically insulated, from said first region and comprising
  - a fourth recess vertically formed through the ohmic layer and the third etch stopper layer so as to expose a second upper surface of the second cap layer, and
  - a fifth recess that is narrower than the fourth recess and which vertically extends from the fourth recess through the second cap layer, the first cap layer and the second etch stopper layer so as to expose a second upper surface of the second depletion barrier layer defining a second Schottky contact region;
- an enhancement transistor formed in first region and comprising
  - first source and drain electrodes formed on, and in ohmic contact with, said ohmic layer in the first region externally to the first recess, and
  - a first gate electrode formed in the third recess in Schottky contact with the upper surface of the enhancement barrier layer defining the first Schottky contact region and extending vertically from said first Schottky contact region through the third, second and first recesses so as to protrude from said first recess; and
- a depletion transistor formed in second region and comprising
  - second source and drain electrodes formed on, and in ohmic contact with, said ohmic layer in the second region externally to the fourth recess, and
  - a second gate electrode formed in the fifth recess in Schottky contact with the second upper surface of the second depletion barrier layer defining the second Schottky contact region and extending vertically from said second Schottky contact region through the fifth and fourth recesses so as to protrude from said fourth recess.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] For a better understanding of the present invention, some preferred embodiments, provided by way of non-limitative example, will now be illustrated with reference to the attached drawings (not to scale), where:

- Figures 1-6 are schematic section views that illustrate successive manufacturing steps of a first enhancement/depletion PHEMT device according to a first preferred embodiment of the present invention; and
- Figures 7 and 8 are schematic section views of a second enhancement/depletion PHEMT device according to a second preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0013] The present invention will now be described in detail with reference to the attached Figures to enable an expert in the field to embody it and use it. Various modifications to the described embodiments will be immediately obvious to experts in the field, and the generic principles described herein can be applied to other embodiments and applications without leaving the scope of protection of the present invention, as defined in the appended claims. Therefore, the present invention should not be considered as limited to the embodiments described and illustrated herein, but be conceded the broadest scope of protection consistent with the principles and characteristics described and claimed herein.

[0014] Figures 1-6 are schematic section views that illustrate successive manufacturing steps of a first enhancement/depletion PHEMT device according to a first preferred embodiment of the present invention, said first enhancement/depletion PHEMT device being indicated as a whole in said Figures 1-6 by reference numeral 1.

[0015] In particular, with reference to Figure 1, the first enhancement/depletion PHEMT device 1 comprises a layered epitaxial structure that includes:

- a superlattice and buffer layer 11, the function of which mainly lies in enabling the growth of the layered epitaxial structure described herein and shown in Figure 1 on semi-insulating gallium arsenide (GaAs) substrates, ensuring effective confinement of electrons in a channel made of indium gallium arsenide (InGaAs) (said InGaAs channel being indicated in Figure 1 by reference numeral 15 and described in detail below) and avoiding the formation

of undesired conductive channels in the layers beneath the indium gallium arsenide (InGaAs) channel; one possible embodiment of said superlattice and buffer layer 11, which in any case envisages multiple alternative solutions, is that of alternating undoped layers of aluminium arsenide (AlAs) and gallium arsenide (GaAs) with thicknesses of around a few tens of nanometres (*nm*), repeating the growth of these layers roughly ten times; however, it is still possible to also make use of solutions that use layers of aluminium gallium arsenide (AlGaAs) instead of the layers of aluminium arsenide (AlAS) or, in any case, other epitaxial solutions used to eliminate the formation of parasitic electrically conductive channels;

- an undoped back-barrier layer 12, formed on the superlattice and buffer layer 11 and made of aluminium gallium arsenide (AlGaAs), said back-barrier layer 12 preferably having a weight concentration of aluminium (Al) within the range of *18%-28%* and a thickness greater than *0 nm* and less than or equal to *50 nm;*
- a doped back delta doping layer 13, formed on the back-barrier layer 12, said back delta doping layer 13 having a doping level greater than *0* and less than or equal to $4e^{12}$;
- an undoped back-spacer layer 14, formed on the back delta doping layer 13 and made of aluminium gallium arsenide (AlGaAs), said back-spacer layer 14 preferably having a weight concentration of aluminium (Al) within the range of *18%-28%* and a thickness within the range of *3-10 nm;*
- an undoped channel layer 15, formed on the back-spacer layer 14 and made of indium gallium arsenide (InGaAs), said channel layer 15 preferably having a weight concentration of indium (In) within the range of *15%-25%* and a thickness within the range of *10-20 nm;*
- an undoped spacer layer 16, formed on the channel layer 15 and made of aluminium gallium arsenide (AlGaAs), said spacer layer 16 preferably having a weight concentration of aluminium (Al) within the range of *18%-28%* and a thickness within the range of *3-10 nm;*
- a delta doping layer 17 formed on the spacer layer 16; in particular, said delta doping layer 17 can be undoped or doped with a doping level greater than 0 and less than or equal to $4e^{12}$;
- an undoped enhancement barrier layer 18, formed on the delta doping layer 17 and made of gallium arsenide (GaAs) (or aluminium gallium arsenide (AlGaAs), preferably with a weight concentration of aluminium (Al) within the range of *18%-28%*), said enhancement barrier layer 18 preferably having a thickness greater than *0 nm* and less than or equal to *30 nm;*
- a doped first etch stopper layer 19, formed on the enhancement barrier layer 18 and made of aluminium arsenide (AlAs), said first etch stopper layer 19 preferably having a doping level greater than *0* and less than or equal to $6e^{18}$, and a thickness within the range of *1.5-2.5 nm;*
- a doped first depletion barrier layer 20, formed on the first etch stopper layer 19 and made of gallium arsenide (GaAs) (or aluminium gallium arsenide (AlGaAs), preferably with a weight concentration of aluminium (Al) within the range of *18%-28%*), said first depletion barrier layer 20 preferably having a thickness within the range of *10-30 nm* and a doping level greater than *0* and less than or equal to $6e^{18}$;
- an undoped second depletion barrier layer 21, formed on the first depletion barrier layer 20 and made of gallium arsenide (GaAs) (or aluminium gallium arsenide (AlGaAs), preferably with a weight concentration of aluminium (Al) within the range of *18%-28%*), said second depletion barrier layer 21 preferably having a thickness greater than *0 nm* and less than or equal to *10 nm*;
- a doped second etch stopper layer 22, formed on the second depletion barrier layer 21 and made of aluminium arsenide (AlAs), said second etch stopper layer 22 preferably having a doping level greater than *0* and less than or equal to $6e^{18}$ and a thickness within the range of *1.5-2.5 nm;*
- a first cap layer 23 doped with n-type doping, formed on the second etch stopper layer 22 and made of gallium arsenide (GaAs), said first cap layer 23 preferably having a doping level within the range of $1e^{17}$-$6e^{17}$ and a thickness within the range of *20-50 nm;*
- an undoped second cap layer 24 formed on the first cap layer 23, said second cap layer 24 preferably having a thickness greater than *0 nm* and less than or equal to *10 nm;*
- a third etch stopper layer 25 doped with n-type doping, formed on the second cap layer 24 and made of aluminium arsenide (AlAs), said third etch stopper layer 25 preferably having a doping level within the range of $1e^{18}$-$6e^{18}$ and a thickness within the range of *1.5-2.5 nm;* and
- an ohmic layer 26 doped with n-type doping, formed on the third etch stopper layer 25 and made of gallium arsenide (GaAs), said ohmic layer 26 preferably having a doping level within the range of $1e^{18}$-$6e^{18}$ and a thickness within the range of *30-70 nm.*

[0016] Again with reference to Figure 1, the first enhancement/depletion PHEMT device 1 also comprises:

- a first region 27 in which an enhancement transistor is manufactured, as will be described in detail below;
- a second region 28 that is laterally spaced apart from the first region 27 and in which a depletion transistor is manufactured, as will be described in detail below;
- a first pair of electrodes 29 comprising a first source electrode and a first drain electrode arranged in the first region 27; said first source electrode being formed on, and in ohmic contact with, a first portion

of the ohmic layer 26 extending in the first region 27 and defining a first ohmic contact region; said first drain electrode being formed on, and in ohmic contact with, a second portion of the ohmic layer 26 extending in the first region 27 and defining a second ohmic contact region laterally spaced apart from the first ohmic contact region, in particular preferably set apart at a distance within the range of *3-6* μm; and

- a second pair of electrodes 30 comprising a second source electrode and a second drain electrode arranged in the second region 28; said second source electrode being formed on, and in ohmic contact with, a third portion of the ohmic layer 26 extending in the second region 28 and defining a third ohmic contact region; said second drain electrode being formed on, and in ohmic contact with, a fourth portion of the ohmic layer 26 extending in the second region 28 and defining a fourth ohmic contact region laterally spaced apart from the third ohmic contact region, in particular preferably set apart at a distance within the range of *3-6* μm.

[0017] Preferably said pairs of electrodes 29 and 30 are manufactured by forming a first mask (for simplicity, not shown in Figure 1) on the ohmic layer 26 so as to leave only the four ohmic contact regions exposed. Said first mask is conveniently formed by means of a layer of photoresist deposited on the ohmic layer 26 and patterned so as to form a respective window on each ohmic contact region. The metallizations of the source and drain electrodes are then deposited on the four ohmic contact regions through the four windows of the first mask and are subjected to an annealing treatment.

[0018] After having made the pairs of electrodes 29 and 30, the first region 27 and the second region 28 of the first enhancement/depletion PHEMT device 1 are electrically insulated through ion implantation.

[0019] In particular, again with reference to Figure 1, a first electrical insulation barrier 31 and a second electrical insulation barrier 32 are formed by ion implantation in the layered epitaxial structure external to the first region 27 and the second region 28, respectively, so as to laterally surround, and therefore electrically insulate, said first region 27 and said second region 28, respectively.

[0020] The ion implantation is preferably carried out using a second mask (for simplicity, not shown in Figure 1) formed on the first enhancement/depletion PHEMT device 1 so as to cover the first region 27 and the second region 28, or rather so as to leave exposed the upper surfaces of a fifth and a sixth portion of the ohmic layer 26 that extend externally to said first region 27 and to said second region 28, respectively.

[0021] Said second mask is conveniently formed by means of a layer of photoresist deposited on the first enhancement/depletion PHEMT device 1 and patterned so as to form a first opening on the upper surface of the fifth portion of the ohmic layer 26 and a second opening on the upper surface of the sixth portion of the ohmic layer 26. The ion implantation is then carried out so as to implant ions through the two openings of the second mask and into the fifth and sixth portions of the ohmic layer 26 and also into the corresponding underlying portions of all layers of the layered epitaxial structure, i.e. up to the superlattice and buffer layer 11.

[0022] With reference to Figure 2, after having electrically insulated the first region 27 and the second region 28 of the enhancement/depletion PHEMT device 1, a first recess 33 and a second recess 34 are formed in said first region 27 and in said second region 28, respectively.

[0023] In particular, said first recess 33 is formed through a seventh portion of the ohmic layer 26 extending in the first region 27 and laterally spaced apart from the first and second portions of the ohmic layer 26, i.e. from the first and the second ohmic contact regions, and also through a first portion of the third etch stopper layer 25 extending in the first region 27 beneath said seventh portion of the ohmic layer 26, so as to leave exposed an upper surface of a first portion of the second cap layer 24 extending in the first region 27 beneath said first portion of the third etch stopper layer 25.

[0024] Furthermore, said second recess 34 is formed through an eighth portion of the ohmic layer 26 extending in the second region 28 and laterally spaced apart from the third and fourth portions of the ohmic layer 26, i.e. from the third and fourth ohmic contact regions, and also through a second portion of the third etch stopper layer 25 extending in the second region 28 beneath said eighth portion of the ohmic layer 26, so as to leave exposed an upper surface of a second portion of the second cap layer 24 extending in the second region 28 beneath said second portion of the third etch stopper layer 25.

[0025] In order to form said first recess 33 and said second recess 34, a third mask 35 is preferably formed on the first enhancement/depletion PHEMT device 1 so as to leave only the upper surfaces of the seventh and eighth portions of the ohmic layer 26 exposed.

[0026] Said third mask 35 is conveniently formed by means of a layer of photoresist deposited on the first enhancement/depletion PHEMT device 1 and patterned so as to form a first window 35a on the upper surface of the seventh portion of the ohmic layer 26 and a second window 35b on the upper surface of the eighth portion of the ohmic layer 26, said first window 35a and said second window 35b of the third mask 35 having a lateral width preferably within the range of *2-5* μm.

[0027] After having formed the third mask 35, the first recess 33 and the second recess 34 are formed by means of a first etching process, dry or wet, carried out through the first window 35a and the second window 35b of said third mask 35.

[0028] In particular, said first etching process, which can be carried out by means of a single chemical solution or an opportune sequence of chemical solutions, removes:

- the seventh portion of the ohmic layer 26 and also

the underlying first portion of the third etch stopper layer 25, stopping at the interface with the second cap layer 24 so as to leave exposed the upper surface of the first portion of said second cap layer 24 extending in the first region 27 beneath the first portion of the third etch stopper layer 25 removed by said first etching process; and

- the eighth portion of the ohmic layer 26 and also the underlying second portion of the third etch stopper layer 25, stopping at the interface with the second cap layer 24 so as to leave exposed the upper surface of the second portion of said second cap layer 24 extending in the second region 28 beneath the second portion of the third etch stopper layer 25 removed by said first etching process.

[0029] With reference to Figure 3, after having formed the first recess 33 and the second recess 34, a third recess 36 is formed in the first region 27.

[0030] In particular, said third recess 36 is formed through a first sub-portion of the first portion of the second cap layer 24, through a first portion of the first cap layer 23 extending in the first region 27 beneath said first sub-portion of the first portion of the second cap layer 24, and also through a first portion of the second etch stopper layer 22 extending in the first region 27 beneath said first portion of the first cap layer 23, so as to leave exposed an upper surface of a first portion of the second depletion barrier layer 21 extending in the first region 27 beneath said first portion of the second etch stopper layer 22.

[0031] In order to form said third recess 36, a fourth mask 37 is preferably formed on the first enhancement/depletion PHEMT device 1 so as to leave exposed only an upper surface of the first sub-portion of the first portion of the second cap layer 24.

[0032] Said fourth mask 37 is conveniently formed by means of a layer of photoresist deposited on the first enhancement/depletion PHEMT device 1 and patterned so as to form a window 37a on the upper surface of the first sub-portion of the first portion of the second cap layer 24, said window 37a of the fourth mask 37 having a lateral width preferably within the range of *0.1-0.5* μm.

[0033] After having formed the fourth mask 37, the third recess 36 is formed by means of a second etching process, dry or wet, carried out through the window 37a of said fourth mask 37.

[0034] In particular, said second etching process, which can be carried out by means of a single chemical solution or an opportune sequence of chemical solutions, removes the first sub-portion of the first portion of the second cap layer 24, the first portion of the first cap layer 23 and also the first portion of the second etch stopper layer 22, stopping at the interface with the second depletion barrier layer 21 so as to leave exposed the upper surface of the first portion of said second depletion barrier layer 21 extending in the first region 27 beneath the first portion of the second etch stopper layer 22 removed by said second etching process.

[0035] With reference to Figure 4, after having formed the third recess 36, said third recess 36 is widened, forming a widened third recess 36* extending in the first region 27 and a fourth recess 38 and a fifth recess 39 are simultaneously formed in the first region 27 and in the second region 28, respectively.

[0036] In particular, said widened third recess 36* is formed through a second sub-portion of the first portion of the second cap layer 24 that extends in the first region 27 and that, before said widening, laterally surrounds the third recess 36, through a second portion of the first cap layer 23 that extends in the first region 27 beneath said second sub-portion of the first portion of the second cap layer 24 and that, before said widening, laterally surrounds the third recess 36, and also through a second portion of the second etch stopper layer 22 that extends in the first region 27 beneath said second portion of the first cap layer 23 and that, before said widening, laterally surrounds the third recess 36, so as to leave exposed an upper surface of a second portion of the second depletion barrier layer 21 that extends in the first region 27 beneath said second portion of the second etch stopper layer 22, and that, before the formation of the fourth recess 38, laterally surrounds the first portion of the second depletion barrier layer 21, while, after the formation of the fourth recess 38, laterally surrounds said fourth recess 38.

[0037] Furthermore, said fourth recess 38 is formed through the first portion of the second depletion barrier layer 21, through a portion of the first depletion barrier layer 20 extending in the first region 27 beneath said first portion of the second depletion barrier layer 21, and also through a portion of the first etch stopper layer 19 extending in the first region 27 beneath said portion of the first depletion barrier layer 20, so as to leave exposed an upper surface of a portion of the enhancement barrier layer 18 that extends in the first region 27 beneath said portion of the first etch stopper layer 19 and defines a first Schottky contact region.

[0038] Furthermore, said fifth recess 39 is formed through a first sub-portion of the second portion of the second cap layer 24, through a third portion of the first cap layer 23 extending in the second region 28 beneath said first sub-portion of the second portion of the second cap layer 24, and also through a third portion of the second etch stopper layer 22 extending in the second region 28 beneath said third portion of the first cap layer 23, so as to leave exposed an upper surface of a third portion of the second depletion barrier layer 21 that extends in the second region 28 beneath said third portion of the second etch stopper layer 22 and defines a second Schottky contact region.

[0039] In order to widen said third recess 36 and to form said fourth recess 38 and said fifth recess 39, a fifth mask 40 is preferably formed on the first enhancement/depletion PHEMT device 1 so as to leave exposed only the upper surfaces of the second sub-portion of the first portion of the second cap layer 24, of the first portion of the second depletion barrier layer 21 and of the first

sub-portion of the second portion of the second cap layer 24.

[0040] Said fifth mask 40 is conveniently formed by means of a layer of photoresist deposited on the first enhancement/depletion PHEMT device 1 and patterned so as to form:

- a first window 40a on the third recess 36 and the upper surface of the second sub-portion of the first portion of the second cap layer 24 that laterally surrounds said third recess 36; and
- a second window 40b on the upper surface of the first sub-portion of the second portion of the second cap layer 24. Preferably, said first window 40a and said second window 40b of the fifth mask 40 have a lateral width within the range of *0.2-0.7* μm or even greater.

[0041] After having formed the fifth mask 40, the widened third recess 36*, the fourth recess 38 and the fifth recess 39 are formed by means of a third etching process, dry or wet, carried out through the first window 40a and the second window 40b of said fifth mask 40.

[0042] In particular, said third etching process, which can be carried out by means of a single chemical solution or an opportune sequence of chemical solutions, removes:

- the second sub-portion of the first portion of the second cap layer 24, the second portion of the first cap layer 23 and the second portion of the second etch stopper layer 22, stopping at the interface with the second depletion barrier layer 21 so as to leave exposed the upper surface of the second portion of said second depletion barrier layer 21 extending beneath the second portion of the second etch stopper layer 22 removed by said third etching process;
- the first portion of the second depletion barrier layer 21, the underlying portion of the first depletion barrier layer 20 and the underlying portion of the first etch stopper layer 19, stopping at the interface with the enhancement barrier layer 18 so as to leave exposed the upper surface of the portion of said enhancement barrier layer 18 that extends beneath the portion of the first etch stopper layer 19 removed by said third etching process and that defines said first Schottky contact region; and
- the first sub-portion of the second portion of the second cap layer 24, the third portion of the first cap layer 23 and the third portion of the second etch stopper layer 22, stopping at the interface with the second depletion barrier layer 21 so as to leave exposed the upper surface of the third portion of said second depletion barrier layer 21 that extends beneath the third portion of the second etch stopper layer 22 removed by said third etching process and that defines said second Schottky contact region.

[0043] With reference to Figures 5 and 6, after having formed the widened third recess 36*, the fourth recess 38 and the fifth recess 39, a first gate electrode 41 and a second gate electrode 42 are formed in the first region 27 and in the second region 28, respectively, thereby making an enhancement transistor in the first region 27 and a depletion transistor in the second region 28.

[0044] In particular, said first gate electrode 41 is formed in the fourth recess 38, in the widened third recess 36* and in the first recess 33, and said second gate electrode 42 is formed in the fifth recess 39 and in the second recess 34.

[0045] In detail, the first gate electrode 41 is formed so as to comprise:

- a Schottky contact portion that is formed on, and is in Schottky contact with, said portion of the enhancement barrier layer 18 defining the first Schottky contact region, vertically extending through all of the fourth recess 38, and can adhere or not adhere to the lateral walls of the fourth recess 38; and
- a field plate portion that vertically extends through all of the widened third recess 36* and all of the first recess 33 arriving to protrude in height from said first recess 33, laterally extending on the upper surface of the second portion of the second depletion barrier layer 21 that laterally surrounds the fourth recess 38 so as to rest on and be mechanically supported by said second portion of the second depletion barrier layer 21, and can adhere or not adhere to the lateral walls of the widened third recess 36*.

[0046] Furthermore, the second gate electrode 42 is formed on, and is in Schottky contact with, said third portion of the second depletion barrier layer 21 defining the second Schottky contact region, is formed so as to vertically extend through all of the fifth recess 39 and all of the second recess 34 arriving to protrude in height from said second recess 34, and can adhere or not adhere to the lateral walls of the fifth recess 39.

[0047] Preferably, as shown in Figure 5, said gate electrodes 41 and 42 are made using the fifth mask 40.

[0048] In particular, the first gate electrode 41 is preferably made by means of chemical vapour deposition self-aligned to the first window 40a of the fifth mask 40 and the second gate electrode 42 is preferably made by means of chemical vapour deposition self-aligned to the second window 40b of said fifth mask 40.

[0049] Figure 6 shows the first enhancement/depletion PHEMT device 1 comprising the enhancement transistor made in the first region 27 and the depletion transistor made in the second region 28 after removal of the fifth mask 40.

[0050] Figures 7 and 8 are schematic section views of a second enhancement/depletion PHEMT device made according to a second preferred embodiment of the present invention, said second enhancement/depletion PHEMT device being indicated as a whole in said Figures

7 and 8 by reference numeral 1'.

[0051] In particular, the second enhancement/depletion PHEMT device 1' is made with the same manufacturing process described in relation to the first enhancement/depletion PHEMT device 1 up to the step of forming the widened third recess 36*, the fourth recess 38 and the fifth recess 39, while the step of forming the gate electrodes of the second enhancement/depletion PHEMT device 1' is different from that previously described in relation to the enhancement/depletion PHEMT device 1.

[0052] In detail, with reference to Figures 7 and 8, after having formed the widened third recess 36*, the fourth recess 38 and the fifth recess 39, a first gate electrode 43 and a second gate electrode 44 of the second enhancement/depletion PHEMT device 1' are formed in the first region 27 and in the second region 28, respectively, of the second enhancement/depletion PHEMT device 1', thereby making an enhancement transistor in said first region 27 of the second enhancement/depletion PHEMT device 1' and a depletion transistor in said second region 28 of the enhancement/depletion PHEMT device 1'. In particular, said first gate electrode 43 of the enhancement transistor of the second enhancement/depletion PHEMT device 1' is formed in the fourth recess 38, in the widened third recess 36* and in the first recess 33, while said second gate electrode 44 of the depletion transistor of the second enhancement/depletion PHEMT device 1' is formed in the fifth recess 39 and in the second recess 34.

[0053] Entering into even greater detail, the first gate electrode 43 of the enhancement transistor of the second enhancement/depletion PHEMT device 1' is formed so as to comprise:

- a respective Schottky contact portion that is formed on, and is in Schottky contact with, said portion of the enhancement barrier layer 18 defining the first Schottky contact region, vertically extending through all of the fourth recess 38, and can adhere or not adhere to the lateral walls of the fourth recess 38; and
- a respective field plate portion that vertically extends through all of the widened third recess 36* and all of the first recess 33 arriving to protrude in height from said first recess 33, laterally extending on the upper surface of the second portion of the second depletion barrier layer 21 that laterally surrounds the fourth recess 38 so as to rest on and be mechanically supported by said second portion of the second depletion barrier layer 21, also laterally extending on the upper surface of a third sub-portion of the first portion of the second cap layer 24 that laterally surrounds the widened third recess 36* so as to rest on and be mechanically supported by said third sub-portion of the first portion of the second cap layer 24, and can adhere or not adhere to the lateral walls of the widened third recess 36*.

[0054] Furthermore, the second gate electrode 44 of the depletion transistor of the second enhancement/depletion PHEMT device 1' is formed so as to comprise:

- a respective Schottky contact portion that is formed on, and is in Schottky contact with, said third portion of the second depletion barrier layer 21 defining the second Schottky contact region, vertically extending through all of the fifth recess 39, and can adhere or not adhere to the lateral walls of the fifth recess 39; and
- a respective field plate portion that vertically extends through all of the second recess 34 arriving to protrude in height from said second recess 34, and laterally extending on the upper surface of a second sub-portion of the second portion of the second cap layer 24 that laterally surrounds the fifth recess 39 so as to rest on and be mechanically supported by said second sub-portion of the second portion of the second cap layer 24.

[0055] Preferably, as shown in Figure 7, in order to form said gate electrodes 43 and 44 of the second enhancement/depletion PHEMT device 1', a sixth mask 45 is formed on the second enhancement/depletion PHEMT device 1' so as to leave exposed only the upper surfaces of the portion of the enhancement barrier layer 18 defining the first Schottky contact region, of the second portion of the second depletion barrier layer 21 that laterally surrounds the fourth recess 38, of the third sub-portion of the first portion of the second cap layer 24 that laterally surrounds the widened third recess 36*, of the third portion of the second depletion barrier layer 21 defining the second Schottky contact region and of the second sub-portion of the second portion of the second cap layer 24 that laterally surrounds the fifth recess 39.

[0056] Said sixth mask 45 is conveniently formed by means of a layer of photoresist deposited on the second enhancement/depletion PHEMT device 1' and patterned so as to form:

- a first window 45a on the widened third recess 36* and the upper surface of the third sub-portion of the first portion of the second cap layer 24 that laterally surrounds said widened third recess 36*; and
- a second window 45b on the fifth recess 39 and the upper surface of the second sub-portion of the second portion of the second cap layer 24 that laterally surrounds said fifth recess 39.

[0057] After having formed the sixth mask 45, the first gate electrode 43 of the enhancement transistor of the second enhancement/depletion PHEMT device 1' is preferably made by means of chemical vapour deposition self-aligned to the first window 45a of the sixth mask 45, and the second gate electrode 44 of the depletion transistor of the second enhancement/depletion PHEMT device 1' is preferably made by means of chemical vapour deposition self-aligned to the second window 45b of said

sixth mask 45.

[0058] Figure 8 shows the second enhancement/depletion PHEMT device 1' comprising the enhancement transistor made in the first region 27 and the depletion transistor made in the second region 28 after removal of the sixth mask 45.

[0059] The present invention has numerous advantages.

[0060] In particular, according to the present invention the etch stopper layers 19, 22 and 25, which enable making the first recess 33, the second recess 34, the third recess 36, the widened third recess 36*, the fourth recess 38 and the fifth recess 39 in a controlled manner, are made of aluminium arsenide (AlAs) instead of indium gallium phosphide (InGaP) as in currently known enhancement/depletion PHEMT devices. This innovative characteristic of the present invention ensures that the previously described manufacturing processes have high uniformity and high repeatability.

[0061] Furthermore, according to the present invention:

- the undoped enhancement barrier layer 18 enables reducing leakage current from the Schottky contact portions of the first gate electrodes 41 and 43 of the enhancement transistors that are formed on, and in Schottky contact with, said enhancement barrier layer 18;
- the undoped second depletion barrier layer 21 enables reducing leakage current from the field plate portions of the first gate electrodes 41 and 43 of the enhancement transistors that rest on and are mechanically supported by said second depletion barrier layer 21;
- the undoped second depletion barrier layer 21 enables reducing leakage current from the Schottky contact portions of the second gate electrodes 42 and 44 of the depletion transistors that are formed on, and in Schottky contact with, said second depletion barrier layer 21; and
- the undoped second cap layer 24 enables reducing leakage current from the field plate portions of the first gate electrode 43 and of the second gate electrode 44 of the second enhancement/depletion PHEMT device 1' that rest on and are mechanically supported by said second cap layer 24.

[0062] In addition, the layered epitaxial structure and the manufacturing processes according to the present invention enable preventing the aluminium-based layers from being exposed to air, so as to reduce the phenomena of current breakdown often observed when aluminium-based layers are exposed to air.

[0063] Furthermore, the enhancement barrier layer 18, the first depletion barrier layer 20, the second depletion barrier layer 21, the first cap layer 23, the second cap layer 24 and the ohmic layer 26 made, according to a preferred embodiment of the present invention, in gallium arsenide (GaAs) instead of aluminium gallium arsenide (AlGaAs) as in currently known enhancement/depletion PHEMT devices enables obtaining a lower barrier for the electrons that flow between the source and drain contacts in the enhancement transistor channel and in the depletion transistor channel.

[0064] Finally, the manufacturing of the field plate portions of the gate electrodes enables reducing the output conductance of the enhancement transistors and the depletion transistors, said output conductance representing a critical factor for the performance of digital circuits.

Claims

1. A layered epitaxial structure for enhancement and depletion PHEMT devices (1;1'), comprising:

- a superlattice and buffer layer (11);
- an undoped back-barrier layer (12) formed on the superlattice and buffer layer (11) and made of aluminium gallium arsenide (AlGaAs);
- a doped back delta doping layer (13) formed on the back-barrier layer (12);
- an undoped back-spacer layer (14) formed on the back delta doping layer (13) and made of aluminium gallium arsenide (AlGaAs) ;
- an undoped channel layer (15) formed on the back-spacer layer (14) and made of indium gallium arsenide (InGaAs) ;
- an undoped spacer layer (16) formed on the channel layer (15) and made of aluminium gallium arsenide (AlGaAs);
- a delta doping layer (17) formed on the spacer layer (16);
- an undoped enhancement barrier layer (18) formed on the delta doping layer (17);
- a doped first etch stopper layer (19), formed on the enhancement barrier layer (18) and made of aluminium arsenide (AlAs);
- a doped first depletion barrier layer (20) formed on the first etch stopper layer (19);
- an undoped second depletion barrier layer (21) formed on the first depletion barrier layer (20);
- a doped second etch stopper layer (22) formed on the second depletion barrier layer (21) and made of aluminium arsenide (AlAs) ;
- a first cap layer (23) doped with n-type doping, formed on the second etch stopper layer (22) and made of gallium arsenide (GaAs);
- an undoped second cap layer (24) formed on the first cap layer (23) and made of gallium arsenide (GaAs);
- a third etch stopper layer (25) doped with n-type doping, formed on the second cap layer (24) and made of aluminium arsenide (AlAs); and
- an ohmic layer (26) doped with n-type doping,

formed on the third etch stopper layer (25) and made of gallium arsenide (GaAs).

2. The layered epitaxial structure of claim 1, wherein the enhancement barrier layer (18), the first depletion barrier layer (20) and the second depletion barrier layer (21) are made of gallium arsenide (GaAs).

3. An enhancement/depletion PHEMT device (1;1') comprising:

- the layered epitaxial structure claimed in claim 1 or 2 ;
- a first region (27) comprising

  - a first recess (33) vertically formed through the ohmic layer (26) and the third etch stopper layer (25) so as to expose a first upper surface of the second cap layer (24),
  - a second recess (36*) that is narrower than the first recess (33) and which vertically extends from the first recess (33) through the second cap layer (24), the first cap layer (23) and the second etch stopper layer (22) so as to expose a first upper surface of the second depletion barrier layer (21), and
  - a third recess (38) that is narrower than the second recess (36*) and which vertically extends from the second recess (36*) through the second depletion barrier layer (21), the first depletion barrier layer (20) and the first etch stopper layer (19) so as to expose an upper surface of the enhancement barrier layer (18) defining a first Schottky contact region;

- a second region (28) laterally spaced apart, and electrically insulated, from said first region (27) and comprising

  - a fourth recess (34) vertically formed through the ohmic layer (26) and the third etch stopper layer (25) so as to expose a second upper surface of the second cap layer (24), and
  - a fifth recess (39) that is narrower than the fourth recess (34) and which vertically extends from the fourth recess (34) through the second cap layer (24), the first cap layer (23) and the second etch stopper layer (22) so as to expose a second upper surface of the second depletion barrier layer (21) defining a second Schottky contact region;

- an enhancement transistor formed in the first region (27) and comprising

  - first source and drain electrodes (29) formed on, and in ohmic contact with, said ohmic layer (26) in the first region (27) externally to the first recess (33), and
  - a first gate electrode (41;43) formed in the third recess (38) in Schottky contact with the upper surface of the enhancement barrier layer (18) defining the first Schottky contact region and extending vertically from said first Schottky contact region through the third (38), the second (36*) and the first recess (33) so as to protrude from said first recess (33); and

- a depletion transistor formed in the second region (28) and comprising

  - second source and drain electrodes (30) formed on, and in ohmic contact with, said ohmic layer (26) in the second region (28) externally to the fourth recess (34), and
  - a second gate electrode (42;44) formed in the fifth recess (39) in Schottky contact with the second upper surface of the second depletion barrier layer (21) defining the second Schottky contact region and extending vertically from said second Schottky contact region through the fifth (39) and the fourth recess (34) so as to protrude from said fourth recess (34).

4. The enhancement/depletion PHEMT device of claim 3, wherein the first gate electrode (41;43) comprises a field plate portion that laterally extends in the second recess (36*) on the first upper surface of the second depletion barrier layer (21) so as to rest on and be mechanically supported by said first upper surface of the second depletion barrier layer (21).

5. The enhancement/depletion PHEMT device of claim 4, wherein the field plate portion of the first gate electrode (43) laterally extends in the first recess (33) on a portion of the first upper surface of the second cap layer (24) so as to rest on and be mechanically supported by said portion of the first upper surface of the second cap layer (24).

6. The enhancement/depletion PHEMT device according to any of claims 3-5, wherein the second gate electrode (44) comprises a field plate portion that laterally extends in the fourth recess (34) on a portion of the second upper surface of the second cap layer (24) so as to rest on and be mechanically supported by said portion of the second upper surface of the second cap layer (24).

7. A method of manufacturing an enhancement/depletion PHEMT device, comprising:

• providing a layered epitaxial structure that includes

- a superlattice and buffer layer (11),
- an undoped back-barrier layer (12) formed on the superlattice and buffer layer (11) and made of aluminium gallium arsenide (AlGaAs),
- a doped back delta doping layer (13) formed on the back-barrier layer (12),
- an undoped back-spacer layer (14) formed on the back delta doping layer (13) and made of aluminium gallium arsenide (AlGaAs),
- an undoped channel layer (15) formed on the back-spacer layer (14) and made of indium gallium arsenide (InGaAs),
- an undoped spacer layer (16) formed on the channel layer (15) and made of aluminium gallium arsenide (AlGaAs),
- a delta doping layer (17) formed on the spacer layer (16),
- an undoped enhancement barrier layer (18) formed on the delta doping layer (17),
- a doped first etch stopper layer (19) formed on the enhancement barrier layer (18) and made of aluminium arsenide (AlAs),
- a doped first depletion barrier layer (20) formed on the first etch stopper layer (19),
- an undoped second depletion barrier layer (21) formed on the first depletion barrier layer (20),
- a doped second etch stopper layer (22) formed on the second depletion barrier layer (21) and made of aluminium arsenide (AlAs),
- a first cap layer (23) doped with n-type doping, formed on the second etch stopper layer (22) and made of gallium arsenide (GaAs),
- an undoped second cap layer (24) formed on the first cap layer (23) and made of gallium arsenide (GaAs),
- a third etch stopper layer (25) doped with n-type doping, formed on the second cap layer (24) and made of aluminium arsenide (AlAs), and
- a ohmic layer (26) doped with n-type doping, formed on the third etch stopper layer (25) and made of gallium arsenide (GaAs) ;

• forming a first pair of electrodes (29) of an enhancement transistor on, and in ohmic contact with, said ohmic layer (26) in a first region (27) of the layered epitaxial structure and a second pair of electrodes (30) of a depletion transistor on, and in ohmic contact with, said ohmic layer (26) in a second region (28) of the layered epitaxial structure laterally spaced apart from said first region (27), said first pair of electrodes (29) comprising a first source electrode and a first drain electrode, said second pair of electrodes (30) comprising a second source electrode and a second drain electrode;
• electrically insulating the first region (27) and the second region (28);
• forming

- in the first region (27), a first recess (33) that is laterally spaced apart from the first pair of electrodes (29) and which vertically extends through the ohmic layer (26) and the third etch stopper layer (25) so as to expose a first upper surface of the second cap layer (24), and
- in the second region (28), a second recess (34) that is laterally spaced apart from the second pair of electrodes (30) and which vertically extends through the ohmic layer (26) and the third etch stopper layer (25) so as to expose a second upper surface of the second cap layer (24);

• forming

- in the first region (27), a third recess (36*) that is narrower than the first recess (33) and which vertically extends from the first recess (33) through the second cap layer (24), the first cap layer (23) and the second etch stopper layer (22) so as to expose a first upper surface of the second depletion barrier layer (21),
- in the first region (27), a fourth recess (38) that is narrower than the third recess (36*) and which vertically extends from the third recess (36*) through the second depletion barrier layer (21), the first depletion barrier layer (20) and the first etch stopper layer (19) so as to expose an upper surface of the enhancement barrier layer (18) defining a first Schottky contact region, and
- in the second region (28), a fifth recess (39) that is narrower than the second recess (34) and which vertically extends from the second recess (34) through the second cap layer (24), the first cap layer (23) and the second etch stopper layer (22) so as to expose a second upper surface of the second depletion barrier layer (21) defining a second Schottky contact region; and

• forming

- in the fourth recess (38), a first gate electrode (41;43) of the enhancement transistor

in Schottky contact with the upper surface of the enhancement barrier layer (18) defining the first Schottky contact region, said first gate electrode (41;43) vertically extending from said first Schottky contact region through the fourth (38), the third (36*) and the first recess (33) so as to protrude from said first recess (33), and
- in the fifth recess (39), a second gate electrode (42;44) of the depletion transistor in Schottky contact with the second upper surface of the second depletion barrier layer (21) defining the second Schottky contact region, said second gate electrode (42;44) vertically extending from said second Schottky contact region through the fifth (39) and the second recess (34) so as to protrude from said second recess (34).

8. The method of claim 7, wherein forming the third recess (36*), the fourth recess (38) and the fifth recess (39) comprises:

- forming a third recess (36) by means of a first etching process carried out by using a first mask (37) formed on the layered epitaxial structure, on the first pair of electrodes (29) and on the second pair of electrodes (30) so as to expose a first portion of the first upper surface of the second cap layer (24) to said first etching process; and
- widening said third recess (36) and forming the fourth recess (38) and the fifth recess (39) by means of a second etching process carried out by using a second mask (40) formed on the layered epitaxial structure, on the first pair of electrodes (29) and on the second pair of electrodes (30) so as to expose the third recess (36), a second portion of the first upper surface of the second cap layer (24) laterally extending from said third recess (36) and a first portion of the second upper surface of the second cap layer (24) to said second etching process.

9. The method of claim 8, wherein the first gate electrode (41) and the second gate electrode (42) are formed by means of chemical vapour deposition carried out by using the second mask (40).

10. The method of claim 8, wherein the first gate electrode (43) and the second gate electrode (44) are formed by means of chemical vapour deposition carried out by using a third mask (45) formed on the layered epitaxial structure, on the first pair of electrodes (29) and on the second pair of electrodes (30) so as to expose the fourth recess (38), the widened third recess (36*), a third portion of the first upper surface of the second cap layer (24) laterally extending from said widened third recess (36*), the fifth recess (39) and a second portion of the second upper surface of the second cap layer (24) laterally extending from said fifth recess (39) to the chemical vapour deposition.

11. The method according to any of claims 7-10, wherein electrically insulating the first region (27) and the second region (28) comprises forming by ionic implantation:

- a first electrical insulation barrier (31) surrounding the first region (27) and vertically extending through all the layers of the layered epitaxial structure; and
- a second electrical insulation barrier (32) surrounding the second region (28) and vertically extending through all the layers of the layered epitaxial structure.

Patentansprüche

1. Eine geschichtete epitaktische Struktur für Anreicherungs- und Verarmungs- PHEMT-Vorrichtungen (1; 1'), umfassend:

ein Übergitter und eine Pufferschicht (11);
eine auf dem Übergitter und der Puffer Schicht (11) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Rücksperrschicht (12);
eine auf der Rücksperrschicht (12) ausgebildete dotierte Rückdeltadotierungsschicht (13);
eine auf der Rückdeltadotierungsschicht (13) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Rückabstandsschicht (14);
eine auf der Rückabstandsschicht (14) ausgebildete und aus Indiumgalliumarsenid (InGaAs) hergestellte undotierte Kanalschicht (15);
eine auf der Kanalschicht (15) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Abstandsschicht (16);
eine auf der Abstandsschicht (16) ausgebildete Deltadotierungsschicht (17);
eine auf der Deltadotierungsschicht (17) ausgebildete undotierte Anreicherungssperrschicht (18);
eine auf der Anreicherungssperrschicht (18) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte dotierte erste Ätzstoppschicht (19);
eine auf der ersten Ätzstoppschicht (19) ausgebildete dotierte erste Verarmungssperrschicht (20);
eine auf der ersten Verarmungssperrschicht (20) ausgebildete undotierte zweite Verarmungssperrschicht (21);

eine auf der zweiten Verarmungssperrschicht (21) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte dotierte zweite Ätzstoppschicht (22);
eine auf der zweiten Ätzstoppschicht (22) ausgebildete und aus Galliumarsenid (GaAs) hergestellte, mit n- Typ Dotierung dotierte erste Deckschicht (23);
eine auf der ersten Deckschicht (23) ausgebildete und aus Galliumarsenid (GaAs) hergestellte undotierte zweite Deckschicht (24);
eine auf der zweiten Deckschicht (24) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte, mit n- Typ Dotierung dotierte dritte Ätzstoppschicht (25);
eine auf der dritten Ätzstoppschicht (25) ausgebildete und aus Galliumarsenid (GaAs) hergestellte, mit n- Typ Dotierung dotierte Ohmschen Schicht (26).

2. Die geschichtete epitaktische Struktur gemäß Anspruch 1, wobei die Anreicherungssperrschicht (18), die erste Verarmungssperrschicht (20) und die zweite Verarmungssperrschicht (21) aus Galliumarsenid (GaAs) hergestellt sind.

3. Eine Anreicherungs- /Verarmungs- PHEMT- Vorrichtung (1; 1') mit:

der geschichteten epitaktischen Struktur gemäß Anspruch 1 oder 2;
einer ersten Region (27) umfassend:

- eine vertikal durch die Ohmsche Schicht (26) und die dritte Ätzstoppschicht (25) ausgebildete erste Vertiefung (33), so dass eine erste obere Oberfläche der zweiten Deckschicht (24) freiliegt,
- eine zweite Vertiefung (36*), die enger als die erste Vertiefung (33) ist, und die sich vertikal von der ersten Vertiefung (33) durch die zweite Deckschicht (24), die erste Deckschicht (23) und die zweite Ätzstoppschicht (22) erstreckt, so dass eine erste obere Oberfläche der zweiten Verarmungssperrschicht (21) freiliegt, und
- eine dritte Vertiefung (38), die enger als die zweite Vertiefung (36*) ist, und die sich vertikal von der zweiten Vertiefung (36*) durch die zweite Verarmungssperrschicht (21), die erste Verarmungssperrschicht (20) und die erste Ätzstoppschicht (19) erstreckt, so dass eine obere Oberfläche der Anreicherungssperrschicht (18), die eine erste Schottky- Kontakt- Region definiert, freiliegt;

einer von der ersten Region (27) lateral beabstandeten und elektrisch isolierten zweiten Region (28), die umfasst:

- eine vertikal durch die Ohmsche Schicht (26) und die dritte Ätzstoppschicht (25) ausgebildete vierte Vertiefung (34), so dass eine zweite obere Oberfläche der zweiten Deckschicht (24) freiliegt, und
- eine fünfte Vertiefung (39), die enger als die vierte Vertiefung (34) ist und die sich vertikal von der vierten Vertiefung (34) durch die zweite Deckschicht (24), die erste Deckschicht (23) und die zweite Ätzstoppschicht (22) erstreckt, so dass eine zweite obere Oberfläche der zweiten Verarmungssperrschicht (21), die eine zweite Schottky-Kontakt-Region definiert, freiliegt;

einem in der ersten Region (27) ausgebildeten Anreicherungstransistor, der umfasst:

- erste Source- und Drainelektroden (29), die in der ersten Region (27) außerhalb der ersten Vertiefung (33) auf der Ohmschen Schicht (26) ausgebildet sind und mit der Ohmschen Schicht (26) in Ohmschen Kontakt stehen, und
- eine in der dritten Vertiefung (38) in Schottky- Kontakt mit der oberen Oberfläche der Anreicherungssperrschicht (18) ausgebildete erste Gatelektrode (41; 43), die die erste Schottky- Kontakt- Region definiert und sich vertikal von der ersten Schottky- Kontakt-Region durch die dritte (38), die zweite (36*) und die erste Vertiefung (33) erstreckt, so dass sie aus der ersten Vertiefung (33) heraus ragt; und

einem in der zweiten Region (28) ausgebildeten Verarmungstransistor, der umfasst

- zweite Source- und Drainelektroden (30), die in der zweiten Region (28) außerhalb der vierten Vertiefung (34) auf der Ohmschen Schicht (26) ausgebildet sind und mit der Ohmschen Schicht (26) in Ohmschen Kontakt stehen, und
- eine in der fünften Vertiefung (39) in Schottky- Kontakt mit der zweiten oberen Oberfläche der zweiten Verarmungssperrschicht (21) ausgebildete zweite Gatelektrode (42; 44), die die zweite Schottky- Kontakt- Region definiert und sich vertikal von der zweiten Schottky- Kontakt- Region durch die fünfte (39) und die vierte Vertiefung (34) erstreckt, so dass sie aus der vierten Vertiefung (34) heraus ragt.

4. Die Anreicherungs- /Verarmungs- PHEMT- Vorrichtung gemäß Anspruch 3, wobei die erste Gateelektrode (41; 43) einen Feldplattenbereich umfasst, der sich lateral in die zweite Vertiefung (36*) auf der ersten oberen Oberfläche der zweiten Verarmungssperrschicht (21) erstreckt, so dass er auf der ersten oberen Oberfläche der zweiten Verarmungsbarriereschicht (21) aufliegt und mechanisch von der ersten oberen Oberfläche der zweiten Verarmungsbarriereschicht (21) gestützt ist.

5. Die Anreicherungs- /Verarmungs- PHEMT- Vorrichtung gemäß Anspruch 4, wobei der Feldplattenbereich der ersten Gateelektrode (43) sich lateral in die ersten Vertiefung (33) auf einen Bereich der ersten oberen Oberfläche der zweiten Deckschicht (24) erstreckt, so dass er auf dem Bereich der ersten oberen Oberfläche der zweiten Deckschicht (24) aufliegt und mechanisch vom Bereich der ersten oberen Oberfläche der zweiten Deckschicht (24) gestützt ist.

6. Die Anreicherungs- /Verarmungs- PHEMT- Vorrichtung gemäß einem der Ansprüche 3-5, wobei die zweite Gateelektrode (44) einen Feldplattenbereich umfasst, der sich lateral in die vierte Vertiefung (34) auf einen Bereich der zweiten oberen Oberfläche der zweiten Deckschicht (24) erstreckt, so dass er auf dem Bereich der zweiten oberen Oberfläche der zweiten Deckschicht (24) aufliegt und mechanisch vom Bereich der zweiten oberen Oberfläche der zweiten Deckschicht (24) gestützt ist.

7. Ein Verfahren zur Herstellung einer Anreicherungs- /Verarmungs- PHEMT- Vorrichtung, umfassend:

Bereitstellen einer geschichteten epitaktischen Struktur, die enthält:

- ein Übergitter und eine Pufferschicht (11);
- ein auf dem Übergitter und der Puffer Schicht (11) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Rücksperrschicht (12);
- eine auf der Rücksperrschicht (12) ausgebildete dotierte Rückdeltadotierungsschicht (13);
- eine auf der Rückdeltadotierungsschicht (13) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Rückabstandsschicht (14)
- eine auf der Rückabstandsschicht (14) ausgebildete und aus Indiumgalliumarsenid (InGaAs) hergestellte undotierte Kanalschicht (15);
- eine auf der Kanalschicht (15) ausgebildete und aus Aluminiumgalliumarsenid (AlGaAs) hergestellte undotierte Abstandsschicht (16);
- eine auf der Abstandsschicht (16) ausgebildete Deltadotierungsschicht (17);
- eine auf der Deltadotierungsschicht (17) ausgebildete undotierte Anreicherungssperrschicht (18);
- eine auf der Anreicherungssperrschicht (18) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte dotierte erste Ätzstoppschicht (19);
- eine auf der ersten Ätzstoppschicht (19) ausgebildete dotierte erste Verarmungssperrschicht (20);
- eine auf der ersten Verarmungssperrschicht (20) ausgebildete undotierte zweite Verarmungssperrschicht (21);
- eine auf der zweiten Verarmungssperrschicht (21) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte dotierte zweite Ätzstoppschicht (22);
- eine auf der zweiten Ätzstoppschicht (22) ausgebildete und aus Galliumarsenid (GaAs) hergestellte, mit n- Typ Dotierung dotierte ersten Deckschicht (23);
- eine auf der ersten Deckschicht (23) ausgebildete und aus Galliumarsenid (GaAs) hergestellte undotierte zweite Deckschicht (24);
- eine auf der zweiten Deckschicht (24) ausgebildete und aus Aluminiumarsenid (AlAs) hergestellte, mit n- Typ Dotierung dotierte dritte Ätzstoppschicht (25);
- eine auf der dritten Ätzstoppschicht (25) ausgebildete und aus Galliumarsenid (GaAs) hergestellte, mit n- Typ Dotierung dotierte Ohmschen Schicht (26);

Ausbilden eines ersten Elektrodenpaars (29) eines Anreicherungstransistors auf der Ohmschen Schicht (26) und mit der Ohmschen Schicht (26) in Ohmschen Kontakt in einer ersten Region (27) der geschichteten epitaktischen Struktur und eines zweiten Elektrodenpaars (30) eines Verarmungstransistors auf der Ohmschen Schicht (26) und mit der Ohmschen Schicht (26) in Ohmschen Kontakt in einer zweiten Region (28) der geschichteten epitaktischen Struktur, die lateral beabstandet von der ersten Region (27) ist, wobei das erste Elektrodenpaar (29) eine erste Sourceelektrode und eine erste Drainelektrode aufweist, wobei das zweite Elektrodenpaar (30) eine zweite Sourceelektrode und eine zweite Drainelektrode aufweist;
Elektrisches Isolieren der ersten Region (27) und der zweiten Region (28);
Ausbilden

- einer ersten Vertiefung (33) in der ersten Region (27), die lateral vom ersten Elektro-

denpaar (29) beabstandet ist, und die sich vertikal durch die Ohmsche Schicht (26) und die dritte Ätzstoppschicht (25) erstreckt, so dass eine erste obere Oberfläche der zweiten Deckschicht (24) freigelegt wird, und
- einer zweiten Vertiefung (34) in der zweiten Region (28), die lateral vom zweiten Elektrodenpaar (30) beabstandet ist, und die sich vertikal durch die Ohmsche Schicht (26) und die dritte Ätzstoppschicht (25) erstreckt, so dass eine zweite obere Oberfläche der zweiten Deckschicht (24) freigelegt wird,

Ausbilden

- einer dritten Vertiefung (36*) in der ersten Region (27), die enger als die erste Vertiefung (33) ist, und die sich vertikal von der ersten Vertiefung (33) durch die zweite Deckschicht (24), die erste Deckschicht (23) und die zweite Ätzstoppschicht (22) erstreckt, so dass eine erste obere Oberfläche der zweite Verarmungssperrschicht (21) freigelegt wird,
- einer vierten Vertiefung (38) in der ersten Region (27), die enger als die dritte Vertiefung (36*) ist, und die sich vertikal von der dritten Vertiefung (33) durch die zweite Verarmungssperrschicht (21), die erste Verarmungssperrschicht (20) und die erste Ätzstoppschicht (19) erstreckt, so dass eine obere Oberfläche der Anreicherungssperrschicht (18), die eine erste Schottky- Kontakt- Region definiert, freigelegt wird, und
- einer fünften Vertiefung (39) in der zweiten Region (28), die enger als die zweite Vertiefung (34) ist, und die sich vertikal von der zweiten Vertiefung (34) durch die zweite Deckschicht (24), die erste Deckschicht (23) und die zweite Ätzstoppschicht (22) erstreckt, so dass eine zweite obere Oberfläche der zweiten Verarmungssperrschicht (21), die eine zweite Schottky- Kontakt- Region definiert, freigelegt wird,

Ausbilden

- einer ersten Gateelektrode (41; 43) des Verstärkungstransistors in der vierten Vertiefung (38) in Schottky- Kontakt mit der oberen Oberfläche der Anreicherungssperrschicht (18), die die erste Schottky-Kontakt- Region definiert, wobei sich die erste Gateelektrode (41; 43) vertikal von der ersten Schottky- Kontakt- Region durch die vierte (38), die dritte (36*) und die erste Vertiefung (33) erstreckt, so dass sie aus der ersten Vertiefung (33) heraus ragt, und
- einer zweiten Gateelektrode (42; 44) des Verarmungstransistors in der fünften Vertiefung (39) in Schottky- Kontakt mit der zweiten oberen Oberfläche der zweiten Verarmungssperrschicht (21), die die zweite Schottky- Kontakt- Region definiert, wobei sich die zweite Gateleketrode (42; 44) vertikal von der zweiten Schottky- Kontakt-Region durch die fünfte (39) und die zweite Vertiefung (34) erstreckt, so dass sie aus der zweiten Vertiefung (34) heraus ragt.

8. Das Verfahren gemäß Anspruch 7, wobei das Ausbilden der dritten Vertiefung (36*), der vierten Vertiefung (38) und der fünften Vertiefung (39) umfasst:

Ausbilden einer dritten Vertiefung (36) durch einen ersten Ätzprozess, der durch Verwendung einer auf der geschichteten epitaktischen Struktur ausgebildeten ersten Maske (37) auf dem ersten Elektrodenpaar (29) und auf dem zweiten Elektrodenpaar (30) ausgeführt wird, so dass ein erster Bereich der ersten oberen Oberfläche der zweiten Deckschicht (24) dem ersten Ätzprozess ausgesetzt wird; und
Verbreitern der dritten Vertiefung (36) und Ausbilden der vierten Vertiefung (38) und der fünften Vertiefung (39) durch einen zweiten Ätzprozess, der durch Verwendung einer auf der geschichteten epitaktischen Struktur, auf dem ersten Elektrodenpaar (29) und auf dem zweiten Elektrodenpaar (30) ausgebildeten zweiten Maske (40) ausgeführt wird, so dass die dritte Vertiefung (36), ein zweiter Bereich der ersten oberen Oberfläche der zweiten Deckschicht (24), die sich lateral von der dritten Vertiefung (36) erstreckt, und ein erster Bereich der zweiten oberen Oberfläche der zweiten Deckschicht (24) dem zweiten Ätzprozess ausgesetzt wird.

9. Das Verfahren gemäß Anspruch 8, wobei die erste Gateelektrode (41) und die zweite Gateelektrode (42) mittels Ausführung einer chemischen Gasabscheidung durch Verwendung der zweiten Maske (40) ausgebildet werden.

10. Das Verfahren gemäß Anspruch 8, wobei die erste Gateelektrode (43) und die zweite Gateelektrode (44) mittels Ausführung einer chemischen Gasabscheidung durch Verwendung einer dritten Maske (45) ausgebildet wird, die auf der geschichteten epitaktischen Struktur, auf dem ersten Elektrodenpaar (29) und auf dem zweiten Elektrodenpaar (30) ausgebildet wird, so dass die vierte Vertiefung (38), die verbreiterte dritte Vertiefung (36*), ein dritter Bereich der ersten oberen Oberfläche der zweiten Deck-

schicht (24), die sich lateral von der verbreiterten dritten Vertiefung (36*) erstreckt, der fünften Vertiefung (39) und ein zweiter Bereich der zweiten oberen Oberfläche der zweiten Deckschicht (24), die sich lateral von der fünften Vertiefung (39) erstreckt, der chemischen Gasabscheidung ausgesetzt wird.

11. Das Verfahren gemäß jedem der Ansprüche 7- 10, wobei das elektrische Isolieren der ersten Region (27) und der zweiten Region (28) die Ausbildung einer Ionenimplementierung umfasst:

eine die erste Region (27) umgebende und sich vertikal durch alle Schichten der geschichteten epitaktischen Struktur erstreckende erste elektrische Isolationssperre (31); und
eine die zweite Region (28) umgebende und sich vertikal durch alle Schichten der geschichteten epitaktischen Struktur erstreckende zweite elektrische Insolationssperre (32).

Revendications

1. Structure épitaxiale en couches pour dispositifs PHEMT à enrichissement et appauvrissement (1 ; 1'), comprenant :

• une couche de tampon et de super-réseau (11) ;
• une couche de barrière arrière non dopée (12) formée sur la couche de tampon et de super-réseau (11) et composée d'arséniure de gallium-aluminium (AlGaAs) ;
• une couche de dopage delta arrière dopée (13) formée sur la couche de barrière arrière (12) ;
• une couche d'écartement arrière non dopée (14) formée sur la couche de dopage delta arrière (13) et composée d'arséniure de gallium-aluminium (AlGaAs) ;
• une couche de canal non dopée (15) formée sur la couche d'écartement arrière (14) et composée d'arséniure de gallium-indium (InGaAs) ;
• une couche d'écartement non dopée (16) formée sur la couche de canal (15) et composée d'arséniure de gallium-aluminium (AlGaAs) ;
• une couche de dopage delta (17) formée sur la couche d'écartement (16) ;
• une couche de barrière à enrichissement non dopée (18) formée sur la couche de dopage delta (17) ;
• une première couche d'arrêt d'attaque dopée (19) formée sur la couche de barrière à enrichissement (18) et composée d'arséniure d'aluminium (AlAs) ;
• une première couche de barrière à appauvrissement dopée (20) formée sur la première couche d'arrêt d'attaque (19) ;
• une deuxième couche de barrière à appauvrissement non dopée (21) formée sur la première couche de barrière à appauvrissement (20) ;
• une deuxième couche d'arrêt d'attaque dopée (22) formée sur la deuxième couche de barrière à appauvrissement (21) et composée d'arséniure d'aluminium (AlAs) ;
• une première couche chapeau (23) dopée avec un agent de dopage du type n, formée sur la deuxième couche d'arrêt d'attaque (22) et composée d'arséniure de gallium (GaAs) ;
• une deuxième couche chapeau non dopée (24) formée sur la première couche chapeau (23) et composée d'arséniure de gallium (GaAs) ;
• une troisième couche d'arrêt d'attaque (25) dopée avec un agent de dopage du type n, formée sur la deuxième couche chapeau (24) et composée d'arséniure d'aluminium (AlAs) ; et
• une couche ohmique (26) dopée avec un agent de dopage du type n, formée sur la troisième couche d'arrêt d'attaque (25) et composée d'arséniure de gallium (GaAs).

2. Structure épitaxiale en couches selon la revendication 1, dans laquelle la couche de barrière à enrichissement (18), la première couche de barrière à appauvrissement (20) et la deuxième couche de barrière à appauvrissement (21) sont composées d'arséniure de gallium (GaAs).

3. Dispositif PHEMT à enrichissement et appauvrissement (1 ; 1') comprenant :

• la structure épitaxiale en couches selon la revendication 1 ou 2 ;
• une première région (27) comprenant

- un premier renfoncement (33) verticalement formé dans la couche ohmique (26) et la troisième couche d'arrêt d'attaque (25) de manière à exposer une première surface supérieure de la deuxième couche chapeau (24),
- un deuxième renfoncement (36*) qui est plus étroit que le premier renfoncement (33) et qui s'étend verticalement depuis le premier renfoncement (33) dans la deuxième couche chapeau (24), la première couche chapeau (23) et la deuxième couche d'arrêt d'attaque (22) de manière à exposer une première surface supérieure de la deuxième couche de barrière à appauvrissement (21), et
- un troisième renfoncement (38) qui est plus étroit que le deuxième renfoncement (36*) et qui s'étend verticalement depuis le deuxième renfoncement (36*) dans la deuxième couche de barrière à appauvris-

sement (21), la première couche de barrière à appauvrissement (20) et la première couche d'arrêt d'attaque (19) de manière à exposer une surface supérieure de la couche de barrière à enrichissement (18) délimitant une première région de contact Schottky ;

• une deuxième région (28) latéralement espacée et électriquement isolée de ladite première région (27) et comprenant

- un quatrième renfoncement (34) verticalement formé dans la couche ohmique (26) et la troisième couche d'arrêt d'attaque (25) de manière à exposer une deuxième surface supérieure de la deuxième couche chapeau (24), et
- un cinquième renfoncement (39) qui est plus étroit que le quatrième renfoncement (34) et qui s'étend verticalement depuis le quatrième renfoncement (34) dans la deuxième couche chapeau (24), la première couche chapeau (23) et la deuxième couche d'arrêt d'attaque (22) de manière à exposer une deuxième surface supérieure de la deuxième couche de barrière à appauvrissement (21) délimitant une deuxième région de contact Schottky ;

• un transistor à enrichissement formé dans la première région (27) et comprenant

- des premières électrodes de source et de drain (29) formées sur ladite couche ohmique (26), et en contact ohmique avec celle-ci, dans la première région (27) à l'extérieur du premier renfoncement (33), et
- une première électrode de grille (41 ; 43) formée dans le troisième renfoncement (38) en contact Schottky avec la surface supérieure de la couche de barrière à enrichissement (18) délimitant la première région de contact Schottky et s'étendant verticalement depuis ladite première région de contact Schottky dans les troisième (38), deuxième (36*) et premier (33) renfoncements de manière à faire saillie depuis ledit premier renfoncement (33) ; et

• un transistor à appauvrissement formé dans la deuxième région (28) et comprenant

- des deuxièmes électrodes de source et de drain (30) formées sur ladite couche ohmique (26), et en contact ohmique avec celle-ci, dans la deuxième région (28) à l'extérieur du quatrième renfoncement (34), et
- une deuxième électrode de grille (42 ; 44) formée dans le cinquième renfoncement (39) en contact Schottky avec la deuxième surface supérieure de la deuxième couche de barrière à appauvrissement (21) délimitant la deuxième région de contact Schottky et s'étendant verticalement depuis ladite deuxième région de contact Schottky dans les cinquième (39) et quatrième (34) renfoncements de manière à faire saillie depuis ledit quatrième renfoncement (34).

4. Dispositif PHEMT à enrichissement et appauvrissement selon la revendication 3, dans lequel la première électrode de grille (41 ; 43) comprend une partie plaque de champ qui s'étend latéralement dans le deuxième renfoncement (36*) sur la première surface supérieure de la deuxième couche de barrière à appauvrissement (21) de manière à reposer sur ladite première surface supérieure de la deuxième couche de barrière à appauvrissement (21) et à être supportée mécaniquement par celle-ci.

5. Dispositif PHEMT à enrichissement et appauvrissement selon la revendication 4, dans lequel la partie plaque de champ de la première électrode de grille (43) s'étend latéralement dans le premier renfoncement (33) sur une partie de la première surface supérieure de la deuxième couche chapeau (24) de manière à reposer sur ladite partie de la première surface supérieure de la deuxième couche chapeau (24) et à être supportée mécaniquement par celle-ci.

6. Dispositif PHEMT à enrichissement et appauvrissement selon l'une quelconque des revendications 3 à 4, dans lequel la deuxième électrode de grille (44) comprend une partie plaque de champ qui s'étend latéralement dans le quatrième renfoncement (34) sur une partie de la deuxième surface supérieure de la deuxième couche chapeau (24) de manière à reposer sur ladite partie de la deuxième surface supérieure de la deuxième couche chapeau (24) et à être supportée mécaniquement par celle-ci.

7. Procédé de fabrication d'un dispositif PHEMT à enrichissement et appauvrissement, comprenant les étapes consistant à :

• fournir une structure épitaxiale en couches qui comprend

- une couche de tampon et de super-réseau (11),
- une couche de barrière arrière non dopée (12) formée sur la couche de tampon et de super-réseau (11) et composée d'arséniure de gallium-aluminium (AlGaAs),
- une couche de dopage delta arrière dopée (13) formée sur la couche de barrière arrière

(12),
- une couche d'écartement arrière non dopée (14) formée sur la couche de dopage delta arrière (13) et composée d'arséniure de gallium-aluminium (AlGaAs),
- une couche de canal non dopée (15) formée sur la couche d'écartement arrière (14) et composée d'arséniure de gallium-indium (InGaAs),
- une couche d'écartement non dopée (16) formée sur la couche de canal (15) et composée d'arséniure de gallium-aluminium (AlGaAs),
- une couche de dopage delta (17) formée sur la couche d'écartement (16),
- une couche de barrière à enrichissement non dopée (18) formée sur la couche de dopage delta (17),
- une première couche d'arrêt d'attaque dopée (19) formée sur la couche de barrière à enrichissement (18) et composée d'arséniure d'aluminium (AlAs),
- une première couche de barrière à appauvrissement dopée (20) formée sur la première couche d'arrêt d'attaque (19),
- une deuxième couche de barrière à appauvrissement non dopée (21) formée sur la première couche de barrière à appauvrissement (20),
- une deuxième couche d'arrêt d'attaque dopée (22) formée sur la deuxième couche de barrière à appauvrissement (21) et composée d'arséniure d'aluminium (AlAs),
- une première couche chapeau (23) dopée avec un agent de dopage du type n, formée sur la deuxième couche d'arrêt d'attaque (22) et composée d'arséniure de gallium (GaAs),
- une deuxième couche chapeau non dopée (24) formée sur la première couche chapeau (23) et composée d'arséniure de gallium (GaAs),
- une troisième couche d'arrêt d'attaque (25) dopée avec un agent de dopage du type n, formée sur la deuxième couche chapeau (24) et composée d'arséniure d'aluminium (AlAs) ; et
- une couche ohmique (26) dopée avec un agent de dopage du type n, formée sur la troisième couche d'arrêt d'attaque (25) et composée d'arséniure de gallium (GaAs) ;

• former une première paire d'électrodes (29) d'un transistor à enrichissement sur ladite couche ohmique (26), et en contact ohmique avec celle-ci, dans une première région (27) de la structure épitaxiale en couches et une deuxième paire d'électrodes (30) d'un transistor à appauvrissement sur ladite couche ohmique (26), et en contact ohmique avec celle-ci, dans une deuxième région (28) de la structure épitaxiale en couches latéralement espacée de ladite première région (27), ladite première paire d'électrodes (29) comprenant une première électrode de source et une première électrode de drain, ladite deuxième paire d'électrodes (30) comprenant une deuxième électrode de source et une deuxième électrode de drain ;
• isoler électriquement la première région (27) et la deuxième région (28) ;
• former

- dans la première région (27), un premier renfoncement (33) qui est latéralement espacé de la première paire d'électrodes (29) et qui s'étend verticalement dans la couche ohmique (26) et dans la troisième couche d'arrêt d'attaque (25) de manière à exposer une première surface supérieure de la deuxième couche chapeau (24), et
- dans la deuxième région (28), un deuxième renfoncement (34) qui est latéralement espacé de la deuxième paire d'électrodes (30) et qui s'étend verticalement dans la couche ohmique (26) et dans la troisième couche d'arrêt d'attaque (25) de manière à exposer une deuxième surface supérieure de la deuxième couche chapeau (24) ;

• former

- dans la première région (27), un troisième renfoncement (36*) qui est plus étroit que le premier renfoncement (33) et qui s'étend verticalement depuis le premier renfoncement (33) dans la deuxième couche chapeau (24), la première couche chapeau (23) et la deuxième couche d'arrêt d'attaque (22) de manière à exposer une première surface supérieure de la deuxième couche de barrière à appauvrissement (21),
- dans la première région (27), un quatrième renfoncement (38) qui est plus étroit que le troisième renfoncement (36*) et qui s'étend verticalement depuis le troisième renfoncement (36*) dans la deuxième couche de barrière à appauvrissement (21), la première couche de barrière à appauvrissement (20) et la première couche d'arrêt d'attaque (19) de manière à exposer une surface supérieure de la couche barrière à enrichissement (18) délimitant une première région de contact Schottky, et
- dans la deuxième région (28), un cinquième renfoncement (39) qui est plus étroit que le deuxième renfoncement (34) et qui

s’étend verticalement depuis le deuxième renfoncement (34) dans la deuxième couche chapeau (24), la première couche chapeau (23) et la deuxième couche d’arrêt d’attaque (22) de manière à exposer une deuxième surface supérieure de la deuxième couche de barrière à appauvrissement (21) délimitant une deuxième région de contact Schottky ; et

• former

- dans le quatrième renfoncement (38), une première électrode de grille (41 ; 43) du transistor à enrichissement en contact Schottky avec la surface supérieure de la couche de barrière à enrichissement (18) délimitant la première région de contact Schottky, ladite première électrode de grille (41 ; 43) s’étendant verticalement depuis ladite première région de contact Schottky dans les quatrième (38), troisième (36*) et premier (33) renfoncements de manière à faire saillie depuis ledit premier renfoncement (33), et
- dans le cinquième renfoncement (39), une deuxième électrode de grille (42 ; 44) du transistor à appauvrissement en contact Schottky avec la deuxième surface supérieure de la deuxième couche de barrière à appauvrissement (21) délimitant la deuxième région de contact Schottky, ladite deuxième électrode de grille (42 ; 44) s’étendant verticalement depuis ladite deuxième région de contact Schottky dans les cinquième (39) et deuxième (34) renfoncements de manière à faire saillie depuis ledit deuxième renfoncement (34).

8. Procédé selon la revendication 7, dans lequel la formation du troisième renfoncement (36*), du quatrième renfoncement (38) et du cinquième renfoncement (39) consiste à :

• former un troisième renfoncement (36) au moyen d’un premier procédé d’attaque réalisé en utilisant un premier masque (37) formé sur la structure épitaxiale en couches, sur la première paire d’électrodes (29) et sur la deuxième paire d’électrodes (30) de manière à exposer une première partie de la première surface supérieure de la deuxième couche chapeau (24) audit premier procédé d’attaque ; et
• élargir ledit troisième renfoncement (36) et former le quatrième renfoncement (38) et le cinquième renfoncement (39) au moyen d’un deuxième procédé d’attaque réalisé en utilisant un deuxième masque (40) formé sur la structure épitaxiale en couches, sur la première paire d’électrodes (29) et sur la deuxième paire d’électrodes (30) de manière à exposer le troisième renfoncement (36), une deuxième partie de la première surface supérieure de la deuxième couche chapeau (24) s’étendant latéralement depuis ledit troisième renfoncement (36) et une première partie de la deuxième surface supérieure de la deuxième couche chapeau (24) audit deuxième procédé d’attaque.

9. Procédé selon la revendication 8, dans lequel la première électrode de grille (41) et la deuxième électrode de grille (42) sont formées au moyen d’un dépôt chimique en phase vapeur réalisé en utilisant le deuxième masque (40).

10. Procédé selon la revendication 8, dans lequel la première électrode de grille (43) et la deuxième électrode de grille (44) sont formées au moyen d’un dépôt chimique en phase vapeur réalisé en utilisant un troisième masque (45) formé sur la structure épitaxiale en couches, sur la première paire d’électrodes (29) et sur la deuxième paire d’électrodes (30) de manière à exposer le quatrième renfoncement (38), le troisième renfoncement élargi (36*), une troisième partie de la première surface supérieure de la deuxième couche chapeau (24) s’étendant latéralement depuis ledit troisième renfoncement élargi (36*), le cinquième renfoncement (39) et une deuxième partie de la deuxième surface supérieure de la deuxième couche chapeau (24) s’étendant latéralement depuis ledit cinquième renfoncement (39) au dépôt chimique en phase vapeur.

11. Procédé selon l’une quelconque des revendications 7 à 10, dans lequel l’isolation électrique de la première région (27) et de la deuxième région (28) comprend la formation par implantation ionique :

• d’une première barrière d’isolation électrique (31) entourant la première région (27) et s’étendant verticalement dans toutes les couches de la structure épitaxiale en couches ; et
• d’une deuxième barrière d’isolation électrique (32) entourant la deuxième région (28) et s’étendant verticalement dans toutes les couches de la structure épitaxiale en couches.

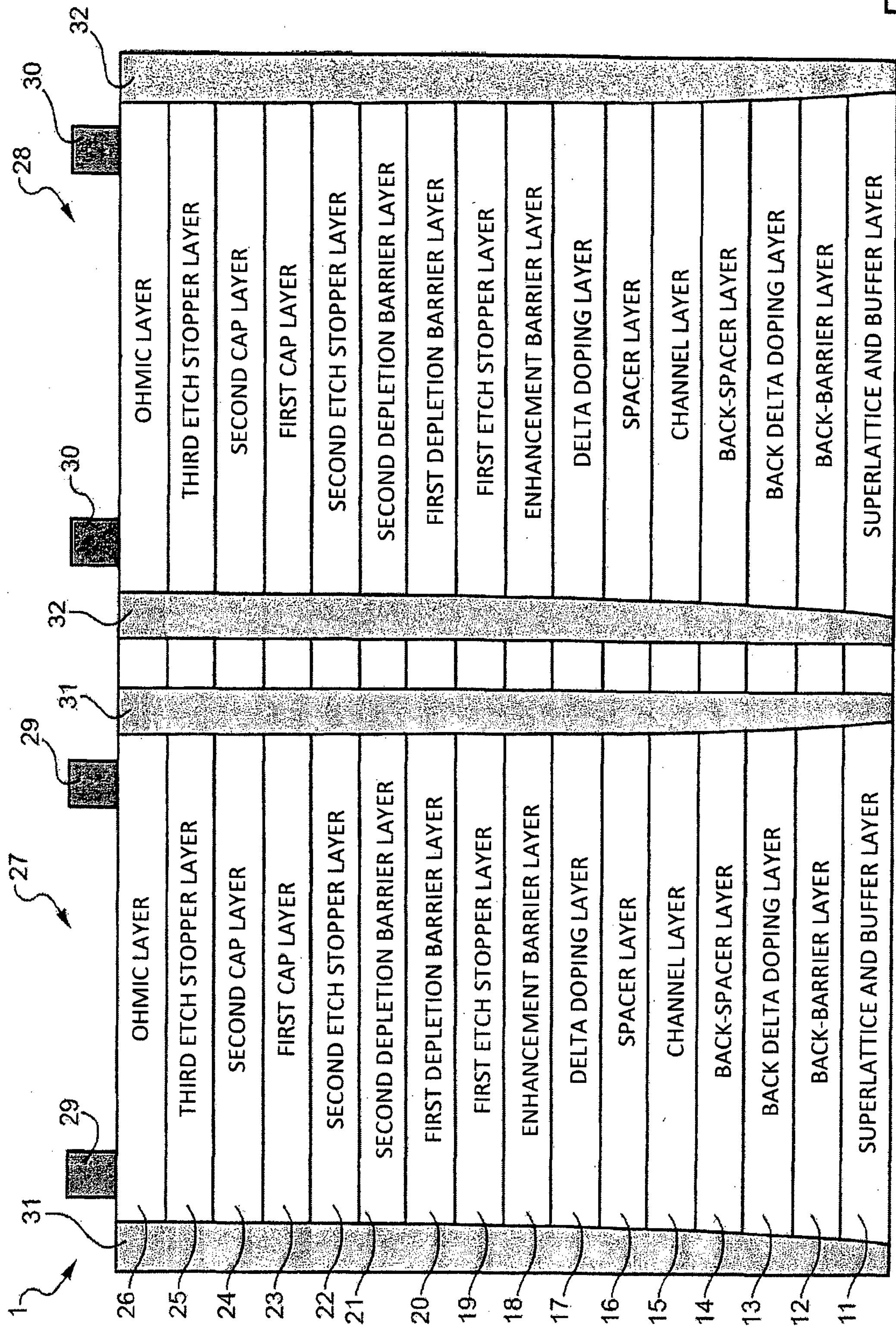

FIG. 1

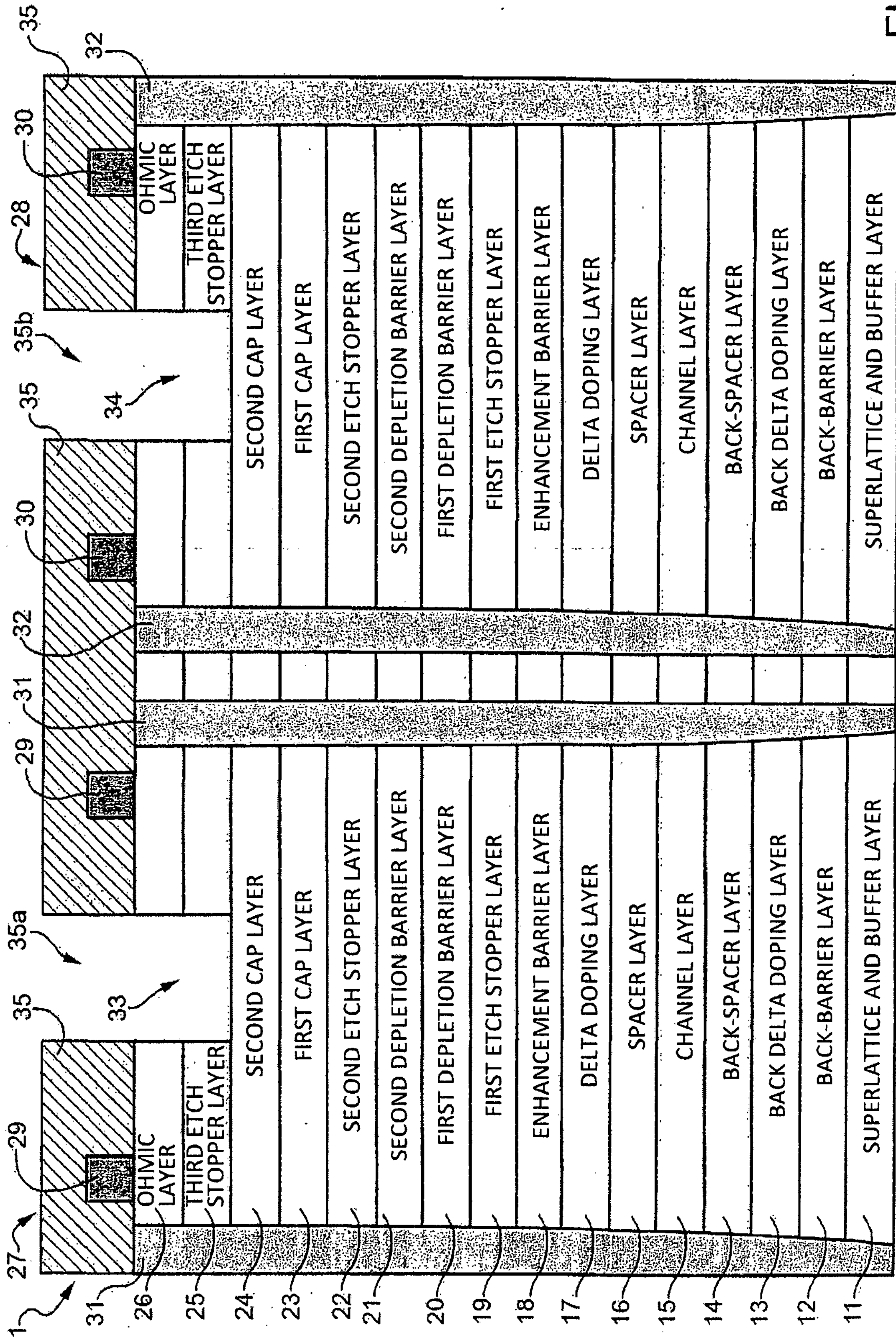

FIG. 2

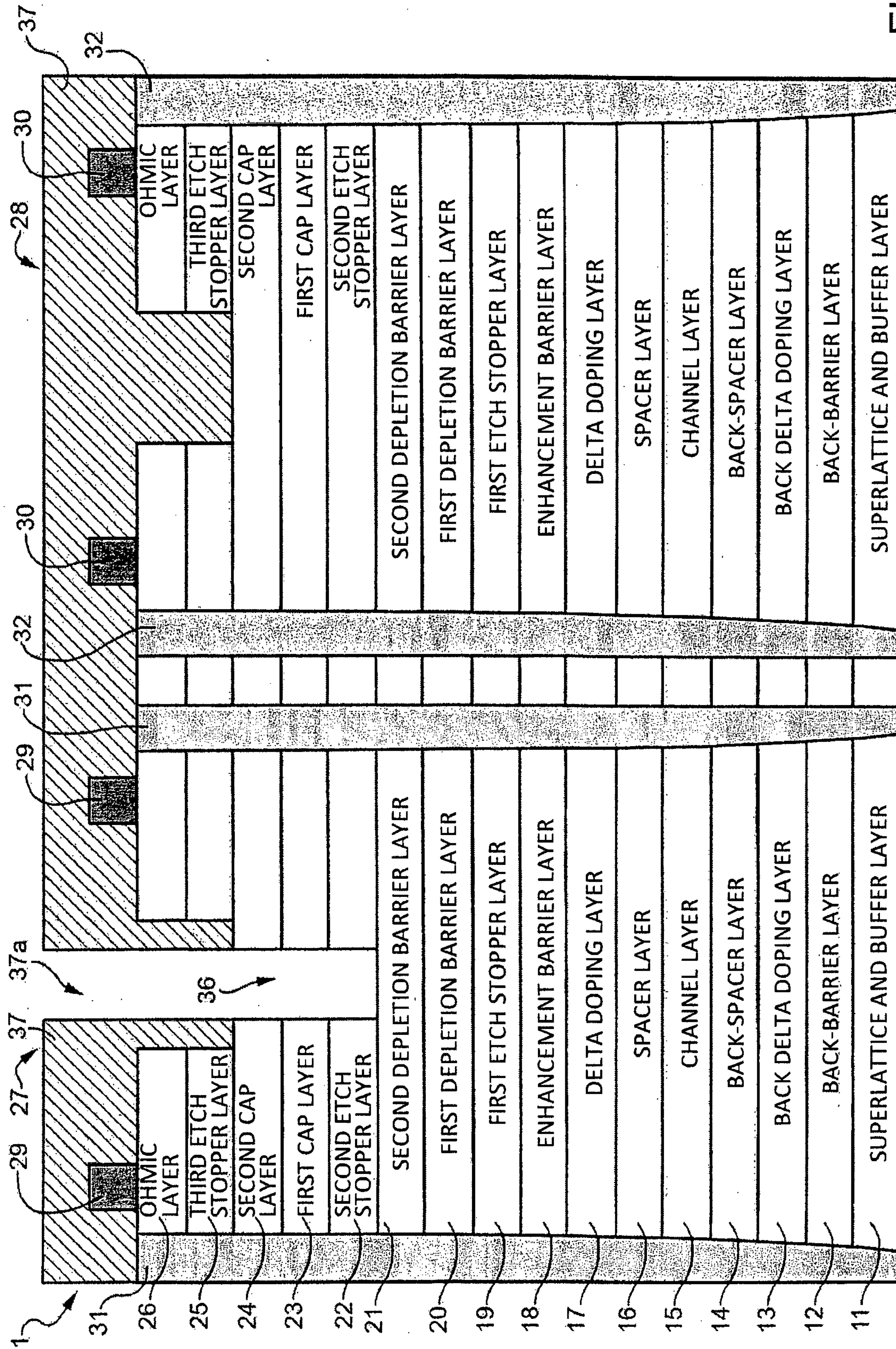

FIG. 3

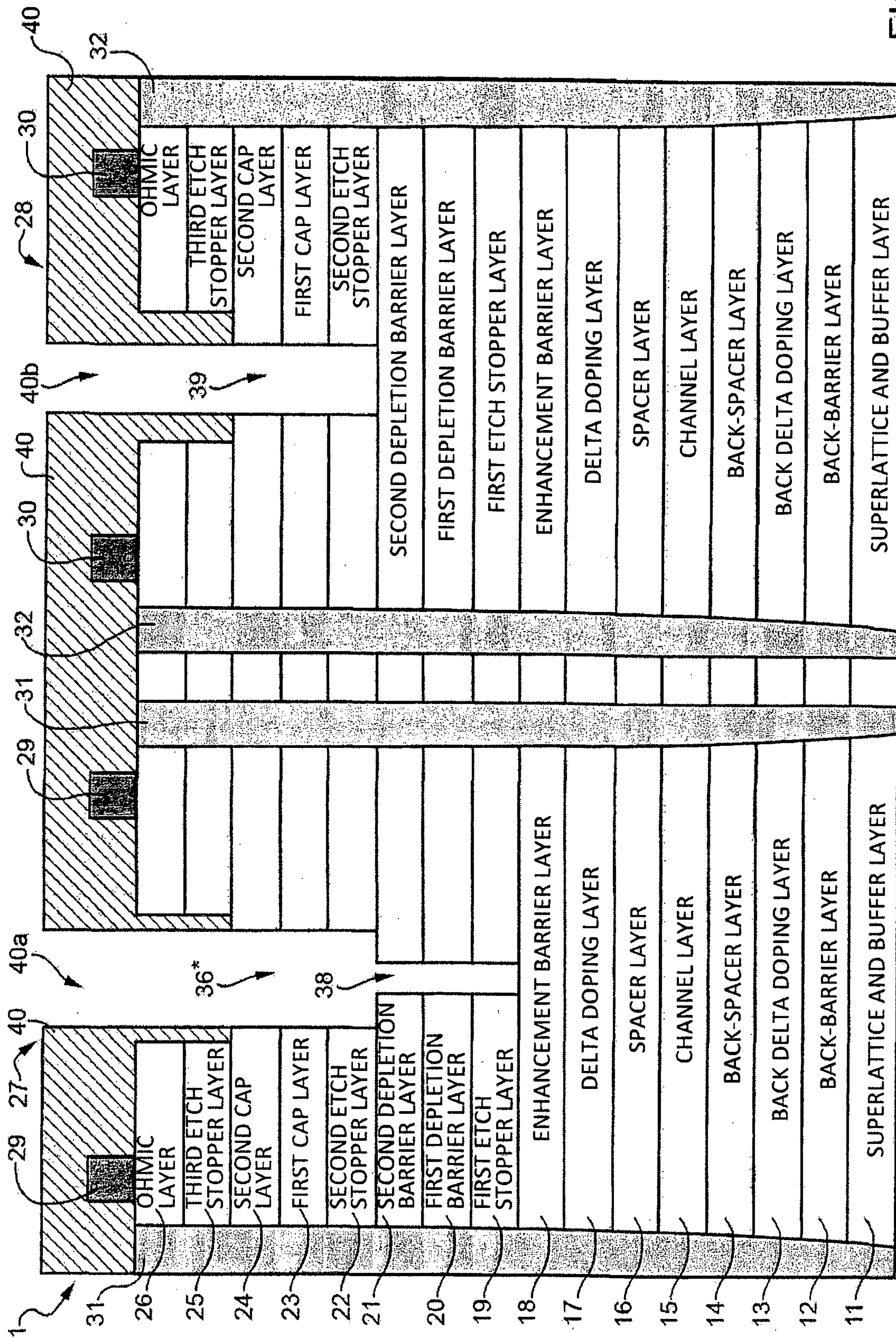

FIG. 4

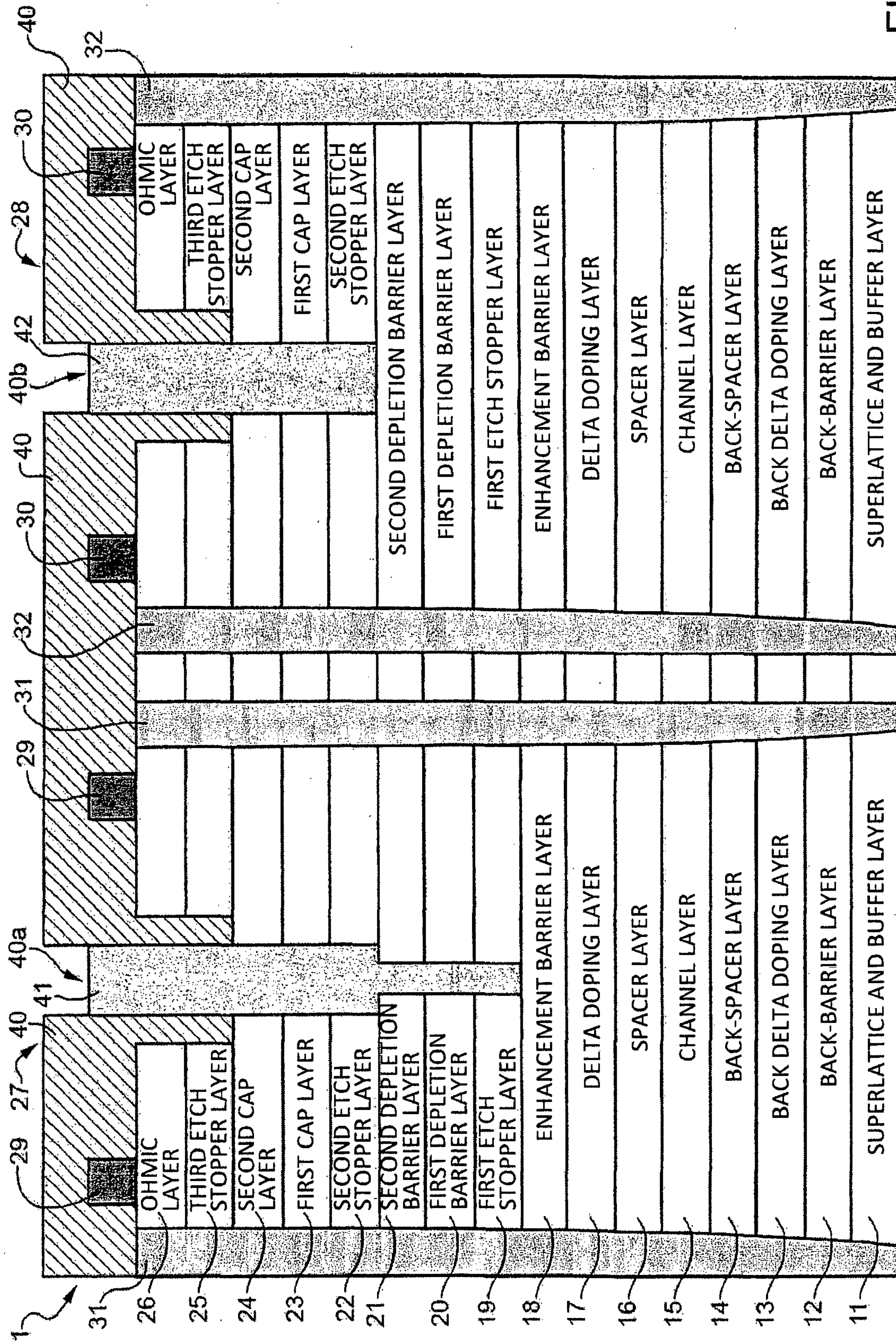

FIG. 5

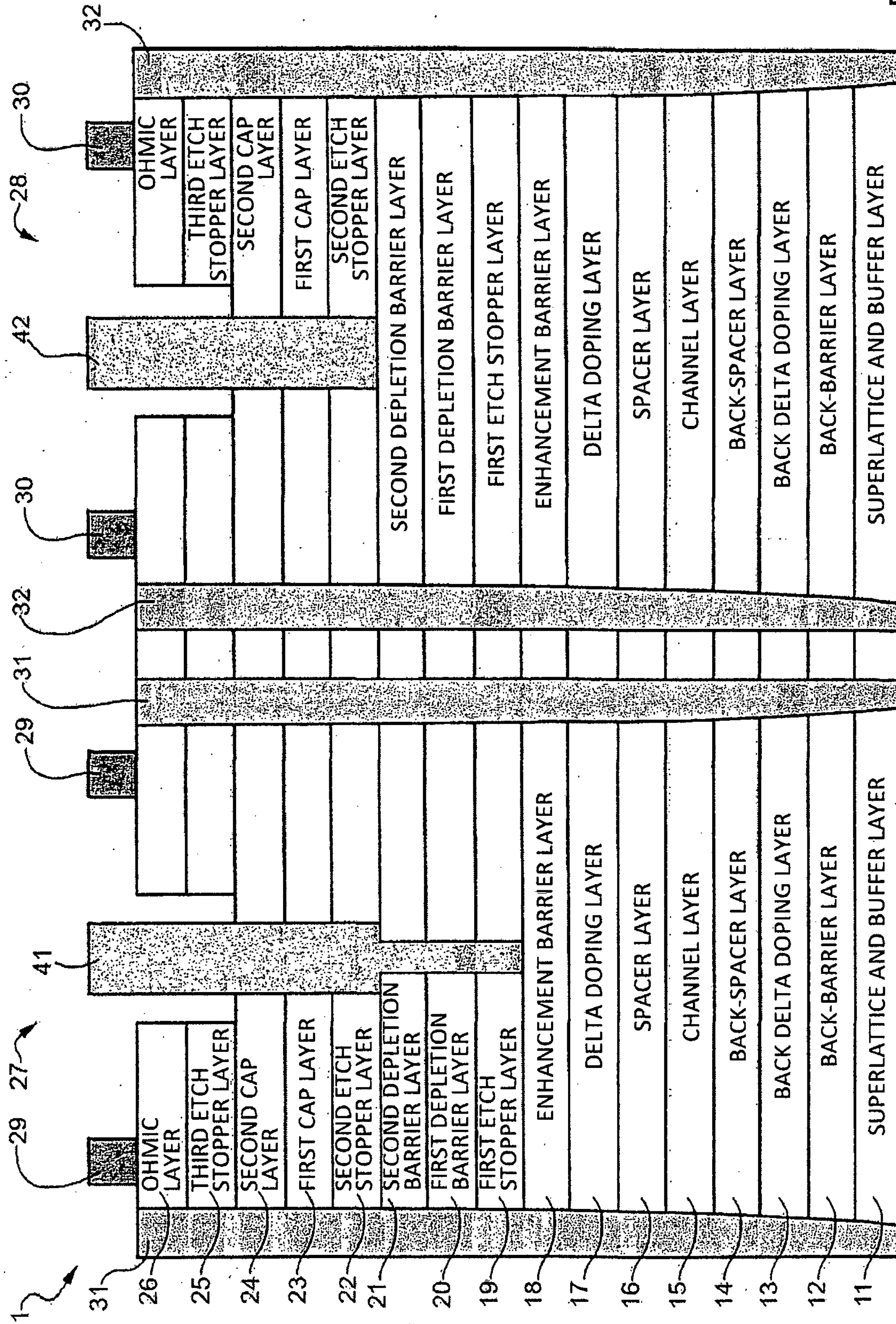
FIG. 6
OHMIC LAYER
THIRD ETCH STOPPER LAYER
SECOND CAP LAYER
FIRST CAP LAYER
SECOND ETCH STOPPER LAYER
SECOND DEPLETION BARRIER LAYER
FIRST DEPLETION BARRIER LAYER
FIRST ETCH STOPPER LAYER
ENHANCEMENT BARRIER LAYER
DELTA DOPING LAYER
SPACER LAYER
CHANNEL LAYER
BACK-SPACER LAYER
BACK DELTA DOPING LAYER
BACK-BARRIER LAYER
SUPERLATTICE AND BUFFER LAYER
1
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
41
42

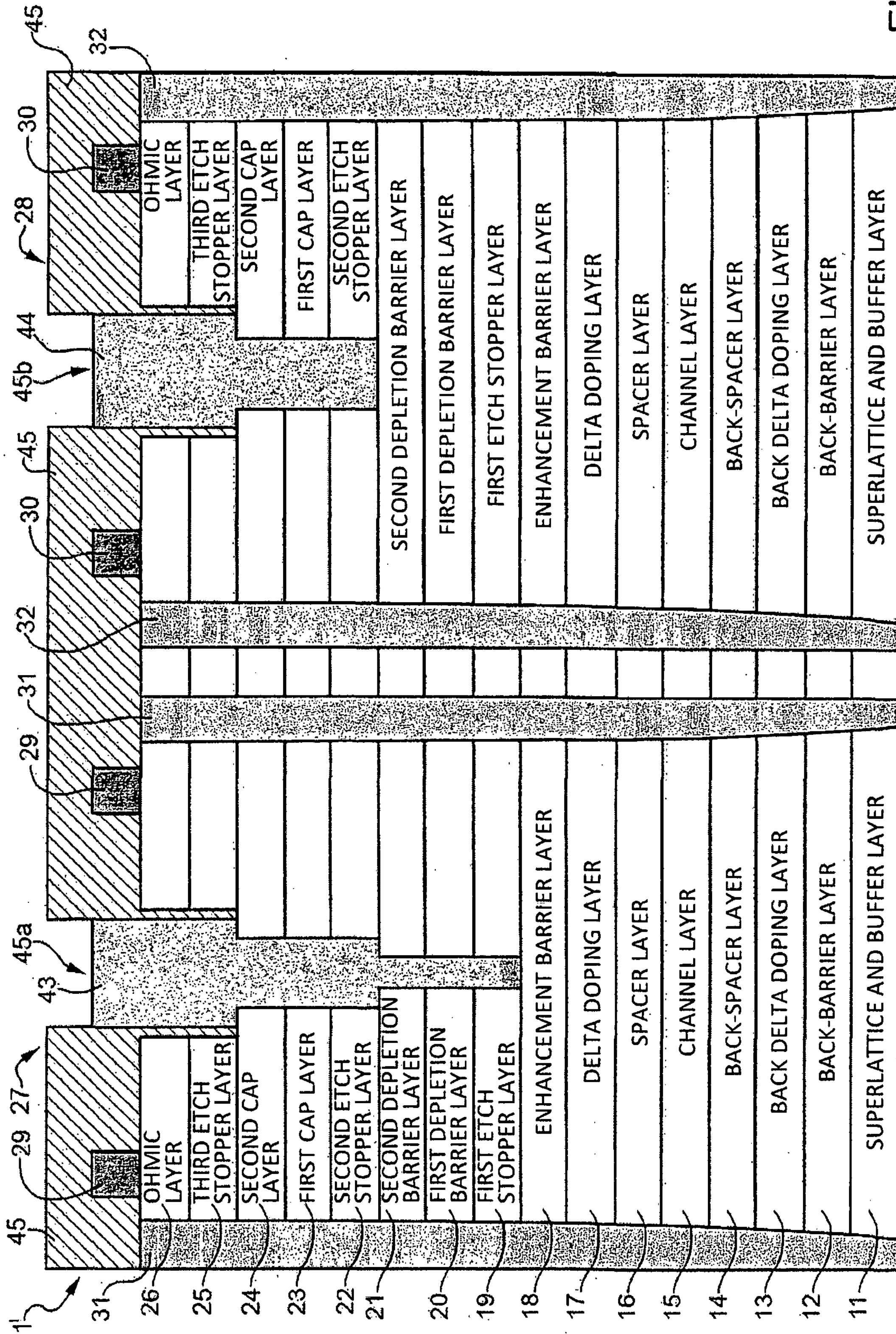

FIG. 7

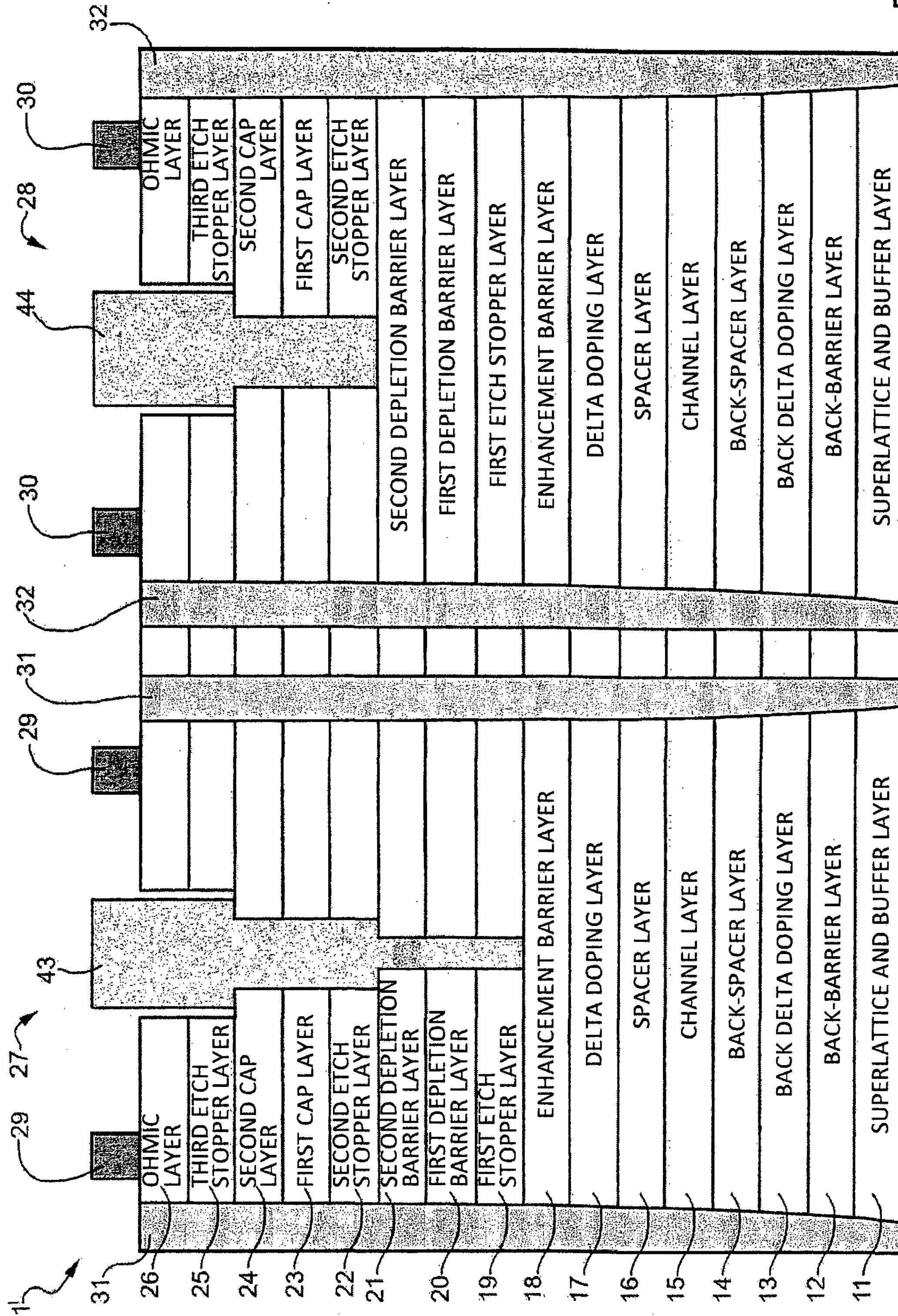

FIG. 8
1
27
28
29
30
31
32
43
44
OHMIC LAYER
THIRD ETCH STOPPER LAYER
SECOND CAP LAYER
FIRST CAP LAYER
SECOND ETCH STOPPER LAYER
SECOND DEPLETION BARRIER LAYER
FIRST DEPLETION BARRIER LAYER
FIRST ETCH STOPPER LAYER
ENHANCEMENT BARRIER LAYER
DELTA DOPING LAYER
SPACER LAYER
CHANNEL LAYER
BACK-SPACER LAYER
BACK DELTA DOPING LAYER
BACK-BARRIER LAYER
SUPERLATTICE AND BUFFER LAYER
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 20060027840 A **[0006] [0007]**
- US 20060208279 A **[0006] [0007]**
- EP 0371686 A **[0006] [0007]**
- US 6670652 B **[0006] [0007]**
- US 6703638 B **[0006] [0007]**
- US 7361536 B **[0006] [0007]**