Tutorial Eight

Logic Design of Asynchronous Circuits

Jordi Cortadella (Coordinating Presenter)
Universitat Politecnica de Catalunya, Spain
jordic@lsi.upc.es

Alex Yakovlev
University of Newcastle upon Tyne, United Kingdom
alex.yakovlev@ncl.ac.uk

Jim Garside
University of Manchester, United Kingdom
jgarside@cs.man.ac.uk

Abstract

This tutorial aims at motivating the audience to consider asynchronous circuits as a competitive alternative to solve some of the design problems inherent to submicron technologies. One of the main reasons why designers are reluctant to incorporate asynchrony in their systems is the difficulty to design asynchronous circuits.

Asynchronous circuits are promising to tackle problems such as electro-magnetic interference, power consumption, performance, and modularity of digital circuits. The tutorial will introduce state-of-the-art tools and methodologies for their design. It will cover aspects such as specification, architectural design and controller synthesis tools, of asynchronous circuits. The tutorial will concentrate on a particular design methodology for control circuits based on specifications with Signal Transition Graphs. It will also cover design strategies for the microarchitecture, data-path and control circuits that have been successfully applied in the design of the asynchronous version of the ARM microprocessor.

The tutorial is organized in three parts. The first part will give an overview of the main concepts related to asynchrony in circuit design: asynchronous communication, design styles, building blocks, control specification and implementation, delay models, classes of asynchronous circuits and advantages of asynchronous circuits.

The second part will focus on the synthesis of control circuits. After a brief presentation of different specification formalisms, this part will describe a design flow based on specifications given as timing diagrams (Signal Transition Graphs). This design flow can be fully automated and the steps involved in this automation will be described: state encoding, derivation of next-state equations for speed-independent circuits, hazard-free logic decomposition and synthesis with relative timing. Some basic concepts on testing and formal verification will also be covered.

The third part is devoted to present real experiences in the design of asynchronous circuits. In particular, the asynchronous ARM microprocessor is used to illustrate the design of relevant parts of an asynchronous system (data-path, control, memory). This part will cover both architectural and design issues that are relevant to asynchronous design: conditional execution, multi-cycle instructions, "elastic" pipelines, self-timed memories, asynchronous caches, asynchronous intra-chip communication and globally-asynchronous locally-synchronous systems.

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The presenters of the tutorial have a wide experience in the design methodologies of asynchronous circuits. All of them are members of the Working Group on Asynchronous Circuit Design (ACiD-WG), a consortium funded by the European Commission to promote RTD activities around the theme of asynchronous circuit design (see http://www.scism.sbu.ac.uk/ccsv/ACiD-WG for more details).

Jordi Cortadella *received the M.S. and Ph.D. degrees in Computer Science from the Universitat Politecnica de Catalunya, Barcelona, Spain, in 1985 and 1987 respectively. He is a Professor at the Department of Software of the Universitat Politecnica de Catalunya. In 1988, he was a Visiting Scholar at the University of California, Berkeley. His research interests include computer-aided design of VLSI systems with special emphasis on synthesis and verification of asynchronous circuits, concurrent systems and HW/SW co-design. He has coauthored over 100 research papers in technical journals and conferences. He has served on the technical committees of several international conferences in the field of Design Automation and Concurrent Systems. He was the Symposium Co-Chair of the 5th International Symposium on Advanced Research in Asynchronous Circuits and Systems in Barcelona, 1999. He is the main author of the tool petrify (www.lsi.upc.es/~jordic/petrify), currently used by several industries and Universities for the synthesis of asynchronous control circuits.*

Alex Yakovlev *received the MSc (1979) and PhD (1982) degrees in Computing Science from Electrotechnical University of St. Petersburg, Russia, where he worked in the area of asynchronous and concurrent systems since 1980, and in the period between 1982 and 1990 held positions of Assistant and Associate Professor at the Computing Science department. Since 1991 he has been a Lecturer, Reader and from 2000 Professor in Computer Systems Design at the Newcastle University Department of Computing Science, where he is heading the VLSI Design research group. His current interests and publications are in the field of modelling and design of asynchronous, concurrent, real-time and dependable systems. He has coauthored over 100 research papers in technical journals and conferences. He has served on the technical committees of several international conferences in the field of Asynchronous Systems, Concurrency and Petri nets. He was the Programme Committee Co-Chair of the 5th International Symposium on Advanced Research in Asynchronous Circuits and Systems in Barcelona, 1999, the Co-Organiser of the IEEE Workshop on Asynchronous Interfaces, Delft, 2000, and the Co-Organiser of two workshops and an advanced tutorial on "Hardware Design and Petri Nets", Lisbon (1998), Williamsburg (1999) and Aarhus (2000).*

Jim Garside *gained a BSc in Physics in 1983 at the University of Manchester and a PhD in Computer Science at the same institution in 1987. Since that time he has worked in hardware systems using Inmos Transputers for investigation into parallel computer architectures and as a programmer on Air Traffic Control systems. He was appointed as a lecturer in the Department of Computer Science at the University of Manchester in 1991. Since that time he has primarily been involved in research into asynchronous logic systems, especially in the design of the AMULET series of asynchronous microprocessors. Most recently he led the design effort on the AMULET3i asynchronous system-on-chip which includes the first asynchronous microprocessor to achieve parity in performance and power-efficiency with its synchronous direct equivalent.*