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A Simple Closed-Loop Active Gate Voltage Driver for Controlling di_C/dt and dv_{CE}/dt in IGBTs

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Abstract: The increase of the switching speed in power semiconductors leads to converters with better efficiency and high power density. On the other hand, fast switching generates some consequences like overshoots and higher switching transient, which provoke electromagnetic interference (EMI). This paper proposes a new closed-loop gate driver to improve switching trajectory in insulated gate bipolar transistors (IGBTs) at the hard switching condition. The proposed closed-loop gate driver is based on an active gate voltage control method, which deals with emitter voltage (V_{Ee}) for controlling di_C/dt and gets feedback from the output voltage (v_{CE}) in order to control dv_{CE}/dt. The sampled voltage signals modify the profile of the applied gate voltage (v_{gg}). As a result, the desired gate driver (GD) improves the switching transients with minimum switching loss. The operation principle and implementation of the controller in the GD are thoroughly described. It can be observed that the new GD controls both dv_{CE}/dt and di_C/dt accurately independent of the variable parameters. The new control method is verified by experimental results. As a current issue, the known trade-off between switching losses and EMI is improved by this simple and effective control method.

Keywords: gate driver (GD); IGBT; switching losses; electromagnetic interference (EMI)

1. Introduction

Insulated gate bipolar transistor (IGBT) power semiconductors with antiparallel freewheeling diodes (FWDs) are widely employed in industrial applications. In order to achieve high-density power converters, attention is focused on the use of fast IGBTs. Hence, the demand for minimizing switching losses and increasing efficiency has encouraged engineers to design more effective IGBT gate drivers. For gate drive (GD) designing, the main task is transient behavior improvement in switching times with minimum penalty in the losses. It is well known that fast switching has a direct effect on the minimization of switching losses; meanwhile, it is the major reason for electromagnetic interference (EMI) generation in switched-mode power converters [1]. Moreover, the higher rates of voltage and current transition (dv_{CE}/dt and di_C/dt respectively) impose stress on the IGBT, which has a harmful effect on device lifetime [2]. Therefore, a trade-off between switching losses and EMI generation should be defined for optimized switching. This will be more challenging when we are dealing with IGBTs, which operate at high frequency and are under hard switching conditions over non-constant load.

In addition, the other challenging issue in GD designing is the definition of di_C/dt and dv_{CE}/dt rates and keeping them in the desired values during operation condition, independent of effective variables such as junction temperature (Tj), parasitic inductance (L_S), and load etc. [3]. Moreover, some other factors such as high-speed operation, low-cost production, simplicity in structure, effectiveness in EMI reduction, and efficiency improvement are important considerations in GD designing. The modification of gate resistor (Rg) in the drive circuit is known as a conventional solution for the switching

control [4–6]. The result of using a conventional gate drive (CGD) is a sub-optimal compromise, which has an undesirable effect on the switching speed and switching losses of IGBTs. To overcome the inherent ineffectiveness of CGDs, many active gate controls (AGC) have been reported [3,7–24]. In order to create a safe operating point for an IGBT with respect to its nonlinearities and dependencies, it is necessary to get some feedback to related concerns and apply them to the GD controller. For this reason, using passive and feedforward controllers with a simple structure and cheaper price is not an ideal solution for industrial applications. Therefore, AGC can mainly be categorized into the closed-loop controller's family. These controllers have been presented and gradually developed to guarantee the safe operation area (SOA) of IGBTs under different load conditions. However, using such controllers increases the cost and complexity of the GDs circuit. For this reason, the goal is to achieve a cost-effective and simple closed-loop controller with respect to robustness factors.

The junction temperature and the load variation as changeable factors and IGBTs' nonlinearity have a significant influence on the structure of closed-loop GDs. A brief review of these factors is summarized here. As an exclusive advantage of this controller, the proposed GD operates no dependence on the mentioned factors.

1.1. Junction Temperature (Tj)

The reliability of IGBTs is a thermal-related issue; as much as half of the total amount of power-related device damage is related to temperature-dependent failures [25,26]. However, the effect of high Tj is not limited to reliability. This factor has a significant effect on IGBT switching characteristic values [27], as it may change the dynamic behaviour of gate voltage (V_{Ge}) and current (i_G). Furthermore, threshold gate-emitter voltage ($V_{Ge,th}$) may vary with different temperatures [28–30]. Therefore, considering Tj for some of the controllers that are dealing with gate side parameters is essential. Otherwise, the applied controller may not be entirely effective for all operating conditions. For instance, an active gate voltage control was presented in [11] to control the values of di_C/dt and $\mathrm{dv_{CE}}/\mathrm{dt}$ at turn on/off, based on gate side transient behaviour. However, the addressed intervals may vary by different Tj values, which are the principal action of the controller. The defined intervals for controller operation have been restricted by constant delays, hence, for such controllers, some criticisms can be raised. Different methods for measuring device temperature have been presented [31]. The proposed closed-loop GD presented in this paper is independent of the temperature of the IGBT. It covers all consequences of temperature variation without installing an additional circuit.

1.2. Load Variation

Missing compensation of the load variation is the main drawback of passive and feedforward controllers [3]. Thereby, the closed-loop concept with negative feedback is promoted to achieve more precise control. The variation in the load affects dv_{CE}/dt and di_C/dt. Especially in hard switching condition when IGBT operates under inductive loads, preserving the dv_{CE}/dt and di_C/dt in proportional slope rates is a serious issue for EMI standards [32]. Moreover, the load and its demanded current have an effect on the Miller plateau area in the IGBT during turn on/off transients [33]. This factor, as in the previous section, may change the behavior of the IGBT in the gate side, and all previous concerns are valid for this case as well. Significantly, in turn-on condition, the load variation affects di_C/dt so that it also has an effect on the inducted "v_{Ee}" voltage that exists between the emitter and the common path of the converter. This voltage, which has been created by stray inductance, is used in the proposed controller. Using this technique, the GD has been benefited by an undesirable phenomenon. More details are explained in the corresponding section. Briefly, the IGBT can be controlled permanently in all load conditions.

1.3. IGBT's Nonlinearity

Typically, the closed-loop AGC is the only possible solution to compensate for the IGBT's nonlinearities in variable operating conditions. Many sophisticated analog closed-loop GDs have

been presented [9,17,34–36]. Due to the different transient behavior of IGBTs at each switching on/off condition [37–39], individual control loops for each switching state (for di_C/dt control at turn-on [18], or dv_{CE}/dt at turn-off [40]) are needed. In addition, for full GDs a combination of both voltage and current feedback in the AGC topology have been presented [3,8,24]. Recently, several digital approaches have been presented in IGBT GDs [19–21], [33,41]. The use of these techniques has benefits for minimization of switching losses, reverse-recovery current, and EMI at desired switching operation. However, the large delay times during conversion of analog to digital (A/D), and vice versa (D/A), in the signal paths and the higher cost are the main drawbacks of digital solutions. In contrast, this paper proposes a simple analog GD that controls both voltage and current transitions in a closed loop.

Various methods for di_C/dt controlling based on the measurement of the collector current have been presented herein, and many different techniques for controlling dv_{CE}/dt through the measurement of the collector-emitter voltage have also been proposed. However, the proposed GDs have been mainly complicated and expensive solutions or, in other cases, they sacrifice additional switching losses. In this study, a simple structure closed-loop GD with voltage type feedback operates independently of variable parameters while maintaining a precise balance between switching losses and EMI effects. The concept, principles, and structure of the proposed control method are explained in Section 2. The controller setting and performance of the new closed-loop GD is evaluated using experimental results, which are presented in Section 3. Section 4 presents a performance index of the new GD through comparisons with conventional gate drive methods. EMI analysis and cost are also evaluated here. The paper closes with a discussion of the presented controller and conclusion.

2. Proposed Active Gate Control Method

The proposed GD controls the IGBT's di_C/dt and dv_{CE}/dt at turn-on and turn-off, respectively. The rise in collector current during turn-on switching creates a v_{Ee} voltage at the IGBT emitter, which is used in the controller as feedback. The output voltage (V_{CE}) as turn-off feedback is applied to the closed-loop controller as well. The principles of the new GD are based on the active gate voltage control method. Thus, an intermediate gate-voltage (v_{gg}) is applied at specific intervals, which covers current (i_C) rise time at turn-on and voltage (V_{CE}) rise time at turn-off. The level of the applied intermediate voltage varies due to the load variation in order to maintain the desired rates for current and voltage transitions. The concept and operation principle of the new closed-loop GD is explained below.

2.1. Philosophy of the Method

The IGBT meets several intervals during its turn on/off under hard switching conditions. Figure 1 shows these intervals schematically. All the details regarding the switching process of the IGBT are fairly well documented in [39]. Here, we have mainly focused on the corresponding intervals to figure out the effective parameters and control the di_C/dt and dv_{CE}/dt rates.

At t0, a voltage step (from $-V_{EE}$ to $+V_{CC}$) is applied to the gate port. At this moment, the gate current (i_G) immediately rises to its maximum value and then starts to decay. In the meantime, the gate voltage v_{Ge} rises in accordance with the time constant (τ_G) of the charging process cf. Equations (1) and (2). The IGBT is still off as long as the v_{Ge} remains lower than the threshold voltage $v_{Ge;th}$. This process happens in the first interval, which covers the time between t0 to t1 cf. Figure 1a. This interval is a so-called gate charge delay and it has a minimal effect on di_C/dt rate; however, the gate charge has remained valid and the potential energy is stored for the next interval.

$$C_{ies} = C_{Ge} + C_{GC} \tag{1}$$

$$\tau_G = R_g \cdot C_{ies} \tag{2}$$

As soon as $v_{Ge(t)}$ passes the $v_{Ge,th}$ value, the GD circuit changes the profile of the v_{gg} voltage signal and delivers a lower voltage value to the gate-emitter (see Figure 1a). In this moment, the IGBT begins to conduct current based on its transfer and output characteristics. Then, the collector current increases

almost linearly from zero, and the load current initiates commutation from the freewheeling diode to the IGBT [39]. The extra gate charge that had been stored in the previous interval can potentially generate the overshoot problem in i_C [42,43]. According to equations below, which have been proved in [17,23], the di_C/dt rates can be calculated as a function of the gate circuit parameter. The gate current i_G *(t)* during the second interval can be represented as

$$i_G(t) = \frac{\Delta v_{gg}}{R_g} \cdot e^{-(t-t1)/\tau_G} \tag{3}$$

That Δv_{gg} is the difference value of the maximum (V_{CC}) and minimum (V_{EE}) gate drive voltage, and R_g is the gate resistor.

$$\Delta v_{gg} = V_{CC} - V_{EE} \tag{4}$$

The i_C and di_C/dt equations in turn-on can be approximately explained as

$$i_C(t) \; = \; g_m \cdot (v_{Ge(t)} \; - \; v_{Ge,th}) \tag{5}$$

where gm is the IGBT's linearized transconductance.

$$g_m = \frac{di_C}{dv_{Ge}} \tag{6}$$

$$\frac{di_C}{dt} = g_m \cdot \frac{dv_{Ge}}{dt} = g_m \cdot \frac{i_G}{C_{ies}} \tag{7}$$

$$I_{os} \approx 2.86 \times 10^{-6} BV_{BD} \sqrt{I_F \frac{di_C}{dt}} \tag{8}$$

C_{GC} is Miller capacitance; I_F is the diode forward current; BV_{BD} is the diode breakdown voltage and L_S is the stray inductance.

The collector current i_C rises rapidly when $v_{Ge(t)}$ exceeds $v_{Ge,th}$ value, cf. Equation (5). Whereas, in high voltage applications (in high v_{CE} values), C_{Ge} is too small; therefore, according to Equation (7), the only possible way to obtain the desired di_C/dt rate is to have constant product in $g_m \cdot i_G$. Hence, the transconductance g_m or gate current value during the current rise time should be controlled. Furthermore, the overshoot in collector current I_{OS} may appear because of the reverse recovery current that is cycling by the freewheeling diode (FWD), cf. Equation (8).

The gate-emitter capacitance depends on the physical structure of the IGBT, so di_C/dt control at turn-on condition can be possible by changing the v_{Ge} or gate current i_G values. In Figure 1a, the gray background demonstrates the controller operation time to apply the intermediate *vgg* voltage value. Based on this technique, the injected i_G will be controlled by changing the v_{gg} voltage profile, cf. Equation (3), in order to control di_C/dt, cf. Equation (7), and remove the current overshoot, cf. Equation (8).

Figure 1b shows schematic waveforms of the IGBT at turn-off. At t6, the v_{gg} voltage pulse is switched to its negative value. With a few exceptions, it can be assumed that voltage and current in the gate side have inverse behavior compared to turn-on condition. Upon applying V_{EE}, the $v_{Ge}(t)$ starts to decay, and at the same time, v_{CE} gradually increases. The slow rising in v_{CE} is because of the large Miller capacitance C_{GC} value. In this process, as soon as both v_{CE} and v_{Ge} arrive at the same value, C_{GC} suddenly falls down in value and the v_{CE} starts to rise fast [39]. The dv_{CE}/dt can be calculated as

$$\frac{dv_{CE}}{dt} = -\frac{i_G}{C_{GC}} \tag{9}$$

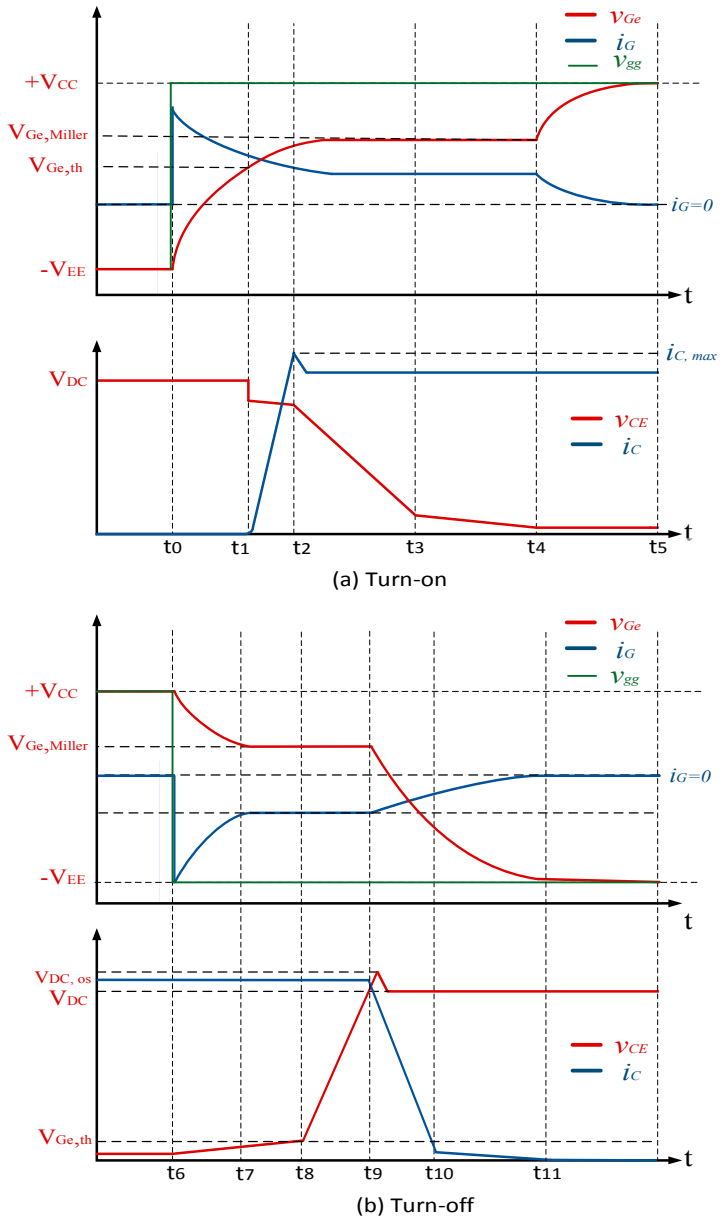


Figure 1. The intrinsic behavior of insulated gate bipolar transistors (IGBTs) at turn-on (**a**) and turn-off (**b**). Switching and controller operation time marked by gray background.

This transition also directly depends on the gate current. Therefore, the method of active gate voltage control could be an effective solution. As shown in Figure 1b, at t8, as soon as V_{CE} exceeds the v_{Ge} value, V_{CE} starts its fast rising until t9. This uptrend is continued as loge as the v_{CE} gets the value of V_{DC}. During this period, the new controller applies a lower voltage to the gate circuit, according to the load condition.

2.2. The Operation Principles

The schematic of the case study and the topology of the new GD are presented in Figure 2. More details regarding the load and circuit component are reflected in Appendix A.

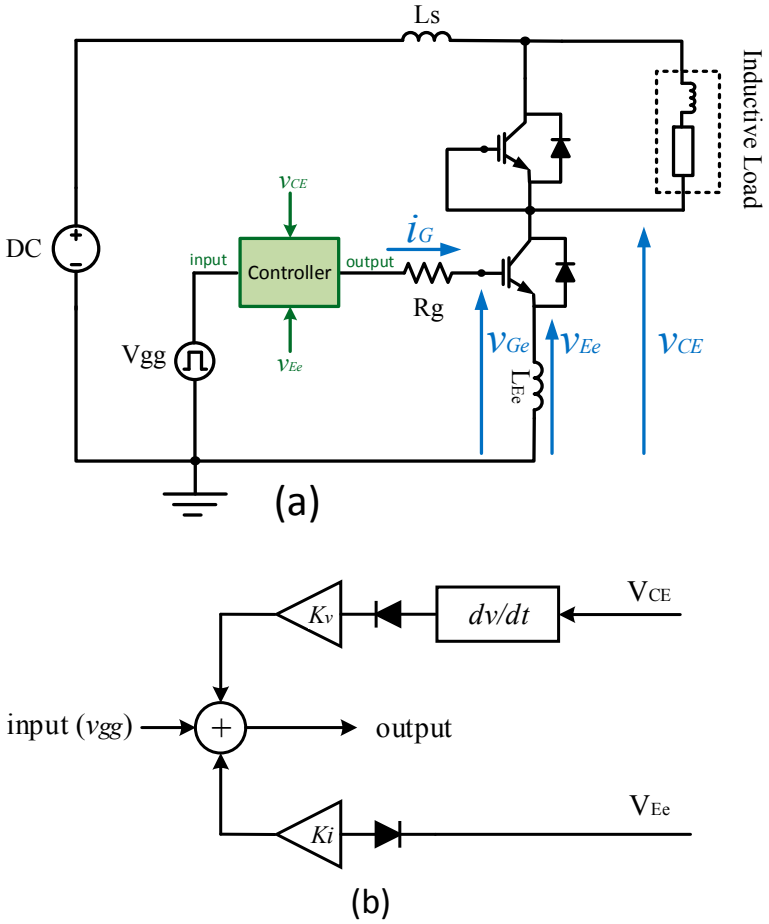


Figure 2. (**a**) The test circuit and the proposed controller in the gate driver (GD). (**b**) General scheme of the controller.

In real condition, an inductance exists between emitter and earth. This inductive factor (L_{Ee}) is a part of stray inductance (L_S), and its value mainly depends on the designed printed circuit board (PCB) layout [44]. During turn-on condition, di_C/dt gets a value and L_{Ee} generates a voltage (v_{Ee}), cf. Equation (10). Based on Lenz's law, the induced voltage has inverse polarity. The positive part of v_{Ee}, which had been created by the current decaying (see Figure 3), is filtered by a diode (see Figure 2b). The created v_{Ee} voltage has di_C/dt factor in itself inherently and that can be used as feedback in the active gate voltage controller instead of getting feedback from the output current. This technique has obvious advantages. For instance, it is simpler because the use of a current sensor would make the circuit more complicated. In conventional closed-loop di_C/dt controllers [3,17], in order to sense error, the measured i_C must be derived in feedback. However, in addition to the use of extra operation (typically by Op-Amp), the transfer function gets an extra dimension, which increases the sensibility of the controller from the stability aspect. Therefore, it can be said that the proposed active gate voltage control method with a simpler structure is more robust as well.

$$v_{Ee} = -L_{Ee} \cdot \frac{di_C}{dt} \tag{10}$$

To achieve the desired di_C/dt and proper transient, the obtained v_{Ee} voltage is adjusted by a Ki coefficient and it is used to reduce the original v_{gg} voltage signal. Thereby, in turn-on condition, the GD feeds the IGBT with proper intermediate voltage. Thus, a controlled current driven by this intermediate voltage at the specific interval (between t1 to t2) will be injected into the gate port.

Moreover, the proposed closed-loop GD makes it possible to control dv_{CE}/dt at the turn-off switching. To maintain voltage transition under control, the positive part of dv_{CE}/dt with a proportional coefficient (Kv) is summed with v_{gg}. The configuration of the proposed closed-loop gate driver as a block diagram is shown in Figure 2b. The voltage type feedback, after summing v_{gg}, modifies its profile. Thereby, di_C/dt and dv_{CE}/dt, during corresponding switching conditions, are controlled by this method of active gate voltage driving.

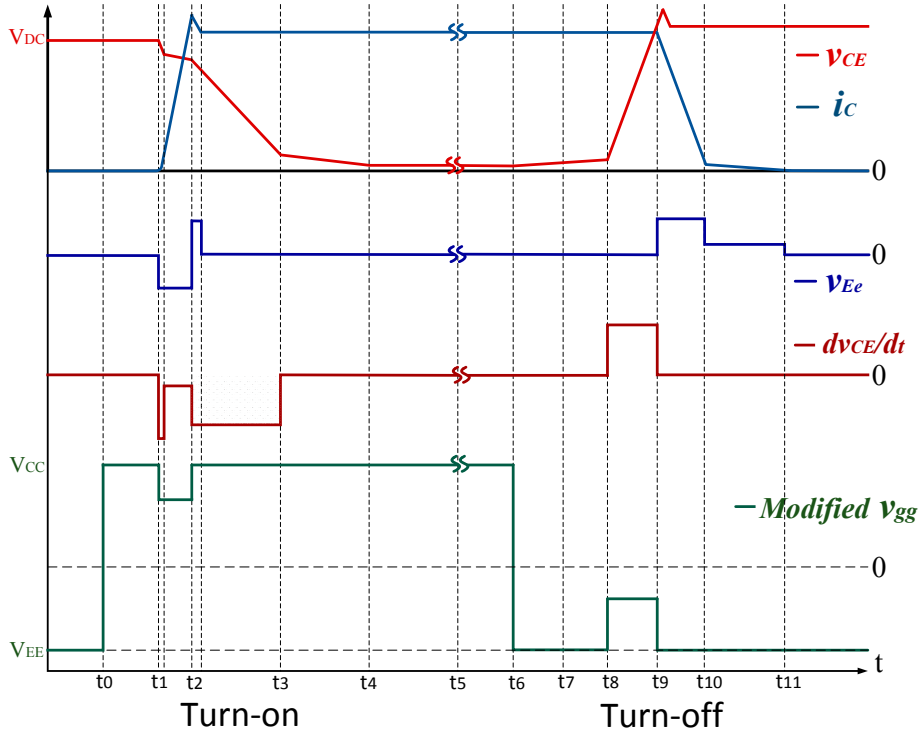


Figure 3. Voltage type feedback signals originated from turn-on and turn-off switching transients and corresponding modified v_{gg}.

3. The Closed-Loop GD Tuning and Experimental Results

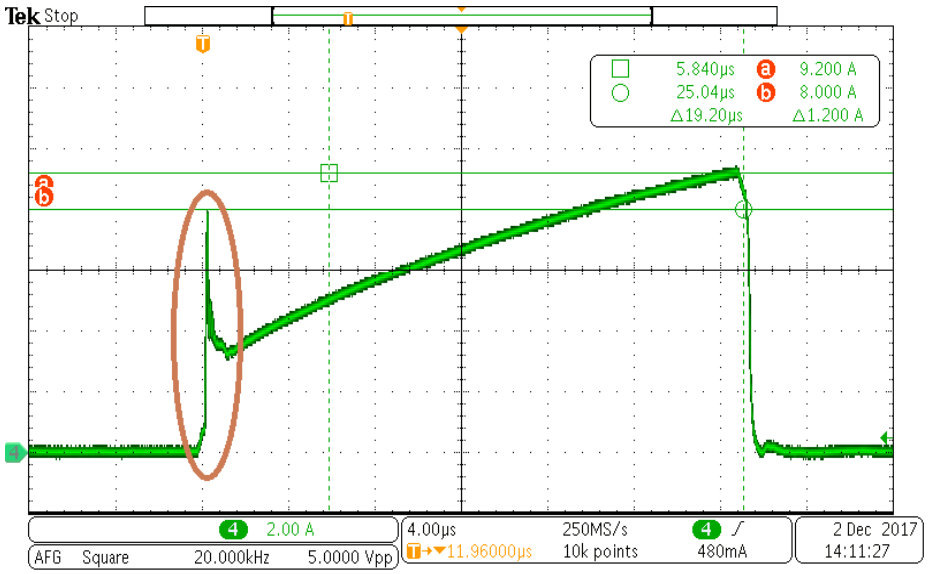
The experimental tests were performed in almost nominal voltage, and a high inductive load created hard switching conditions for the IGBT. The voltage of the dc-bus is 550 V, and the IGBT operates at 5KVA. Two DC power supplies (XFR 300V-9A, Xantrex Technology Inc., Burnaby, Canada) as a series connection provide the power for the test bench.

For each switching state, only one adjustment parameter is necessary, which should be located in the corresponding feedback paths. Through a proper Ki coefficient, a suitable voltage value will be applied to the gate. Therefore, in order to control the di_C/dt at turn-on, the determination of Ki coefficient is necessary, from which a reduction on gate voltage is provoked. As a desirable purpose, a significant reduction in current overshoot and EMI problem will result.

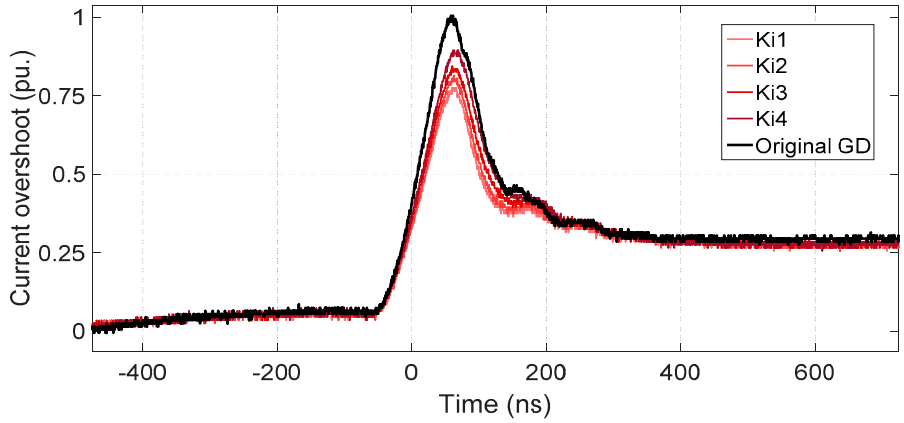
The mathematics logic for di_C/dt and dv_{CE}/dt controlling and overshoot suppression by modification of Δv_{gg} is based on Section 2.1. However, the practical tuning based on the experimental behavior of the IGBT is explained here.

At turn-on condition, in order to allow the IGBT to remain in on-state, the minimum value of intermediate v_{gg} should be higher than the threshold value ($v_{Ge,th}$), whose maximum value is 6.5 V for this device. Therefore, the minimum intermediate voltage (by Ki1) selected is not lower than 6.8 V. Although the IGBT stayed in the active region while applying intermediate voltage, only switching-off condition (see [39]) is able to challenge its operation; however, due to the stability and SOA considerations, the minimum Ki coefficient was selected with high margin. The reflected

experimental results in Figure 4 and Table 1 show how di_C/dt and the overshoot in collector current are both influenced by Ki. The desired Ki can be realized with a simple voltage divider.



(**a**)



(**b**)

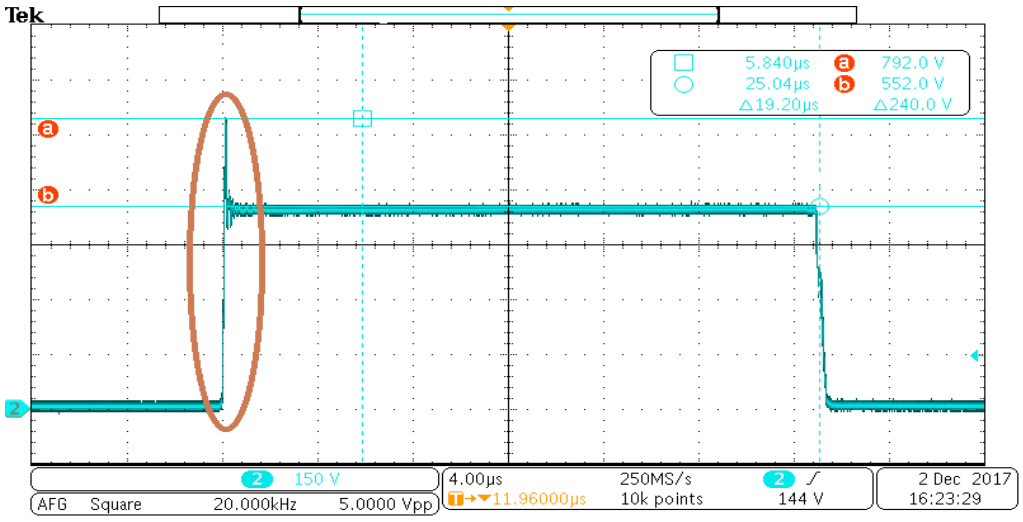
Figure 4. (**a**) The collector current waveform, performed by the original gate driver. (**b**) The zoomed view to show the performance of the Active Gate Driver (AGD) with different Ki coefficient and its effect on the current at turn-on.

Table 1. Collector current trajectory controlled by closed-loop GD with different Ki coefficients.

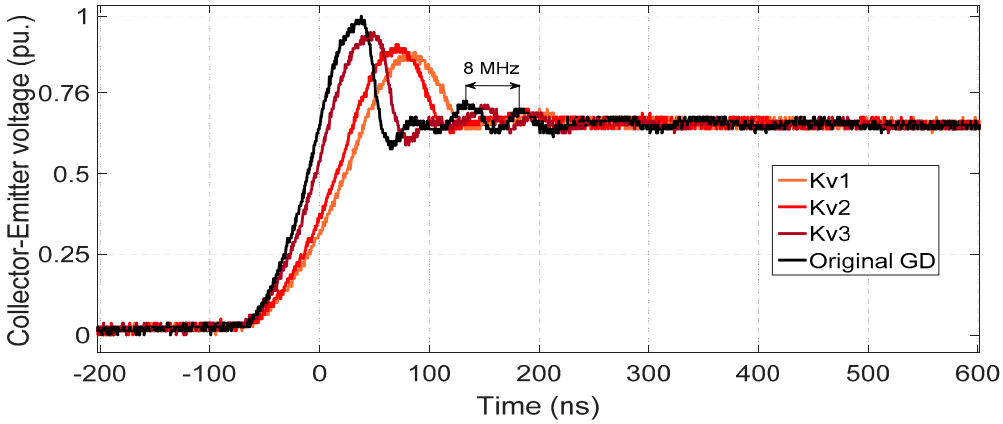
Ki Coefficient	Intermediate Gate-Voltage Levels	di_C/dt (pu.)	Over Current (pu.)
Ki1	6.8	0.54	0.77
Ki2	7.6	0.58	0.8
Ki3	8.4	0.65	0.85
Ki4	9	0.69	0.9
Original GD	-	1	1

The control of dv_{CE}/dt and overshoot suppression at the turn-off switching can be achieved by the feasible solution shown in Figure 2b. The voltage transition will be under control when the controller operates with a proper Kv coefficient. Figure 5 and Table 2 present the role of choosing Kv at turn-off

on the IGBT switching. It should be noted that there is a minimum limit for the differential voltage value (ΔV_{gg}), which has been defined by the application note. Based on this rule, in order to apply minimum ΔV_{gg} to the IGBT (during turn-off condition) and considering a safe margin, Kv1 is set on 3.5 V, which presents the slowest possible turn-off switching.



(**a**)



(**b**)

Figure 5. (**a**) The waveform of collector-emitter voltage, performed by the original gate driver. (**b**) The zoomed view to show the performance of the AGD with different Ki coefficient and its effect on the voltage at turn-off.

Table 2. V_{CE} trajectory controlled by closed-loop GD with different KV coefficients.

Kv Coefficient	Intermediate Gate-Voltage Levels	dv_{CE}/dt (pu.)	V-Overshoot (pu.)
Kv1	3.5	0.64	0.886
Kv2	1.5	0.72	0.911
Kv3	-1	0.79	0.93
Kv4	-4	0.93	0.95
Original GD	-	1	1

The proposed gate driver deals with the changing voltage value of the gate signal (v_{gg}) during switching time. As we know, the IGBT in active region loses its function if the v_{Ge} *(t)* value is less

than its threshold value. This concern has been considered by defining a safe margin area in turn-on and turn-off conditions. All the generated intermediate voltages using the GD in both switching conditions do not affect the operation of the IGBT regarding stability. It should be noted that the previous studies [11] and [45] approve the SOA of the active gate voltage driver technique on the IGBT when it operates with an intermediate voltage of v_{gg}. However, the mentioned references were limited to manual adjusting and the feedforward control method, which are not adaptive with variable load conditions. For this reason, in this study the stability analysis was ignored.

This part does not present an optimization method for the tuning of the controller, because the new GD has a better performance index compared to CGDs in any gain value. In fact, the Tables express the trajectory of the controlling process that affects the slope current/voltage and overshoot, which consequently has an effect on efficiency and EMI. Based on this information, the user may select the level of control on the turn-on or turn-off switching. This advantage of active gate voltage control compared to conventional methods has been already approved in [11] and [45]. The new section details the performance index of the closed-loop GD.

With relation to the effect of temperature, in the Introduction we declared that the proposed closed-loop GD is independent of the IGBT's temperature. It covers all consequences of temperature variation without installing an additional circuit. The consequence of gate side changes (e.g., temperature) can be seen on switching behaviour. This is the essence of the story and the controller may adapt itself through getting feedback from *di/dt* and *dv/dt* and applying it on the profile of the gate voltage.

Temperature influences on the switching time or/and it varies the threshold gate-emitter voltage ($v_{Ge,th}$) value. In the case of switching time, the controller is adaptive and it operates throughout the required switching time. However, the change in threshold voltage value is important from a SOA viewpoint and should be considered in the adjustment of the margin value of the intermediate voltages.

Several studies evaluate the variations of the threshold voltages in IGBTs [28,29]. In [29], the effect of temperature on the threshold v_{Ge} value was evaluated using different device manufacturers. The results showed that the threshold voltage in different IGBTs was reduced up to 1 V by increasing the temperature from 25 °C to 120 °C. It is a key point that the increase of temperature has a negative effect on the $v_{Ge(th)}$ value. In fact, this change even enhances the level of the SOA when the controller reduces the gate voltage value in its operation time (see Figure 3).

4. The Performance Index of Closed-Loop GD

4.1. The Comparison with CGD

In order to evaluate the performance of the proposed GD, the obtained results using the new GD and CGD are compared together experimentally. The meaning of the CGD is the increase of gate resistor Rg value to achieve the desired transient behavior, which is a known technique [3,10,11,20,24]. In this evaluation, both control methods are compared when they have the same rate of overshoot suppression (i.e., a very similar electrical behavior, as shown in Figures 6 and 7). This suppression is for current overshoot at turn-on and also for voltage overshoot at turn-off. To better understand this phenomenon, the resultant di_C/dt and dv_{CE}/dt from the new GD and CGD are compared, including the switching losses (E_{on} and E_{off}). Figure 6 shows the current waveforms at turn-on which resulted from the new GD and CGD. At the same time, the waveforms of collector-emitter voltage are shown in Figure 7. In addition, Table 3 presents all aspects of this comparison.

The Ki1 coefficient regulates the suppression rate of the collector current. The gate resistance is increased up to 23 ohms. It should be noted that the amplitude of Rg in the original GD and in the new GD was 12 ohms, which has been calculated using the IGBT's application note.

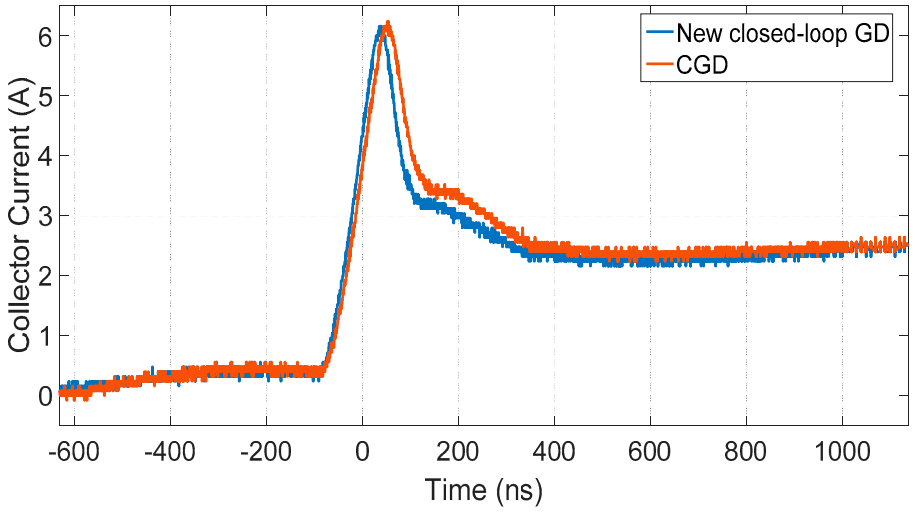


Figure 6. The resultant i_C from the closed-loop GD and conventional gate drive (CGD) at turn-on condition.

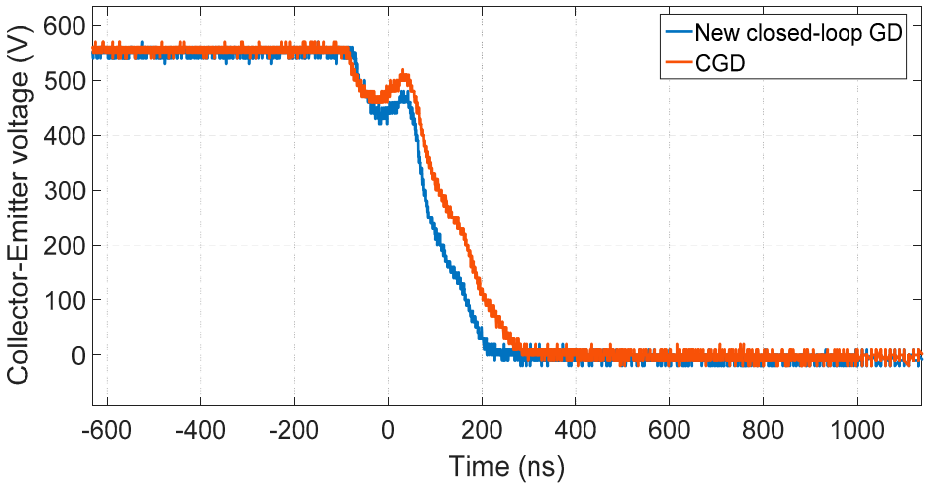


Figure 7. The resultant v_{CE} from closed-loop GD and CGD at turn-on condition.

Table 3. The performance index.

Gate Drivers	Overshoot Value in I_C (A)	Overshoot Value in V_{CE} (V)	E_{on} (μJ)	E_{off} (μJ)
Original GD	8	790	397	716
New GD	6.1	700	465	931
CGD	6.1	700	512	986

To realize the turn-on switching loss (E_{on}), v_{CE} (t), and i_C (t) waveforms should be multiplied together during the active region of the IGBT. The area of the product can be calculated using the equation below.

$$E_{on} = \int_{t0}^{t5} v_{CE(t)} \times i_{C(t)}\, dt \tag{11}$$

Where the elapsed time during t0 < t < t5 cf. Figure 1a is the turn-on switching time, then E_{on} is the turn-on lost energy (in joule) at each switching time.

For comparison at turn-off, the closed-loop GD operates with Kv1 coefficient, while the CGD has increased the gate resistance up to 50 ohms in order to achieve the same damping rate on voltage

overshoot. The performance of both gate drivers is presented as comparative figures, which illustrate collector-emitter voltage and collector current waveforms at turn-off.

The switching loss at turn-off (E_{off}) can be obtained using Equation (11) as well, but the considered domain in the calculation is t6 < t < t11, which includes turn-off switching time cf. Figure 1b. Figures 8 and 9 offer a graphic comparison, and the numerical results are presented in Table 3.

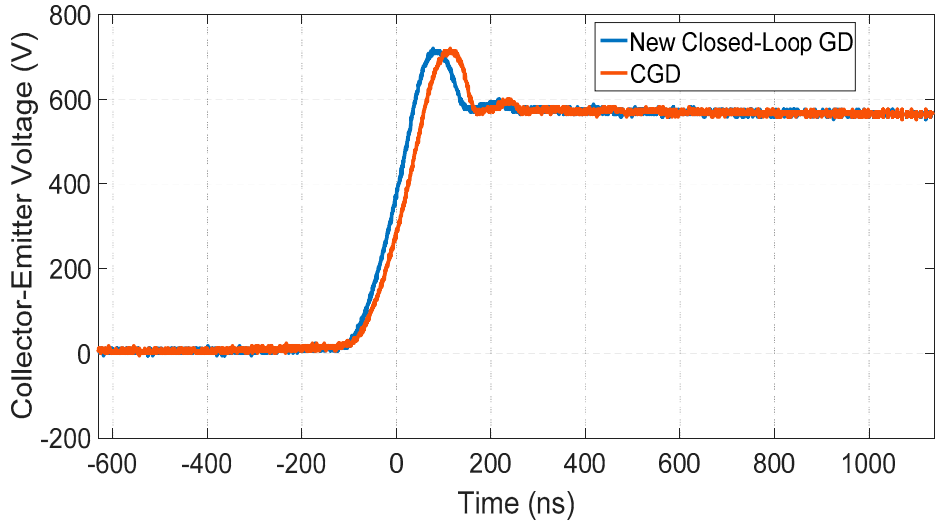


Figure 8. The resultant V_{CE} from closed-loop GD and CGD at turn-off condition.

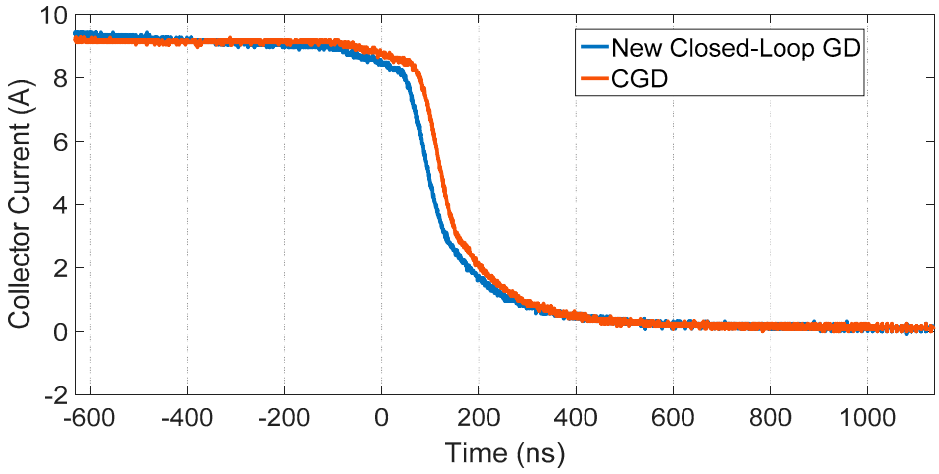


Figure 9. The resultant i_C from the closed-loop GD and CGD at turn-off condition.

It is distinguishable that the new closed-loop gate driver has improved the trade-off between switching losses and overshoot suppression.

4.2. Electromagnetic Interference Analysis

The proposed closed-loop GD has the capability of improving the dynamical behaviour of the IGBT. The high rate of current and voltage transitions (di_C/dt and dv_{CE}/dt respectively) are known reasons of EMI generation in power converters. In addition to the ability of the new GD to reduce the overshoots in output current and voltage with minimum losses penalty, it moderates the oscillation and other effective parameters, which have an impact on EMI appearance.

The following evaluation does not include all the aspects of EMI phenomena; however, the deference rate of EMI through driving with Rg and the new GD can be monitored. The analysis carried out is based on the trajectory of the current and voltage waveforms, which had been experimentally

extracted using an oscilloscope Tektronix MDO3024 (Johnston, OH, USA). The obtained data are applied to the Fast Fourier Transform (FFT) in MATLAB software (version 2015b, MathWorks, Natick, MA, USA) for processing. The effective parameters in EMI production can be characterized using FFT analysis as a periodic trapezoidal pulse. It should be considered that the measured output current and voltage are in common mode (CM) conditions. Figure 10 shows the spectrum for both collector current and collector-emitter voltage. The results show that the closed-loop GD can eliminate the noise in V_{CE} voltage with a resonant frequency of 8 MHz and in I_C current with a resonant frequency of 11 MHz.

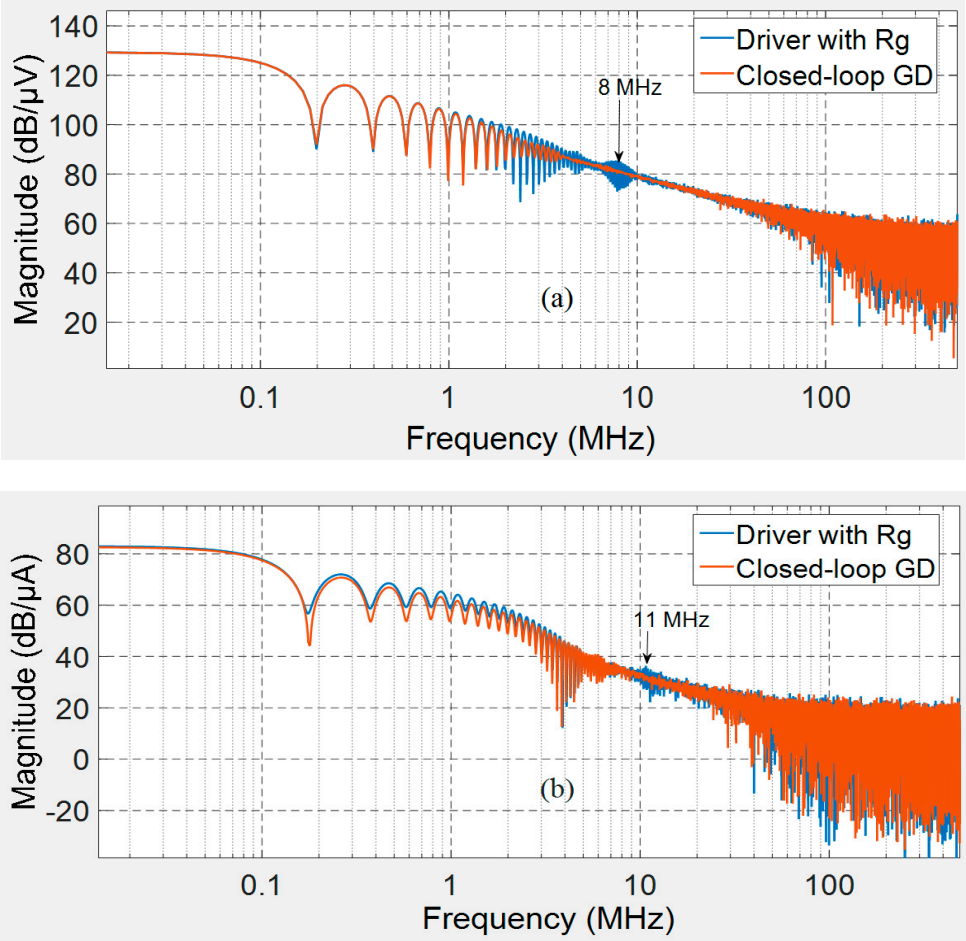


Figure 10. The comparison of resultant spectrum between closed-loop GD and CGD with Rg = 12 Ω tested on V_{CE} and i_C experimentally. (**a**) Spectrum approximation of V_{CE} and (**b**) spectrum approximation of I_C.

4.3. The Cost Study

All MOS-channel switches require a driver to supply the device and provide the desired performance. In power converters with a simple gate driver, snubber circuits are a well-known solution to reduce EMI problems and overshoots. On the other hand, snubber circuits may reduce the system efficiency and it is a large circuit for high-density power converters. However, the main advantage of snubber circuits are the cost and its simple structure. Although snubber-less methods (GD based techniques) compensate for the weak points of the snubber circuits, they increase the cost [44].

The simple structure of the proposed closed-loop GD has already been presented. In this part, the cost study is evaluated. As a reference price, the total cost of the driver plus snubber circuit is considered 1 per unit (pu), which is calculated based on the components price. Accordingly, the price of an implemented totem-pole interface unit cf. Figure A2 consisting of a pair of bipolar NPN and PNP transistors and corresponding resistors is 0.13 per unit. A pair of dual high-speed operational amplifiers and a quad general-purpose Op-Amp is 1 pu. The rest of the components, including diodes, two potentiometers, and some other resistors, represents 0.12 pu of the base cost. The cost of closed-loop GDs may be increased mainly by the high-speed comparators and MOSFETs, whereas in the proposed GD, the use of these components is not needed. As a result, in addition to its effective performance, the new closed-loop GD does not impose a significant extra cost.

In Table 4, the approximated costs of the main characteristics of the proposed closed-loop are compared to the corresponding parameters of a CGD plus snubber network.

Table 4. Cost and characteristic comparison.

Drivers	Cost (pu)	Efficiency	EMI Reduction	Overshoot Reduction
GD+Snubber	1	Medium	High	High
Proposed AGD	1.25	High	High	High

5. Conclusions

This paper proposed a robust closed-loop gate driver for IGBTs. It has been shown that the new GD is able to improve switching transient under hard switching condition with a minimum penalization in switching loss. The following results were obtained from the experimental evaluations:

- The proposed GD has the capability to control di_C/dt and dv_{CE}/dt in turn-on and turn-off respectively. Controlling the GD is possible with very simple tuning in both switching states.
- The closed-loop GD has eliminated the overshoot from collector current by more than 20%. Furthermore, the V_{CE} overshoot has been reduced by more than 10%. Therefore, the IGBT lifetime will be extended.
- The performance index showed that the closed-loop GD has lower switching losses compared to CGD in both turn-on and turn-off conditions.
- This novel closed-loop controller keeps its performance versus Tj and load variations without applying an extra circuit in its topology.
- Based on spectrum analysis of the current and voltage transition obtained from experimental tests, the radiated emission of EMI is reduced during switching transient.
- The proposed gate driver is simple enough to allow its use in real industrial applications. In addition, based on the evaluation carried out it is a fairly cost-effective solution.

According to the philosophy of the proposed closed-loop GD, IGBTs can be controlled permanently in all variable conditions, allowing a novel and real solution for industrial applications.

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Appendix A

The test circuit cf. Figure 2a, consists of the features and components below. The tested IGBT is NGTG50N60FLWG (ON Semiconductor, Phoenix, AZ, USA), clamped to 550 V DC bus-voltage. The applied inductive load is composed of R_{Load} = 59 Ω, L = 780 µH. The switching frequency is 20 kHz.

Figure A1 illustrates the schematic of the controller. In this circuit, the operations and integrations are done by general-purpose LT1364/LT1365 Op-amps (Linear Technology Corporation, Milpitas, CA, USA). Furthermore, both Ki and Kv coefficients are created by simple voltage divider circuits. The model of implemented diodes is 1N4148-TR.

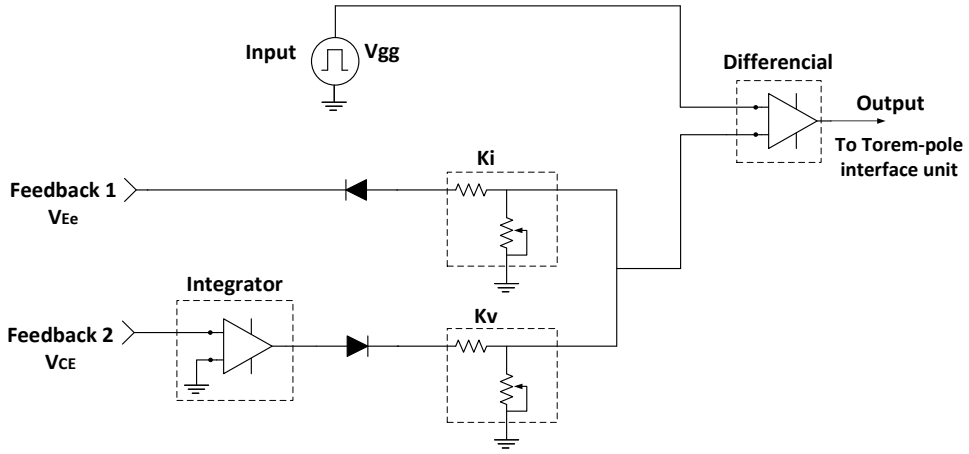

Figure A1. The schematic of the proposed closed-loop controller.

In order to make the connection between the closed-loop controller and IGBT, an interface unit (see Figure A2) is considered which is composed of low power bipolar NPN (2N2222) and PNP (2N2907) transistors. It was supplied by V = ±15 V.

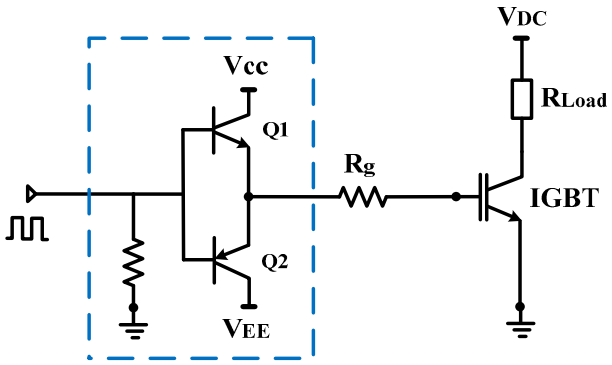

Figure A2. Totem-pole interface unit to gate current supply.

Signal generator (Agilent 33220A-20MHz, Santa Rosa, CA, USA) generates a symmetric gate signal (±2.5 V). In the conventional GD method, this signal is applied to a HCPL-3120 optocoupler (Avago Technologies, San Jose, CA, USA) to have a ±15 V gate signal. Since the proposed controller modifies the profile of the gate signal (v_{gg}) and optocouplers are not able to maintain this modification, a Totem-pole interface unit (see Figure A2) generates ±15 V gate signal for our driving method. The designed interface unit is able to conduct both positive and negative parts of input signals. The Totem-pole circuit does not eliminate the changes of v_{gg} signal.

The active gate driver circuit was designed and implemented as shown in Figure A3.

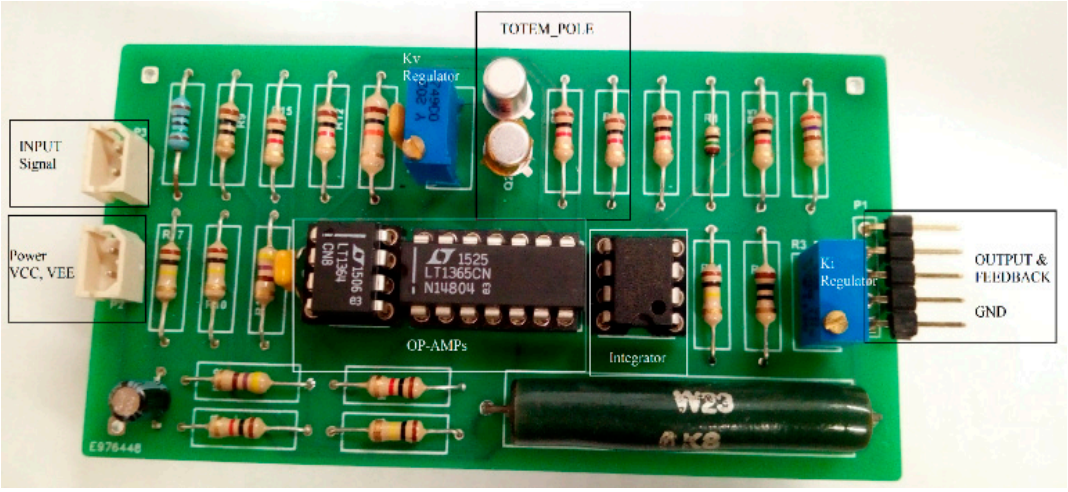

Figure A3. AGD prototype manufactured.

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