Department of Electrical and Computer Engineering

Stabilised Control of Converter Interfaced DERs for Reliable Operation of Microgrid and Microgrid Clusters

Blessy John

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Declaration

To the best of my knowledge and belief, this thesis contains no material previously published by any other person except where due acknowledgment has been made. This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

Signature: 

Date: 22/06/2018

To Lord Almighty for the blessings

and

my family for their unconditional love and support.

Abstract

The demand for power electronic converter interfaced Distributed Energy Resources (DERs) are rapidly growing in present grid systems. In the near future, this trend will replace dominance of fossil-fuel based energy sources in electrical power generation systems. The prime objective of this thesis is to achieve the stabilised control for converter interfaced DER dominated MicroGrid (MG) and MG clusters so that the reliability and resiliency of power generation can be ensured.

With the increasing number of Voltage Source Converter (VSC) fed DERs, the stability and harmonic issues in grid interfaced systems can be aggravated, which necessitates advanced control measures to rectify them. This thesis evaluates the suitability of voltage and current control mode operation for VSCs that have different types of output filters. Voltage control is preferred in an LC filter fed VSC, where a closed loop space vector modulation scheme is proposed to facilitate the effective DC link voltage utilization, in addition to the reduced switching frequency and losses. Furthermore, discrete quadratic regulator control designed considering the filter dynamics is more robust to parameter variations and can provide stable system operation. On the other hand, the current control mode is preferred in L or LCL filter fed VSCs, where a proportional resonant controller is used for regulating the converter current or grid current. The stability issues in these two configurations have been analysed and the need for suitable damping techniques for grid current regulated systems are identified. It has been demonstrated that

the proposed proportional resonant feedback controller can eliminate the stability issues and delay effects in converter current regulated converters. The stability study has also been extended to wide bandgap high frequency converters which can operate at high frequencies. Although an L type filter can sufficiently eliminate the switching frequency harmonics at higher frequencies, the analysis verifies the need for a low value filter capacitor to limit the voltage harmonic distortion in weak grids.

Demand for VSC fed DERs are rapidly increasing in MGs and these energy sources are mainly responsible for sharing loads in islanded mode of operation. In high voltage MGs with inductive feeder lines, the real power demand is distributed among converter dominated DERs by conventional angle droop control. In this thesis, the traditional angle droop control is modified such that the dependence on the output inductance on the real power sharing is removed. Therefore, the lower droop coefficients are adequate for droop sharing and the system stability is not endangered. In addition, a harmonic term has been added to the outer voltage loop to improve the accuracy in reactive power sharing. In medium voltage lines with low X/R ratio, strong coupling between real and reactive power degrades rating based load distribution among converters. Inclusion of a power decoupling term in reference voltage calculation has been found to be more reliable to overcome coupling effects in load power sharing. Angle droop concept along with power decoupling factor has an additional advantage of enhanced reactive power sharing with improved accuracy in active power distribution. This will allows more effective harmonic power distribution among DERs under various operating conditions. In low voltage resistive MGs, the conventional droop control is reversed to obtain adequate load power distribution among DGs. A virtual resistive factor is introduced along with inverse angle droop control to facilitate the improved real and reactive power sharing among converter dominated DERs. The reactive power sharing in an islanded MG is usually achieved by decentralised voltage droop

control, in which the magnitude of PCC voltage is dropped as per reactive power requirements. But the voltage magnitude cannot be reduced below a pre-specified value, otherwise it will adversely affect the power system stability. A low power rated distribution static compensator can actively satisfy a portion of reactive power demand in autonomous MGs. This will help a MG to maintain the PCC voltage drop within permissible standards. A coordinated control strategy is proposed in this thesis to effectively distribute the reactive power demand among DERs and DSTATCOM. Although the harmonic interaction among parallel connected grid converters can be neglected due to the reduced filter requirements in high frequency converters, the circulating current among these converters will result in controller interaction among them. An advanced controller is discussed in this thesis to damp out the circulating currents among parallel converters that can effectively eliminate the controller interaction.

Interconnecting a cluster of neighbouring MGs is inevitable in future power distribution systems, where the reliability and resiliency of energy deployment infrastructure can be achieved by suitable power flow management strategies. A DC Power Exchange Highway (DCPEH) concept is utilized in this thesis to effectively connect multiple MGs placed under a defined geographical area. A power flow controller is developed to manage the power flow between an MG and DCPEH such that, it can respond to the power shortfall in some of MGs by supplying a portion of the surplus power of other MGs. A dynamic droop control strategy is also developed for DCPEH to adequately distribute the power demand between MGs.

The efficacy of the proposed strategies is validated using PSCAD/EMTDC. Stability analysis is performed in MATLAB to analyse the effectiveness of proposed closed loop control systems. Furthermore, the experimental studies with CREE SiC based power converter prototype verify the filtering and control needs of grid connected converters at a various range of frequencies.

Keywords

Grid Converters

Voltage Control

Current Control

Stability Issues

Microgrids

Real and Reactive Power Distribution

Angle Droop Control

Remote Communities

Power Decoupling

Power Quality

Reactive Power Management

DSTATCOM

Interconnected Microgrids

Direct Current Power Exchange Highway

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Nomenclature

Abbreviations

AC	Alternating Current
AFE	Active Front End
AHC	Active High Complementary
CHB	Cascaded H Bridge
CHP	Combined Heat and Power
CLSVPWM	Closed Loop Space Vector Pulse Width Modulation
CPWM	Continuous Pulse Width Modulation
DB	Dead Band
DC	Direct Current
DCPEH	DC Power Exchange Highway
DFE	Diode Front End
DLQR	Discrete Linear Quadratic Regulator
DG	Distributed Generators
DER	Distributed Energy Resources
DS	Distributed Storage
DSTATCOM	Distributed STATtic COMpensator

DSP	Digital Signal Processor
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESR	Equivalent Series Resistor
FC	Flying Capacitor
FFT	Fast Fourier Transform
HPF	High Pass Filter
HRPWM	High Resolution Pulse Width Modulation
IGBT	Insulated Gate Bipolar Transistor
L	Inductive (Filter)
LC	Inductive-Capacitive (Filter)
LCL	Inductive-Capacitive-Inductive (Filter)
LPF	Low Pass Filter
LQR	Linear Quadratic Regulator
MC	Master Controller
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MG	Microgrid
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
OLTF	Open Loop Transfer Function
PCC	Point of Common Coupling
PEH	Power Exchange Highway
PFC	Power Flow Controller

PI	Proportional Integral
PID	Proportional Integral Derivative
PR	Proportional Resonant
PRF	Proportional Resonant Feedback
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
Si	Silicon
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
TBCTR	Time Base Counter
TBPRD	Time Base Period
THD	Total Harmonic Distortion
TI	Texas Instruments
TNP	Transmission Network Provider
VSC	Voltage Source Converter
VSD	Variable Speed Drive
ZSSPWM	Zero Sequence Signal Pulse Width Modulation

Symbols		**Chapter**
V_{dc}	DC Link Voltage	2,3,4,5,6,7
V1-V6	Voltage Active Vectors	2
V0,V7	Voltage Zero Vectors	2
S_1-S_6	Switches of Three Phase Converter	2,3,4,5,6
f_{sw}	Switching Frequency	2,3,4,5,6,7
V_x, V_{x+1}	Two Adjacent Space Vectors	2
T_a, T_b	Time Duration for Active Vectors	2
T_0	Time Duration for Zero Vector	2
Ts	Sampling Period	2,3,4
k	Sector for Reference Vector	2
V_o	Maximum Possible Output Voltage	2
i_f	Current Through Filter inductor	2
$\|V_p\|$	Pre-specified Network Voltage Magnitude	2
L_f	Filter Inductor	2
L_s	Grid Inductor	2
L_1	Feeder Inductor	2
C_f	Filter Capacitor	2
R_f	Converter losses	2
R_s	Grid Resistance	2
R_1	Feeder Resistance	2
V_g	Grid Voltage	2

k_1, k_2	DLQR Gains	2,5,6
v_p^*	Filter Capacitor Reference Voltage	2,5,6
v_p	Filter Capacitor Measured Voltage	2,5,6
u	State Feedback Controller Output	2
h	Harmonic Order	2
X	State Vector	2,5,6,7
K_p	Proportional Gain	2,3,6,7
K_i	Integral Gain	2,3,6,7
V_i	Inverter Voltage	3
V_c	Capacitor Voltage	3
V_g	PCC Voltage	3
i_i	Inverter Current	3
i_c	Capacitor Current	3
i_g	Grid Current	3
i_{cfun}	Filter Capacitor Current-	
	Fundamental Component	3
i_{ch}	Filter Capacitor Current-	
	Harmonic Component	3
i_{chrms}	RMS Value of Capacitor	
	Harmonic Current	3
i_{chrms}^{upper}	Upper Value of RMS Capacitor	
	Harmonic Current	3
i_{chrms}^{lower}	Lower Value of RMS Capacitor	

R_{dmin}	Minimum Value of Damping Resistor	3
m	Modulation Index	3
$m_{1,2,...i}$	Angle Droop Gain of $DG_{1,2,...i}$	4,5,6,7
$n_{1,2,...i}$	Voltage Droop Gain of $DG_{1,2,...i}$	4,5,6,7
$DG_{1,2....i}$	Distributed Generator 1,2....i	4,5,6,7
P_L	Real Load Demand	4,5,6,7
Q_L	Reactive Load Demand	4,5,6,7
$P_{D1,2,...i}$	Real Power Delivered by 1,2,...ith DG	4,5,6,7
$Q_{D1,2,...i}$	Reactive Power Delivered by 1,2,...ith DG	4,5,6,7
$P_{Dirated,i=1,2..n}$	Rated Real Power of ith DG	4,5,6,7
$Q_{Dirated,i=1,2,..n}$	Rated Reactive Power of ith DG	4,5,6,7
$V_i\angle\delta_i$	Bus Voltage	4
$V_{gi}\angle\delta_{gi}$	Voltage across Output Capacitor	4
$R_{Di} + jX_{Di} \quad i=1,2..n$	Feeder Impedance of DG_i	4,5,6,7
$L_{1,2,...i}$	Output Inductance of $DG_{1,2...i}$	4
$G_v(s)$	Transfer Function of Voltage Controller	4
$G_I(s)$	Transfer Function of Current Controller	4
T_i	Time Constant	4
$P_{Didrop} + jQ_{Didrop}$	Drop Across the Feeder Impedance of ith DG	5
$P_{dec1} + jQ_{dec1}$	Real and Reactive Decoupling Factor of DG_1	5

$I_{D\alpha 1} + jI_{D\beta 1}$	Stationary axis Components of Current through Feeder Lines	5
$K_{D\alpha 1}$, $K_{D\beta 1}$	Additional Control Variables in Droop Control	5
T	Transformation Matrix	5
Z_{vi}	Virtual Impedance	5
I_{g1}	Fundamental of Current through Feeder Lines	5
$R_{La,b,c} + jL_{La,b,c}$	Local Load of DG	5
$R_{Lma,b,c} + jL_{Lma,b,c}$	Common Load of DG	5
$v_{pda,b,c}*$	Reference Value for DSTATCOM Voltage	6
$\|V_{pd}\|$	Pre-specified Magnitude of DSTATCOM Voltage	6
Q_g	MG Reactive Power	6
$P_{Gi} * + jQ_{Gi}*$	Reference Value of MG Power	6
$P_{Gi} + jQ_{Gi}$	Measured value of MG Power	6
P_i^*	Total Generation Capacity of ith DG in an MG	7
P_{Li}^*	Total Demand of ith DG in an MG	7
P_{MG}^*	Sum of Local Load Power and Power Supplied to other MGs	7
Trg	Trigger Signal	7
P_{dc}^*	Reference Power to be Drawn from DCPEH	7
P_{SC}	Reference Value of MG Power	7
P_{rsv}	Reserve Value of MG Power	7
V_{dc}	Interlinking Converter DC Link Voltage	7
I_{dc}	Interlinking Converter DC Current	7

V_{dc}^{ref}	DCPEH Reference Voltage	7
$V_{dcj,j=1,2}$	DCPEH Operating Voltage	7
$V_{dcj,j=1,2}$	DCPEH Operating Voltage	7
n_1, n_2	DCPEH Droop Gains	7
R_{f1}, R_{f2}	DCPEH Feeder Resistances	7
e_{d3}	Error in Power Drawn by MG from DCPEH	7
K_{Pd}	Proportional Gain - Overload Prevention Loop	7
K_{Id}	Integral Gain - Overload Prevention Loop	7
V_{dcj}^{*}	Generated DC Capacitor Voltage Reference	7
P_{max}	Maximum Power Supplied to Overloaded MGs	7

Greek Letters

ϕ	Desired Angle of PCC Voltage	2,4,5,6,7
θ	Voltage Space Vector Angle in rad	2
ω	Rated Frequency	2,3
δ	Angle which Maintains Power Flow from VSC	2
ω_{cmax}	System Crossover Frequency	3,4
ω_{res}	Resonant Frequency in radians	3,4
$\omega_{5,7,11...}$	5^{th}, 7^{th}, 11^{th}...Order Harmonic Frequency	3,4
α, β	Stationary Axis Components	3,4
$\delta_{1rated,2rated,...irated}$	Reference Angle of $DG_{1,2,..i}$	4,5
$\delta_{1,2,...i}$	Measured Angle of $DG_{1,2,..i}$	4,5
Δ	Difference between Rated and Measured Value	4,7

ΔV_{max}	Maximum Allowable Voltage Drop	7
β	Lower Limit of Power Band	7
γ	Upper Limit of Power Band	7
λ	Constant Defines the Percentage of Generation Capacity	7
α	Preset Value	7

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Chapter 1

Introduction

The consolidation of Distributed Energy Resources (DERs) has significantly increased in energy deployment infrastructure for the past few years, where Distributed Generators (DG) and Distributed Storage (DS) are together termed as DERs. Although present grids are dominated by conventional power plants (nuclear, gas or hydropower), which produce ac power at a specified frequency of 50 or 60 Hz, it is not sustainable. The technological advances have paved the way for the increased proliferation of power electronic converter fed DERs into existing grid systems. This makes the power grids more resilient and sustainable [1]. Several countries like Denmark, Germany are aiming to achieve above 50 % of rated power from inverter interfaced renewable energy resources like solar, wind and energy storage devices [1], whereas in Australia, Queensland and South Australia are targeting for more than 50 % of power generation from renewable sources by 2030 [2] - [4]. This will form a converter dominated grid in future which can either operate autonomously or grid connected mode. The present and future grid scenario are shown in Figure 1.1. The change from centralized network to these bidirectional Microgrids (MGs) demands the practice of inventive technologies and solutions, including advanced power hardware, associated control devices and software algorithms. Also, the grid regulations need further refinement

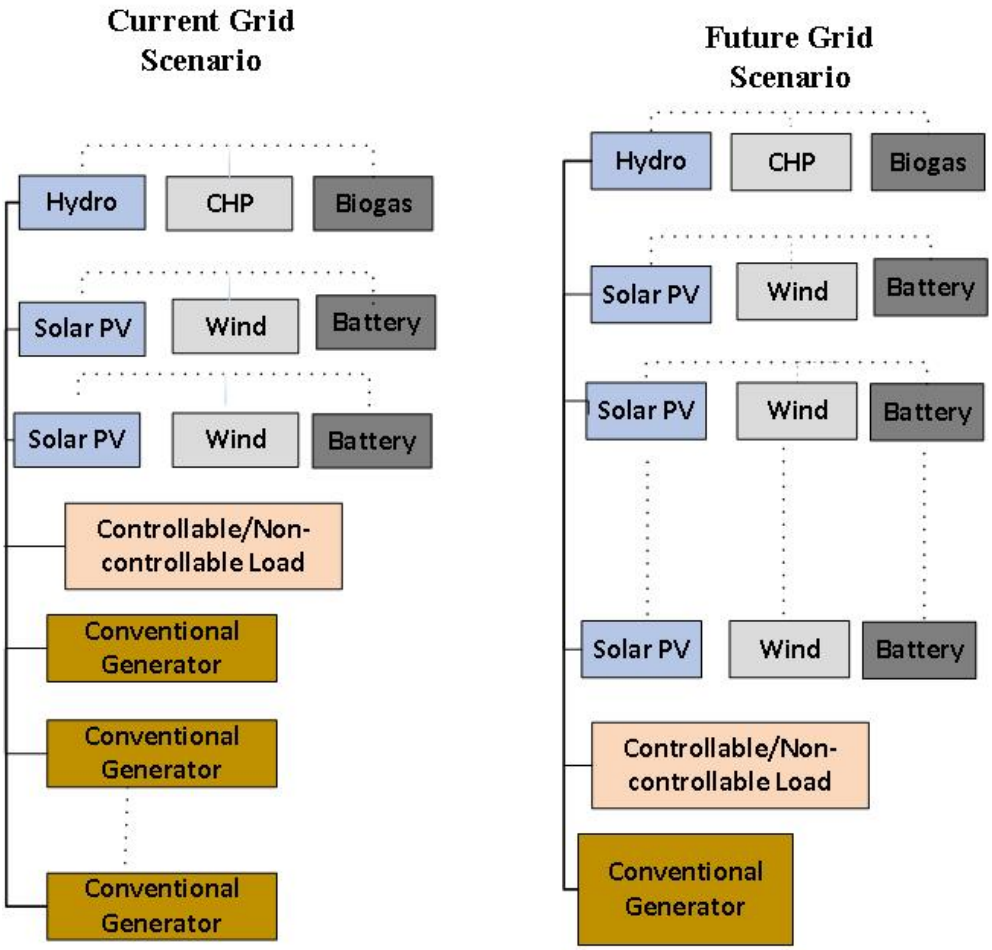

Figure 1.1: Present and future grid scenario

to ensure the quality of power flowing through the grid.

The unprecedented developments in power electronics technology have played a crucial role to solve some of the global warming problems facing by the electricity industry today. Such technologies can be effectively used in renewable power generation, battery storage systems and variable speed drives [5] - [8]. Power electronic semiconductor based controllable converters are the heart of such systems, but the high frequency switching of these devices may affect the power quality of the integrated system. In such scenarios, the individual system level study is very important to mitigate the power quality and harmonic issues due to

high frequency switched power electronic converters [9] - [11]. Grid connected bidirectional converters are usually termed as Active Front End (AFE) converters , where output filters are used to eliminate the switching frequency harmonics. In order to eliminate harmonic resonances in the system, the accurate design of output filters and proper damping methods are necessary to ensure the individual DER stability. Traditional Silicon (Si) based IGBTs are the building blocks of AFE in industrial converters, and these switches can operate at a maximum frequency of around 15 - 20 kHz in high power applications. But, the increased switching losses at high frequency minimize its usage at high frequencies. Recent advances in wide bandgap semiconductor devices like Silicon Carbide (SiC) MOSFETs lead the AFE to operate at high frequencies even with much reduced switching and conduction losses [12] - [14]. Moreover, studies verify that the usage of wide bandgap devices in renewables helps to achieve high energy conversion efficiency [6]. IEEE standards 519 - 2004 and IEC 61000.3.2 define the necessary regulations for individual converters operating in grid connected mode [15] - [17]. The individual converter control includes two feedback control loops, a slow outer loop, for voltage control and an inner faster current control loop. Resonant oscillations and harmonic issues can be tackled by using advanced current control algorithms in the inner loop [18] - [23].

The DERs can either operates in grid connected or islanded mode. In grid connected DERs, the power electronic converter has to ensure the maximum power transfer and real/reactive power control, meanwhile following the acceptable standards for power quality and stability limits. In autonomous or islanded mode of operation, a number of DERs are connected to the point of common coupling and decentralised droop control or communication based methods are used to achieve precise load power sharing among these distributed sources. The conventional droop control techniques, which do not need any explicit communication medium is most desired for primary control in islanded grids for effective rating based

sharing of load power amongst DERs [24] - [27]. These methods are based on the assumption of highly inductive nature of feeder lines. Conventionally, a frequency (P - f) or angle (P - δ) droop method is applied to share the real power whereas voltage (Q - V) droop is preferred to effectively distribute the reactive power among DERs in dominant inductive feeder interfaced islanded MGs [27] - [29]. These methods need further modifications to improve the power sharing accuracy depending on the nature of feeder lines - highly inductive or highly resistive or strong coupled lines. Several factors may affect the accuracy in load power sharing, in which output impedance effect is an important concern in highly inductive MGs [30]. Even though these effects can be nullified by using higher droop gains, it may lead the system to instability [31]. Active power sharing accuracy can be improved by advanced droop control methods, but the reactive load power distribution needs further refinement and studies since it affects the power quality and leads to the non-permissible voltage drop at Point of Common Coupling (PCC). Remote area MGs can have either resistive feeder behavior or strongly coupled nature. Usually, these MGs are located in isolated places where there is minimal or no access to the utility grid. Decentralized power sharing strategy needs further improvement in such cases [32] - [37], where the effective sharing of real and reactive power is inevitable to maintain the power quality within permissible limits.

High penetration of converter interfaced DERs to the utility will aggravate the power quality and harmonic issues at the PCC. These issues have some deleterious effects such as excessive heating in transformers and generators, equipment malfunction and damage, EMC issues and overvoltages due to excitation of power system resonance [38]. Normally passive or active filtering methods are used to eliminate the power quality issues, in which active filters like Distributed STATCOM (DSTATCOM) is preferable and cost-effective. In an islanded MG, DSTATCOM can also participate in reactive power distribution and therefore compensates for the excessive voltage drop at PCC [39] - [43]. In grid connected mode,

the feeder impedance can create resonance with the output filter capacitor, which further results in circulating current among DERs [12], [44] - [46]. This will lead to additional power quality issues in parallel connected AFEs. At higher frequencies (in the range of 100 kHz), these harmonics effects are negligible due to the drastic reduction of output filter size at high frequencies. But in grid following converters, the effects of controller interaction among parallel converters needs further investigation. Interconnecting MGs is a viable solution for maintaining the resiliency and reliability of autonomous distribution system as per the IEEE standard. 1547.4 [47]. Clustering neighboring AC MGs will become unavoidable in future smart grids, where the power shortfall in a particular MG can be compensated by the surplus power from neighbouring MGs [48] - [50].

This chapter provides a short synopsis of current and future grid scenarios, mainly

- The role of MGs and their power management strategies.
- Individual converter interfaced DER topologies and their control methods.
- Harmonic issues in grid connected converters at high switching frequencies.
- Power quality issues due to the parallel connection of a number of DERs.
- and the necessity of effective reactive power distribution in MGs when operated in either grid connected or islanded mode.

1.1 Grid Converters

The DERs or variable speed drives (VSDs) should undergo multiple power conversion process such as AC - DC or DC - DC or DC - AC before being integrated to the grid. The final stage of this power conversion system is DC - AC conversion (AC

- DC in VSDs). This stage is necessary to make the ac electricity compatible with the ac grid power system in addition voltage and frequency synchronisation. Grid connected converters should meet the necessary harmonic limits; otherwise, it can create harmonic issues which may affect the other DERs and loads connected to the system. In addition, it will negatively impact the stability of the power grid. Typical examples of harmonic sources are arc furnaces, switched mode power supplies, VSDs, transformer magnetising currents and electronic ballasts [38], [51] - [52]. Harmonic standards are defined not only in terms of total harmonic distortion (THD) but also the individual harmonic order limits. IEEE 519 - 2014 and IEC 61000 3.2 have defined the necessary power quality requirements and harmonic limits for grid interfaced bidirectional converters [15] - [17].

Table 1.1: Voltage distortion limits according to IEEE 519-2014

PCC Voltage (kV)	Individual Harmonics (%)	THD (%)
V$\leq$1 kV	5	8
1 kV $<$ V $\leq$ 69 kV	3	5
69 kV $<$ V $\leq$ 161 kV	1.5	2.5
161 kV $<$ V	1	1.5

The recommended harmonic current injection and voltage distortion guidelines provided by IEEE 519 - 2014 are given Table 1.1 and Table 1.2 respectively, where V is the bus voltage at PCC, I_{sc} and I_L are the maximum value of short circuit current and demand load current under normal operating conditions at PCC respectively. Even current harmonics should be limited to 25 % of odd current harmonics.

Table 1.2: Current distortion limits for systems rated 120 V through 69 kV: maximum percentage distortion of individual odd order current harmonics

$x = I_{sc}/I_L$	$3 \leq$ h < 11 (%)	$11 \leq$ h < 17 (%)	$17 \leq$ h < 23 (%)	$23 \leq$ h < 35 (%)	$35 \leq$ h < 50 (%)	TDD (%)
$x < 20$	4	2	1.5	0.6	0.3	5
$20 < x < 50$	7	3.5	2.5	1	0.5	8
$50 < x < 100$	10	4.5	4	1.5	0.7	12
$100 < x < 1000$	12	5.5	5	2	1	15
$x > 1000$	15	7	6	2.5	1.4	20

The detailed study on grid converters can be categorized into three different parts, viz. the power converter and associated output filters, control techniques and the Pulse Width Modulation (PWM) techniques, as explained below.

1.1.1 Classification of Grid Converters Based on Power Circuit Structure

Grid converters can be classified as two types viz. Diode Front End (DFE) converter or AFE converter based on the structure employed.

Diode Front End Converter

DFEs are traditionally followed in VSDs (low or medium voltage), where a 6 pulse rectifier is used for AC-DC conversion. The main disadvantage of this configuration is the harmonic distortion at the supply side since DFEs are uncontrolled. But the harmonic distortion can be reduced by using multi-winding transformers fed DFEs. The harmonic distortion is lesser in 12 pulse rectifiers, but necessitates

the use of three winding transformers. Further moving to multi-pulse configuration say 24 or 36 pulse can reduce the harmonic content with the additional cost of multi-winding transformers [52] - [54].

Active Front End Converter

In contrast, AFEs are bidirectional power electronic IGBT or MOSFET based converters. In case of electric drives, the initial implementation cost is higher in AFEs compared to DFEs, but it reduces the harmonics in network side [55]. In addition, it can also provide the reactive power compensation. AFE is also utilised in DGs (DERs), where it performs the DC-AC conversion. In battery energy storage systems, power flow is AC-DC or DC-AC during charging or discharging mode respectively [6] - [8]. Based on power converter structure, AFE can be classified into two types two level converter and multilevel converter.

- Two Level Converter

  Two level converters are extensively used in a wide power range for industrial applications. PWM techniques are utilized to generate the sinusoidal AC output, but the quality of the waveform is compromised due to increased higher order harmonics. This topology possesses attractive features such as simple circuitry, small DC capacitors, small footprint and size in addition to the same duty cycle pattern for all semiconductor devices [55]. But the need for large AC filters to mitigate the switching frequency harmonics and the high switching losses of semiconductor devices under high switching frequency are main shortfalls. Furthermore, each switch has to withstand the large blocking voltage. These drawbacks can be overcome by adopting the emerging SiC semiconductor devices, which can switch at higher switching frequencies with lower losses [13], [55] - [56].

- Multilevel Converter

  Multilevel converters have gained acceptance in medium and high power applications. In multilevel converters, the switching frequency of semiconductor devices is substantially lower. While comparing with a two level converter of the same rating, multilevel converter offers lesser harmonic distortion and reduced switching losses. This means, the converters can operate for high power applications with reduced losses, but the significant increase in number of switches will result in increased cost. The three basic multilevel topologies are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB). CHB is preferred in renewable applications as it uses independent power sources for individual H-Bridge [55], [58]. Modular multilevel converter (MMC) is an advanced topology of CHB, and these are used for HVDC applications due to its promising features. The potential drawbacks of multilevel converters are the increased number of semiconductor devices and complexity in PWM implementation.

1.1.2 Classification Based on Power Semiconductor Devices

Traditionally accepted Si based IGBTs are mostly utilized in AFEs, and these devices can switch at relatively high frequencies. But the recent development in wide bandgap SiC devices allows the semiconductors to switch at higher frequencies for high power applications.

- Si Devices

  Si based devices are mature, inexpensive and traditionally utilized in most of the industrial applications. Si IGBTs includes the advantage of both Si BJTs and Si MOSFETs, where the switching control is same as in MOSFETs and the output structure is a replica of BJTs. But it cannot operate at higher switching frequencies ($>$ 20 kHz). In addition, the increased switching

losses due to the tail current during turn-off is a challenging problem for high power applications . Even though it can operate at higher voltages, the need for semiconductor devices that can operate at high switching frequencies with lower losses and high temperature withstanding capability opens the way to wide bandgap devices.

- SiC Devices

  The emergence of high efficiency SiC technologies allows the semiconductors to switch at several kHz frequencies with lower switching and conduction losses [59] - [68]. Studies reveal that the switching loss can be reduced to half by replacing the silicon freewheeling diodes with SiC schottky diodes [13]. The attractive features of these promising devices are

  ✓ 10-fold higher electrical breakdown strength allows 1/10 times drift layer thickness, which ultimately results in very low on state resistance.

  ✓ 3 times higher bandgap which prevents the flow of leakage current and enables the high temperature operation. These devices can operate up to an extreme junction temperature of 600 ^{o}C.

  ✓ Due to the superior dynamic characteristics of SiC devices, conduction and switching losses are much reduced and thus the total power loss in semiconductor devices are reduced.

  ✓ 3-fold higher thermal conductivity allows better heat dissipation. This feature reduces the cooling requirements.

  ✓ Efficiency level can be increased up to 99 % in SiC based three phase converters.

Comparisons between Si and SiC devices are summarised in Table 1.3 [59] - [61].

Table 1.3: Performance comparison of Si and SiC devices

Semiconductor Device	**Electric Breakdown Field** (MV/cm)	**Bandgap** (eV)	**Thermal Conductivity** (W/cm^{o}C)
Si	0.3	1.1	1.5
SiC	3	3.2	4.9

1.1.3 Classification Based on Output Filters

As mentioned earlier, the high frequency switching of power converters produces switching harmonics, which are usually filtered out by the output filters [69]. Filter configuration can be of L or LC or LCL type as shown in Figure 1.2.

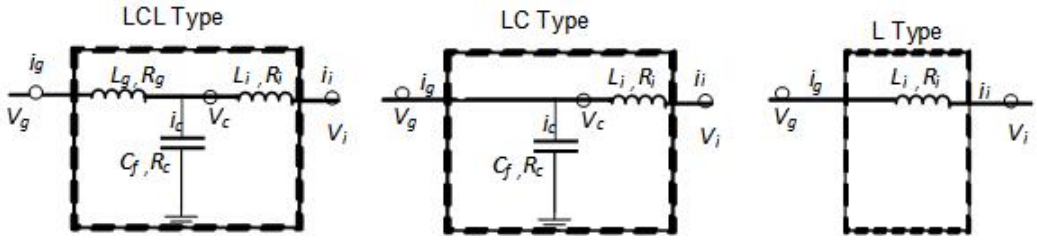

Figure 1.2: Different filter configurations for grid converters

The design of these filters depends on many factors such as the current ripple, DC link voltage, switching frequency, tolerable reactive power, THD and voltage drop [69] - [71]. Among these, switching frequency is an important parameter in reducing the passive component size.

- L Type

  A first order L filter provides 20 dB/decade attenuation to the frequencies

above the control frequency. In this type, inductor value depends only on output current ripple and voltage drop across the inductor. In this case, the resonance phenomenon can be avoided, but a large inductance is necessary to limit the high frequency switching ripple content. The main shortcomings of this type are the larger size and high cost in addition to the excessive voltage drop across filter inductor. L filter is used only in low kW applications. But if the switches can operate at high switching frequencies ($>$ 50 kHz), this type can be adopted in high power applications [72]. SiC power converters are newly introduced in markets [67] - [68], which enables only an L type filter to effectively eliminate the switching ripples.

- LC Type

  LC filters are mainly preferred for applications in which offers high load impedance to switching frequency components and its multiples. Usually, it provides -40 dB attenuation to higher order harmonics, but the resonance created with varying grid impedance conditions is a hindrance in its usage for industrial applications. LC filters are preferred with voltage controlled grid connected converters [39], [42] which will be discussed in Chapter 2.

- LCL Type

  Since traditionally accepted Si based IGBTs can operate at a maximum of 15 kHz, an LCL filter is required to effectively attenuate the switching frequency related components. The shunt component can even produce reactive power based on its sizing. In addition, LCL offers -60 dB attenuation for frequencies higher than the resonant frequency. Filter parameter design is influenced by the resonant frequency, output current ripple, reactive power limits, grid impedance variations as well as the voltage drop across inductor [70] - [71]. LCL filter design and corresponding stability issues are still an ongoing area of interest for researchers since any inaccuracy in LCL filter and damping

techniques may lead the system to exceed the accepted grid harmonic limits [73] - [79].

1.1.4 Control Techniques for Grid Converters

Closed loop control of AFEs consists of two control loops; a slower outer loop and a fast acting inner loop.

- Outer Loop Control

  The outer loop requires lesser bandwidth and it determines the overall stability of the system. Outer loop control varies depending on the different operating modes [2], [6], [8], such as

  ✓ Grid Following

  ✓ Grid Forming

- Inner Loop Control

  The control of this loop can be achieved in two different ways, namely current control or voltage control.

  ✓ Current Control

  Current control plays a prime role in grid connected converters and the design of such algorithm has a substantial impact on system stability. Current regulators usually operate by passing the difference between the reference and measured values of current to a controller. Grid current or converter current can be chosen as a feedback variable, in which converter current mostly opts in industries where the system possesses inherent damping capability due to the existence of resonant zero in the system transfer function [18] - [21], [73] - [76]. In addition, choosing converter current for current regulation can be an appropriate

solution in grid converters as it ensures the protection of semiconductor devices without additional sensors. But literature suggest that delay factor has a negative impact on system stability, where the inherent damping capability of converter current feedback control cannot ensure system stability due to the adverse influence of delay in system phase-frequency characteristics [78]. As a result, damping should be necessary for converter current feedback control scheme so as to limit the harmonic distortion of grid current and voltage in line with the standards. This effect mainly depends on control and switching signal generation in digital processors.

On the other hand, the plant (LCL type) with grid current as the current regulator is always unstable due to the oscillations around its resonant poles. It has been identified in [21] - [23], [74] that, in certain regions of frequency, the inherent capability of LCL type with grid current regulator can result in a stable system. This is due to the shifting of the resonant region to high frequency region which falls outside controller bandwidth. This means, if the LCL filter is designed such that the resonant frequency falls outside the bandwidth of the system, the inherent damping capability will be improved and this further eliminates any passive or active damping requirements. This advantage is utilized in many of the researches conducted recently, but the negative impacts of these high frequency resonances when a number of such converters are connected in parallel to a distributed grid has been identified in [9]. Also, these higher order harmonics may affect the communication in addition to causing EMC issues. Furthermore, the resonant frequency may vary over a wide range under weak grid conditions, so inherent damping capability or any damping methods tuned to specific resonant frequency cannot be a permanent solution in such systems. Current

regulators can be implemented in abc frame or synchronous frame or stationary axis frame, in which synchronous (dq) and stationary frame ($\alpha\beta$) controllers are popular in industries.

- Synchronous Frame (dq) PI control

  Direct and quadrature axis based decoupled control is most commonly adopted in current controlled grid converters. A linear proportional integral (PI) control is used for regulating direct and quadrature axis currents in synchronous frame [74], but it cannot completely eliminate the steady state error. It also requires high bandwidth controller to effectively control steady state error and harmonics [18] - [20].

- Stationary Frame ($\alpha\beta$) PR control

  In this type, stationary axis current components are regulated using Proportional Resonant (PR) controllers. Although the steady state error can be eliminated by using a proportional resonant controller, the increased individual lower order harmonics are considered as the main drawback of this controller [18] - [20]. But these harmonics can be controlled by adding resonant terms for individual dominant harmonics [22] - [23]. In addition, the discrete implementation is not straightforward for this second order controller [80].

✓ Voltage Control

In voltage control, Discrete Linear Quadratic Regulator (DLQR) based state feedback method is utilized to regulate the PCC voltage. Current control methods do not incorporate output filter characteristics, but the voltage control has the advantage of included filter dynamics [39], [42]. In addition, DLQR based converter inner loop control method provides robustness to the individual converters under different

types of loads. In [39], [42], a DLQR based state feedback control is used to control the interfacing VSIs, where the voltage across the filter capacitor is controlled irrespective of the filter structure (LC or LCL). Even though aforementioned control is robust to any parameter variations, the switching controller employed may lead to excessive converter losses. The main drawback of voltage control for converters is the complexity in control with LCL type configuration. This is due to the increased number of state variables (three state variables instead of two in LC) which necessitates additional number of sensors. The type of inner loop control along with suitable filter configuration and its advantages are summarised in Table 1.4. This filter and control configuration is followed for grid converters throughout this thesis.

Table 1.4: Different filter and controller configuration in grid converters

Grid Converter Control	**Filter Type**	**Features**
Current Control	L	-20 dB attenuation to higher order harmonics, Suitable for high frequency converters
Current Control	LCL	-60 dB attenuation to higher order harmonics, Suitable for low and high frequency converters, Minimal number of state variables, which avoids usage of additional sensors.
Voltage Control	LC	-40 dB attenuation to higher order harmonics, Suitable for low and high frequency converters Included filter dynamics, Robust to parameter variations.

1.1.5 Damping Methods for Grid Converters

The output filters used for eliminating the switching frequency harmonics create resonance in grid converters. The unwanted oscillations in this resonant region may lead the system to instability unless otherwise provided with any damping mechanisms. Two types of damping methods are used in industries.

- Passive Damping

  An effective way to cope up with the resonant oscillations in strong grids is passive damping. A simple passive damping incorporates a resistor in series with the filter capacitor. Damping resistance can provide attenuation to resonant oscillations, but it will introduce additional losses in the system [81]. Even though the increased resistance will result in better stability and lesser harmonic distortion, it can adversely affect the attenuation capability of third order filters.

- Active Damping

  Active damping can introduce the similar effect of passive damping by modifying the control algorithm. The damping effect is achieved by the feedback of additional control variables in the system or by other compensation measures. Basically, in active damping, a virtual resistor concept is introduced to provide a damping effect to the resonant oscillations. Several active damping methods have been described in literature where damping is achieved by feeding back additional filter control variables such as capacitor current or capacitor voltage or grid current [82] - [85], but the need of additional sensors and complex control algorithms for sensorless damping compromises their merits.

1.1.6 PWM Techniques Adopted in Grid Converters

The fundamental aim of PWM is to produce a train of switching pulses to create the desired voltage or current [86]. The controller generates the suitable reference modulation signal for the PWM block which is used to implement the switching pulses for power semiconductor devices.

PWM techniques can be divided as asynchronous and synchronous schemes. In asynchronous mode, the switching signals for voltage source converters are synthesized by comparing a high frequency triangular carrier with a reference voltage. Asynchronous PWMs are commonly used in hard switched industrial grid connected three phase converters. Literature mentioned several PWM strategies for three phase AFEs [86] - [93], which are briefly discussed below.

- Sine-Triangle PWM (SPWM)

  The asynchronous SPWM compares the three phase sinusoidal reference with a high frequency triangular carrier to generate the switching pulses. It is the most simplified PWM technique. But it has few drawbacks viz. poor DC link voltage utilization, reduced maximum peak fundamental output line voltage and higher harmonic distortion.

- Third Harmonic Injection PWM

  In this case, a common mode third harmonic signal is added with the reference waveform to increase the modulation index, which further results in better DC link voltage utilization. By adding a one-sixth magnitude third harmonic term to the reference, a 15 % increase in modulation index can be achieved. The magnitude of the third harmonic term depends on the harmonic distortion and the maximum modulation index. Literature show that adding one-fourth third harmonic term results in reduced harmonic distortion with slightly retarded modulation index increase of 12 % [86] - [89].

- Space Vector PWM (SVPWM)

  In space vector PWM, the arbitrary reference waveform is generated by averaging the space vectors over a switching period. Similar to third harmonic injection PWMs, SVPWM also possesses the attractive features of a 15 % increase in maximum modulation index, lesser harmonic distortion and improved DC link voltage utilization. Zero vectors can be positioned symmetrically or asymmetrically in a switching period and based on that SVPWM can be classified as asymmetrical SVPWM and symmetrical SVPWM. Symmetrical PWMs offer lesser harmonic distortion [86] - [90]. SVPWM is commonly used in current controlled AFEs and electric drives.

- Sliding Mode Control

  In [91], authors propose a sliding mode control in which VSIs are designed to operate the system space to a different sliding surface in the state space. The scheme fails to operate in different operating conditions and loads.

- Selective Harmonic Elimination

  Although the synchronous selective harmonic elimination method eliminates pre-specified lower order harmonics with a reduced switching frequency, the variations in the power grid may change the behavior of lower order harmonics [92].

1.2 Microgrid

MG is an integrated system consisting of DERs and controllable loads which can either operate in grid connected or autonomous mode [94] - [98]. It has the remarkable potential to enhance reliability and resiliency with reduced fossil-fuel dependency. The advances in power electronics will lead to the increased penetration of renewables in MGs. A typical example of MG is shown in Figure

1.3. A set of controllable DGs like Biogas, Hydro, Combined Heat and Power (CHP) or conventional Generator) or intermittent DGs like solar or wind, DS and controllable loads form an MG, which can either be connected to the power grid or can work autonomously [95]. ABB has pioneered 8S concept to evaluate the best mix of DGs, DS and control technologies in an MG [97]. Accordingly, the 8S power system functions are Stabilizing, Spinning reserve, STATCOM, Standalone operation, Smoothing, Shaving, Shifting and Seamless transfer. A renewable dominated MG should include more functions from 8S for improved performance [97]. Rapid penetration of DERs in MG market has eliminated the limitations in power generation and distribution capability, even in islanded or remote place operations. These DERs can be constant or variable power sources.

Power quality can be controlled by interfacing DERs using power electronic converters, where in addition to simple power conversion, any unbalance or deviations in utility voltage due to unbalanced zero or negative sequence currents can be compensated by modern control techniques [6] - [7]. In rural areas, the autonomous operation of MGs is desirable as the rural electrification is not cost-effective. In addition, the developments in Renewable Energy Sources (RESs) like wind and solar lead to converter dominated DERs in MGs with considerably reduced capital costs [2] - [3]. The developments in battery storage systems can provide necessary ancillary services to remote MGs, therefore maintain the power quality as well as provide compensation for the non-inertial nature of renewable sources [8], [99]. In autonomous MGs, decentralised droop control methods or communication based control techniques have been used so far for the effective load sharing and voltage regulation. These are explained as follows.

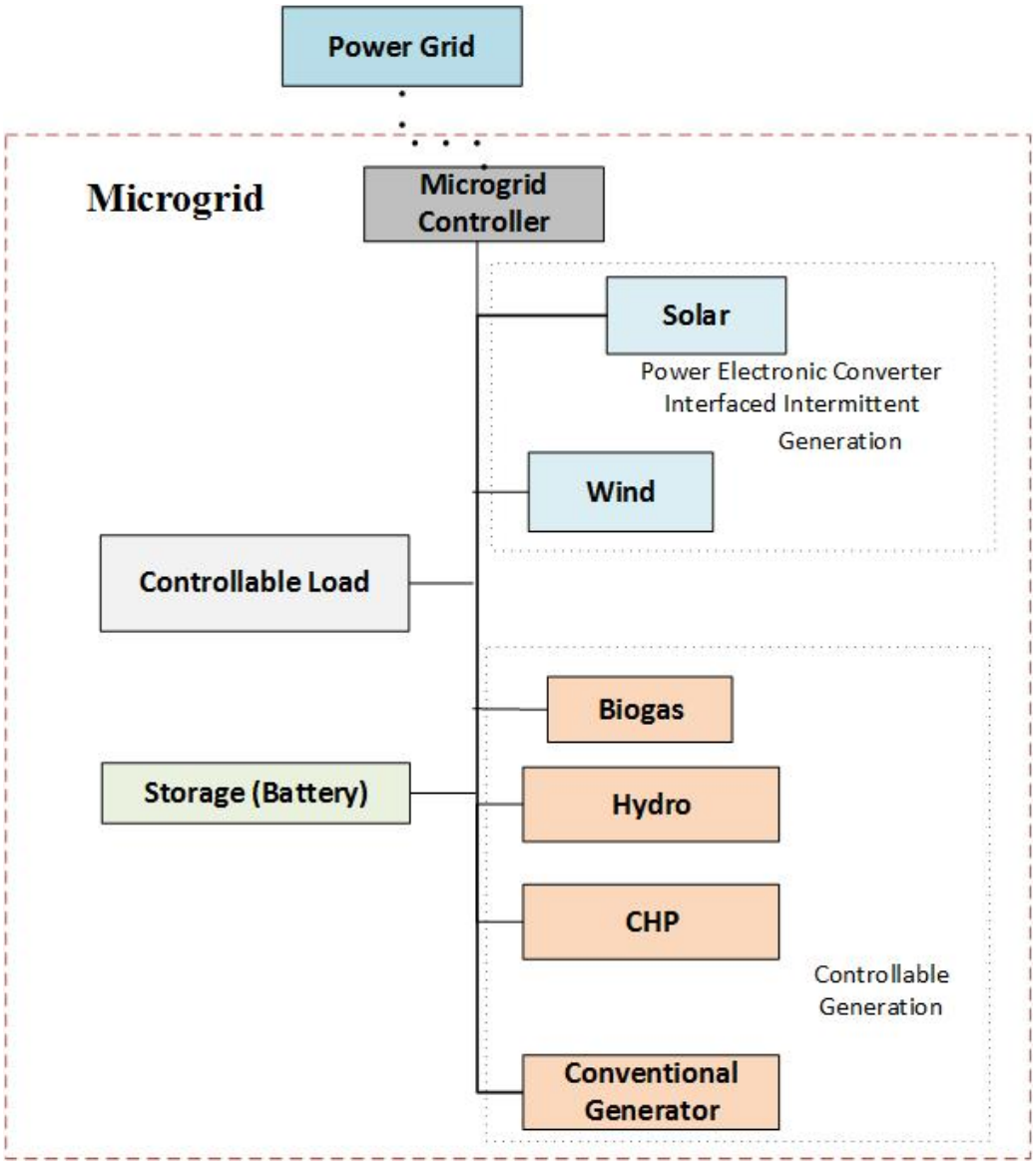

Figure 1.3: Different filter configurations for grid converters

1.2.1 Communication Based Control Techniques

Communication based methods offer excellent load power sharing and effective voltage regulation, albeit at an increased cost of communication medium between different DERs. Commonly used communication based control methods are master slave method, concentrated control and distributed control.

1. Master Slave Method

   In this method, the first DER will act as a master converter and the others will remain as slave converters. The master converter will take care of parallel control by regulating the PCC voltage and setting the current reference for slave converters. Slave converter currents will follow this reference for effectively distributing the load current. Even though this method has a pitfall of system shutdown during master converter failure, a random selection of master converter will improve the reliability [24], [99].

2. Concentrated Control

   In this method, a common synchronisation signal and individual current sharing modules are necessary for each DERs. Current sharing modules will define the reference current for individual DERs based on the sensed total load current. The required angle or the frequency of PCC voltage is ensured by the synchronisation signal of individual DER Phase Locked Loop (PLL). This method offers adequate load current sharing under steady state and transients but requires high bandwidth communication medium [99] - [100]. Also, the difficulty in expanding centralised control reduces the system redundancy.

3. Distributed Control

   In this method, the central controller is not required, but an individual controller is used in each DER. A common current sharing bus is necessary to provide the average current reference for an individual DER. Sophisticated load power sharing and voltage regulation can be achieved in this method, but the need for interconnection between DERs result in reduced flexibility and redundancy [99], [101].

1.2.2 Droop Based Control Techniques

In the standalone operating mode, decentralised droop control methods that offer voltage and frequency regulation without complex and costlier communication systems are widely adopted [26] - [29]. Droop methods possess improved redundancy, reliability needs of supervisory control and plug and play feature. However, it has few drawbacks namely, deviations in frequency and voltage, dependency on output and line impedance and poor power quality. Voltage and frequency regulation at the PCC can be achieved by conventional droop methods as described below.

1. Conventional Droop Control

   Conventional droop control is derived from the basic concept of synchronous generators, where the real power is increased by drooping the frequency. This method is mimicked in DERs based on the assumption of highly inductive lines where the frequency and voltage are regulated by drooping real and reactive power respectively [26] - [28]. But frequency droop control has a pitfall of large frequency deviation and therefore additional control loops are needed for frequency regulation. Also, the choice of droop coefficients has an impact on frequency limits.

2. Angle Droop Control

   Angle droop is found to be a promising concept which overcomes the aforementioned limitation of conventional frequency droop by utilizing the angle of network voltage to share the real power distribution among DGs, especially when they are converter interfaced [29]. It has been demonstrated in [29] - [31] that conventional angle droop method has almost no frequency deviation, which is not true for frequency droop control. However, it has the drawback of load sharing is dependent on the output and feeder impedances. In general, in the angle droop control method, the voltage across the filter

capacitor is taken as the reference DG voltage by neglecting the effect of grid side inductor or by considering only LC output filter structure [30]. In this, it is highly unlikely that lower droop coefficients can allow adequately accurate sharing of the load demand. It has been shown in [31] that higher droop gains can improve the load active power sharing among DERs, albeit at the cost of system stability. To enhance stability with high droop gains, a supplementary controller has been used in [31]. Furthermore, the above methods described do not mention reactive and harmonic sharing among the DGs. The angle based control may necessitate GPS synchronization of the DERs [102] - [104] in addition to the inaccurate real and reactive power sharing.

3. VPD/FQB Droop Control

   Conventional droop methods are based on the assumption of the dominant inductive behaviour of feeder lines. In low voltage line with dominant resistive lines, conventional droop control is reversed [26], [33] - [34]. In such cases, the voltage magnitude and frequency are regulated by drooping the real and reactive power respectively.

1.2.3 Advanced Droop Methods

1. Methods to Incorporate the Output Impedance Effect in Highly Inductive Lines

   In conventional droop methods, power sharing among common loads is also affected by the unbalance by the sum of the output and line inductances. Controlled power electronic converters play a crucial role in maintaining the individual DER power quality. The output filter is connected to each VSI to attenuate the switching frequency harmonics produced by high frequency switching of power semiconductor devices. Grid side impedance

of an LCL filter is usually considered as the output impedance of DER in islanded MGs, where the output voltage is assumed to be impressed across the filter capacitor. Several innovative control studies were performed by including the effect of output impedance in droop control design to nullify the degradation in power sharing amongst DERs. One such concept is to add a virtual impedance to modify the output impedance so that the reactive, as well as harmonic power, can be shared in addition to the real power [108] - [111]. This is crucial as more and more nonlinear loads are proliferating into electric grids. Moreover, the accuracy in load power sharing depends on the selection of virtual impedance values and its optimization under different grid conditions. In [35], a robust droop control was proposed to mitigate the numerical calculation or computation delay in dominant resistive feeder lines, but the response and delay effects are not significant in highly inductive lines. Therefore, further studies are necessary for droop control methods for dominant inductive MGs to effectively achieve the active and imaginary power distribution among DERs.

2. Droop Methods for Strong Coupled Feeder Lines

   In the medium and few low voltage MGs, line inductance values are comparatively small with cable resistive behaviour and normally possess unity or low X/R ratio. Due to strong coupling between real and imaginary power, load sharing cannot be accurately achieved with conventional voltage and angle droop method. As decoupling between active and reactive load power cannot be possible in this scenario, a transformation matrix can be utilized to modify droop equations to incorporate coupling effects as discussed in [32]. Although the percentage deviation in real power sharing is improved to 9%, the intercommunication needs between converters remain as a shortfall. In addition, it does not mention any unbalances in the load, which are more common in rural areas. [37], [101] mentioned virtual frame transformation

method which can decouple real and imaginary power and provide better system stability, but the difficulty in finding accurate transformation angle for DGs with different ratings or line impedances cause lack of synchronism between them.

Quality of the power delivered to loads is another main concern in islanded grids since most of the loads are unbalanced where load at different phases may differ frequently. In addition, the loads can also be non-linear due to the presence of power electronic components. In parallel DC converters and Uninterruptable Power Supply (UPS) applications, a virtual impedance concept, along with conventional frequency droop methods is commonly used for sharing both linear and non-linear loads [110] - [111]. The same concept is adopted in parallel connected AC converter interfaced systems, in which the decoupling between active and reactive power is achieved by subtracting a proportional term of DG output current from the reference voltage, thus making it possible to share real and harmonic power [112] - [116]. Authors in [114] - [115] proposed additional control algorithm with conventional frequency droop method to share harmonic power between DGs, by utilizing the concept of virtual resistive or inductive terms in voltage reference calculation.

1.3 Reactive Power Management in Converter Dominated Microgrids

In islanded MGs, reactive power plays a crucial role in determining power system voltage stability. Usually, the reactive load demand is distributed among the DERs by drooping the voltage magnitude. But drop in voltage magnitude below a specified limit has negative impacts on the system, viz. equipment malfunctions and damage. In grid connected mode, the utility can provide support to an MG, but in

islanded mode, MG has the sole responsibility for maintaining the PCC voltage and power quality within permissible limits. In synchronous generator dominated MGs, it can maintain the voltage within limits and supply enough reactive power due to its inertial characteristics. In converter interfaced DERs, integrating suitably sized battery energy storage systems can also supply the required VAR and maintain the voltage within limits. The integration of RESs (Solar, Wind) into Australian power grid is increasing rapidly due to the demand of natural sources for electricity [116] - [119]. A case study in South Australia reveals that increased penetration of PV systems in household applications not only created power quality issues in neighbourhood customers but also reduced the efficiency of PV panels [120]. This is because the power electronic converters in the renewables and other nonlinear loads feed harmonics into the grid.

In islanded MGs with dominant converter interfaced renewable resources, the reactive power requirement of common loads are satisfied by drooping the voltage magnitude. PCC voltage magnitude should be kept within limits, otherwise will affect the voltage stability of the system. In such cases, where the controllable loads require more reactive power than the connected DERs can supply, capacitor banks or any static compensating devices should be installed to meet the excessive reactive power requirement of the common load. A low power rated DSTATCOM is a promising device in such scenarios, where it can satisfy the excessive reactive power demand of load as well as mitigate the harmonics caused by the loads in a system and other voltage unbalance issues in utility connected systems [40] - [43]. VSI is the heart of DSTATCOM and its harmonic performance gain varies upon different switching modulation methods. Certain PWMs can effectively reduce the unnecessary distortions in PCC voltage and effectively utilize the DC link voltage. There is a need for an efficient pulse width modulation scheme for closed loop operation of DSTATCOM such that it can operate in a constant and reduced switching frequency with reduced switching losses and lesser harmonic distortion.

1.4 Power Quality Issues in Parallel Connected DERs

In terms of IEEE Standard 1159 - 1995 [121], The term power quality refers to a wide variety of electromagnetic phenomena that characterize the voltage and current at a given time and at a given location on the power system.

The various electromagnetic phenomena have been defined in [121], in which Section 4.4.5 of the report classifies the primary waveform distortions as DC offset, harmonics, inter-harmonics, notching, and noise. Power quality requirements are very stringent in grid connected system around the world. In grid connected systems, the parallel connection of voltage source converters is adopted to incorporate with the power handling capability of the power semiconductor devices and output filter requirements. Moreover, converters can be switched ON /OFF according to the load demand. Voltage Source Converters (VSC) can operate in current controlled mode or voltage controlled mode. Normally an LC filter is utilized in voltage controlled converters, whereas LCL filter can eliminate switching harmonics in current controlled converters. These filters can induce series or parallel resonances in the system [122] - [123]. Harmonic mitigation in grid connected or islanded grids are possible by means of passive or active or hybrid filters at PCC as shown in Figure 1.4. Passive filters consist of tuned single or multiple arms LC filter, whereas active filters are power electronic converter based compensating devices like DSTATCOM. In hybrid filters, the most dominant harmonic is compensated by the passive filter and other harmonics are mitigated by active filter.

Furthermore, the harmonics can be aggravated when interfacing more number of VSC based RESs into the grid [44] - [46]. The filter capacitors are the main source of harmonic propagation into the main grid as well as between the neighboring loads. The cable inductance along with the shunt capacitors can also act as a source for harmonic resonance [124] - [126]. As most of the power electronic converters are switched at a frequency range between 2 - 150 kHz, the sizing of

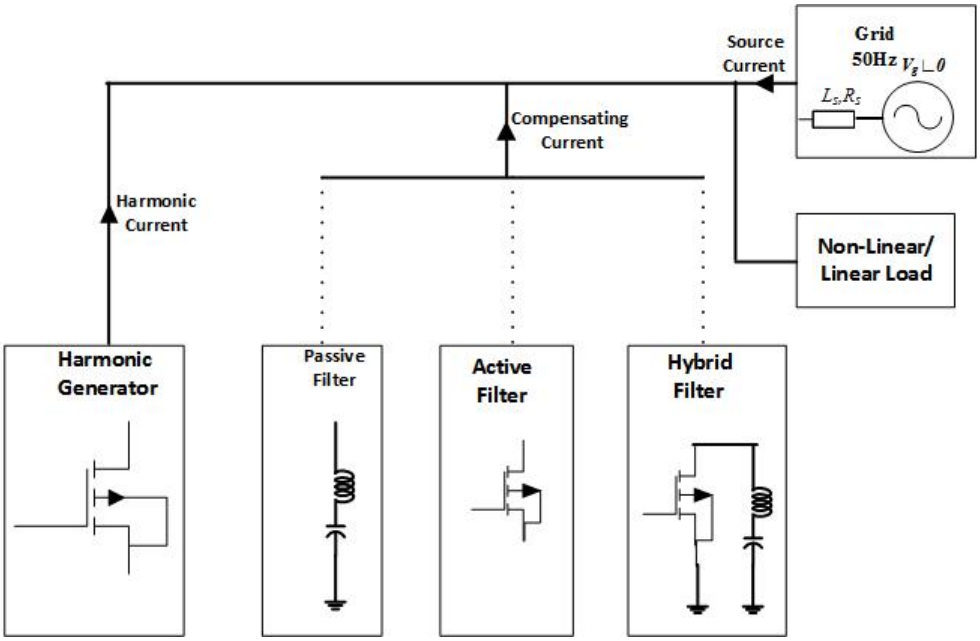

Figure 1.4: Harmonic elimination in grid connected systems by different filtering methods

filter capacitors and their high frequency harmonic issues are the recent area of interest [9] - [12].

With the recent developments in high frequency switching devices like SiC MOSFETs and JFETs, converters can operate at higher switching frequency with reduced switching losses, which will drastically reduce the size of output filters. Since output capacitors can cause resonance with cable inductances, the reduction in capacitor value will reduce the harmonic oscillations due to the output capacitor. Harmonic interaction and resonance effects in high frequency converters will fall in the range of 2 - 150 kHz, due to the reduction in filter size at high frequency. IEC 61000 and AZ/NZS standards restrict the harmonic limits to 40^{th} harmonic ($<$ 0.3 %) and IEEE recently introduced harmonic standards up to 50^{th} and it highly recommends to reduce the higher order ($>$ 50) harmonics to a minimum [15].

Increased penetration of grid connected converters in high frequency range can introduce harmonic and EMC issues and further degrades the network power

quality. Thus LCL filters have to be carefully designed so as to limit the harmonic emissions in high frequency region. However, the harmonics regulations in the frequency range 2 - 150 kHz are still under development stage [38]. The harmonic study in the high frequency range is very important as it introduces high frequency distortions and can interfere with power line communications [9]-[12]. The poor knowledge of distortions in high frequency region can even cause equipment damage or Electro-Magnetic Interference (EMI) issues or extra filter requirements. In parallel connected systems, the harmonic interaction between converters or controller interaction due to circulating currents can develop sustained oscillations in the system. Many studies are conducted to study the harmonic effects in parallel connected grid converters [9] - [11], [124] - [126]. In [44], the harmonic interaction in multiple current controlled and voltage controlled converters are modelled to show the effect of dynamic interaction between the controllers. Direct and quadrature axis based decoupled control is most commonly adopted in current controlled grid converters, whereas in [45], PR controller is utilized for eliminating circulating currents. Small signal modelling was carried out to analyse the stability issues in parallel connected standalone inverters [46], [122] and droop control based frequency and voltage control is utilized in [195] to obtain stable operation of distributed energy resources in microgrid. These studies are carried out at converters switching at few kHz frequencies. The stability issues caused by circulating currents due to the interaction of controllers in parallel converters are still present at high frequency operation. This characteristic needs further investigation and proper control methods are necessary to maintain the grid stability.

1.5 Interconnection of AC Microgrids

Increasing number of renewable energy resources such as PV, wind and microhydro are leading to a substantial amount of electric energy generation in the form of DGs within the electric networks. Integration of the DGs will benefit the electric networks by reducing the network upgrade costs, minimizing the power losses in long feeders and increasing the reliability of the network. They may also be helpful to achieve faster recovery following a fault in the network.

As per case studies in the US, wind turbine mostly produces power during the night and power production can drop rapidly [1] - [2]. The uncertainty of these renewable sources necessitates the use of either the storage devices or extra generators. For example, consider interconnected systems where an MG is dominated by solar converters and energy storage devices, while another MG is mostly equipped with converter fed wind energy conversion systems. During a sunny, but a low windy day, the power surplus in the first MG can supply power to the other MG in order to fulfill its local load requirements and thereby compensating the diurnal rhythm of wind systems. These intermittent effects can be partially overcome by incorporating energy storage devices or fuel cells to wind and solar energy systems [8], [49].

In existing macrogrids, network upgrade and the need for long distance transmission lines or poles are not cost-effective approach. MGs are considered as a feasible solution to power future grids, rather than existing macrogrids, where a cluster of DERs together with distributed storage devices can power remote communities. The contingent power shortfall under maintenance or fault conditions can adversely affect the local loads connected to the MGs and negatively impact the stability of the integrated system. The reliability of MG can be improved by interconnecting MGs which are under a smaller geographical area. Different MGs possess dissimilar competences reliant on individual DERs, DS, and local

load. The histrionic reduction in costs of renewable technologies has considerably increased the penetration of converter fed distributed energy resources to existing grids [1] - [2]. Although the DERs - wind and solar power generation strongly depend on the weather conditions, the interconnection of neighbouring MGs will reduce the curtailment of generation from these renewables in addition to the unexpected load shedding during contingencies. Furthermore, integrating DS to these micro sources will enhance the stability of its power output. In [49], a frequency regulation reserve based approach is proposed to investigate the participation of volatile renewable energy resources from multiple MGs. IEEE Std. 1547.4 considered MG as an element for constructing active distribution systems and recommends interconnecting MGs as a viable option to increase the resiliency and reliability [47].

Interconnecting MGs paves the way to smarter grids where power shortfall in one MG can be compensated by the excess power available from other interconnected MGs. Different methods are proposed to achieve the power trading among multiple MGs in recent literature [125] - [129]. In [125], a cooperative power dispatching algorithm is proposed to optimize the load demand management in interconnected MGs. In [127], Nash bargaining solution based power management framework is proposed to achieve optimized power distribution between different MGs. In [128], the authors utilized the game model theory is to effectively trade the power distribution among several MGs, whereas David et al proposed a distributed optimization strategy to minimize the global operational cost in the multi-MG system [128]. Model predictive control based algorithm is utilized in [129] to improve the resiliency of multi-MGs. Future smart grids can be formed by clustering neighboring autonomous MGs, in which the concept of Power Exchange Highway (PEH) [48] can be employed for the effective power transfer between MGs. In [130] - [131], an AC PEH with back to back converter topology is proposed as a suitable method to interconnect MGs for better power transfer between AC MGs.

But, the back to back converter topology is not cost-effective due to additional converter hardware and associated devices. This necessitates further investigation of new configurations to interconnect AC MGs.

1.6 Objectives of the Thesis and Specific Contributions

1.6.1 Objectives of the Thesis

Based on the gaps found in literature, the key objectives of the thesis are presented as follows.

- To introduce a suitable pulse width modulation scheme for voltage controlled grid converters to facilitate the effective DC link utilization and reduce switching frequency of operation.
- To design the output filtering requirements in current controlled AFEs and to analyse and mitigate the stability issues in converter side or grid side current regulated current controlled converters.
- To analyse the harmonic issues and filter requirements in wide bandgap SiC MOSFET based high frequency grid converters.
- To achieve an accurate real and reactive power sharing in high voltage islanded MGs with inductive feeder lines by eliminating the effect of output inductance in conventional angle droop control method.
- To eliminate the coupling effects in strong coupled remote MGs with the ratio X/R = 1, and thus facilitate the effective active and imaginary power sharing.
- To effectively meet the load demand in resistive MGs by introducing a virtual impedance concept with inverse angle droop control.

- To accomplish a co-ordinated control for DERs and DSTATCOM in order to effectively distribute the reactive power demand in autonomous MGs by keeping the voltage drop within 5 %.
- To eliminate the controller interaction among parallel connected high frequency grid converters by developing advanced control algorithms.
- To interconnect a cluster of converter dominated AC MGs to facilitate an efficient and resilient future power system.

1.6.2 Specific Contributions of the Thesis

The main contributions of this thesis are listed as follows.

- Proposing a closed loop space vector modulation scheme for voltage controlled grid connected converters that offer the advantage of better DC link voltage utilization and reduces the switching frequency. In this, the output filter dynamics are incorporated in a DLQR based state feedback voltage control.
- A new approach to design the filter dynamics of output LCL filter is introduced for current controlled grid connected converters. The stability issues and damping requirements are analysed using control system design and simulation studies. Based on the stability studies, an advanced control algorithm is proposed for converter current regulated LCL filter fed grid connected converters, which can eliminate the stability issues as well as hardware delay effects. The developed control algorithm is validated with simulation as well as experimental tests.
- Filter requirements and stability implications of SiC MOSFET based high frequency grid converters are investigated with the help of transfer function

analysis and simulation studies. The obtained findings are validated using the SiC semiconductor analytical model in LTspice. In addition, an experimental prototype of single phase converter is constructed with two CREE SiC device based experimental half bridge kit and the results are validated under practical operating conditions.

- An advanced droop controlled strategy for highly inductive feeder line fed AC MGs is proposed to achieve effective real and reactive load demand distribution among DERs. Therefore, the effect of output impedance is eliminated and successfully achieved the system stability with lower droop gains.

- A decoupled droop control strategy for strong coupled AC MGs is proposed to obtain an accurate real and imaginary power sharing between converter dominated DERs in remote communities.

- An inverse angle droop control with virtual impedance concept is proposed for resistive MGs to meet the load demand successfully.

- Controller and harmonic interaction in parallel connected high frequency VSC fed grid connected DERs are studied and a scheme is proposed to mitigate the controller interaction among parallel connected grid converters.

- Proposed a control strategy for DSTATCOM to support the DERs to effectively meet the reactive power demand in islanded MGs, in addition to the harmonic mitigation capability. Furthermore, the reactive power management help to maintain the voltage drop in MGs within acceptable limits.

- A DC Power Exchange Highway (DCPEH) is introduced to interconnect a cluster of AC MGs, which facilitates an efficient and resilient energy system. An advanced control algorithm is developed to manage the power flow between DCPEH and MGs.

1.7 Thesis Organisation

The thesis has been organized into 8 chapters. In this chapter, a literature review is presented to find out the specific needs in future power systems, which sets the motivations to carry out this research.

It is evident from the literature that, grid connected converter can be operated in voltage control mode or current control mode. Chapter 2 describes voltage control of grid connected converters. Furthermore, this Chapter proposes a closed loop SVPWM based voltage control for grid connected converters such that the DC link voltage can be effectively utilized.

In Chapter 3, the current controlled grid connected converter, its output filter requirements and stability implications are discussed. An accurate design of output LCL filter and its stability issues with closed loop control are explained with the help of design and control system analysis. This area is of importance due to the increased penetration of power electronic converter interfaced DERs and loads to existing grids and stringent power quality requirements. A study on the converter and grid current regulated AFE is conducted to analyze the stability and damping requirements of grid converters. Moreover, a new Proportional Resonant Feedback (PRF) controller is proposed to overcome the stability issues in converter current regulated AFEs, which also overcomes the impact of hardware delays. The emergence of high switching frequency devices necessitates the power quality and harmonic studies in the high frequency region. Chapter 3 also analyzes the impact of high frequency operation in AFEs power hardware as well as stability effects on its control implementation.

Once the individual converter control and stability issues are identified and mitigated, it is essential to study the parallel operation of these converter interfaced DERs. In high voltage islanded MGs, the effect of output filter inductance

(LCL Type) on angle droop control has been overcome by setting high droop gain, but it adversely affects the overall system stability. In Chapter 4, an advanced control strategy is discussed to eliminate the effect of output filter inductance on angle droop control and thereby achieving the accurate real and reactive power sharing among parallel connected converter interfaced with highly inductive lines. It is shown that, by modifying the individual converter control, the reactive power demand is also properly shared among DERs and thus meets the power quality requirements in converter dominated DER based MGs.

In high voltage lines, sharing real and reactive load power demands can be achieved by conventional droop control methods. Nevertheless strong coupling between active and reactive power in medium voltage lines with low X/R ratio degrades rating based load sharing among converters. Chapter 5 proposes a new droop control method to effectively achieve the decoupling of real and imaginary components of load power and thus share the active and reactive power requirements of common load among converter interfaced DERs. The power decoupling factor introduced in this method along with angle droop concept has the added advantage of reactive and harmonic power sharing with surplus accuracy in active power distribution. Moreover, this chapter proposes a new control strategy for accurate load power sharing in resistive MGs, by incorporating the virtual impedance concept along with inverse angle droop method.

Chapter 6 discuss the harmonic interaction and power quality issues in parallel connected converters operating either in autonomous or grid connected mode. In the autonomous mode, the reactive power distribution among DERs is achieved by voltage droop. The voltage magnitude cannot be dropped below a certain value as it affects the system stability. A low rated DSTATCOM can provide reactive power support to DERs in such cases in addition to the harmonic mitigation capability. In this chapter, a new control strategy is proposed to achieve the coordinated sharing of reactive power demand among DSTATCOM and DERs.

In grid connected operation of parallel converters, harmonic interaction due to the circulating currents among DERs is an important concern and it may affect the overall system stability. But the harmonic interaction effects are less pronounced in high frequency switched SiC semiconductor based converters as the output filter requirements are much reduced at high frequencies. Still, the controller interaction between parallel converters needs further investigation and mitigation strategies. This chapter also discusses the controller interaction among parallel connected DERs and introduces a new scheme to mitigate the controller associated stability issues in parallel connected grid converters.

Chapter 7 introduces a DC power exchange highway concept to interconnect converter dominated AC microgrid clusters in a small geographical area to enhance a resilient future energy system. A power flow controller is introduced to manage the power flow between DCPEH and individual MGs based on the surplus power, local load demand, and power shortfall. A dynamic droop control strategy is utilized in DCPEH to effectively distribute the excessive power from MGs to other MGs with power shortfall.

The general conclusions drawn from this research and the scope for future research are given in Chapter 8.

Chapter 2

Voltage Controlled Grid Connected Converters - Closed Loop SVPWM

Power electronic converters are treated as the building blocks of today's electric power conversion systems. Three-phase, two-level voltage source converters are widely accepted topology in industrial applications. However, these converters introduce power quality issues due to the high frequency switching of the power semiconductor switches. Although an output filter interfaced with this converters can eliminate the high frequency switching harmonics, these filters can cause phase shifts while operating in current control mode. As outlined in Chapter 1, the voltage controlled mode is most suitable for the closed loop operation of VSC with LC type filters. SVPWM has proved its benefits in current controlled VSCs, whereas in voltage controlled VSCs SPWM is commonly adopted due to its simplicity. In this chapter, the effect of PWM techniques in voltage controlled grid connected converter is discussed and a closed loop SVPWM technique is proposed for LC filter fed DLQR based voltage controlled converters. AFEs can either operate as a grid feeding converter or grid forming converter and inner loop voltage or current control is similar in all modes of operation. Thus the closed loop SVPWM based voltage control is also applicable to DSTATCOMs. The material in this chapter is

organised in two sections. First, a brief review of open loop SVPWM is undertaken to provide the necessary background information for CLSVPWM implementaion. Following section, a closed loop SVPWM is introduced in DQLR based voltage control algorithm for an LC filter fed AFE. As this technique incorporate the output filter characteristics, it eliminates the phase shift introduced by output filter in grid converters. Most of the materials discussed in this chapter are taken from our published papers [130, 131].

2.1 Operation of Voltage Controlled Converters

2.1.1 Open Loop SVPWM

The classic asynchronous method, SPWM which compares the three phase regularly sampled sinusoidal reference with a triangular carrier to generate the switching instants is commonly adopted in voltage controlled converters due to its simplicity. But the DC link voltage is not fully utilized in SPWM. As discussed in Chapter 1, SVPWM possesses significant advantages over other asynchronous PWMs and its switching pulse location identification can be exploited to attain better harmonic elimination [86]. In SVPWM, the reference voltage is generated in every switching cycle using different switching states. It is based on the concept that a 120° displaced three phase sinusoidal waveform can be obtained by rotating a constant magnitude voltage space vector at a constant speed. A typical voltage space vector is represented in (2.1).

$$V\angle\theta = (ae^{j\theta} + be^{j(\theta-\frac{2\pi}{3})} + ce^{j(\theta-\frac{4\pi}{3})})V_{dc} \tag{2.1}$$

where $V\angle\theta$ is the arbitrary output voltage vector and V_{dc} is the DC link voltage. SVPWM is used to produce the appropriate values of a, b and c in order to generate the reference voltage at a desired angle. Figure 2.1 shows the representation of

three phase two level voltage source converter and it's orthogonal co-ordinates. The reference voltage is generated by two adjacent active vectors (V1-V6) at the boundary and two zero vectors (V0 (000), V7 (111)) located at the origin of the hexagon as shown in Figure 2.1. When a reference voltage vector rotates through each sector, the switches S_1-S_6 will be turned ON/OFF, to generate the three phase balanced sinusoidal waveform. SVPWM implementation incorporates, the iden-

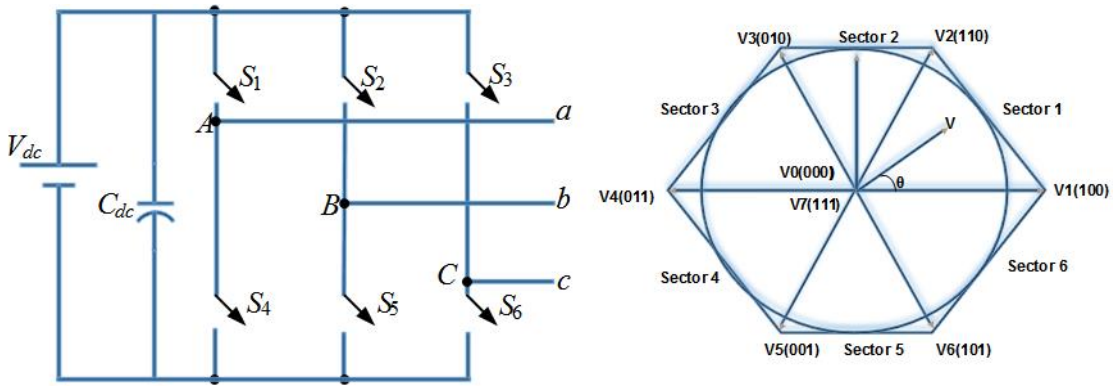

Figure 2.1: Three phase VSC and orthogonal co-ordinate representation

tification, definition, and sequencing of switching vectors as illustrated in Figure 2.2.

Initially, the magnitude and angle of reference voltage space vector $V\angle\theta$ have to be determined from the three phase modulation signal. Three phase quantities have been transferred to stationary two phase quantities using the Clarke transformation. Thereafter, the sector in which the voltage reference vector lies is defined. Next step is the determination of the switching time for active and zero vector. Each Triangular sector is formed by two active state vectors of amplitude $\frac{4}{3}V_{dc}$ as shown in Figure 2.3. After determining the sector, the reference space vector V can be mapped into two adjacent vectors V_x and V_{x+1}. The switching instants of each sector can find out in terms of these adjacent active vectors and zero vectors, where T_a and T_b denote the time duration for active vector V_x, V_{x+1} and T_0 is the

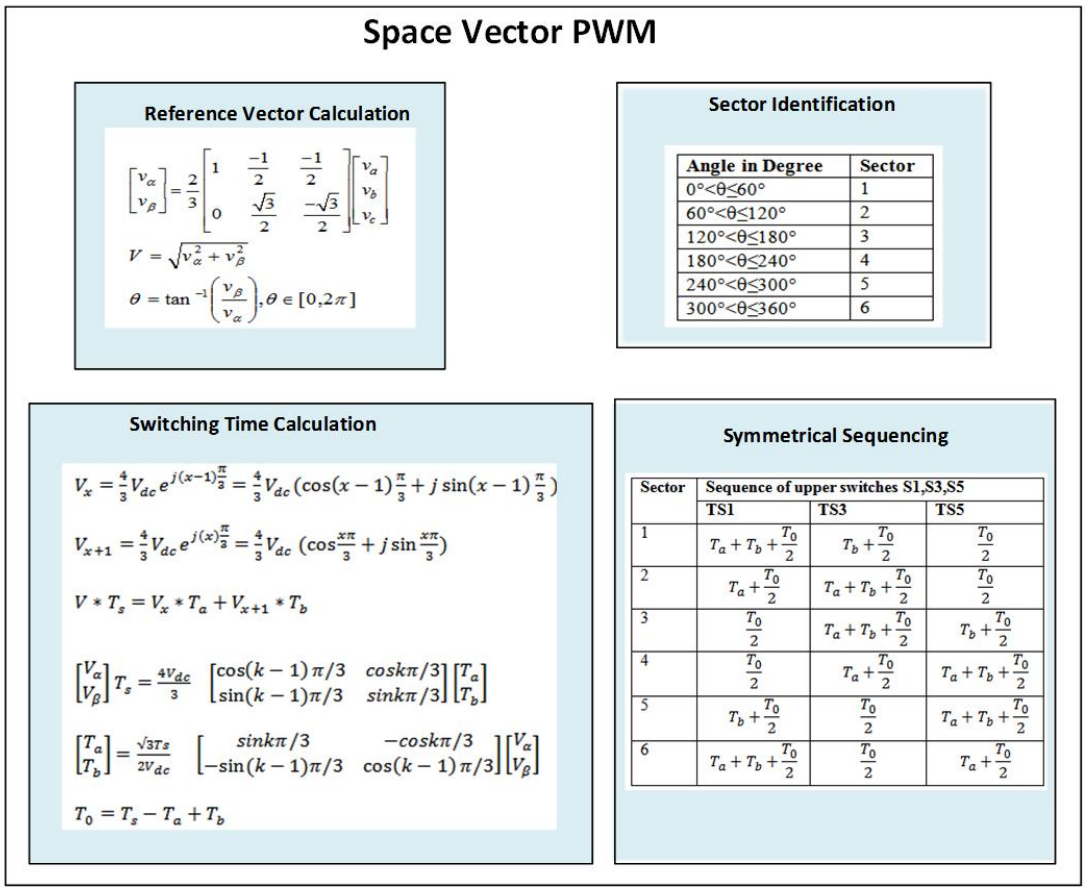

Figure 2.2: SVPWM implementation

switching time for zero vector states. T_s is chosen as half of the switching period.

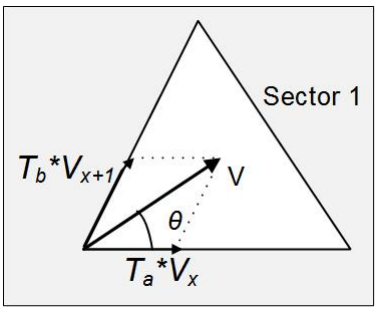

Figure 2.3: Triangular sector for sector 1

$$V = V_x \frac{T_a}{T_s} + V_{x+1} \frac{T_b}{T_s} + V0 \frac{T_0}{T_s} \tag{2.2}$$

The switching time for two active vectors can be obtained from the derivation shown in Figure 2.3 as

$$\begin{bmatrix} T_a \\ \\ T_b \end{bmatrix} = \frac{\sqrt{3} T_s}{2 V_{dc}} \begin{bmatrix} sin(k\frac{\pi}{3} - \theta) \\ \\ sin(\theta - (k-1)\frac{\pi}{3}) \end{bmatrix} = \frac{T_s}{V_o} \begin{bmatrix} sin(k\frac{\pi}{3} - \theta) \\ \\ sin(\theta - (k-1)\frac{\pi}{3}) \end{bmatrix} \tag{2.3}$$

$$T_0 = T_s - (T_a + T_b)$$

where k is the sector in which the reference vector falls and θ is the angle in rad. It is clear from (2.3) that the maximum possible magnitude of output voltage $V_o = \frac{2}{\sqrt{3}} V_{dc}$, which permits the modulation index to increase 15 % over the regularly sampled conventional SPWM.

Symmetrical switching pattern is chosen to reduce the switching losses. The zero vector $V7(111)$ is placed at the center of switching period and $V0(000)$ is at the start and end of switching period. Thus the zero vectors are symmetrically distributed in each switching period. The switching pattern for three phases in each sector is shown in Figure 2.4. Once identified the switching vectors, these signals are scaled in terms of the sampling period and the control voltage signals for phase a, b and c can be modeled as the summation of these active and zero vectors over a switching period. The generated control signals are then compared with a triangular carrier signal of frequency same as switching frequency to generate the pulses for the upper and lower switches of phases a, b, c. The shape of the control signal is same as adding a third harmonic signal to the sinusoidal voltage waveform.

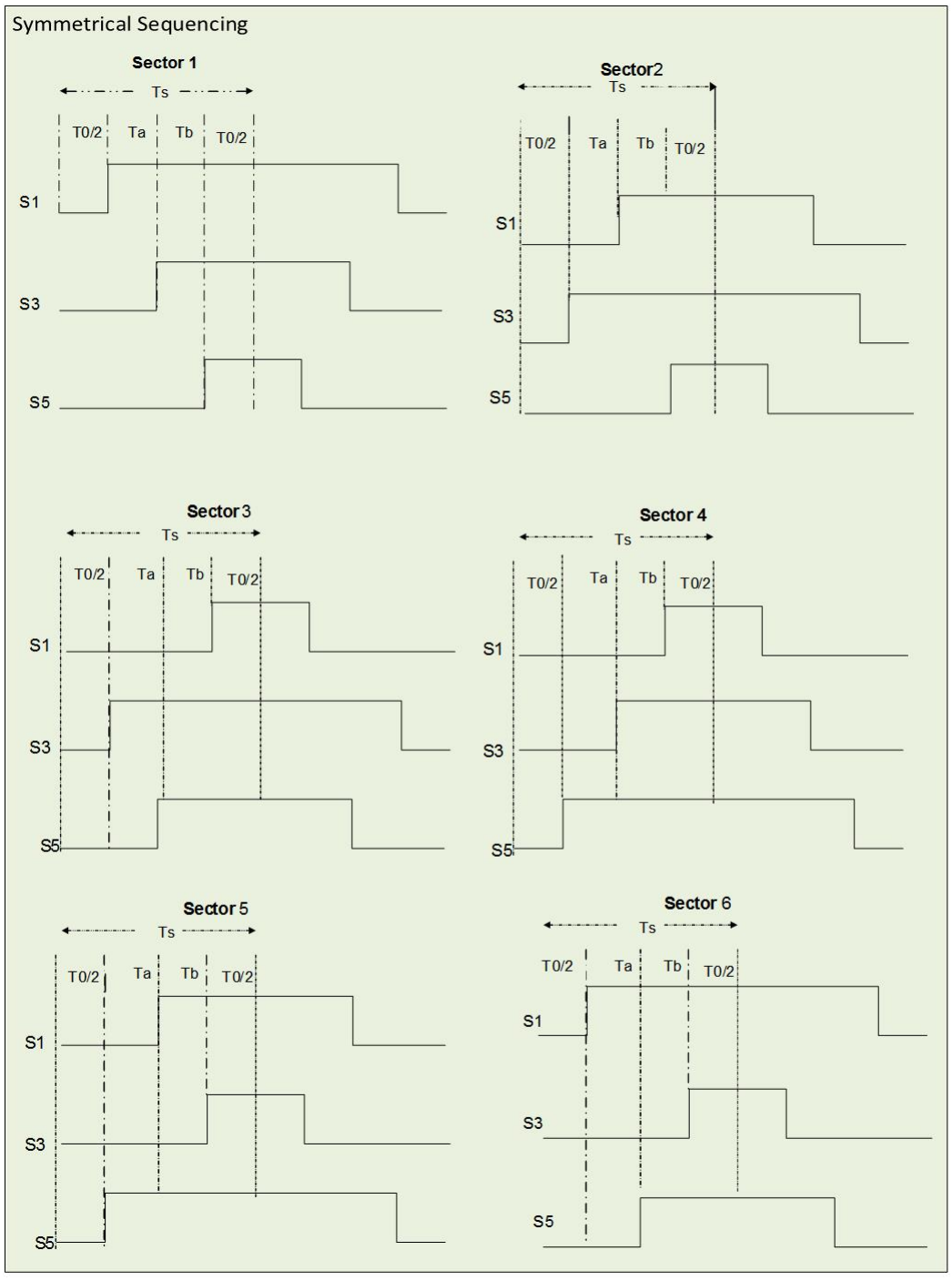

Figure 2.4: Sequencing of switching vectors in different sectors

2.1.2 Closed Loop SVPWM

In current controlled converters with open loop SVPWM, the filter parameters are not included in the system modelling and the controller design. In such cases, the output passive filters can introduce a phase shift. In traditionally used d-q axis current control, a PI regulator can control this phase shift to a minimum value. However, the complete elimination of this error is impossible. A DLQR based voltage controlled converter with closed loop control with SVPWM is introduced in this section, where the controller is designed by considering the filter characteristics. Thus, it eliminates the possibility of any phase alteration. In addition, the clear identification of switching vector location will help to achieve better harmonic performance [86], [88].

An equivalent circuit of a VSC connected to the grid through a feeder is depicted in Figure 2.5. In this, uV_{dc} is the converter voltage, L_s and R_s respectively are the grid inductance and resistance, L_1, R_1 are the feeder inductance and resistance of the converter and L_f, C_f constitutes the filter. Assuming the feeder is highly inductive, average real power can be defined as

$$P = \frac{V_p V_t}{X} sin(\delta_p - \delta_t) \tag{2.4}$$

where $V_t \angle \delta_t$ is the voltage at PCC and X is the equivalent impedance. Assuming the angle difference is small, the power is proportional to the angle $\delta_p - \delta_t$. Normally grid voltage V_g is considered as $V_g \angle 0$. Considering the negligible drop across the feeder impedance, the magnitude of the voltage at filter capacitor is assumed as network voltage. Thus, active power feeding to the grid can be controlled by controlling the voltage angle.

Figure 2.6 represents the closed loop control diagram for the voltage controlled grid connected converter. The control law consists of two loops, outer active power

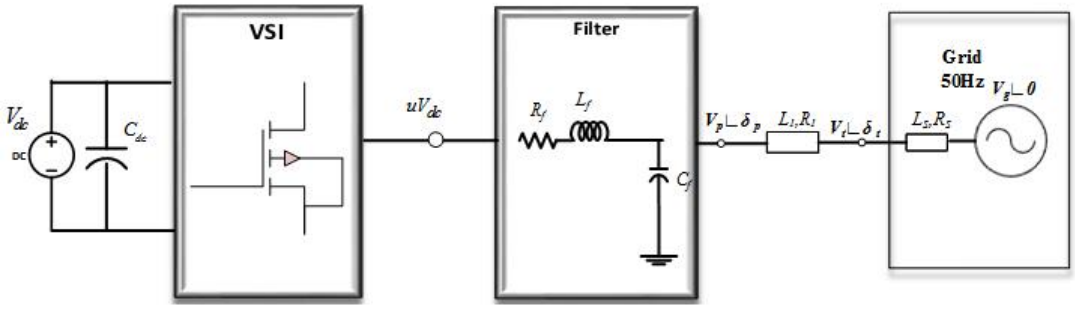

Figure 2.5: One line diagram of VSC connected to the grid through LC filter

control and inner state feedback control. The measured instantaneous power is passed through a low pass filter to obtain the average value, and it is compared with the reference power to be supplied to the grid. The error is then passed through a controller to generate the required voltage angle. The output of this converter gives angle δ, which is used to find the desired voltage reference in state feedback control. A PI or PID controller is used to track the actual power to the amount of power feeding to the grid.

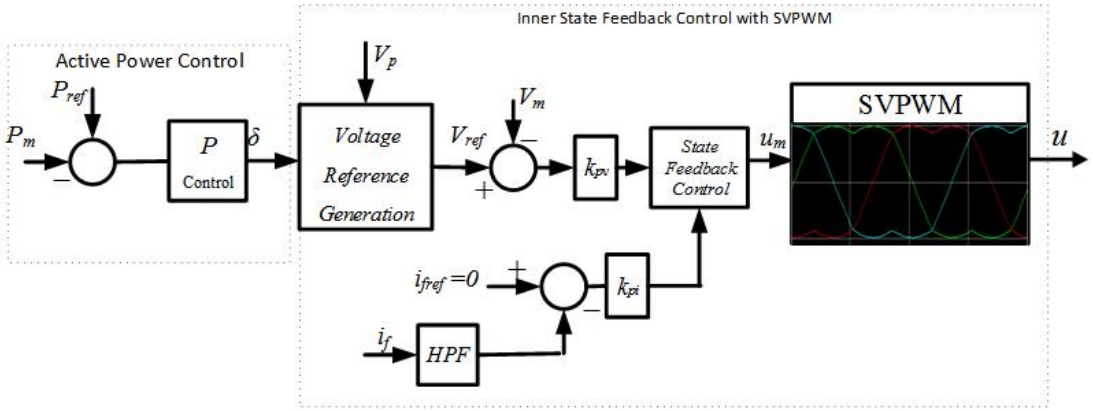

Figure 2.6: Closed loop SVPWM control for grid converter

The voltage source converter along with the output LC filter is connected to the grid as shown in Figure 2.7 (a). The corresponding one line diagram of the converter with output LC filter is illustrated in Figure 2.7 (b). The converter can be

bidirectional and can operate either in grid forming or grid feeding mode. L_f and C_f represent the filter inductor and capacitor respectively and they are designed to eliminate the switching frequency harmonics. R_f denotes the converter losses.

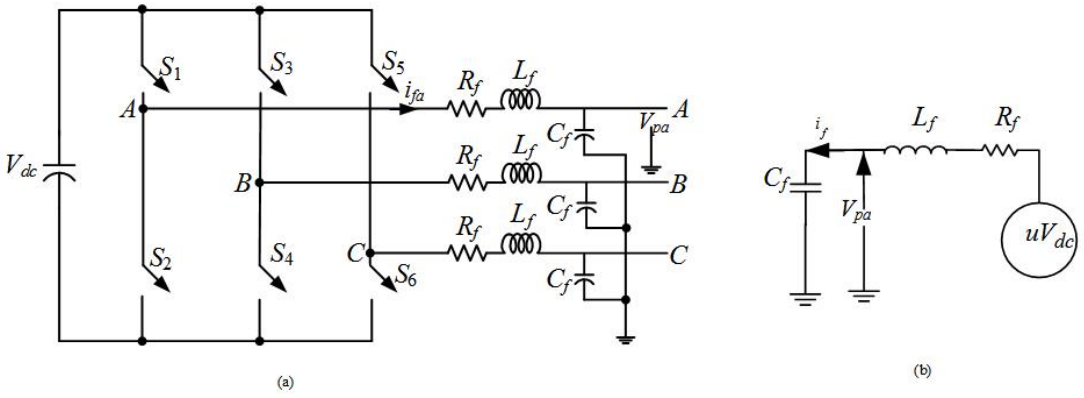

Figure 2.7: (a) Three phase VSC with output LC filter (b) per phase equivalent of the converter with an output filter

The three phase reference voltages at the PCC can be defined as,

$$\begin{aligned} v_{pa}* &= |V_p|sin(\omega t + \delta) \\ v_{pb}* &= |V_p|sin(\omega t + \delta - 120^\circ) \\ v_{pc}* &= |V_p|sin(\omega t + \delta + 120^\circ) \end{aligned} \tag{2.5}$$

where, $|V_p|$ is a pre-specified network voltage magnitude, δ is an angle that maintains the power flow from VSC to the grid and ω is the rated frequency.

State variables for a converter with output LC filter are

$$x_i = \begin{bmatrix} v_p \\ \\ i_f \end{bmatrix} u \tag{2.6}$$

where i_f is the current through filter inductor and v_p is the filter capacitor voltage. The state space equation is then given by

$$(\dot{x}_i) = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix} x_i + \begin{bmatrix} 0 \\ \frac{V_{dc}}{L_f} \end{bmatrix} \tag{2.7}$$

The output capacitor voltage v_p and the inductor current i_f are the states used in discrete linear quadratic regulator based state feedback proportional control as shown in Figure 2.6. As this technique accounts the filter characteristics, the effect of phase shift generated by the use of passive LC filters has been included in the control algorithm. Since it is hard to define the reference value of i_f, it is passed through a high pass filter (HPF) such that only the low frequency components of i_f are present. Assuming that, converter side inductor has the capability of eliminating the higher order harmonics, the filtered converter side current is then compared with zero. This concept also provides a damping effect to higher order dominant harmonics which ultimately results in much reduced total harmonic distortion. The references for v_p are chosen as given in (2.5). The state feedback control is then given as

$$u_c = k(x_{ref} - x) \tag{2.8}$$

where, feedback gain matrix is $k = [k_1\ k_2]$ and $x_{ref} - x$ is the error signal. The gains k_1 and k_2 are calculated using discrete time quadratic regulator [42]. The filter capacitor voltage reference v_p^* is compared with the measured value v_p and corresponding voltage and current errors are fed to a linear quadratic regulator based state feedback control. The resultant output of state feedback control is then utilized to obtain the modulating signal used for PWM generation. It should be noted that the state feedback controller output u is regularly sampled at a rate of

twice the switching frequency to obtain a discretised modulation signal. This step is not necessary for SVPWM as the algorithm finds the switching vectors in every switching period.

The current through converter side inductor and the voltage across filter capacitor are taken as the state variables. The obtained modulation voltage is then passed through symmetrical SVPWM block to generate the switching pulses for semiconductor devices.

As the harmonics generated by the converter rely upon the type of PWM scheme, a closed loop space vector modulation SVPWM [20] which can effectively utilise the DC link voltage is selected for converter switching pulse generation. The modulating signal generated by closed loop SVPWM is capable of utilizing 15% more DC link voltage compared with traditional sinusoidal PWM. Moreover, lower harmonic distortion due to the inherent addition of a third harmonic signal to sinusoidal waveform in SVPWM enhances its suitability to grid connected applications.

2.2 Simulation Study

In this example, the applicability of closed loop SVPWM in grid connected converter is tested. System parameters used for study is given in Table 2.1. Control algorithm described in Section 2.1.2 is used for the closed loop operation. Here, a PI controller is used to regulate the real power. The input and output signal from SVPWM block are shown in Figure 2.8, which clearly shows the carrier signals are fully utilized to generate the constant switching frequency switching signals for upper and lower switches in VSI.

Table 2.1: System under simulation study

Parameters	Details
Converter rating	1.12 MVA
PCC Voltage	11 kV (L-L)
Source Frequency	50 Hz
Converter Losses R_f	0.001 Ω
Filter Capacitor C_f	10 μF
Filter Inductor L_f	5 mH
DC Link Voltage V_{dc}	16 kV
Switching Frequency f_{sw}	15 kHz

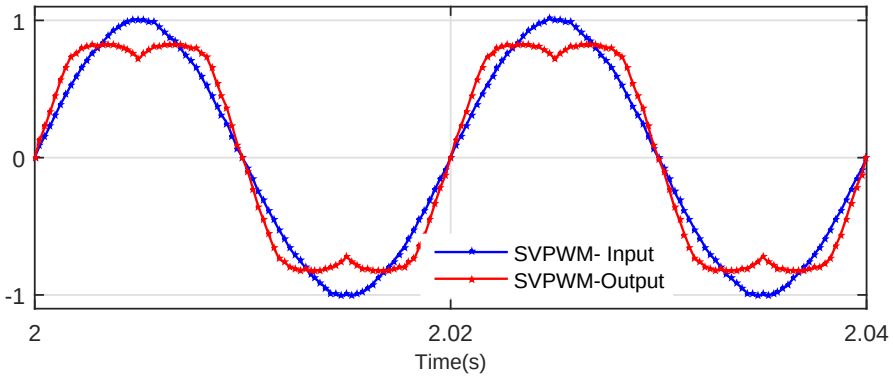

Figure 2.8: Closed loop control of grid converter

It is clear from Figure 2.9.a that, real power is following the reference value and feeding 1000 kW to the grid. At time, t = 0.7 s, the controller acquired steady state and the maximum overshoot and the steady state error are negligible. Inner loop voltage and current controller are operating well within the defined limit and corresponding phase - a converter voltage measured and reference waveforms are illustrated in Figure 2.9. The three phase grid side currents are depicted in Figure

2.10.

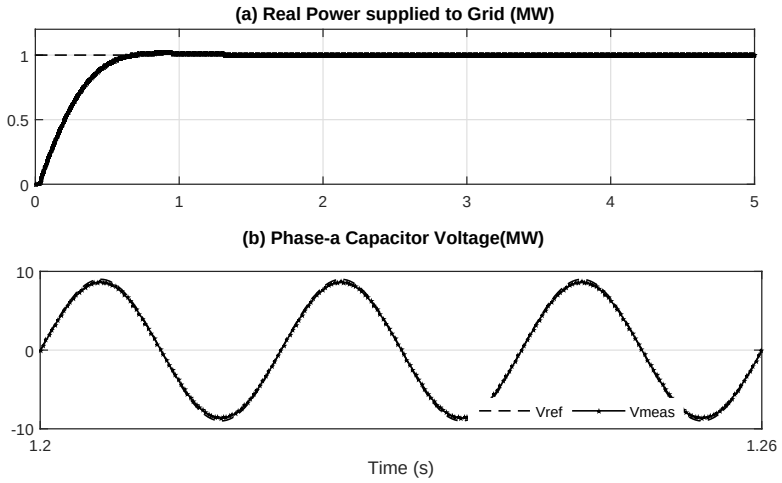

Figure 2.9: Closed loop control of grid converter

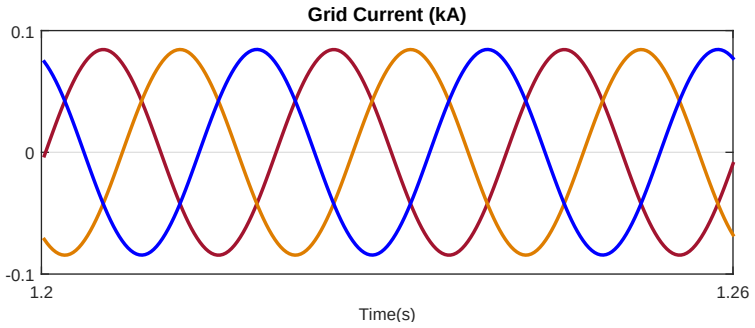

Figure 2.10: Three phase grid currents

2.3 Conclusion

This chapter investigates the role of pulse width modulation scheme in voltage controlled converter fed DERs. Initially, a closed loop SVPWM based voltage controller is proposed for an LC filter fed converter interfaced DER, which possesses attractive features such as, effective DC link voltage utilization, constant

and reduced switching frequency compared to traditionally used PWM schemes. Also, the phase shift due to the output filter is eliminated in this control. Since proposed control is based on state feedback DLQR, it is not sensitive to the parameter variations and other disturbances.

Chapter 3

Grid Connected Current Controlled Converters - Design and Stability Analysis

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In Chapter 2, the closed loop operation of the voltage controlled VSC has been discussed. These converters are usually equipped with LC type filters whereas LCL or L filters are commonly used in current controlled converters. The prime reason for this trend is the well-established nature of current control methods in industrial converters. In addition, the increased complexity of voltage control algorithm in LCL type filter and the lack of capacitor voltage control with simple L type make current control more dominant in industrial applications. As mentioned in Chapter 1, several factors will affect the stability of current controlled Active Front End (AFE) rectifiers. Even though the filter design and suitable damping techniques are well established from the early 2000s, it is still an ongoing area of interest for current researchers. The output filters should be designed such that it can eliminate the high frequency switching components from the converter output voltage, thereby preventing distortion in grid voltage or current. But the resonance phenomenon in certain regions of frequency may lead to system instability. This necessitates the study on accurate filter design and the factors which affect the filter performance such as switching frequency, PWM techniques, resonance region

selection, controller parameter design. The resonance behaviour and damping requirements are different in converter current regulated and grid current regulated systems. In this chapter, a detailed study of filter and controller design is conducted initially. Subsequently, the effect of filter parameters and controller parameters on system stability is investigated on the converter or grid current regulated systems. Since the delay factor can affect the inherent damping capability of converter current regulated systems, a new proportional resonant feedback controller is proposed for converter current regulated AFEs, which can successfully eliminate the adverse effects of system delay on stability. The basic considerations for adopting wide bandgap devices in grid connected converters have been discussed in Chapter 1. The development of wide bandgap SiC MOSFETs allows the high power converters to switch at high frequencies with lower switching and conduction losses in addition to the drastic reduction in output filter size. At high frequencies, the output filter requirements and its design have to be modified for exploiting the attractive features of wide bandgap devices. Furthermore, the stability and harmonic issues need to be analysed at high frequency regions of 2 - 150 kHz. Section 3.2 of this chapter deals with the operational needs and stability issues in high frequency grid connected converters [132]. The findings and conclusions from stability studies are validated by conducting a simulation in PSCAD/EMTDC. Also, an experimental platform of single phase converter is built with the SiC MOSFETs and diodes to understand the operational capabilities of SiC semiconductors at lower and higher switching frequencies. In addition, the findings achieved from theoretical and simulation studies are validated under practical scenarios.

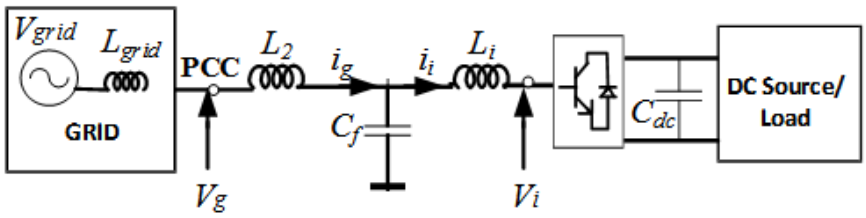


Figure 3.1: One line diagram of grid connected converter

3.1 Filter and Controller Design

Figure 3.1 shows the single line diagram of a grid connected AFE. A third order LCL filter is connected at the output of the converter to ensure the proper attenuation of switching harmonics produced by semiconductor switches.

3.1.1 Filter Design

The design procedure followed for finding LCL filter values is explained below [22], [70] - [71], [76]. Filter parameters can be defined as a percentage of their base values. In order to select the filter parameters, knowledge on ripple attenuation at switching frequency, its multiples, and base bands are necessary. Current harmonics of grid connected electrical systems should comply with IEC 61000-3-2 & 61000-3-12 or IEEE 519 limits [15] - [17]. Accordingly, the respective attenuation factor can be chosen. Since AFE rectifiers are bidirectional and they can operate as power generation equipment, the higher harmonic orders $35 \leq h \leq 50$, h being the harmonic number, should be limited within 0.3 % as per IEEE 519-2014. In most of the reported works, the total inductance is taken as 10 % of total base inductance [70] - [76], but the PWM methods and converter structure have a strong dependency on finding the exact filter inductance values [88]. The maximum total inductance and minimum converter side inductance for single phase and three phase two level grid converters with different PWM schemes are summarised in Table 3.1 [71], [77], [86], [88].

Table 3.1: Inductance design for LCL filter

AFE	PWM	L_{max}	L_{imin}
3ϕ 2L VSI	SPWM	$\frac{\sqrt{\frac{V_{dc}^2}{8}-V_{g1}^2}}{\omega_g i_{g1}}$	$\frac{V_{dc}}{6f_{sw}\Delta i_{max}}$
	ZSSPWM, SVM(Asymmetric),	$\frac{\sqrt{\frac{V_{dc}^2}{6}-V_{g1}^2}}{\omega_g i_{g1}}$	$\frac{V_{dc}}{2\sqrt{6}f_{sw}\Delta i_{max}}$
	SVM(symmetric), CPWM,	$\frac{\sqrt{\frac{V_{dc}^2}{6}-V_{g1}^2}}{\omega_g i_{g1}}$	$\frac{V_{dc}}{4\sqrt{6}f_{sw}\Delta i_{max}}$
1ϕ 2L VSI	SPWM-Bipolar	$\frac{\sqrt{\frac{V_{dc}^2}{4}-V_{g1}^2}}{\omega_g i_{g1}}$	$\frac{V_{dc}}{4f_{sw}\Delta i_{max}}$

1) Converter Side Inductance: It is selected based on the peak to peak current ripple at switching frequency. Assuming the maximum converter ripple current to be 10 - 20 % of output current and symmetric space vector modulation scheme, the minimum value of converter side inductance is defined based on the volt-second across the converter side inductance [88].

$$L_{imax} = \frac{\sqrt{\frac{V_{dc}^2}{6} - V_{g1}^2}}{\omega_g i_{g1}}$$

$$L_{imin} = \frac{V_{dc}}{4\sqrt{6}f_{sw}\Delta i_{max}} \tag{3.1}$$

2) Grid Side Inductance: Total grid side inductor L_g can be sized as a fraction of converter side inductance,

$$L_g = aL_i, 0 \leq a \leq a_{max} = \frac{L_{max}}{L_i} - 1 \tag{3.2}$$

According to [76] and [85], the parameter, $a = 1$ will result in a minimum value of filter capacitor, which in turn results in minimal reactive power. In this thesis, the grid side inductance is chosen as equal to converter side inductance,

by choosing $a = 1$. Since total grid side inductance is the sum of grid self-inductance and grid side inductor, this value strongly depends on variations in the grid parameters.

3) Filter capacitor: The role of shunt capacitor is to provide a low impedance path to high frequency harmonics which falls outside the controller bandwidth. Assume an average of 5 % rated reactive power is absorbed by the filter capacitor, C_f. Then

$$C_f = 5\% \frac{P_n}{2\pi f_g {V_g}^2} \tag{3.3}$$

Even though an initial value for filter capacitor is obtained from (3.3), the capacitance value can be selected based on resonant frequency expression given in (3.4), depending on inherent damping capability of the system under certain regions of frequency. Selection of the resonant frequency will also depend on the system bandwidth and it is given as

Resonant Frequency,

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \tag{3.4}$$

3.1.2 Modelling of LCL Filter in s-domain

The equivalent circuit of LCL filter can be redrawn as shown in Figure 3.2, where V_i, V_c and V_g are the inverter, capacitor and PCC voltage respectively and i_i, i_c and i_g are the inverter, capacitor and grid currents. R_i and R_g are parasitic resistance at converter and grid side and R_c is the equivalent series resistance of filter capacitor. R_i, R_g and R_c are taken as zero in ideal conditions.

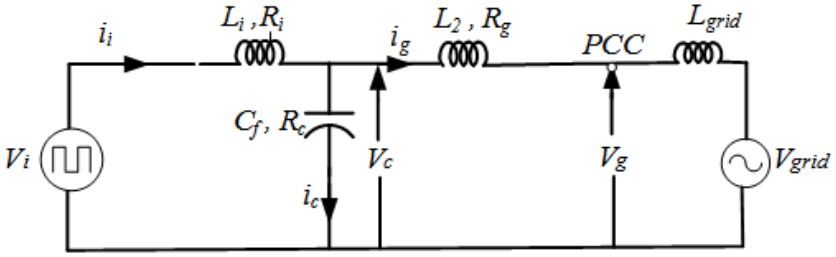


Figure 3.2: Per phase equivalent circuit of grid connected converter.

Grid Current as Feedback Signal

For grid current feedback control, the transfer function is written as a function of grid current and inverter voltage by assuming grid side as short circuit.

$$G(s) = \frac{i_g}{v_i}, |v_g = 0 \tag{3.5}$$

Then the equivalent LCL filter transfer function can be written as

$$\begin{aligned} G_g(s) = 1/(&s^3 L_i L_g C_f + s^2(L_i(R_c + R_g) + L_g(R_c + R_i)) \\ &+ s(L_i + L_g + C_f(R_c R_g + R_i R_g + R_c R_i)) + R_i + R_g) \end{aligned} \tag{3.6}$$

Assuming worst case scenario, by neglecting all parasitic and damping resistances as zero, $R_i = R_g = R_c = 0\ \Omega$, (3.6) can be rewritten as

$$G_g(s) = \frac{1}{s(s^2 L_i L_g C_f + L_i + L_g)} = \frac{1}{L_i L_g C_f} \frac{1}{s(s^2 + \frac{L_i + L_g}{L_i L_g C_f})} \tag{3.7}$$

The above system is always unstable unless provided with any passive or active damping to the system. In practical scenarios, filter inductances and capacitor have small internal resistance, $R_i \neq R_g \neq R_c \neq 0\ \Omega$.

Converter Current as Feedback Signal

Assuming grid side as short circuited, the transfer function for a current controlled converter with inverter current as chosen control variable can be defined as $G_c(s) = i_c/v_i$, provided $v_g = 0$

By substituting, $i_g = i_c/(s^2 L_g C_f + 1)$ in (3.7) gives,

$$G_i(s) = \frac{s^2 L_g C_f + 1}{s(s^2 L_i L_g C_f + L_i + L_g)} = \frac{1}{L_i} \frac{(s^2 + \frac{1}{L_g C_f})}{s(s^2 + \frac{L_i + L_g}{L_i L_g C_f})} \tag{3.8}$$

Above transfer function has inherent damping capability as it is having a resonant zero and resonant pole. Thus the system is stable at all ranges of frequency.

3.1.3 Controller Design

Figure 3.3 illustrates the overall control algorithm for a grid connected converter. DC link voltage is regulated using a proportional integral controller and the output of this controller will provide the reference value for quadrature axis component of grid current. Direct axis current reference is assumed as zero. A phase locked loop is used to determine the angle required for inverse park transform, which is utilized for converting synchronous axis components to stationary axis ($\alpha\beta$) components. After comparing the measured current (grid or converter side) with the reference values, the error is passed through the current controller. The output of the current controller provides the required modulation signal, which is further applied to the PWM block to generate the switching pulses for the converter switches. Conventional SVM implementation described in Chapter 2 has limitations since high speed digital processors are necessary to attain acceptable performance at switching frequencies above 10 - 15 kHz. Therefore, naturally sampled symmetrical SVM is selected as the PWM scheme, which is capable of operating at higher switching

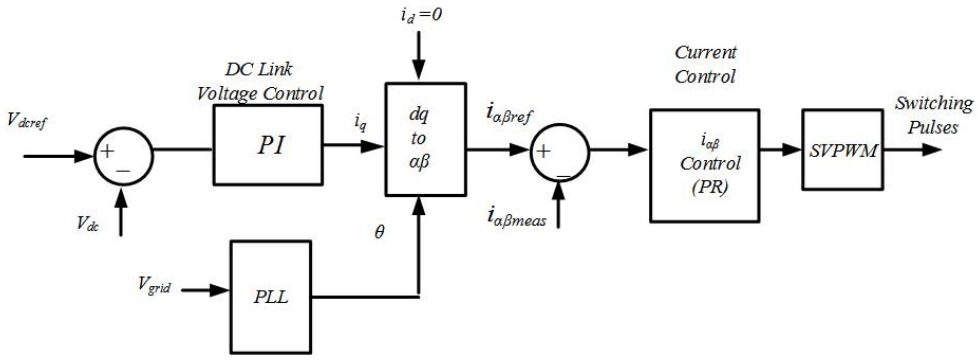


Figure 3.3: Control of AFE

frequencies based on the semiconductors switching capability. The modulation signal generation is described in (3.9).

$$V_{ma} = V_a - \frac{max(V_a, V_b, V_c) + min(V_a, V_b, V_c)}{2} \tag{3.9}$$

As our main concern is current controller, the detailed design and stability analysis of the inner current control loop is explained in this section. By taking into account the drawbacks of the conventional PI controller, stationary axis based proportional resonant (PR) controller is selected as the current controller, this is given by,

$$G_c(s) = K_p + K_i\left\{\frac{2s}{s^2 + \omega^2}\right\} \tag{3.10}$$

where, K_p and K_i are the proportional and integral coefficient of the controller and ω is the fundamental frequency. (3.10) can be further extended to reduce the effect of individual dominant lower order harmonics as given below.

$$G_c(s) = K_p + K_i\left\{\frac{2s}{s^2 + \omega^2} + \sum_{n=5,7,11..} \frac{2s}{s^2 + \omega_n^2}\right\} \tag{3.11}$$

where, ω_5, ω_7 and ω_{11} are the individual 5^{th}, 7^{th} and 11^{th} order harmonic

frequencies and the integral control of these harmonic terms will reduce the effect of individual dominant lower order harmonics. Note that third and triple order harmonics are not considered in this case, since it is limited within grid standards by utilizing the third harmonic injection based PWM scheme.

Design of proportional and resonant coefficients of PR controller can be performed in a similar way as in proportional integral controller [20]. The initial value of K_p is determined based on the system crossover frequency, which is defined as given in (3.12), where, PM is the defined phase margin and T_{delay} is the sum of sampling and transport delay. Phase margin is selected as 45^o.

$$\omega_{cmax} = \frac{\frac{\pi}{2} - PM}{T_{delay}}, \quad T_{delay} = 1.5T_s. \tag{3.12}$$

Note that, the K_p value is designed by neglecting the effect of the capacitor as it is mainly used for bypassing the high frequency current components. Thus for finding controller coefficients, the third order transfer function of LCL filter has been assumed as first order by neglecting the filter capacitor effects (C_f = 0). The plant transfer function can then be written as

$$G_g(s) = \frac{1}{s(L_i + L_g) + (R_i + R_g)} = \frac{1}{sL + R} \tag{3.13}$$

Comparing the closed loop transfer function of system and controller with the generalized second order equation, the gain K_p and integral gain K_i are obtained as

$$K_p = \frac{L\omega_{cmax}}{V_{dc}}, K_i = \frac{\omega_{cmax}}{10}, \tag{3.14}$$

Even though the initial approximation of K_p can be obtained from (3.14), this value needs further tuning based on filter capacitor value. Effects of K_p on system stability and its fine tuning will be explained in next section. As integral coefficient mainly contributes to limiting steady state error, the designed value will work for

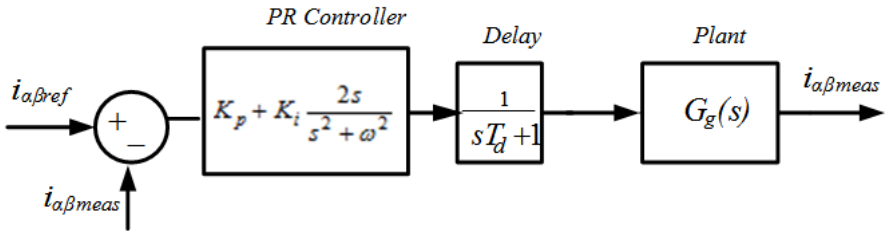


Figure 3.4: System under stability study with grid current feedback

different filter capacitor values.

3.1.4 Stability Analysis

In practical converters, the effect of sampling and transport delay cannot be avoided due to the discrete implementation delay in digital processors. The sampling and delay time can be approximated as 1.5 times the sampling time T_s in fast processors, whereas this value may vary in slow processors. Assuming the controller is implemented in a fast processor, a total delay time of $T_d = T_{pwm} + T_{delay}$ is considered for the stability analysis, in which $T_{pwm} = T_s$ and $T_{delay} = 0.5T_s$. The LCL filter without parasitic resistances is considered for stability study by assuming worst case scenario.

Effect of Controller Parameters

Initially, the study is based on grid current feedback and PR controller with the only fundamental resonant term is taken for analysis. As per the filter design mentioned in subsection (3.1.2) and assuming 6 % of reactive power is absorbed by the capacitor, the filter parameters are chosen as L_i = L_g = 0.0016 H, C_f = 15 μF to fall resonant frequency in the region $6 \leq f_{sw}/f_{res} < 10$. A different value for filter capacitor can be chosen based on the percentage of reactive power absorbed and the range in which resonant frequency has to remain same.

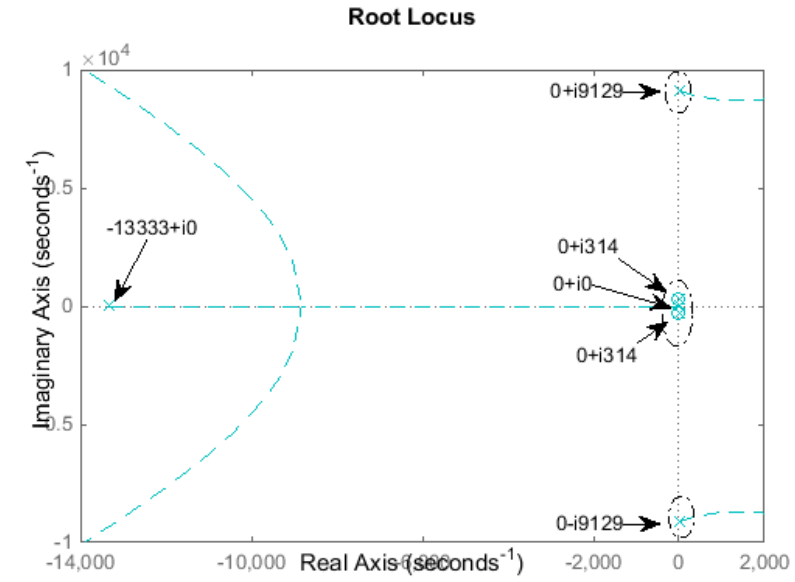
The Open Loop Transfer Function (OLTF) of the system under stability study is obtained as

$$G(s) = \frac{K_p}{L_i L_g C_f} \frac{1}{s(s^2 + \omega_{res}^2)} \frac{s^2 + 2\frac{K_i}{K_p}s + \omega^2}{s^2 + \omega^2} \frac{1}{sT_d + 1} \tag{3.15}$$

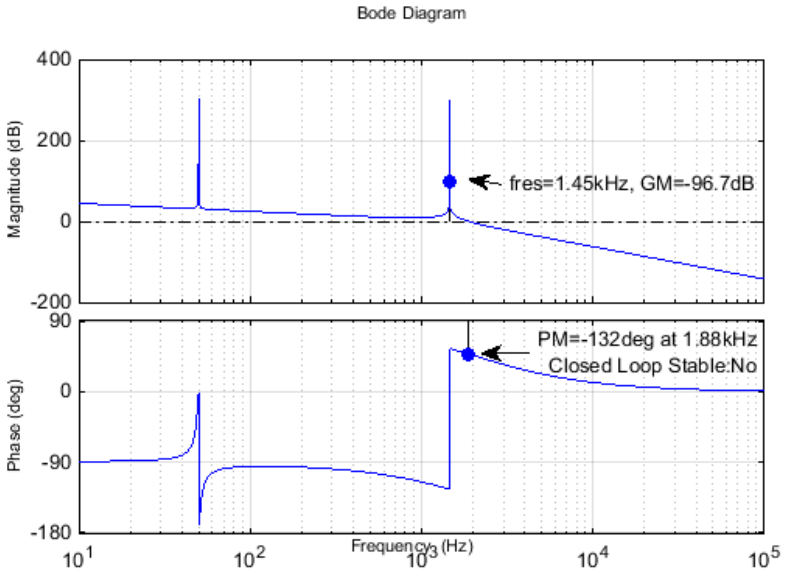
Root loci and the Bode plot of OLTF is depicted in Figure 3.5, which clearly show that four poles reside on the imaginary axis and one is located at the origin. The poles at the imaginary axis lead to a marginally stable system, but the oscillations around resonant frequency poles further force the system to an unstable region.

However, in practical scenarios, the parasitic resistances cannot be taken as zero, since the passive components can never be treated as lossless. With the parasitic resistances, $R_i = R_g = R_c$ = 0.1 Ω, the Bode plot of modified OLTF is shown in Figure 3.6, which verifies that the designed value of K_p = 47.89, leads the closed loop system to unstable region due to the shifting of closed loop poles to the right half side of imaginary axis.

An approximate value of interactive proportional gain which can lead the system to stability can be extracted from root loci analysis given in Figure 3.6 using MATLAB tools. The maximum value of K_p that leads the closed loop system stable is K_p = 1.299, and above which the system will shift to the unstable area. Table 3.2 summarizes the system frequency domain response at different K_p values. It is evident that, at K_p = 10.89, 6, 3.5, the magnitude plot crosses 0 dB axis at three different instants (only two is shown here). Even though the first value determines the bandwidth of controller, the resonance region leads the system to unstable with a negative phase margin. Fine-tuning of the proportional gain can move the poles on the right half side towards imaginary axis and further to the left half of s-plane; satisfactory response cannot be achieved only by adjusting the proportional gain. The necessary time domain requirements such as percentage overshoot and the



(a)



(b)

Figure 3.5: Stability analysis with grid current feedback under worst case (a)Root locus (b) Bode plot

settling time are found to be 3.21 and 8 s respectively, which is not acceptable for a fast response grid connected system. In addition, steady state error cannot be eliminated by only proportional control. This necessitates the incorporation of

either integral or resonant term to the proportional term, but it can only impact the steady state response. As a result, either passive or active damping is essential to limit the current and voltage distortions within acceptable IEEE limits. This can also improve the transient performance of grid current regulated AFE rectifiers.

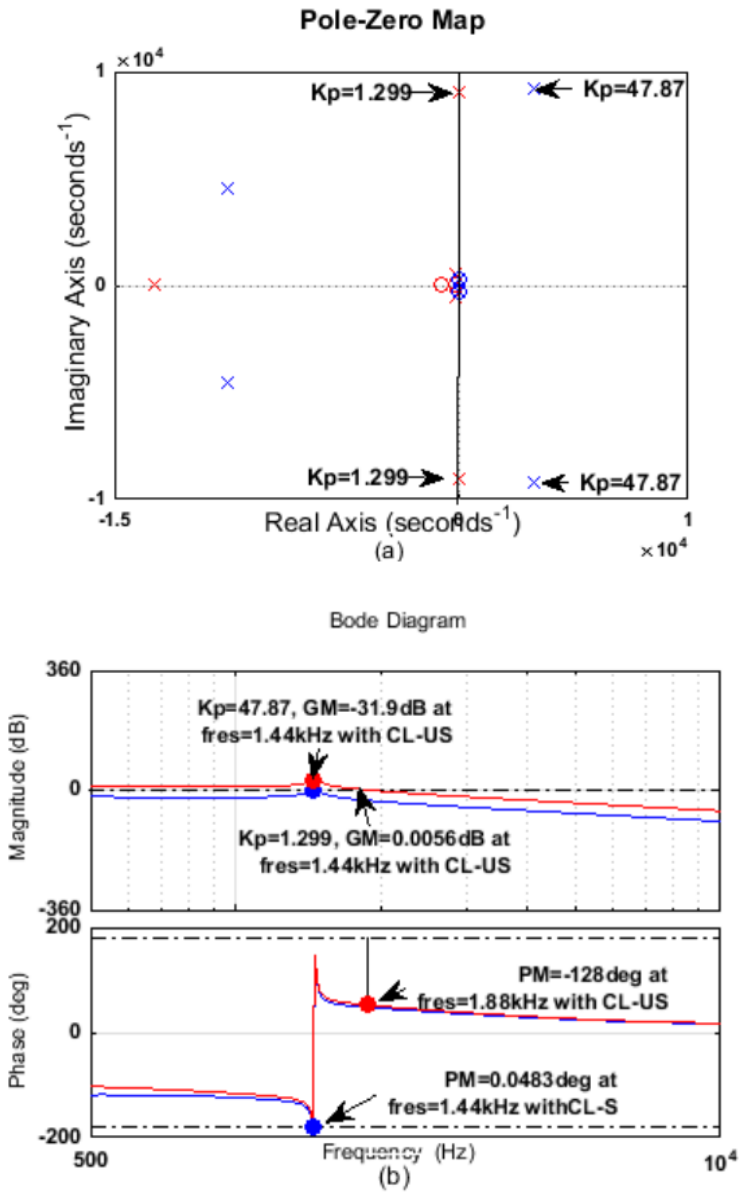


Figure 3.6: Effect of K_p on stability (a) Pole-zero map (b) Bode plot

Table 3.2: Effect of filter parameter K_p

K_p	PM (^{o})	f_{PM} (kHz)	Stable/Unstable
33.5	-130	1.78	Unstable
10.89	76.1 -120	0.41 1.59	Unstable
6	71.7 -115	0.22 1.53	Unstable
3.5	54.3 -109	0.15 1.5	Unstable
1.299	22.9	0.12	Stable

Figure 3.7 illustrates that the resonant coefficient K_i does not have a strong impact on the stability since it affects mainly the steady state error. Therefore, K_i has to be selected to achieve minimal steady state error.

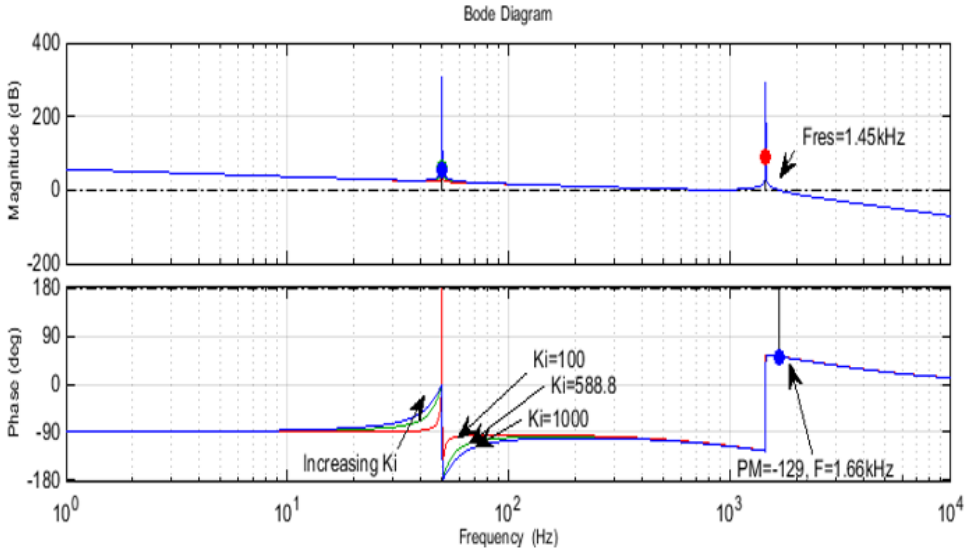


Figure 3.7: System under stability study with grid current feedback

Effect of Filter Parameters on stability

Even though in [21], [74] state that AFE with grid current feedback is stable under certain regions of frequency, the stability of the system cannot guarantee that the higher order harmonics are within accepted grid standards. The frequency response characteristics with various filter capacitances are selected to analyze the stability effects in different frequency regions as elaborated in Table 3.3.

Table 3.3: Effect of filter and controller parameters

C_f μF	f_{res} kHz	$\frac{f_{res}}{f_{sw}}$	Phase Margin (PM) ^{o}	Gain Crossover Frequency(f_{cp}) kHz
4.7	2.59	3.85	71.7 -137	0.67 2.78
7.5	2.05	4.86	70.8 -132	0.70 2.25
15	1.44	6.87	-123	1.66
20	1.25	7.94	-120	1.47

The Bode response is shown in Figure 3.8. The system is unstable with a negative phase margin, if the frequency ratio resides in $f_{res}/f_{sw} > 6$ band, but the system might lead to the stable area inside the region $2 < f_{res}/f_{sw} < 6$, in which the resonant frequency falls outside system bandwidth. Although with C_f = 4.7 μF and 7.5 μF, the resonant frequency falls outside the bandwidth, the resonant region crosses the 0 dB line which leads the resonant frequency related higher order harmonics to exceed the allowed limits. In practical scenarios, the filter capacitance is assumed to bypass all the higher order harmonics fall outside the bandwidth. Thus in systems with stringent grid requirements, a damping should

be provided to make sure all the higher order harmonics are within acceptable grid limits under different operating conditions and loading scenarios. To summarize, if the resonant frequency falls inside system bandwidth, the control algorithm can be modified to include active damping to the system, otherwise passive damping will be the only solution to damp out unwanted higher order harmonics in the system as per grid standards.

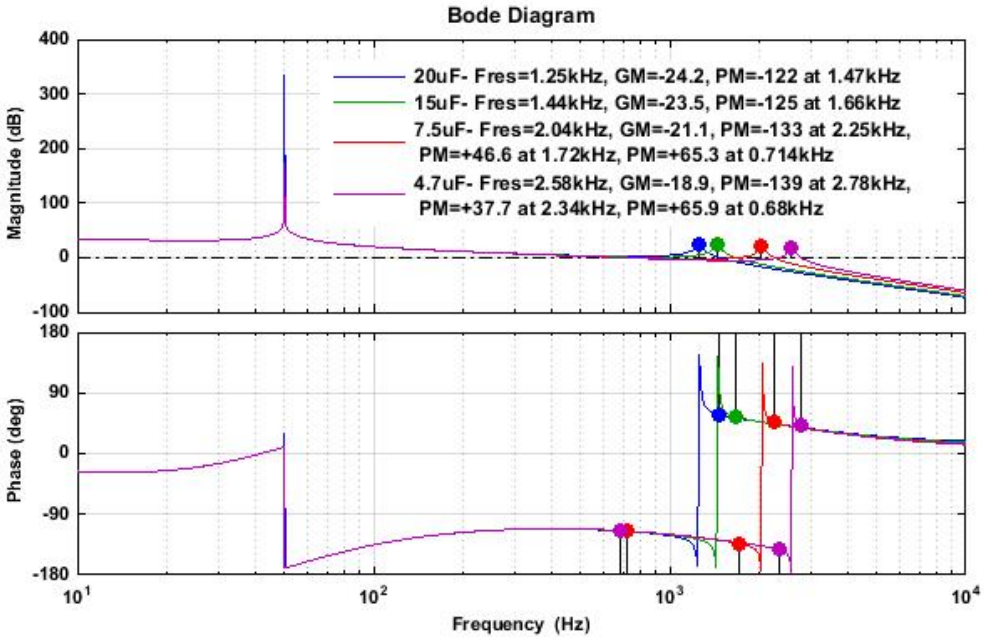


Figure 3.8: Effect of C_f on stability - Bode plot

The percentage of ripple current allowed at converter side varies depending on applications. With strong grid requirements, usually, 10 % has chosen as the ripple. Also, under low frequency applications, the skin effect of winding can be omitted, but care should be taken in choosing the high frequency inductor above 20 kHz. Thus the effect of L_i can be minimized with careful design.

In weak grids, the resonant frequency is also affected by grid impedance variations. The root loci in Figure 3.9 show the effect of grid impedance in system resonant region. In this case, the converter side inductance and the filter capacitance values are fixed. The grid side impedance value under consideration are 0.0006 H, 0.0016 H and 0.0026 H. It is evident from the Figure 3.9 that, the resonant region moves to low frequency region as the grid side impedance increases. In those cases, grid impedance measurement or parameter estimation using any optimization method is necessary to exactly determine the resonance region.

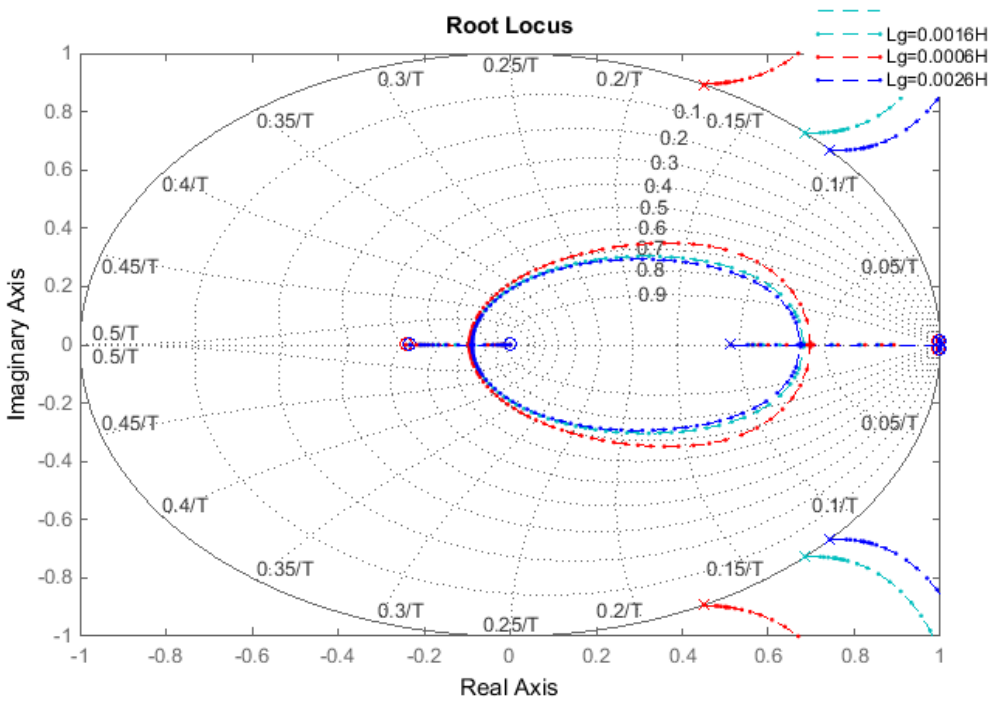
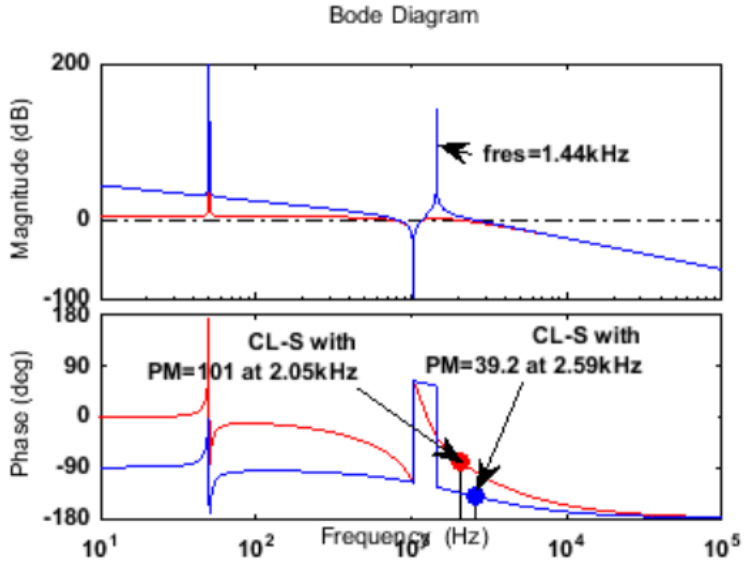
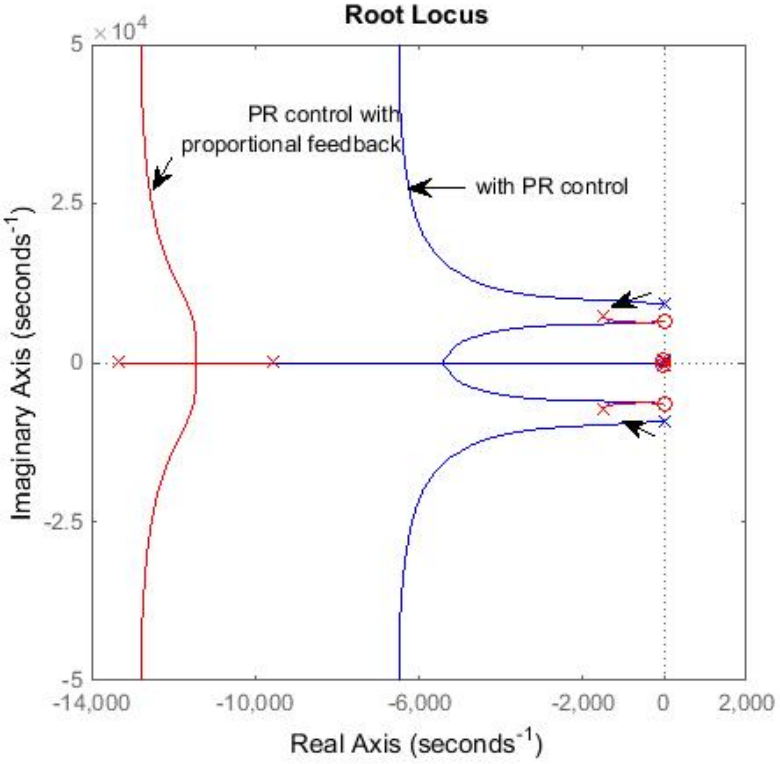


Figure 3.9: Effect of L_g on stability - Root locus

In contrast, the system is stable by considering converter current as a feedback signal. This is because the additional resonant zeros modify the phase plot to achieve positive phase margin as shown in Figure 3.10.



(a)



(b)

Figure 3.10: Stability analysis with converter current feedback (a) Bode plot (b) Root locus

The system under stability study is same as in the previous case with a fixed time delay of 1.5 times the sampling period and the plant transfer function is taken as $G_i(s)$. The root loci of OLTF clearly indicates that the resonant peaks introduced due to poles are at the imaginary axis which leads the harmonics near resonant peaks considerable. It is obvious from the frequency domain analysis that the resonant poles and zeros reside inside the bandwidth of the system. But the amount of individual harmonics at resonant frequencies and its side-bands can usually cross the limits specified by IEC 61000-3-2 standards. Bode plot validates that the resonance occurs at two different frequencies which correspond to resonant zero and resonant pole. In case of C_f = 15 μF, resonant zero and pole occurs at 1.03 kHz and 1.45 kHz respectively. The system is inherently stable in all frequency regions with a positive phase margin under pre-specified time delay and controller parameters, but the harmonics due to resonant poles need to be controlled as per grid standards.

The above mentioned stability analysis was conducted with a fixed time delay of 1.5 T_s. But in the actual case, this delay will depend on several factors, but mainly the processing speed of digital controller. In case of the fast processor, a total delay of 1.5 T_s is acceptable with sampling frequency as twice the switching frequency. Studies show that decreasing or increasing the delay time has adverse effects on system stability [9], [20], as it tempts the resonant poles to fall outside the unit circle. To see the effect of time delay T_d, the continuous domain OLTF is discretised with a fixed sampling time which replicates the digital domain implementation. Bode plot of the discretised OLTF with different time transport delays, $T_{delay} = 0.5T_s$, T_s, and $2T_s$ are demonstrated in Figure 3.13, from which it is clear that system is going to an unstable mode with T_d below $0.6T_s$ and above $3.5T_s$. This is also evident in pole movement of Figure 3.13, where it can be seen that the poles move outside the unit circle.

In order to achieve the damping without additional passive components and

sensors, an additional negative proportional feedback is introduced to the PR controller as illustrated in Figure 3.11. Since the feedback effect is only affecting the denominator of $G_c(s)$, the oscillations around resonant poles and its sidebands can be damped out.

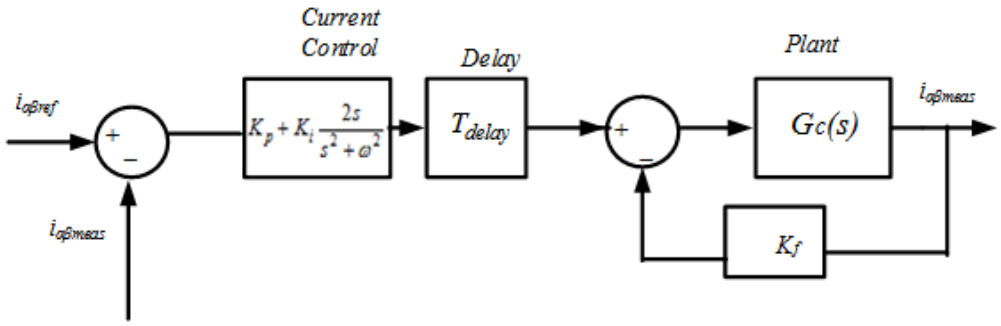


Figure 3.11: CLTF of system and controller with converter current feedback

The current control algorithm of PR controller is modified with respect to proportional resonant feedback (PRF) controller as given in (3.16).

$$V_m(s) = (i_{\alpha\beta ref} - i_{\alpha\beta meas})(K_p + K_i \frac{2s}{s^2 + \omega^2}) - K_f \times i_{\alpha\beta meas} \tag{3.16}$$

where, K_f is the feedback control variable and it is calculated by comparing the closed loop transfer function with the generalized second order equation.

$$K_f = \frac{2\zeta\omega_{cmax}L - R - K_pL}{V_{DC}} \tag{3.17}$$

The damping factor ζ can be adjusted to achieve sufficient damping to the system. Normally, ζ should fall in the range $0.7 \leq \zeta < 1$, and ζ = 0.7074 is chosen for this stability study. The system chosen for stability analysis is given in Figure 3.12.

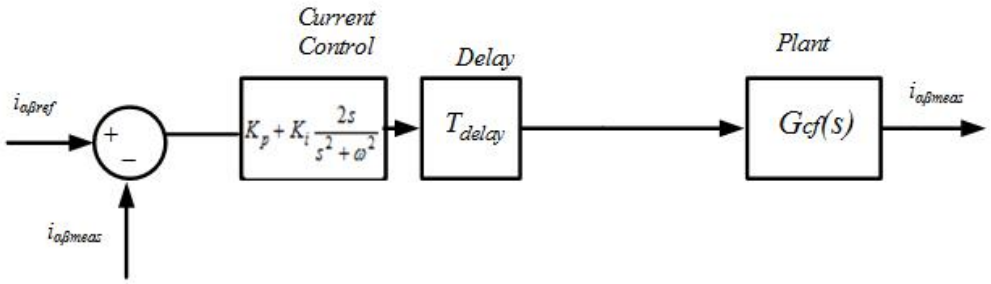


Figure 3.12: System under stability study with converter current feedback

$$G_{cf}(s) = \frac{s^2 C_f L_g + 1}{s^3 L_i L_g C_f + s^2 K_f C_f L_g + s(L_g + L_i) + K_f)} \tag{3.18}$$

From the above transfer function, it is clear that PRF controller has the same effect of connecting a damping resistor in series with the converter side inductance. The open loop bode plot of the system with PRF controller indicates that the peak overshoot and oscillations due to resonant pole are damped out by the modified controller. Interestingly, the phase plot depicted in Figure 3.13 verifies that the phase margin is further increased to 104^o, which improves the stability of the system. The main aim of additional control feedback is to push the resonant poles inside the unit circle. Also, the magnitude plot verifies that the resonant peak is at 1.45 kHz. The pole-zero map of PR controlled grid converter (Figure 3.13) reveals that the resonant poles are in the marginal area of the unit circle. In contrast, the converter current negative feedback in PRF control provides damping to the system and moves the resonant poles to inside the unit circle, which ensures stability to the overall system. One of the major disadvantages of PR controlled converter current regulated AFE is its dependence on delay which determines the stability of the overall system. PRF controller overcomes this drawback, as the feedback control pushes all marginally stable and unstable poles inside the stability region.

As evident from the pole - zero plot, all unstable poles are moved inside the unit circle - for example the system was unstable with T_{delay} = 0.5T_s with PR control, but the unstable poles are moved to the inside region of the unit circle, using the PRF control.

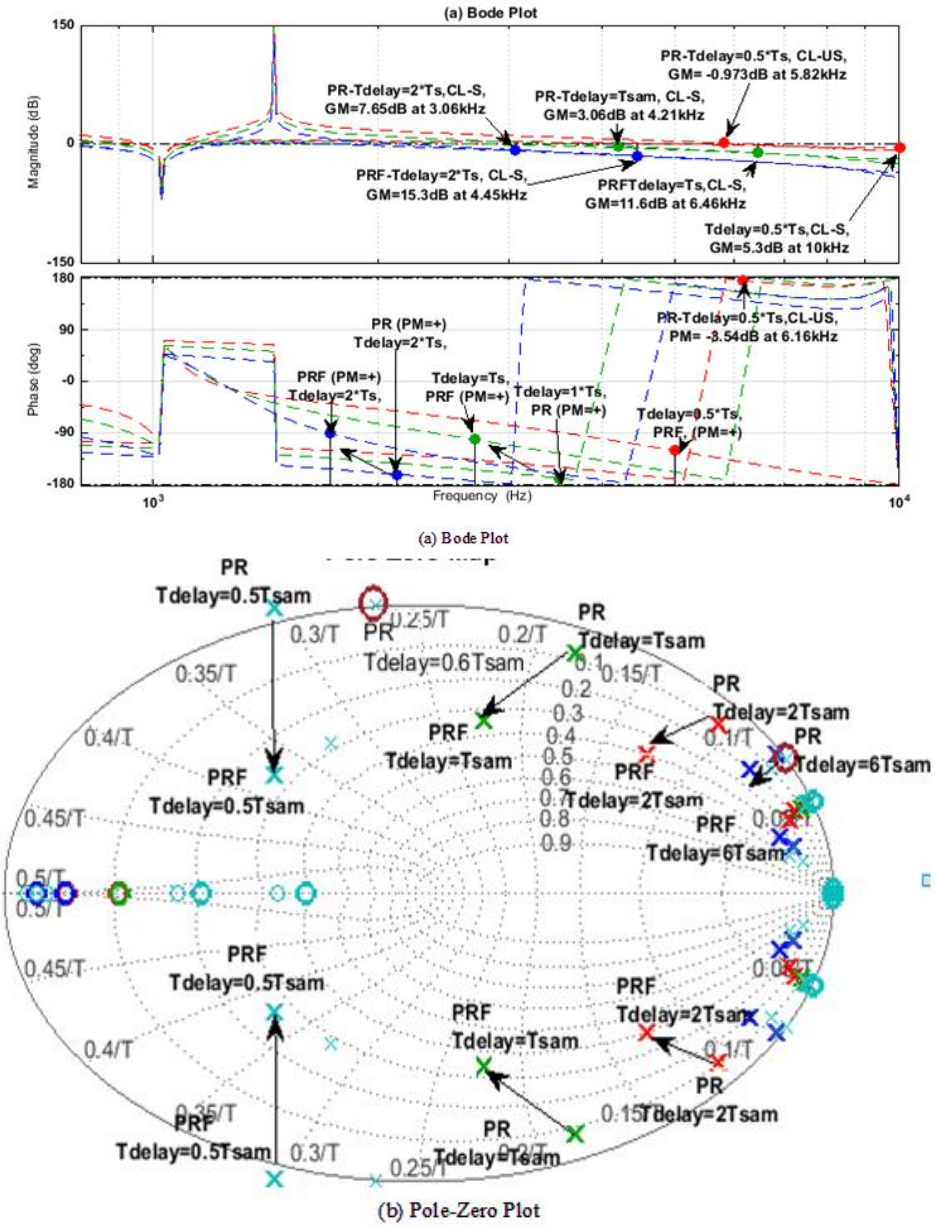


Figure 3.13: CLTF with converter current feedback (a) Bode plot(b)Pole - zero map

3.1.5 Damping Methods

As clear from the previous section that in grid current regulated systems, the resonance oscillations can lead the system to instability, especially when the resonant frequency falls within system bandwidth. These oscillations can be eliminated by applying suitable damping techniques to the system. Two methods of damping are studied in this chapter, viz. passive and active damping as illustrated in Figure 3.14.

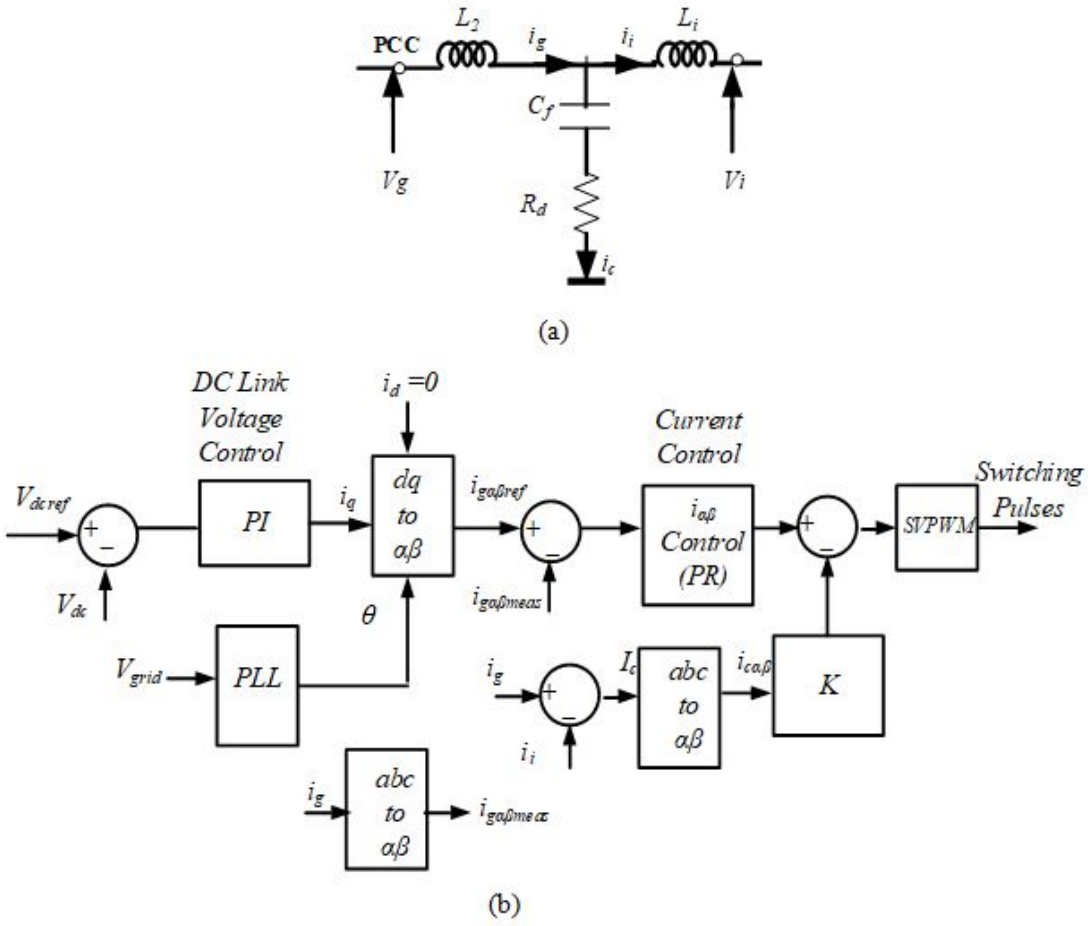


Figure 3.14: Damping methods (a) passive damping (b) capacitor current feedback based active damping

Passive Damping

A resistor can be connected in series with the filter capacitor to provide passive damping to the system as shown in Figure 3.14. Passive damping does not depend whether the resonant frequency falls inside or outside the system bandwidth. But this method is the only solution to limit the higher order harmonics to acceptable limits, when the resonant frequency falls outside the system bandwidth region since the controller cannot be modified to provide damping actively. As per IEEE 519, the harmonics order greater than or equal to 35 should be limited to 0.3 % of nominal current.

The minimum value of damping resistor, R_{dmin} can be defined as [133]

$$R_{dmin} = \frac{1}{6\pi}\frac{L_g}{L_i}\frac{f_{sw}}{f_{res}}\frac{1}{\omega_{res} * C_f} \quad for \;\; f_{sw} \gg f_{res} \;\; and \;\; \frac{L_g}{L_i} \gg 1$$

$$R_{dmin} = \frac{1}{\omega_{res} * C_f} \quad for \;\; f_{sw} \approx 2 * f_{res} \;\; and \;\; \frac{L_g}{L_i} < 2 \tag{3.19}$$

Power loss due to damping resistor can be calculated based on the current passing through filter capacitor. It can be split as loss due to the fundamental component i_{cfun} and harmonic component i_{ch} as described in [133]. The loss due to fundamental component of capacitor current P_{dfun} can be written as

$$P_{dfun} \approx 3 \times i_{cfun}^2 \times R_d \tag{3.20}$$

If C_f is designed to absorb below 5 % of rated reactive power, i_{cfun} and thus P_{dfun} will be small. The converter side harmonic current can be treated as the filter capacitor harmonic current as it provides low impedance path to higher order harmonics above the resonant frequency. The derivation of converter harmonic current for symmetrical space vector PWM has been provided in [88]. The rms value of capacitor harmonic current is given by,

$$i_{chrms} = \frac{1}{2\sqrt{3}} \frac{1}{\sqrt{48}} \frac{V_{dc}}{f_{sw} L_i} \sqrt{\frac{2}{3}m^2 - \frac{4\sqrt{3}}{\pi}m^3 + \frac{9}{8}(\frac{3}{2} - \frac{9}{8}\frac{\sqrt{3}}{\pi})m^4} \tag{3.21}$$

where m is the modulation index. An upper and lower boundary have defined in [133] to obtain the power loss due to harmonic components of capacitor current, which are given by

$$P_{dh}^{lower} = 3 \times i_{chrms}^{lower^2} \times R_d$$

$$P_{dh}^{upper} = 3 \times i_{chrms}^{upper^2} \times R_d, \tag{3.22}$$

where

$$i_{chrms}^{lower} = i_{chrms}$$

and

$$I_{chrms}^{upper} = i_{chrms}^{lower} | \frac{i_c (m_f - 6) w_f}{i_c^{lower} (m_f - 6) w_f} |$$

The average of P_{dh}^{lower} and P_{dh}^{upper} is used to estimate P_{dh}. Lower bound corresponds to the harmonics $\omega \geq \omega_{res}$ and upper bound represents the sideband centered on the switching frequency and its multiples. It is clear from (3.21) and (3.22) that the switching frequency is inversely proportional to the damping losses. But a compromise between switching loss and damping loss is necessary for increased switching frequencies, as the switching loss is directly proportional to f_{sw} in traditional Si devices. In low switching frequency converters, active damping is preferable as it can damp the resonant oscillations without physical losses.

Bode response of a grid current regulated AFE operating at a frequency of 10 kHz is shown in Figure 3.15, where the filter parameters are chosen as L_g = L_i = 1.6 mH and C_f = 15 μF. The system is unstable due to resonant oscillations and a damping resistor of 5.4 Ω is connected in series with the capacitor to damp out the

resonant oscillations. In latter case, filter capacitor value of 4.7 μF is chosen and a reduced value of 4.4 Ω is sufficient to attain stability of the system.

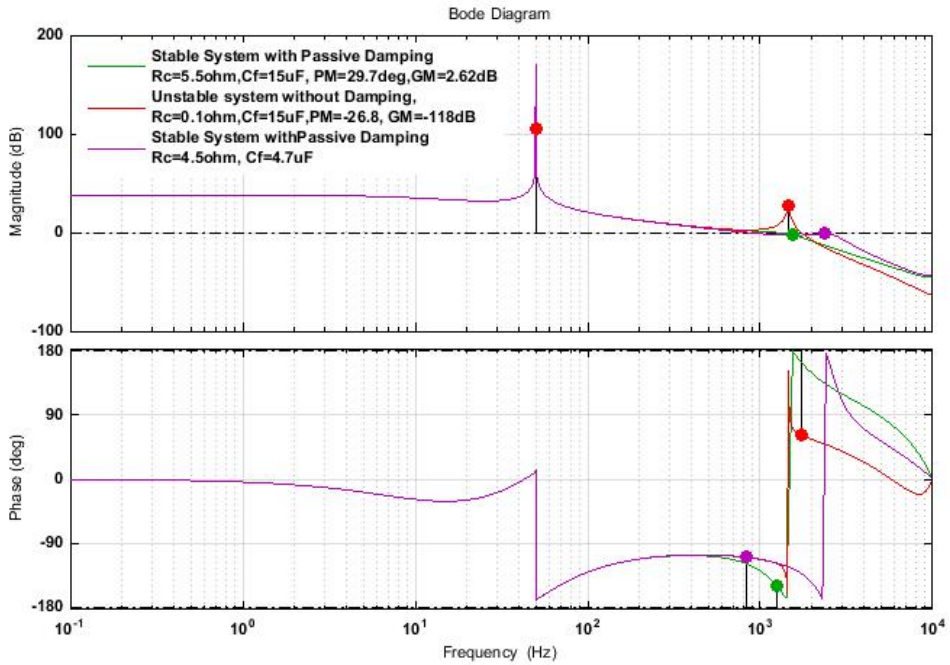


Figure 3.15: Bode plot of system with LCL filter- with and without passive damping

Active Damping

In this case, damping can be achieved by means of modifying the current control algorithm, if and only if the resonant frequency falls inside system bandwidth. This method does not cause any additional power loss since it does not utilize any physical components. In this section, the current through the filter capacitor is negatively fed back to the modulating voltage as shown in Figure 3.14. The proportional constant K should be designed to provide optimum damping to the system. In this

case, it is taken as equal to the proportional constant of PR controller.

3.2 Stability Analysis in High Frequency Converters

The stability studies in grid connected converters discussed in the previous section were based on the assumption that the switching frequency is in few kHz ranges (low frequency region). As mentioned in Chapter 1, the traditional IGBTs are limited to operate at a low frequency of 15 - 20 kHz due to their physical restrictions. However, the introduction of SiC semiconductors to commercial markets leads the adoption of high frequency converters for grid interfaced applications. The filter design discussed in the last chapter is suitable for selecting the filter parameters at higher frequencies. This section discusses the filter and controller requirements for high frequency grid connected converters. Following, the stability analysis is conducted for converters switching at high frequency region around 50 kHz.

3.2.1 Filter Design

The filter design discussed in subsection 3.1.1 is suitable for selecting the filter parameters at higher frequencies. However, the following aspects need to be considered:

- Converter side inductor:

  Converter side filter is designed by considering the minimum and maximum value of filter inductor as per Table 3.1. At lower frequencies, the skin effect of windings is negligible, but as the frequency increases, this skin effect results in increased resistance. For converters operating above 20 kHz, stranded wires are used to build filter inductors, which can reduce the skin as well as proximity effects, and therefore results in reduced losses. In industrial

applications, Litz wire is preferred for constructing filter inductors at high frequencies [134].

- Grid side inductor:

  It is normally taken as the transformer inductance; otherwise, the same value of converter side inductance can be chosen.

- Filter capacitor:

  Filter capacitor value is initially determined based on the percentage reactive power absorbed by the capacitor. Another factor which further refines the value of capacitance is the resonant frequency. The resonant oscillations created by the LCL filter can be controlled by suitable damping method. Passive damping is more suitable at higher frequencies rather than active damping, as the switching frequency is inversely proportional to the damping losses P_{dh}. Since SiC devices offer lower switching losses at higher switching frequencies, higher switching frequency operation is possible for high power converters in contrast to traditional Si IGBT based converters.

After fixing the filter inductors, the capacitor value must be chosen in order to satisfy the bandwidth requirements and resonant frequency. Even though it does not possess direct relation with switching frequency, the resonant frequency and controller bandwidth play a role in finding the value of C_f. A detailed study on filter capacitor influence on the system stability is discussed in the next section.

3.2.2 Stability Analysis

Initially, a simple L filter is considered for the study. At higher frequencies, even an L filter can satisfactorily eliminate the switching frequency harmonics, but the ripple in grid current and PCC voltage is still a concern. A first order L filter

provides 20 dB/decade attenuation at the frequencies above control loop bandwidth (8 kHz) as illustrated in open loop Bode plot given in Figure 3.16.

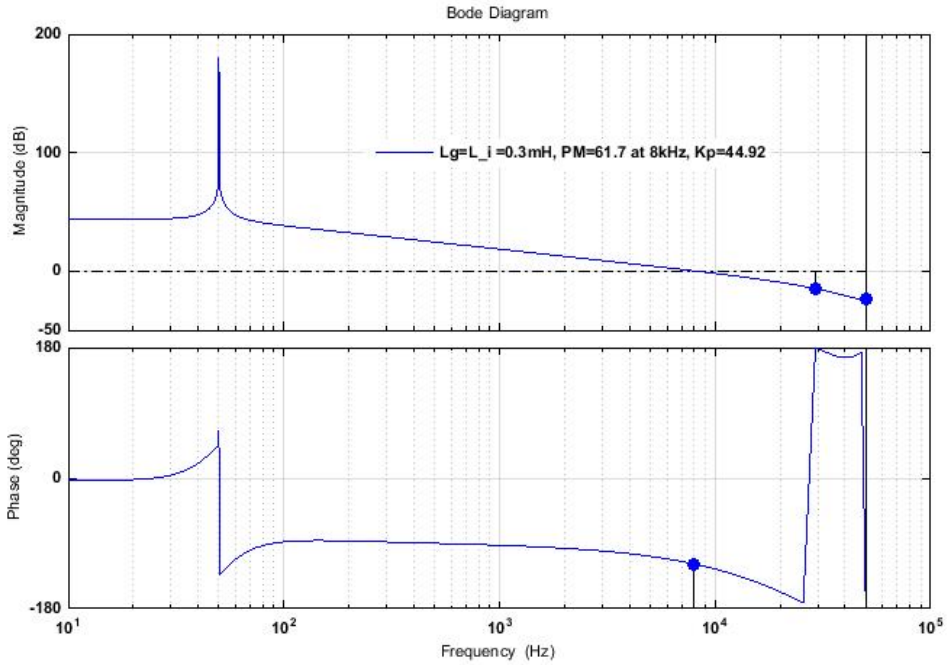


Figure 3.16: Bode plot of system with L filter

As evident from the third order LCL filter transfer function given in (3.7) that it has two poles on the imaginary axis and one pole at the origin. The two imaginary poles are responsible for the resonance oscillations and these oscillations can lead the system to instability. The controller bandwidth f_c and resonance frequency should meet the following requirements.

At high switching frequencies, fast processors are necessary to meet these requirements. Even the hardware delay may adversely affect the system stability if the processor delay is larger. In this stability study, a total delay of 1.5 times the sampling time is considered. Also, the measurement devices should need higher

bandwidth in order to effectively capture all the data.

A bode plot for converter switching at 10kHz with output filter values L_g = L_i = 1.6 mH, C_f= 15 μF is shown in Figure 3.17. In this case, the resonance occurs at 1.45 kHz and damping is necessary to damp out the unwanted oscillations. Filter inductor value is drastically reduced at 50 kHz since the switching frequency is inversely proportional to the filter inductor value. A decreased value of L_g = L_i = 0.3 mH is sufficient to restrict the current ripple and bound the higher order harmonics to permissible limits.

For a converter switching at 50 kHz, the controller bandwidth should have a minimum value of 5 kHz. Increased bandwidth and resonant frequency should only be attained by decreasing the filter value as illustrated in Bode plot given in Figure 3.17. Also, it is evident that, with C_f = 15 μF, the controller bandwidth is less than 5 kHz.

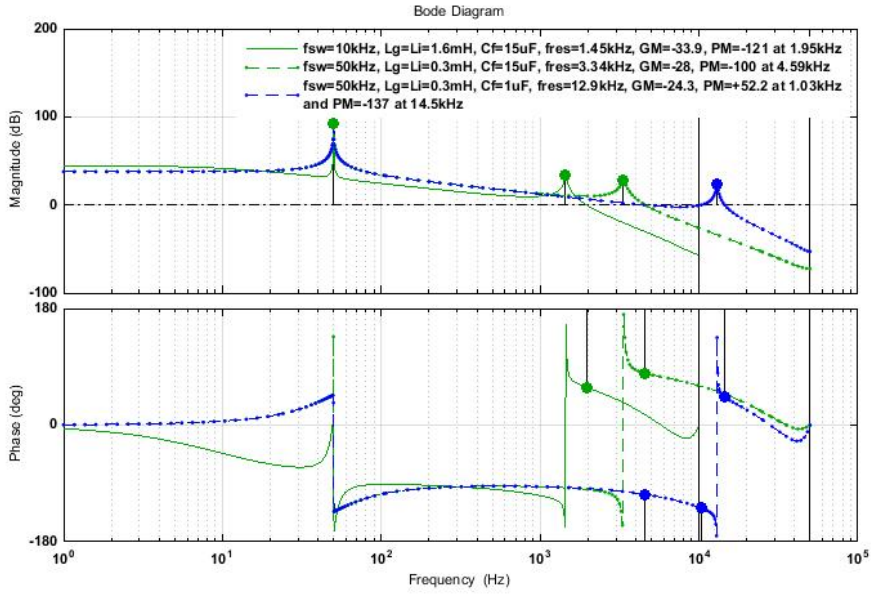
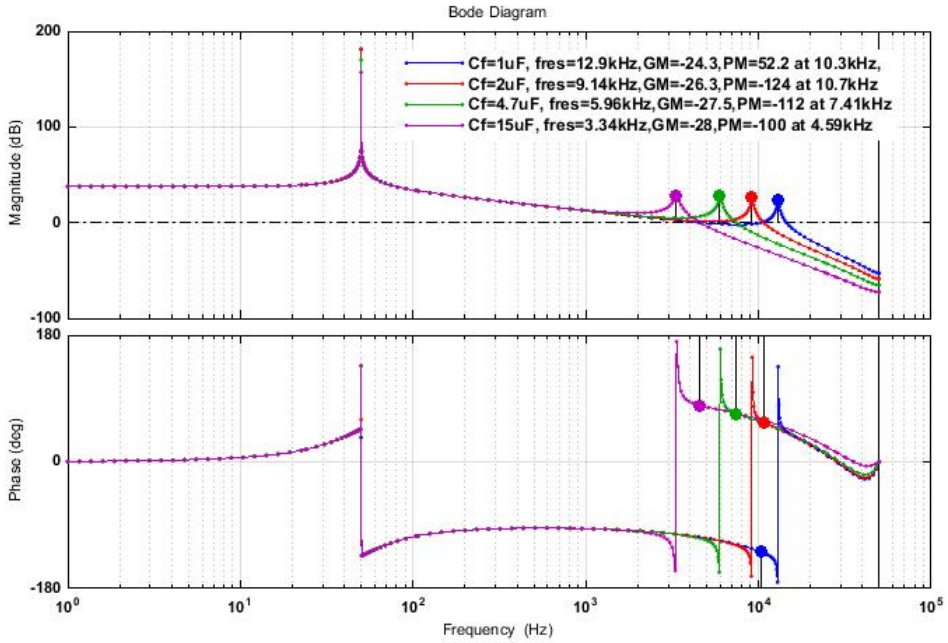
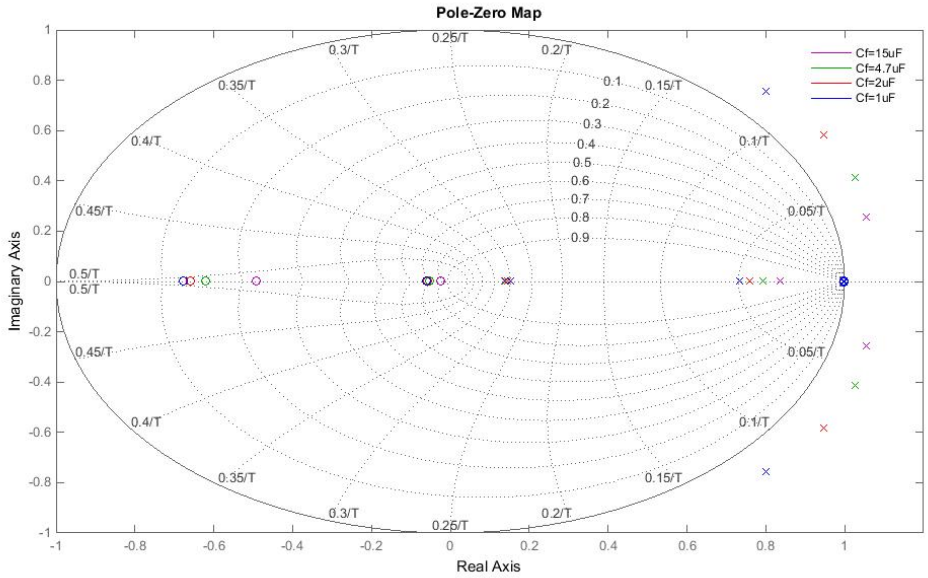


Figure 3.17: Bode plot showing the impact of switching frequency and filter parameters on system response



(a)



(b)

Figure 3.18: Effect of filter capacitor on system stability (a) Bode plot (b) Pole-zero map

A further refined value of filter capacitor should be based on the following analysis given in Figure 3.18, where the frequency response of the system with capacitor values of 1 μF, 2 μF, 4.7 μF and 15 μF is shown. Since the decreased value C_f results in reduced damping requirements, a capacitor value of 1 μF is enough to effectively achieve the power quality. In this case, the resonant frequency falls outside the controller bandwidth, which in turn eliminates the necessity of additional damping for the unwanted oscillations.

The pole zero plot with various values of filter capacitances is shown in Figure 3.18. It is clear that the resonant poles fall outside the unit circle in all cases and a damping resistor can move the poles residing outside of the unit circle to inside stability region. Although SiC devices have low switching and conduction losses, the loss due to passive components has to be limited to fully utilize the capabilities of wide bandgap devices. It should be noted that, the amplitude of resonant peaks decrease as the filter capacitor value increases, and this reduces the damping requirement and a small value of damping resistor is sufficient to damp the resonant oscillations at higher frequencies. An active damping might be a possible solution to achieve damping without physical losses, but the additional sensors should be capable of measuring the high frequency components.

Controller design also plays a critical role in selecting the bandwidth of the high frequency converters. Since K_p possess strong impact on controller bandwidth, it has to be selected to meet the necessary controller requirements. The relation between K_p and the controller bandwidth is illustrated in the frequency response shown in Figure 3.19.

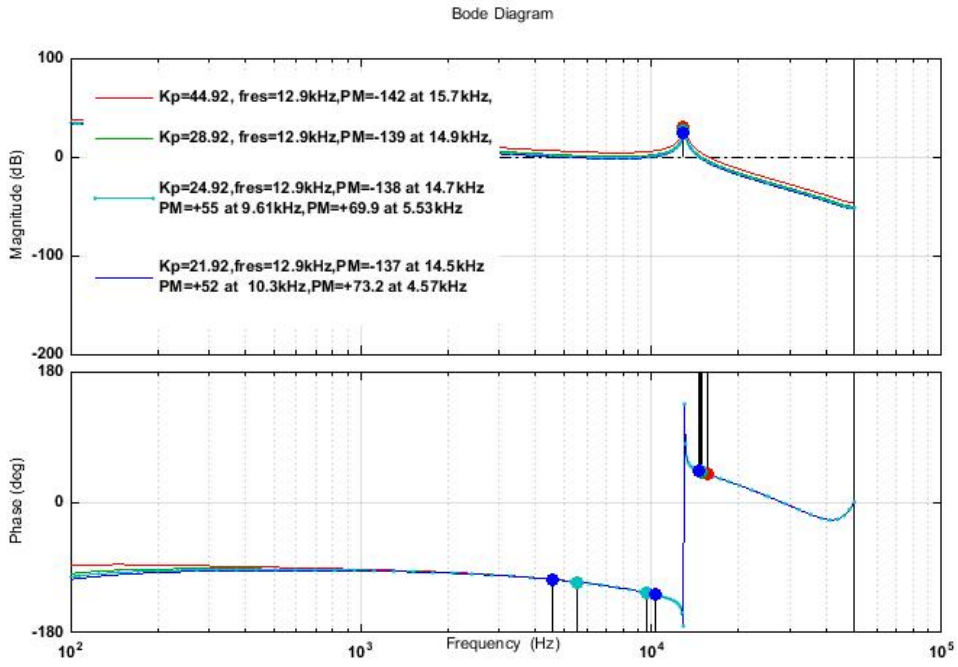


Figure 3.19: Bode plot showing the effect of K_p on stability

In this analysis, the filter parameters are chosen as $L_g = L_i = 0.3$ mH and $C_f = 1$ μF. It should be noted that the ratio f_{sw}/f_{res} falls in the range < 4. The initial value of $K_p = 44.92$ can be obtained as per design. It is clear from the Bode plot shown in Figure 3.19 that, with K_p values of 44.92 and 28.92, the resonant frequency falls inside the controller bandwidth. This necessitates additional damping methods which further compromise the advantage of reduced losses in wide bandgap device based converters.

In order to avoid the additional costs or losses in active or passive damping methods, K_p value is further decreased to 24.92. As clear from the Bode response that the magnitude plot crosses the 0 dB line 3 times and the middle value results in positive phase margin of 55^o at 9.61 kHz. The other two values occur at 5.53 kHz

and 14.7 kHz and none of them fails to meet the minimum controller bandwidth. The response of a further reduced value of K_p = 21.92 is also shown, which verifies that, although it has positive phase margin at 10.3 kHz, one of the 0 dB crossing occurs at f = 4.57 kHz which does not meet the necessary bandwidth requirements.

3.3 Simulation Study

In order to verify the findings and conclusions made with design and stability studies, a computer simulation is conducted using PSCAD/EMTDC for grid/converter current regulated AFE converters. The system parameters are given in Table 3.4.

Table 3.4: System under simulation study

System Parameters	**Values**
Line to Line Voltage	440 V
Source Frequency	50 Hz
Rated Power	10 kW
DC Link Voltage	700 V
Rated Current	20 A
Low Frequency Converter	
Switching Frequency	10 kHz
Sampling Frequency	20 kHz
Converter Side Inductance	0.0016 H
Grid Side Inductance	0.001 H
Grid Self-Inductance	0.0006 H
Filter Capacitor	15 μF/4.7 μF
High Frequency Converter	
Switching Frequency	50 kHz
Sampling Frequency	100 kHz
Converter Side Inductance	0.0003 H
Grid Side Inductance	0.0003 H
Filter Capacitor	4.7 μF/ 1 μF

3.3.1 Low Frequency Converters-Grid Side Current Feedback

Case I: Effect of K_p on system stability

In this case, grid current is used as a feedback control variable with filter capacitor value of 15 μF and the resonant frequency resides in the region $6 \leq f_{sw}/f_{res} < 10$. The equivalent values of series resistances are taken as $R_i = R_g = R_c$ = 0.1 Ω. The results obtained for grid voltage and current are shown in Figure 3.20.

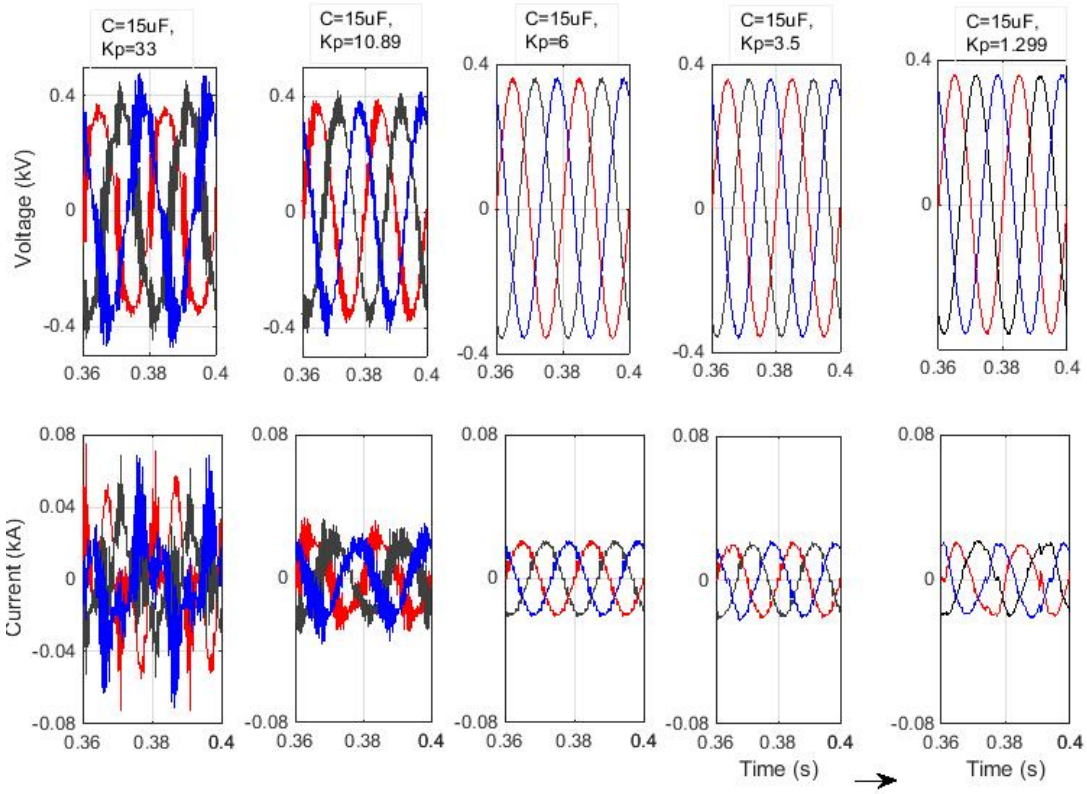


Figure 3.20: Grid current regulated AFE PCC voltage and grid current with L_i = L_g = 1.6 mH, C_f = 15 μF, and K_p = 33, 10.89, 6, 3.5 and 1.299

It is clear from the results that with proportional constant K_p = 33, the system is unstable as the resonant frequency is falling inside system bandwidth. As per stability analysis, a reduced value of K_p = 1.299 can make the system stable, but

this will narrow the system bandwidth below the acceptable limits. In order to illustrate the effect of proportional constant on stability, the simulation is repeated with the reduced value of K_p = 10.89, 6, 3.5 and 1.299 respectively. It is evident from the corresponding results that as the proportional constant reduces, the system is approaching to marginally stable state, but the total harmonic distortion in grid current is more than 15 %, even with K_p = 1.299. This verifies that reducing K_p will narrow bandwidth of the system, but it will significantly increase the lower order harmonics. Thus either passive or active damping is necessary to keep the system stabilized with limited grid current distortion.

Case II: Effect of Filter Parameters on System Stability

In this case, the role of a filter capacitor in grid connected converters stability is investigated. It is evident from the previous case study and stability analysis that, grid current regulated systems are unstable if the resonant region falls inside the controller bandwidth. To clearly analyse the effect of filter parameters in the system stability and harmonic issues, the simulation is extended with two additional filter capacitor values, say 20 μF and 4.7 μF, such that the resonant frequency falls in frequency regions $f_{sw}/10 < f_{res} < f_{sw}/6$ and $f_{sw}/6 < f_{res} < f_{sw}/2$ respectively. In the first case, ratio f_{sw}/f_{res} is selected as 7.95 whereas in the latter case, it is 3.8. Grid voltage and current waveforms are shown in Figure 3.21. The system is unstable with C_f = 20 μF, as the resonant frequency falls inside the controller bandwidth. This validates the stability analysis in the previous section, where the system was unstable with negative phase margin. But in the latter case with C_f = 4.7 μF, the resonant frequency falls outside system bandwidth region which makes the system stable as the minimal phase margin is positive. Figure 3.21 illustrates the grid current individual harmonic spectrum with C_f = 4.7 μF, when the Fast Fourier Transform (FFT) is performed for harmonic order 1 - 63. As discussed in the stability analysis, although it has minimal positive phase margin at a frequency less than resonant region, the 0 dB crossing at resonant region makes the considerable

higher order harmonics at resonant frequency and sidebands. The total harmonic distortion in grid current is found to be 4.77 %, where the resonant frequency falls at 1260 Hz and the sidebands corresponding to harmonic order 47, 49 and 53 are above 1 % of the fundamental grid current component. A passive damping can be provided to make the higher order harmonics within IEEE limits (<0.3 %).

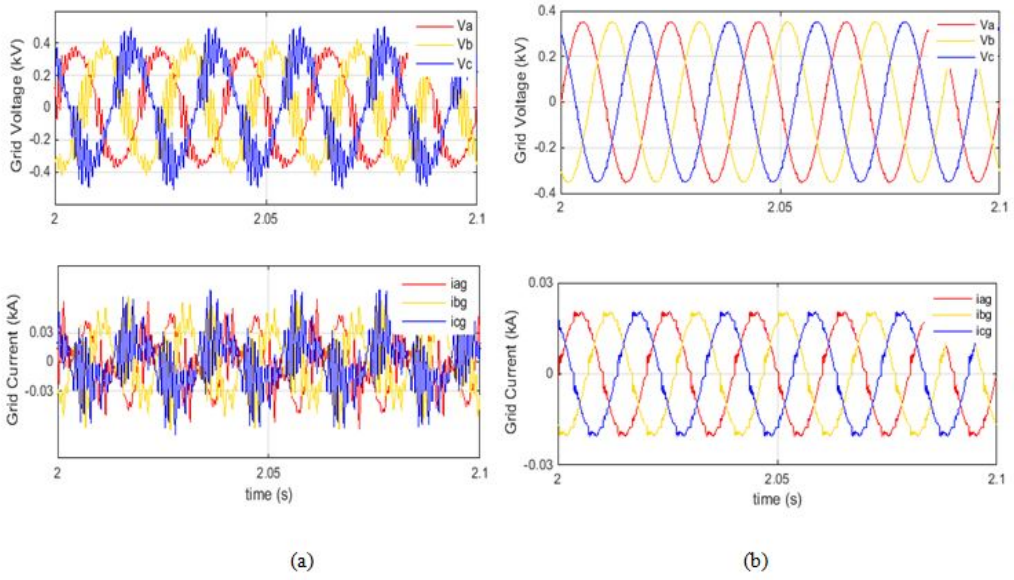


Figure 3.21: PCC voltage, grid current and converter current (a) C_f = 20 μF (b) C_f = 4.7 μF

Case III: Damping Requirements in Grid Current Regulated Systems

In this case study, the semiconductor devices are switched at a frequency of 10 kHz and the bandwidth of the controller is set high to evaluate the resonance phenomenon in the region. The filter parameters are taken as $L_g = L_i$ = 0.0016 H, C_f = 15 μF and the ESR of filter parameters, $R_g = R_i = R_c$ = 0.1 Ω, assuming a practical scenario. Initially, the grid converter is operated without any damping and the obtained grid voltage and current waveforms are illustrated in Figure 3.22. It is clear that the grid current regulated converter is unstable unless otherwise provided with any passive or active damping to damp out the resonant oscillations.

In the second case, a damping resistor of 5.4 Ω is connected in series with the filter capacitor and the grid current harmonic spectrum is depicted in Figure 3.23. The individual harmonics near the resonant region are found to be in permissible limits (< 0.3 %). The experiment is repeated with a different capacitor value of C_f = 4.7 μF and please note that the resonance is now falling under the frequency region $f_{sw}/6 < f_{res} < f_{sw}/2$. It has to be noted that, the minimal phase margin of the system OLTF leads the system to stability. Since the resonant frequency falls in the above specified region, the magnitude of resonant peak introduced by the poles is lesser compared with case C_f = 15 μF. Thus, a reduced value of damping resistor (4.4 Ω) is sufficient to keep the individual harmonics inside the permissible limits. Capacitor value cannot be further reduced, which shifts the resonant region to an undesirable area near to the switching frequency.

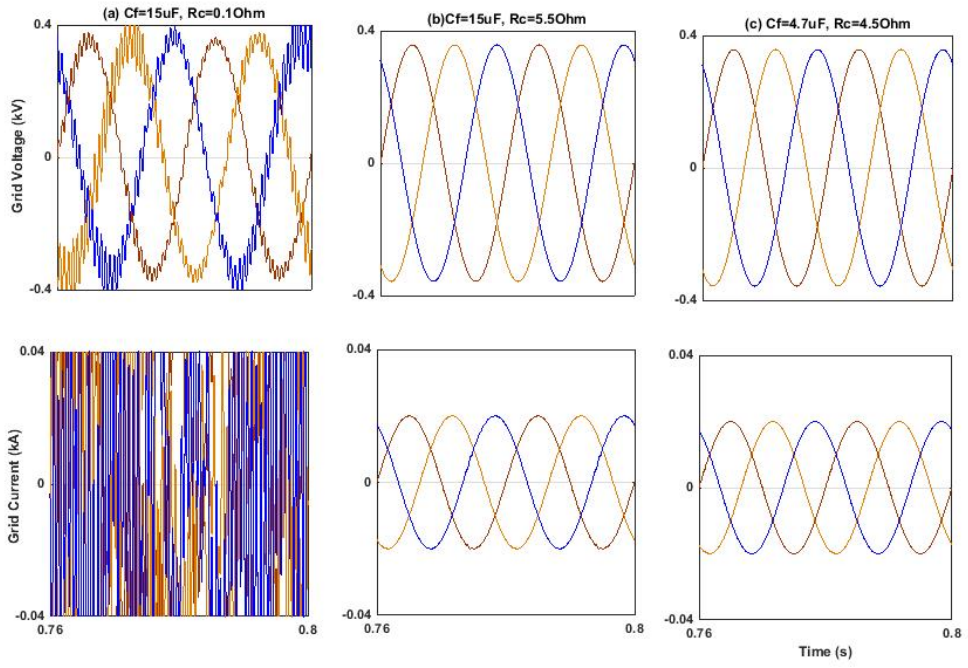
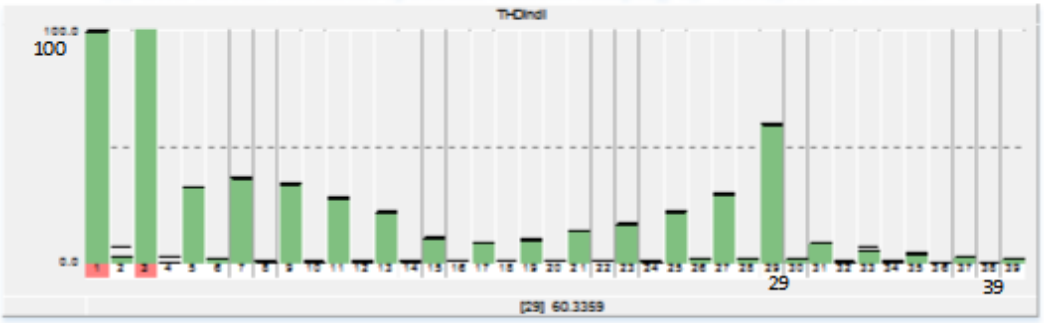
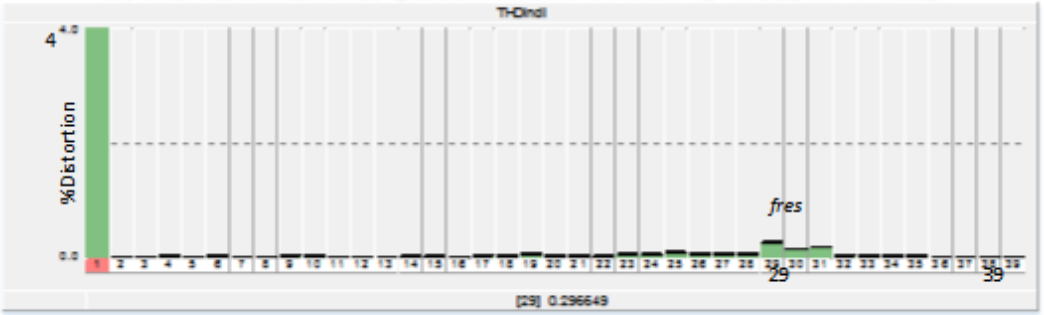


Figure 3.22: PCC voltage and grid current (a) C_f = 15 μF, R_d = 0.1 Ω, (b) C_f =15 μF, R_d = 5.5 Ω (c) C_f = 4.7 μF, R_d = 4.5 Ω

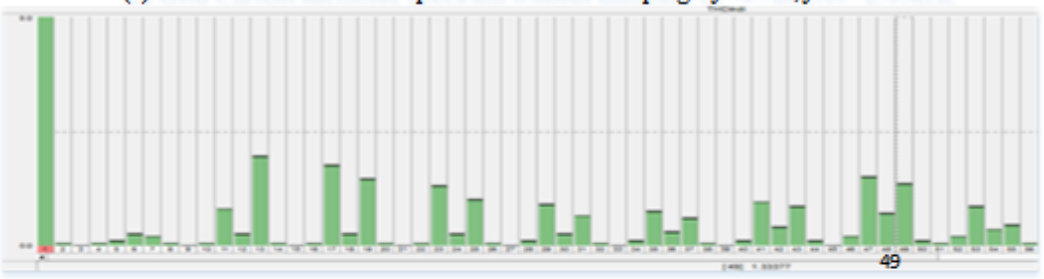
(a) Grid Current harmonic spectrum without damping-*Cf*=15uf, *fres*=1.45kHz



(b) Grid Current harmonic spectrum with Rc=5.5Ohm -*Cf*=15uf, *fres*=1.45kHz



(c) Grid Current harmonic spectrum without damping-*Cf*=4.7uf, *fres*=2.45kHz



(d) Grid Current harmonic spectrum with Rc=5.5Ohm- *Cf*=4.7uf, *fres*=2.45kHz

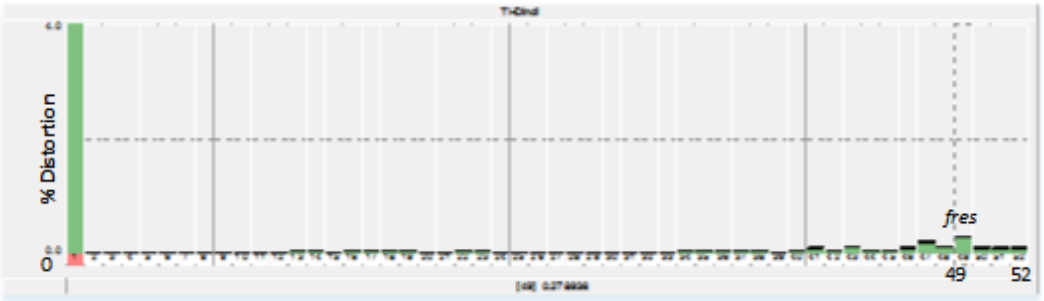
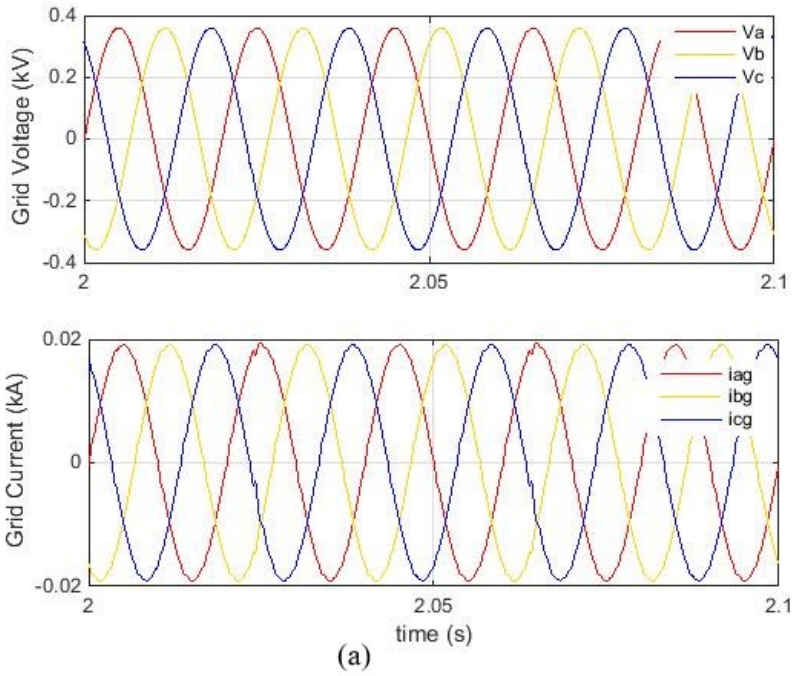
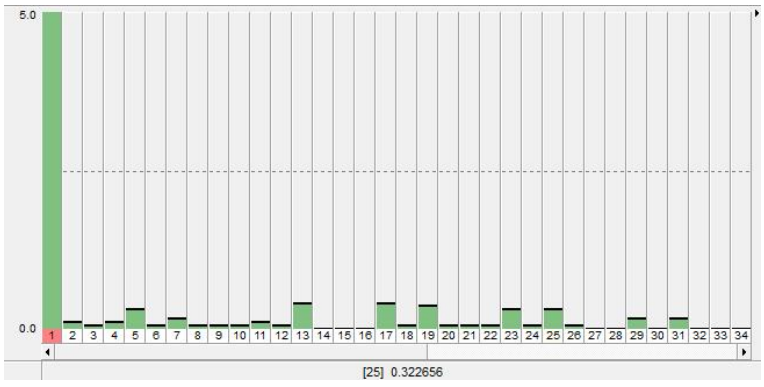


Figure 3.23: Grid current harmonic spectrum (a) C_f = 15 μF, R_c = 0.1 Ω, (b) C_f = 15 μF, R_c = 5.5 Ω (c) C_f = 4.7 μF, (d) C_f = 4.7 μF, R_c = 5.5 Ω

An example of active damping is discussed here, where the capacitor current is negatively fed back to grid current controller output to provide damping without additional losses.



(a)



(b)

Figure 3.24: PCC voltage and grid current (L_i=L_g = 0.0016 H, C_f = 20 μF) (a) with active damping (capacitor current feedback) (b) grid current total harmonic distortion

Figure 3.24 illustrates the grid voltage and grid current waveforms of a grid connected converter and the respective harmonic spectrum for grid current. In this case, filter values are considered as $L_i = L_g$ = 1.6 mH, C_f = 20 μF. Using passive damping, the total harmonic distortion for grid current is found to be 3.83 %, whereas, by providing active damping to the system, it is further reduced to 0.93 %. Figure 3.24 shows the individual harmonics in grid current, where the percentage of individual harmonics are more in passive damping compared to active damping. This can be reduced by increasing the value of the resistor, but it will result in higher losses, which should be limited to 1 % of active power.

3.3.2 Low Frequency Converters-Converter Side Current Feedback

In this case, converter current is chosen as a feedback variable. The test is conducted with stationary axis based PR and PRF controller. The filter parameters ($L_i = L_g$ = 1.6 mH, C_f = 15 μF) are selected such that resonant frequency falls in $6 \leq f_{sw}/f_{res} < 10$ band. The obtained results for grid voltage and grid current are shown in Figure 3.25. Even though PR controller is successfully achieved a grid current THD of < 5 %, the individual harmonics are not within acceptable limits. On the other hand, the lower order harmonics strictly follows the IEEE and IEC standards with added negative feedback control. In addition, the grid current THD is reduced to 1.64 %, whereas a percentage THD of 3.35 is obtained with only PR control. Adding the negative feedback will not only improve harmonic performance but also provides additional damping at the resonant pole. In case of C_f = 4.7 μF with the same filter inductance values, the resonant frequency falls in $2 < f_{sw}/f_{res} < 6$, the results verifies that, the system stability is improved and the lower order harmonics are within IEC 61000 limits. The resonant pole has shifted to 2 - 3 kHz range (f_{res} = 2.6 kHz, 53^{rd} order), and the resonant zero falls at the 36^{th} harmonic order, and its sideband components are 0.21 % (35^{th}) and 0.22

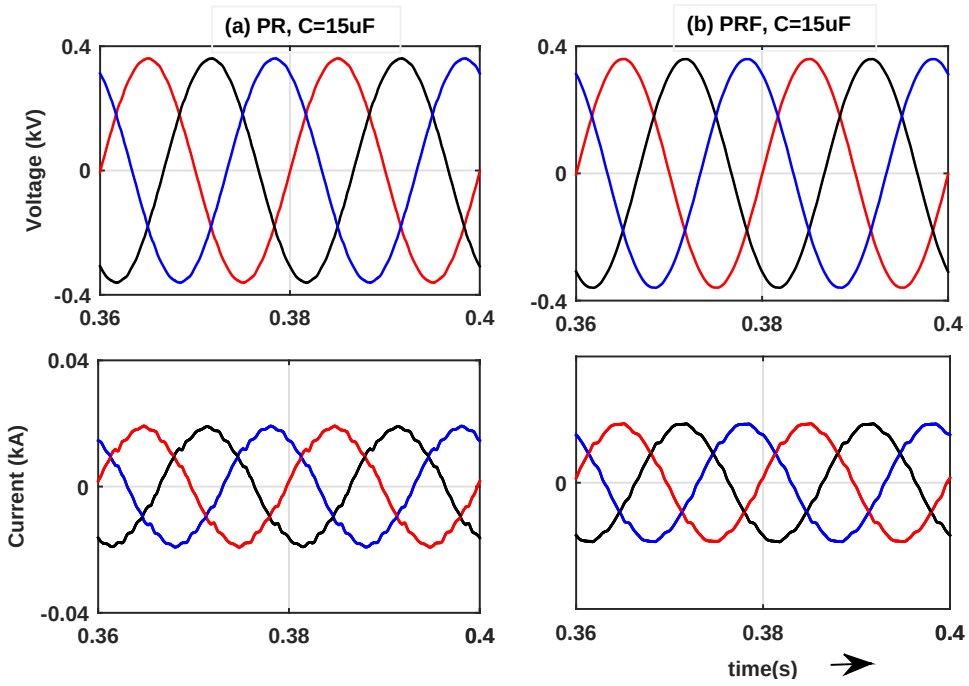


Figure 3.25: Converter current regulated AFE - PCC voltage and grid current waveforms-with PR and PRF control(L_i = L_g = 1.6 mH, C_f = 15 μF)

% (37^{th}) of fundamental component respectively. As the resonant peaks meet the required standards, feedback is not necessary for $2 < f_{sw}/f_{res} < 6$ region.

Thus converter current regulated systems are found to be more efficient as it does not require any additional passive components or measurements to damp the unwanted resonances in the system.

3.3.3 High Frequency Converters

In this case study, the switching frequency is increased to 50 kHz and the filter parameters are reduced to a low value accordingly. Converter and grid side inductors are selected as L_g=L_i = 0.0003 H and the filter capacitor is selected as C_f = 4.7 μF to keep the resonant frequency in the desired range. Note that in this case f_{sw}/f_{res} = 8.39 and it falls inside controller bandwidth. It is clear from the grid

current individual harmonic spectrum shown in Figure 3.26 that the harmonics in the resonant region and other lower order harmonics exceed the permissible limits which lead to an unstable system. Thus passive damping is necessary to achieve a stable system and as per design, where a minimum value of 4.5 Ω is necessary to damp out the resonant oscillations. The grid voltage and current waveforms for a grid current PR regulated system are shown in Figure 3.26 and the corresponding grid current harmonic spectrum verifies that the resonant components are within permissible limits.

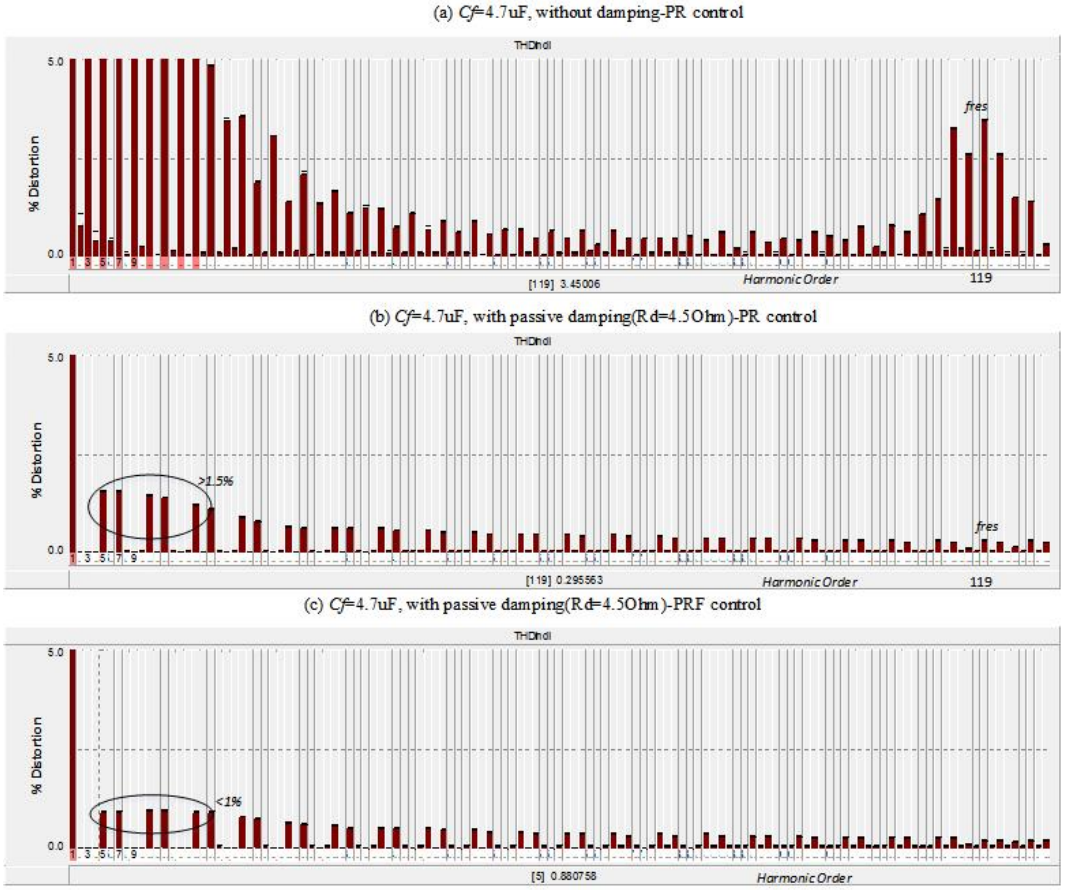


Figure 3.26: Grid current harmonic spectrum with LCL type filter C_f = 4.7 μF

However the THD is 4.35 % due to the lower order harmonics. At high frequencies, adding the odd order resonant terms 5,7,... to the controller is not a viable solution as it increases the complexity and computational delay of the system. Another option is to increase the damping resistor, which might result in increased losses. In order to reduce the individual lower order harmonics, PRF controller can be utilized and the obtained results and grid current harmonic spectrum is shown in Figure 3.26 and Figure 3.27 respectively. Even though the improved harmonic performance is not visible in grid current waveform, the spectrum clearly indicates the lower order harmonics are reduced and thereby the THD is reduced to 3.28 %. The main drawback of using PRF controller in grid current regulated systems that a compromise in reduced system bandwidth is inevitable as the bandwidth decreases with increase in feedback coefficient.

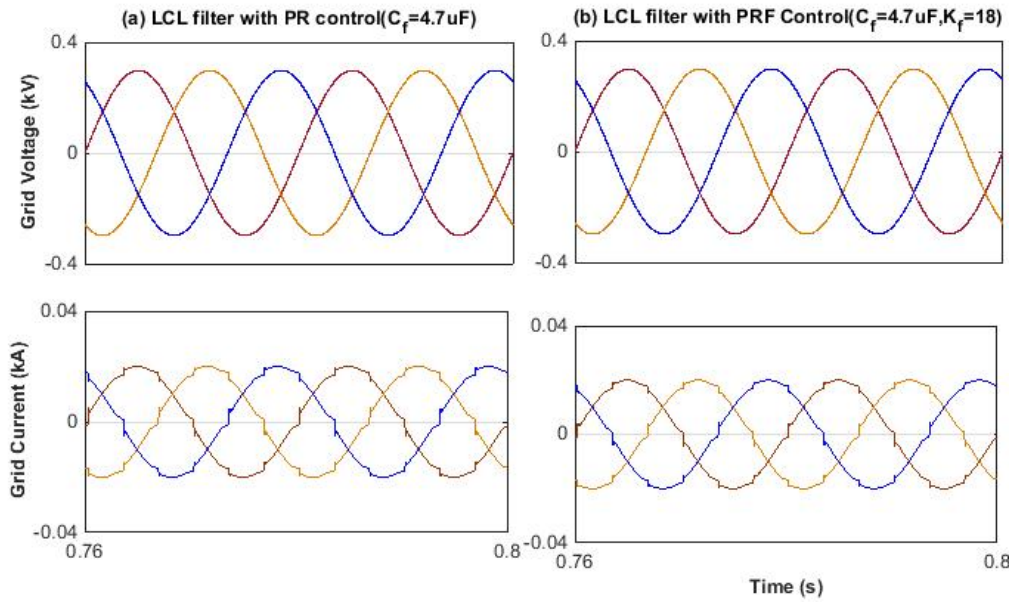


Figure 3.27: PCC voltage and grid current- f_{sw} = 50 kHz, C_f = 4.7 μF (a) PR controller (b) PRF controller

The simulation is performed with a decreased filter capacitor value of 1 μF, such

that the resonant frequency falls outside the controller bandwidth. Since the percentage of higher order harmonics decrease with increase in switching frequency, even under worst conditions $R_g = R_i = R_c$ = 0 Ω, the magnitude of resonant harmonics (f_{res} = 12.55 kHz) is very low, but the lower order harmonics which are under controller bandwidth need to be controlled. Under practical scenario, with $R_g = R_i = R_c$ = 0.1 Ω, lower order harmonics are also under 2 %, which results in grid current THD of 4.4 %. Further reduction in THD is possible with PRF controller where a reduction of 0.5 % is achieved in grid current. As a significant reduction in THD is not achieved, PR controller is more preferred than PRF controller. The grid voltage and current waveforms with PR and PRF controller under practical conditions are shown in Figure 3.28.

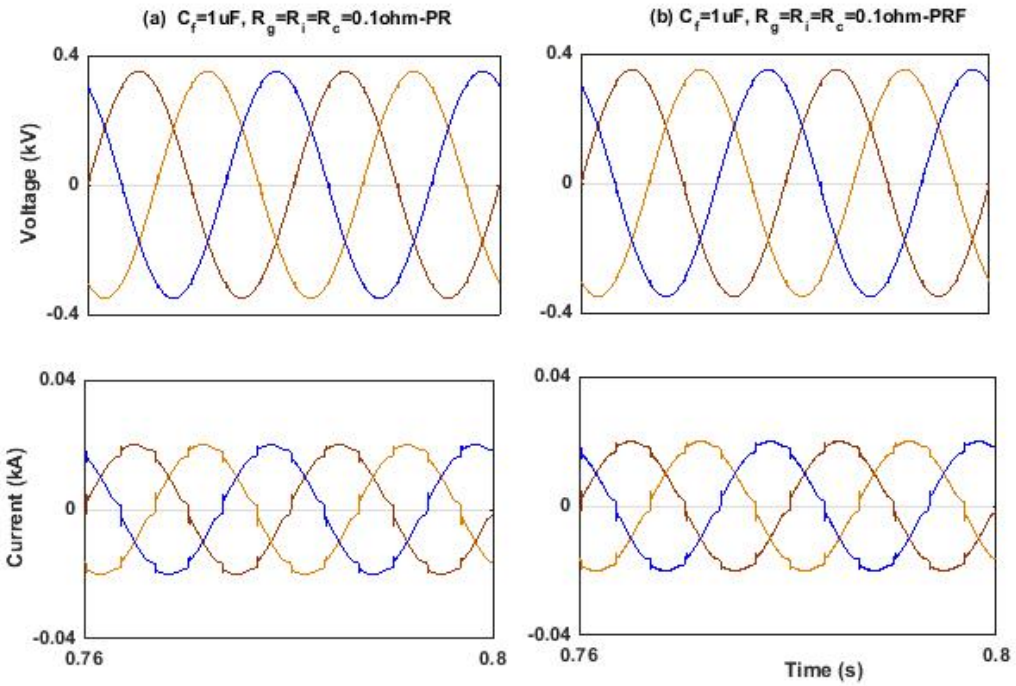


Figure 3.28: PCC voltage and grid current- f_{sw} = 50 kHz, C_f = 1 μF (a) PR controller (b) PRF controller

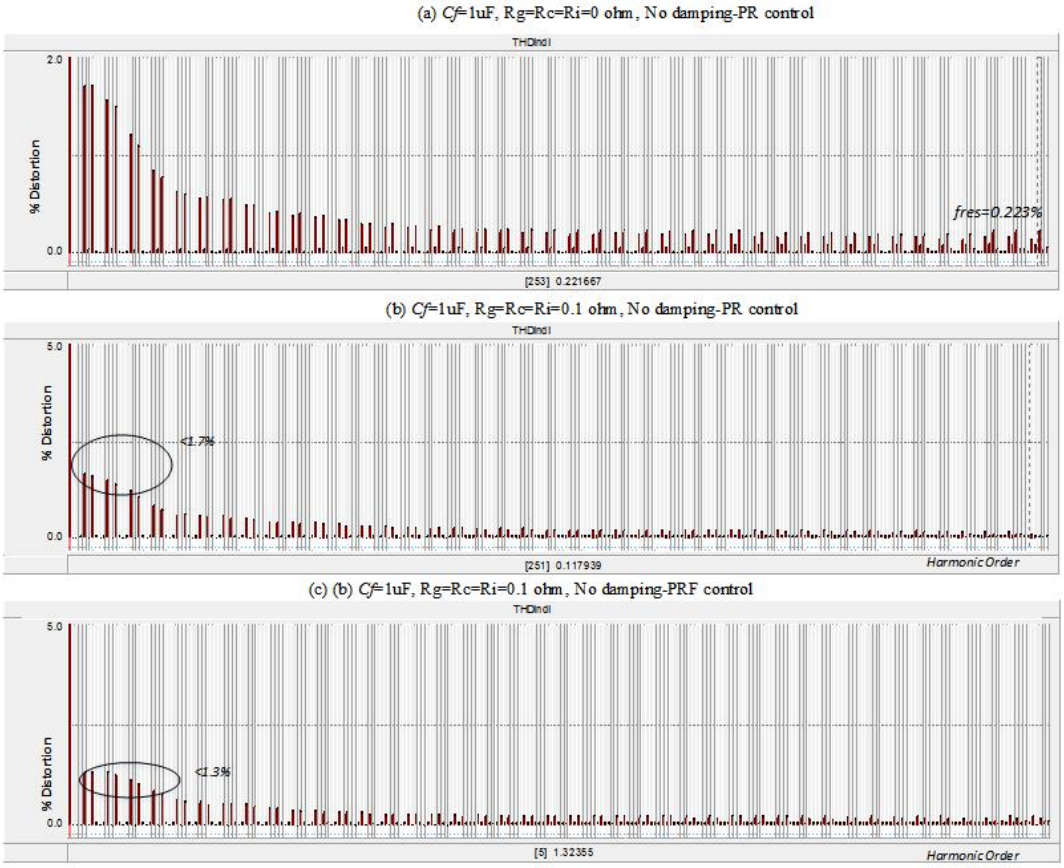
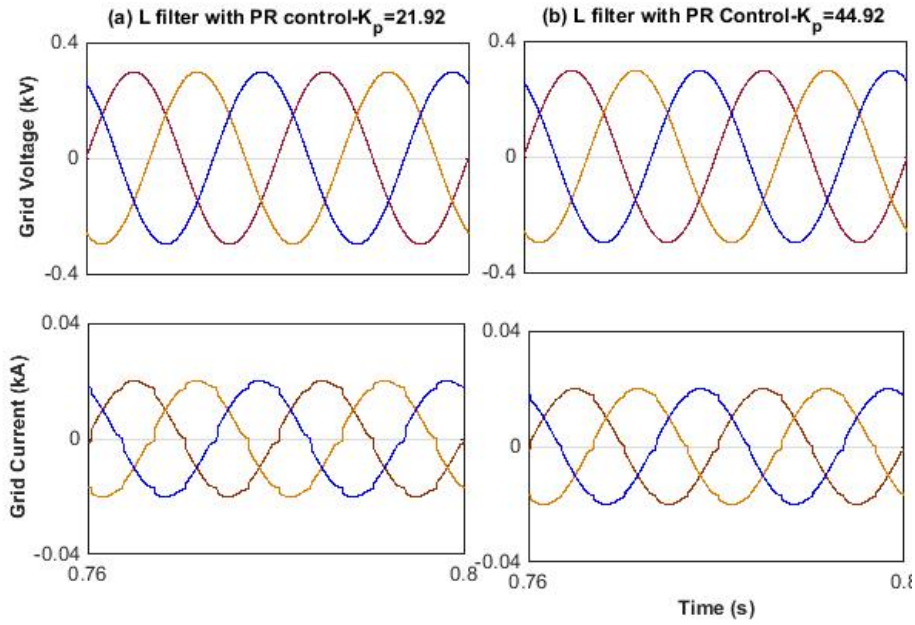


Figure 3.29: Grid current harmonic spectrum with LCL type filter C_f = 1μF

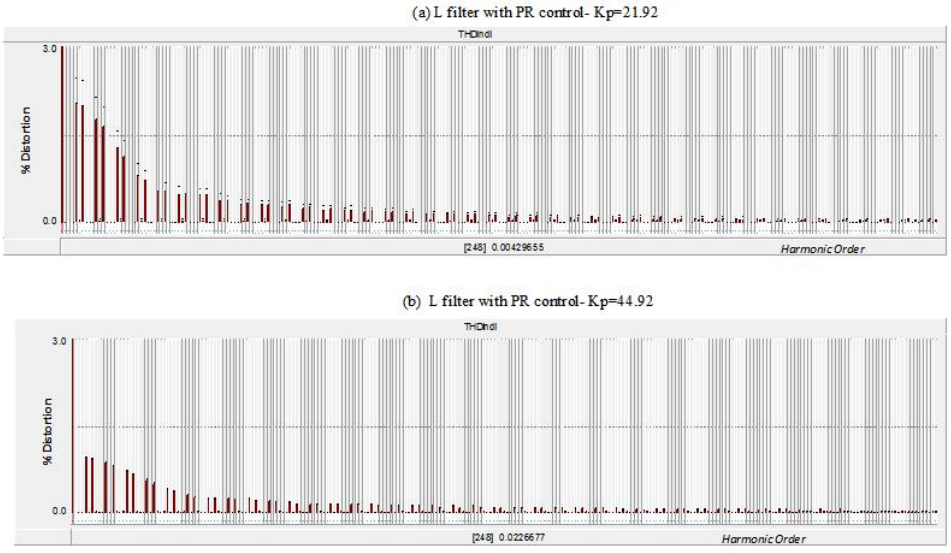
The grid current harmonic spectrum shown in Figure 3.29 reveals that, under high switching frequency operation, even the equivalent series resistance of filter parameters can limit the resonance and lower order harmonics to permissible limits, which avoids the additional losses with passive damping.

The study is extended with L filter configuration, a slightly higher value of total filter inductance is selected in this case, L = 0.005 H, excluding the grid self-inductance. PCC voltage and current waveforms for K_p = 21.2 and K_p = 44.92 are depicted in Figure 3.30(a). In this case, the designed value of K_p = 44.92 is preferable as it gives the minimum grid current THD of 2.47 %. The

harmonic spectrum for grid current is depicted in Figure 3.30(b). Decreasing K_p will decrease the bandwidth of the system in addition to the increased THD.



(a)



(b)

Figure 3.30: (a) PCC voltage and grid current with L type filter, (b) grid current harmonic spectrum with L type filter

It is evident that with K_p = 21.92, the lower order harmonics are dominant and thereby the THD in grid current spectrum is increased to 4.62 %. As expected, the higher order harmonics are within defined IEEE 519 limits.

3.4 Experimental Study

3.4.1 Analysis of CREE MOSFET Evaluation Kit in LTspice

Discretised SiC MOSFETs and diodes with a voltage rating of 1200 V are recently introduced commercially and the experimental kits are now available with half bridge configuration [135] - [137]. An evaluation kit KIT8020CRD8FF1217P-1 [135] manufactured by Cree is used to build the experimental prototype, which includes two Cree 80 mΩ, 1200 V CREE MOSFETs and two 1200 V, 20 A schottky diodes with associated gate drivers and power supplies. Cree has provided the analytical model of C2M0080120D and C4D20120D, which can be used as a building block for analysing the characteristics of newly industrialised SiC devices [136] - [137].

Double Pulse Testing

A double pulse test is conducted on LTspice to analyse the turn ON and turn OFF characteristics of Cree SiC MOSFET as shown in Figure 3.31 [138]. The analytical model of C2M0080120D and C4D20120D are used for the LTspice simulation. Since this simulation is based on the analytical model with parameters mentioned in the datasheet, an approximate evaluation of switching characteristics can be performed. The analysis is important in designing the switching frequency and setting dead time between upper and lower switches in a half bridge. An RC damper circuit is also provided to dampen the switching oscillations due to high frequency switching. A DC voltage of 500 V is applied to establish the desired

voltage.

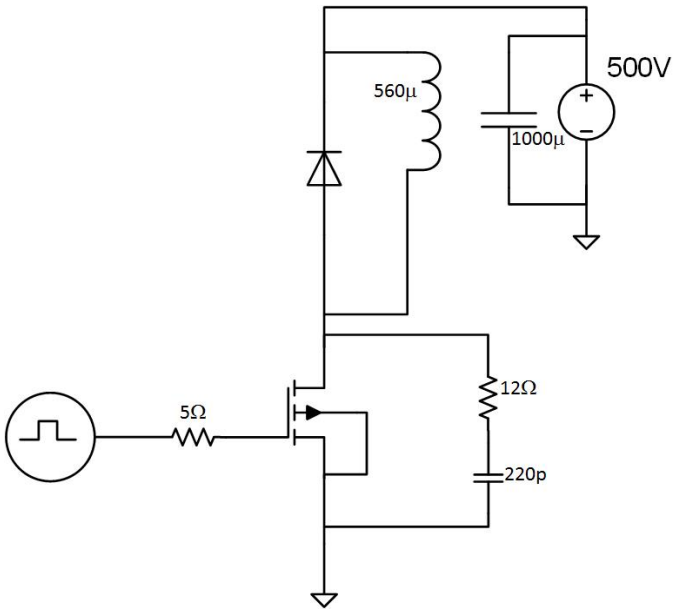


Figure 3.31: Double pulse testing circuit

It is evident from the gate voltage shown in Figure 3.32 that, two pulses are applied at the gate; the first pulse allows the inductor to build up the required current. At the end of the first pulse, drain current commutates from MOSFET C2M0080120D to freewheeling diode C4D20120D [136] - [137]. At this stage, the turn OFF characteristics can be analysed. Note that the first pulse lasts for 9.5 μs and a delay of 0.5 μs is allowed in between first and second pulse to ensure the voltage and current transients have been settled out. Since the turn ON and turn OFF time of C2M0080120D is in nanoseconds, 0.5 μs is enough, but in case of silicon IGBTS, this time has to be increased accordingly. The second pulse of 0.5 μs is applied at 11 μs. During this transition period, the turn off characteristics can be analysed and the drain current is commutated from freewheeling diode to SiC MOSFET. The waveforms for drain current I_d and drain to source voltage V_d are shown in Figure 3.32.

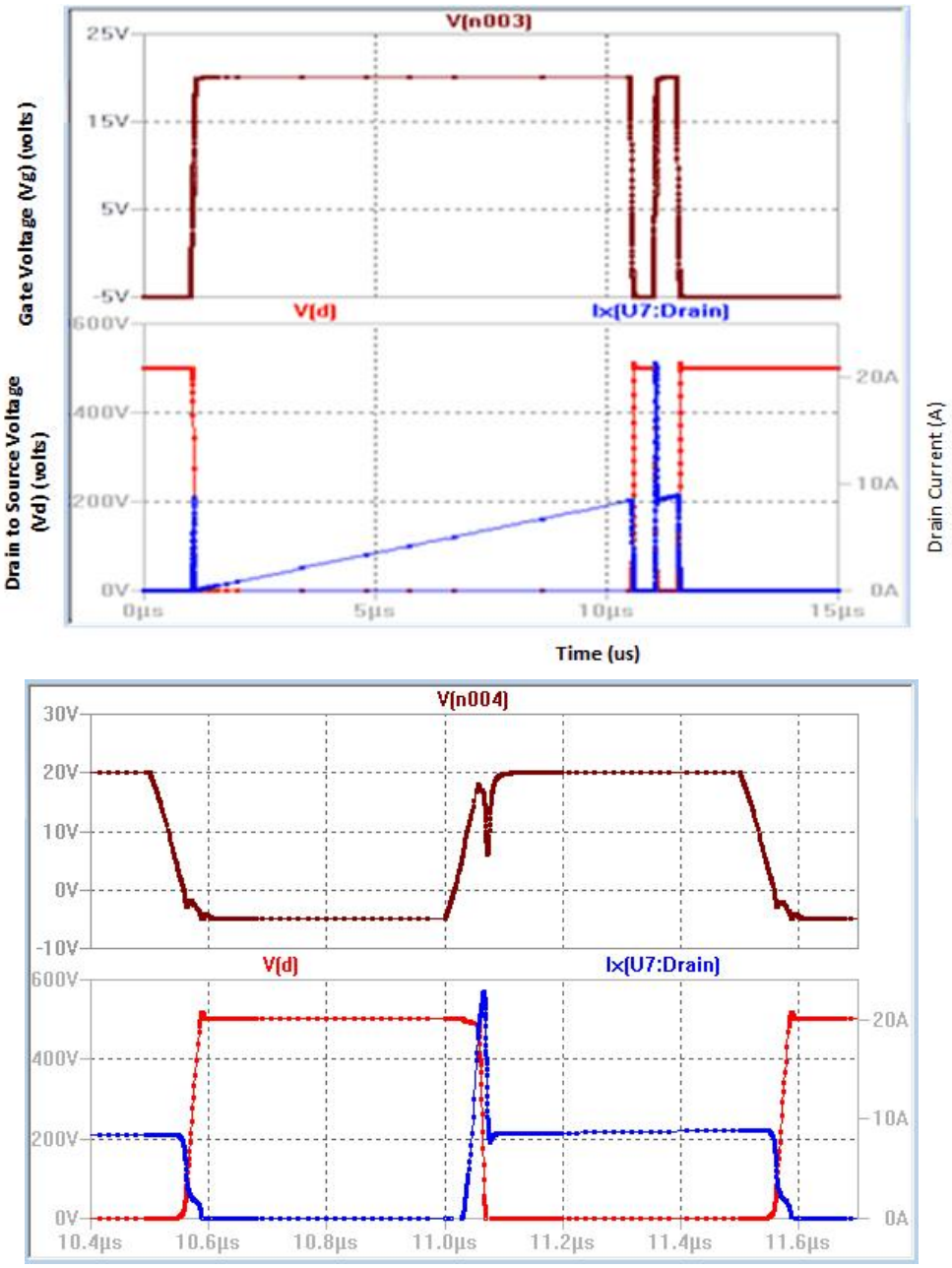


Figure 3.32: Double pulse testing-waveforms (gate voltage(brown), drain to source voltage(red) and drain current(blue))

SiC MOSFETs - Gate Driver Analysis

Isolated gate driver circuit and power supply are incorporated with CREE MOSFET Evaluation Kit KIT8020CRD8FF1217P - 1 [135] as shown in Figure 3.33. The gate drive requirements of SiC MOSFETs are different from traditional Si IGBTs. The positive threshold and negative bias of gate pulse are 19 V and -5 V respectively. Note that the turn OFF voltage is a negative voltage in contrast to 0 V in Si IGBTs. This leads to grounding issues unless otherwise fed with isolated gate driver circuits.

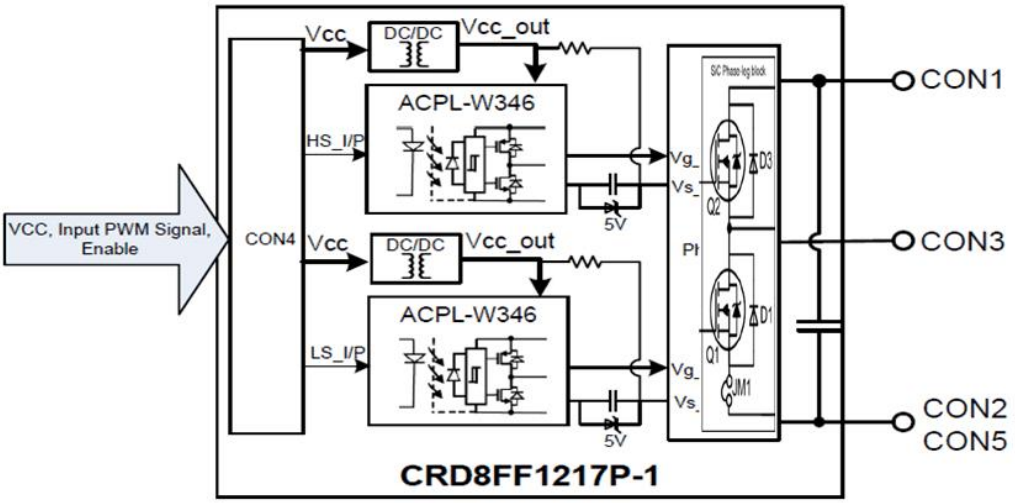


Figure 3.33: CREE MOSFET evaluation kit KIT8020CRD8FF1217P-1 [135]

The gate driver CRD8FF1217P - 1 consists of two isolated DC - DC converters - G1212S - 2W and two 2.5 A optocoupler integrated gate drivers ACPL - W346 for upper and lower switch of half bridge configuration [139] - [140]. G1212S - 2W converts 12 V DC voltage to 24 V with 6 kV DC isolation. A 5 V Zener is used to produce -5 V turn OFF voltage of SiC MOSFET. This negative turn OFF voltage aids lower switching losses and faster turn OFF. Gate resistors can control the switching transients and different turn ON and turn OFF resistances are chosen

in the board. Turn OFF resistance is smaller than turn ON gate resistor and this is achieved with the help of a diode. Decoupling capacitors provide the current during switching transients. Also, crosstalk suppression circuit can be adopted to further reduce the switching losses. Gate driver circuit is simulated in LTspice software to analyse the operation of gate driver board. The turn ON and turn OFF transients in upper switch gate voltage is illustrated in Figure 3.34. It is clear that turn OFF transients is more than turn ON transients due to the reduced value of gate turn OFF resistance. The asymmetry in gate resistance will ultimately result in reduced switching losses due to reduced overshoots in drain voltage and current.

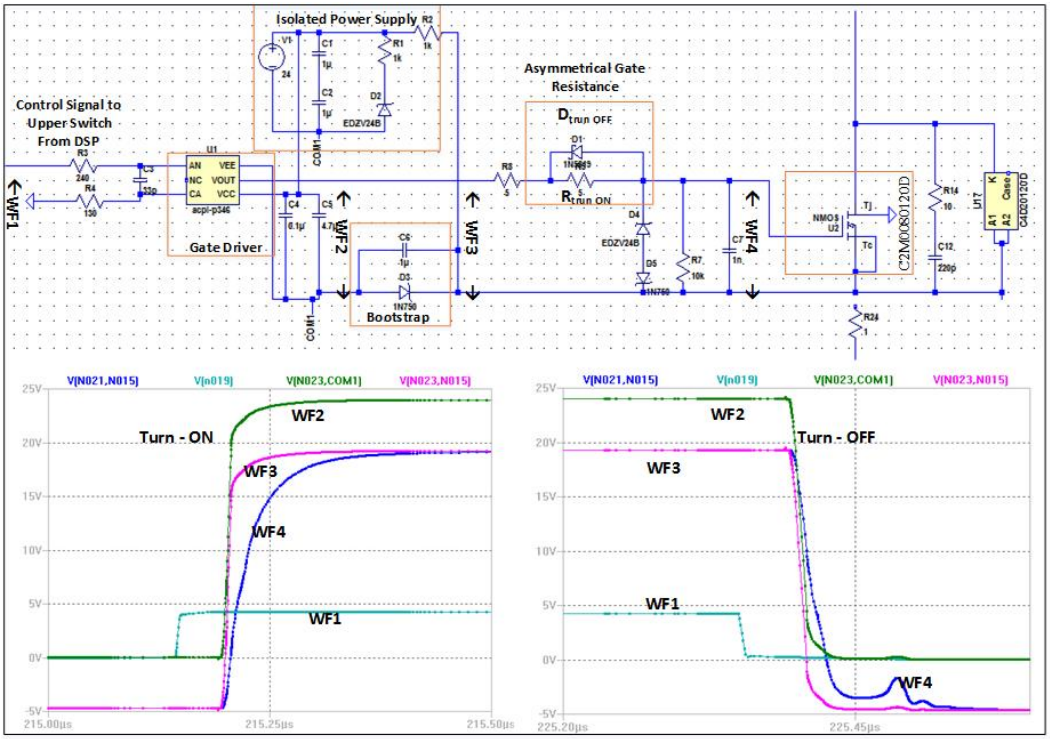


Figure 3.34: Gate driver circuit for SiC MOSFET (upper switch) and the measured waveforms at different instants

It is clear from Figure 3.35 that the input switching pulse has low and high state of 0 V and 4 V respectively. This has been converted to -5 V and 19 V by the gate driver board as the low and high state required for SiC MOSFET is -5 and +19 V

respectively.

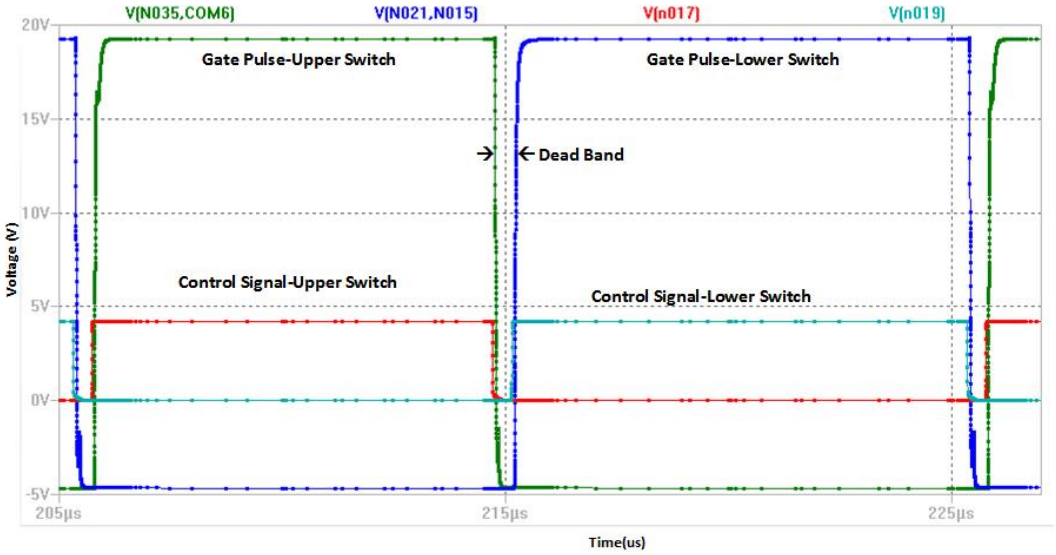


Figure 3.35: Gate driver- input signal from DSP processor and output signal to SiC MOSFET

Dead Band Implementation

It has been mentioned in the user manual that, the input pulse to the gate driver board should incorporate dead time. The purpose of Dead Band (DB) is to avoid short circuit between upper and lower switch pulses due to cross conduction between switches during turn OFF and turn ON process. Dead time can be implemented in the analog or digital domain. A schmitt trigger buffer IC - 74HCT125 along with an RC circuit can be utilized to provide dead band as shown in Figure 3.36. This will provide a blanking period between switching transitions by ensuring the complete turn OFF of upper switch before turning ON the lower MOSFET and vice versa. The dead time should be greater than the turn ON and turn OFF time of MOSFET. A higher value of dead band may result in an error in output voltage, so it has to be carefully designed. Here, the DB is selected by considering the switching characterisation using double pulse testing and datasheet. For LTspice

simulation, the dead band of 300 ns is generated using the analog method.

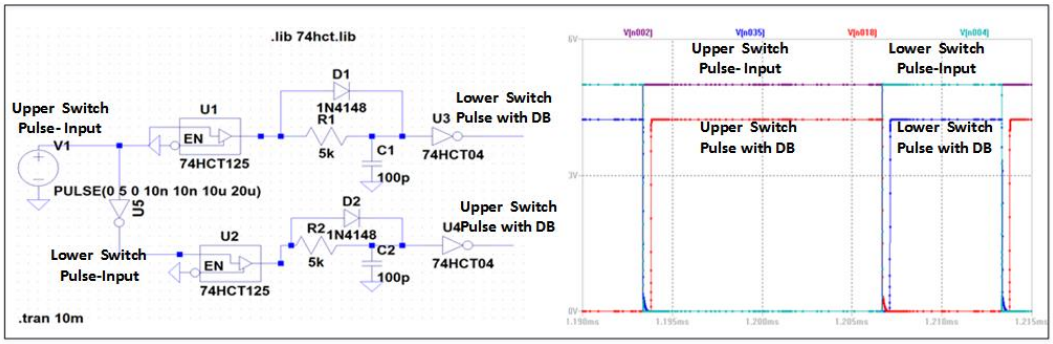


Figure 3.36: Blanking circuit and results for analog implementation

3.4.2 Experimental Prototype Implementation for Testing

An experimental prototype of H - bridge converter is built with CREE MOSFET Evaluation Kit KIT8020CRD8FF1217P - 1. Each kit can build a half bridge configuration using CREE SiC MOSFETs (C2M0080120D) with anti-parallel SiC schottky diodes (C4D20120D). For validating the theoretical findings and simulation results, a hardware prototype of single phase converter with an output filter is established as shown in Figure 3.37.

Figure 3.37: Photo of experimental set-up

Figure 3.38 depicts the functional block diagram representation, where the different blocks such as power circuit, gate drivers, control platform, and associated measurement and conditioning circuits are separately shown to demonstrate its functionalities.

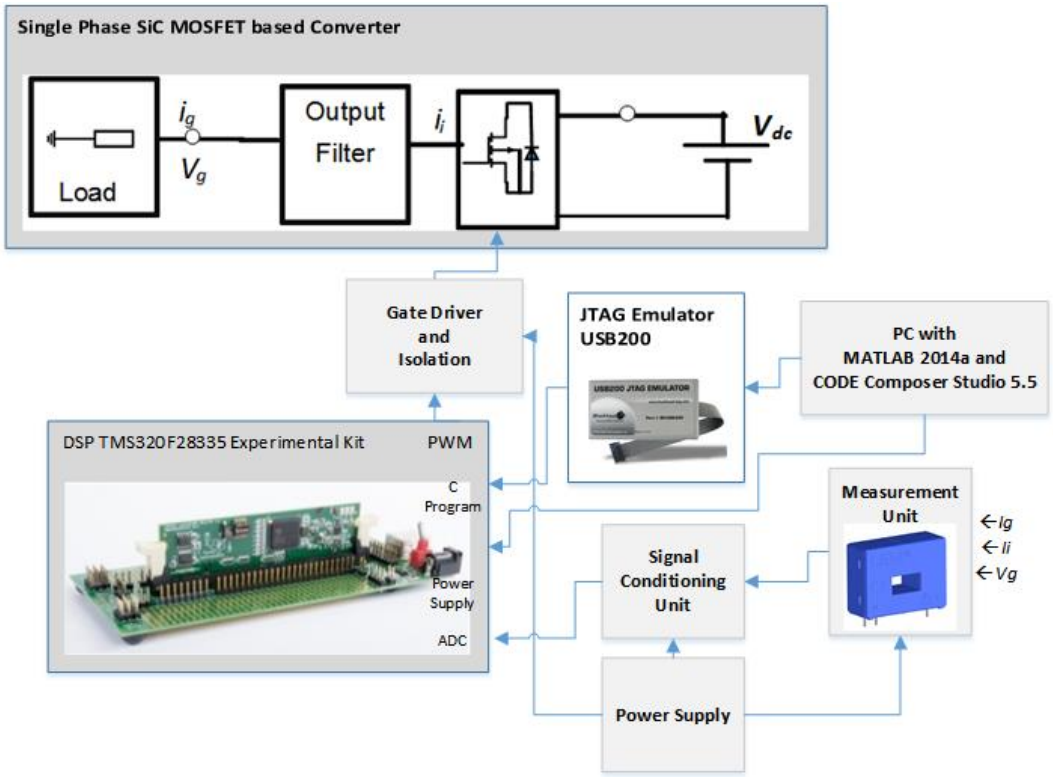


Figure 3.38: Experimental set up- block diagram

Power Circuit:

The converter is based on the Cree SiC MOSFET evaluation kit KIT8020CRD 8FF1217P-1. The kit consists of two Cree 80 mΩ, 1200 V CREE MOSFETs and two 1200 V 20 A schottky diodes. The gate driver circuitries and the isolated power supplies are incorporated in the board. Two such boards are used to build a single phase H-bridge configuration. DC supply from California Instruments-2253iX is chosen as a power source. An output filter of L or LCL type is constructed based

on the filter requirements. Converter side inductor is made up of square designed RM core which possesses the advantages of POT cores, in addition to the improved magnetic performance with minimum size.

Controller Implementation in DSP TMS320F28335 through automatic code generation from MATLAB

A Texas instruments digital signal floating point processor TMS320F28335 experimental kit is used to implement the control algorithms and PWM generation for the switching pulses [141] - [142]. TMS320F28335 is a 150 MHz 32 - Bit Processor and it is mainly used in prototyping power converter applications due to its attractive features such as IEEE - 754 Single-Precision Floating-Point Unit, 18 PWM Outputs, up to 6 HRPWM Outputs, up to 6 Event Capture Inputs, up to 2 Quadrature Encoder Interfaces, 2 CAN Modules, 3 SCI (UART) Modules and 16 Channels 12 - Bit ADC [141] - [145]. A Blackhawk XDS200 USB JTAG emulator is used to control the information flow between target processor and emulation hardware [146]. ADC channels and PWM outputs are mainly used for developing the control platform for prototype testing. The discretised controller is implemented in MATLAB/SIMULINK and the corresponding C - code generated is loaded into the DSP processor using code composer studio. ADCs incorporated in the DSP processor convert the measured analog signals to the digital domain. The sampling time of processor is set as 50 μs. The C program loaded in the DSP processor is generated from the Simulink block schematic created in MATLAB/Simulink. The necessary toolboxes used for automatic code generation are Simulink coder and embedded coder support package for Texas Instruments c2000 processors.

Texas Instruments TMS320F28335 Experimental kit is used to implement the control system for voltage source converter. The experimental kit is based on

TMS320F28335 processor mounted in the F28335 Delfino control card which is connected to the board through a DIMM connector. The board has an inbuilt USB100 emulator for code debugging and this can be connected to the computer through a USB cable in addition to the sufficient power supply from PC. The switching pulses for H bridge converter are generated using sinusoidal PWM. The triangular carrier waveform with a fixed frequency is generated using a Time Base Counter ($TBCTR$) configured in Up - Down mode. This means it starts counting from 0 to maximum value and then after reaching the maximum value, the counter will be going down in a reverse manner. The maximum value of the counter is stored in a timer base period register ($TBPRD$). PWM module can be configured using the following expression [143] - [144].

$$TBPRD = \frac{1}{2}\frac{T_{PWM}}{T_{SYSCLKOUT} \times CLKDIV \times HSPCLKDIV} \tag{3.23}$$

where $CLKDIV$ and $HSPCLKDIV$ are time base clock pre-scaler divider and high speed clock pre-scaler divider. Both are taken as 1 in this case. The factor 1/2 represents the up-down mode. As our aim is to generate the PWM pulse of 50 kHz or 10 kHz with the F28335 control card operating at $T_{SYSCLKOUT}$=$\frac{1}{150MHz}$, $TBPRD$ can be calculated as

for 10 kHz,

$$TBPRD = \frac{1}{2}\frac{150 \times 10^6}{50 \times 10^3 \times 1 \times 1} = 1500$$

for 50 kHz,

$$TBPRD = \frac{1}{2}\frac{150 \times 10^6}{10 \times 10^3 \times 1 \times 1} = 7500 \tag{3.24}$$

A dead band of 500 ns is generated using the hardware dead band unit of ePWM module. An Active High Complementary (AHC) operating mode with raising and falling edge DB period of 75 is chosen for dead band generation. A 50 kHz complementary switching pulses with software generated 500 ns dead band is

shown in Figure 3.39.

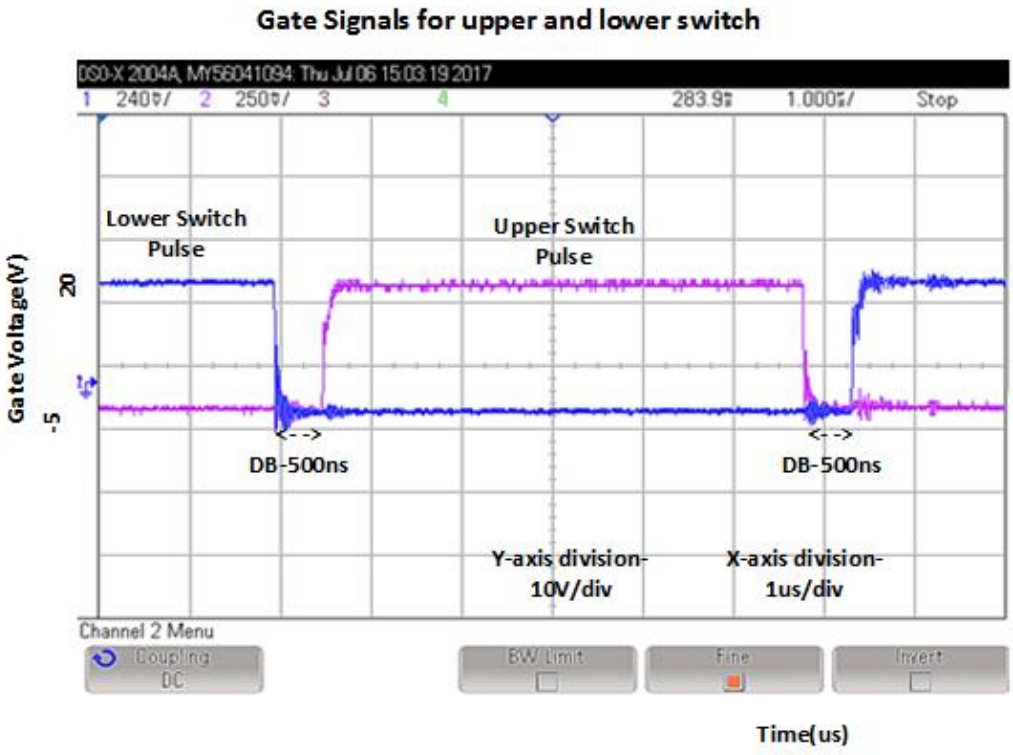


Figure 3.39: Gate signals for upper and lower switch incorporating dead band

Measurement and Signal Conditioning:

A four channel three phase IntegraVision power analyser - PA2203A is used to analyse and record the individual harmonics and waveforms [147]. Tektronix AC current probes (A621) are used to measure the currents and high voltage differential probe (P5200) are used to measure the gate and drain voltages of SiC MOSFETs [148] - [149]. LEM sensors LA 25 - P and LV 25 - P are used to measure the necessary voltage and current feedback signals for the controller [150]. The output range of measured signals is - 5 V to + 5 V. A conditioning circuit is used to condition the signals before feeding to DSP processor which accept signals in the range 0 to 3.3 V as illustrated in Figure 3.40 [151].

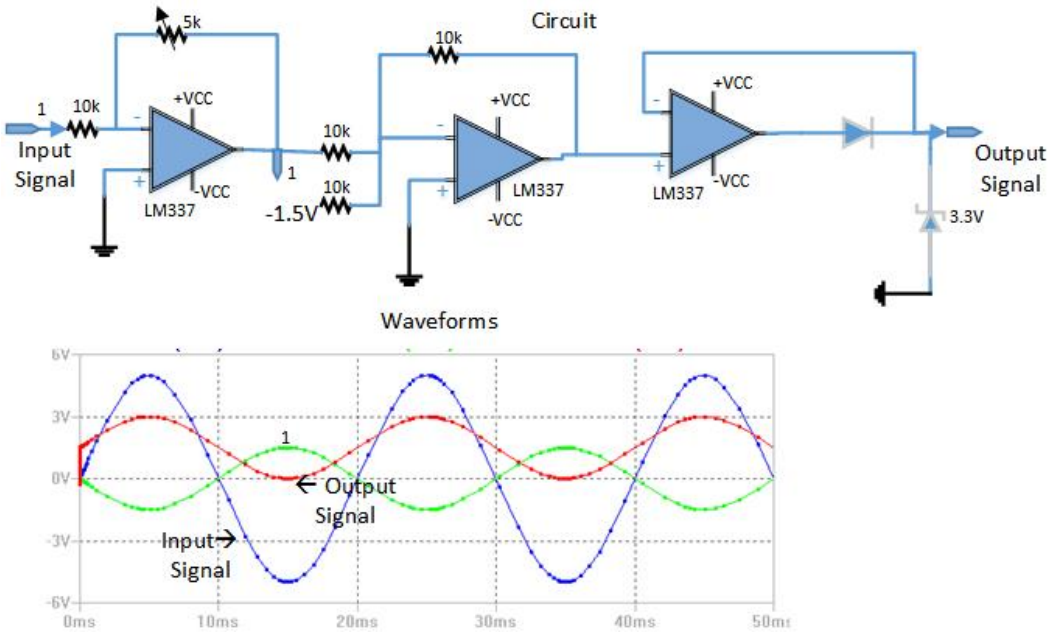


Figure 3.40: Signal conditioning circuit and obtained results

Gate Driver- Switching Characteristics

The driver circuit is also associated with the evaluation kit is tested to analyse the switching characteristics during turn ON and turn OFF process.

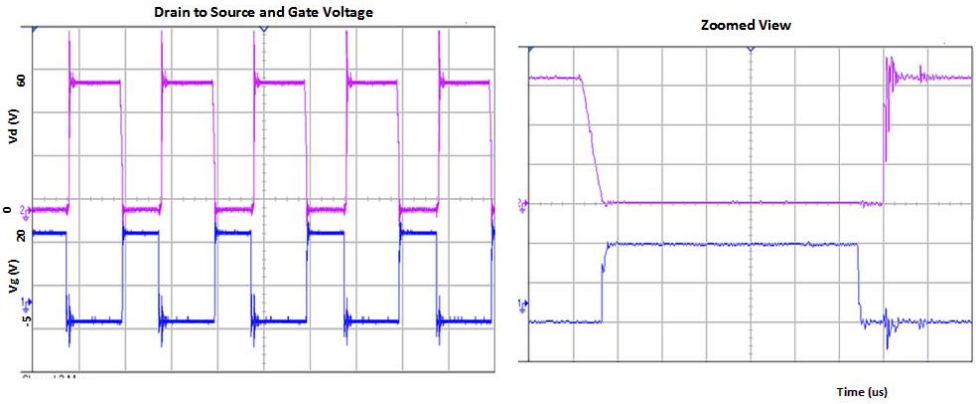


Figure 3.41: Transients in drain to source voltage and gate voltage during switching

Figure 3.41 shows the turn ON and turn OFF transients in the gate and drain voltages of upper and lower side MOSFETs. It is clear from the zoomed version of switching characteristics that turn on is faster than turn off process and this necessitates the inclusion of fixed dead time between complementary PWM signals. Although the switching ON and OFF transients of the individual switch is controlled using the proper design of gate drive and snubber circuits, the overshoot in lower side MOSFET drain voltage is more than 20 % during the turn ON process of the upper switch as depicted in Figure 3.42. Also, the asymmetry in the gate resistance turn ON and turn OFF process makes leads to the excessive transients in drain voltage during turn OFF. Note that turn ON resistance has a higher value than turn OFF resistance. This asymmetry in the gate resistors reduce the switching losses.

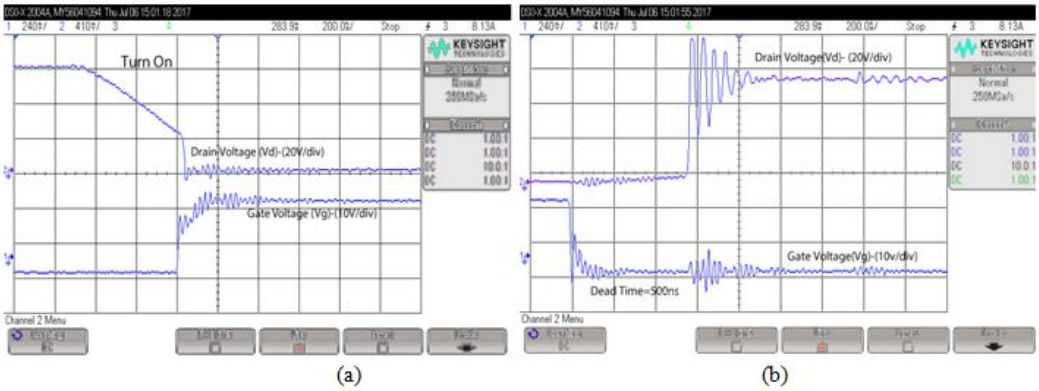


Figure 3.42: Switching characteristics (a) during turn ON (b) during turn OFF

3.4.3 Performance Analysis in PR and PRF Controlled Converter Current Regulated Grid Converters

In this section, the performance of PRF control over PR regulated converter current feedback control is evaluated using the experimental prototype of LCL type single phase converter. Filter parameters are chosen as per the design and it is given as L_i = 11 mH, L_g = 25 mH and C_f = 3 μF. The switching frequency is chosen as

f_{sw} = 10 kHz, and the resonant pole falls at 1.05 kHz. DC link voltage of 60 V is chosen. With the setup implemented, Figure 3.43.a shows the experimental results obtained for grid voltage, grid current and converter current with PR controller is used for the converter current regulation. It has already been evident from the simulation results that grid current has significant ripple content with PR control, which leads to higher harmonic distortion. Distortion in grid current ultimately resulted in distorted grid voltage. The similar up-shots are obtained from hardware where the grid variables are stable, but the current and voltage are significantly distorted. Although the dead time for SiC switches is in nanoseconds, its effect can be neglected. But, the effect of transport and sampling delay still influence the stability. In contrast, Figure 3.43.b verifies that the harmonic distortions in grid voltage and current due to lower order and resonant harmonics have kept within the acceptable IEC 61000.3.2 limits. Even though the resonant harmonics are partially damped by the equivalent series resistance of filter parameters, the lower order harmonics are further reduced by implementing PRF controller.

The individual harmonic analysis was conducted using power analyser as per IEC 61000.3.2 standards, which clearly verifies that dominant lower order harmonics are significantly reduced with PRF regulated converter. In addition, the grid voltage THD has decreased by 2.9 % in the proposed controller. Also, the higher order harmonics near resonant frequency are damped out by the modified controller. Moreover, the delay effects in system stability have been eliminated by the negative proportional feedback.

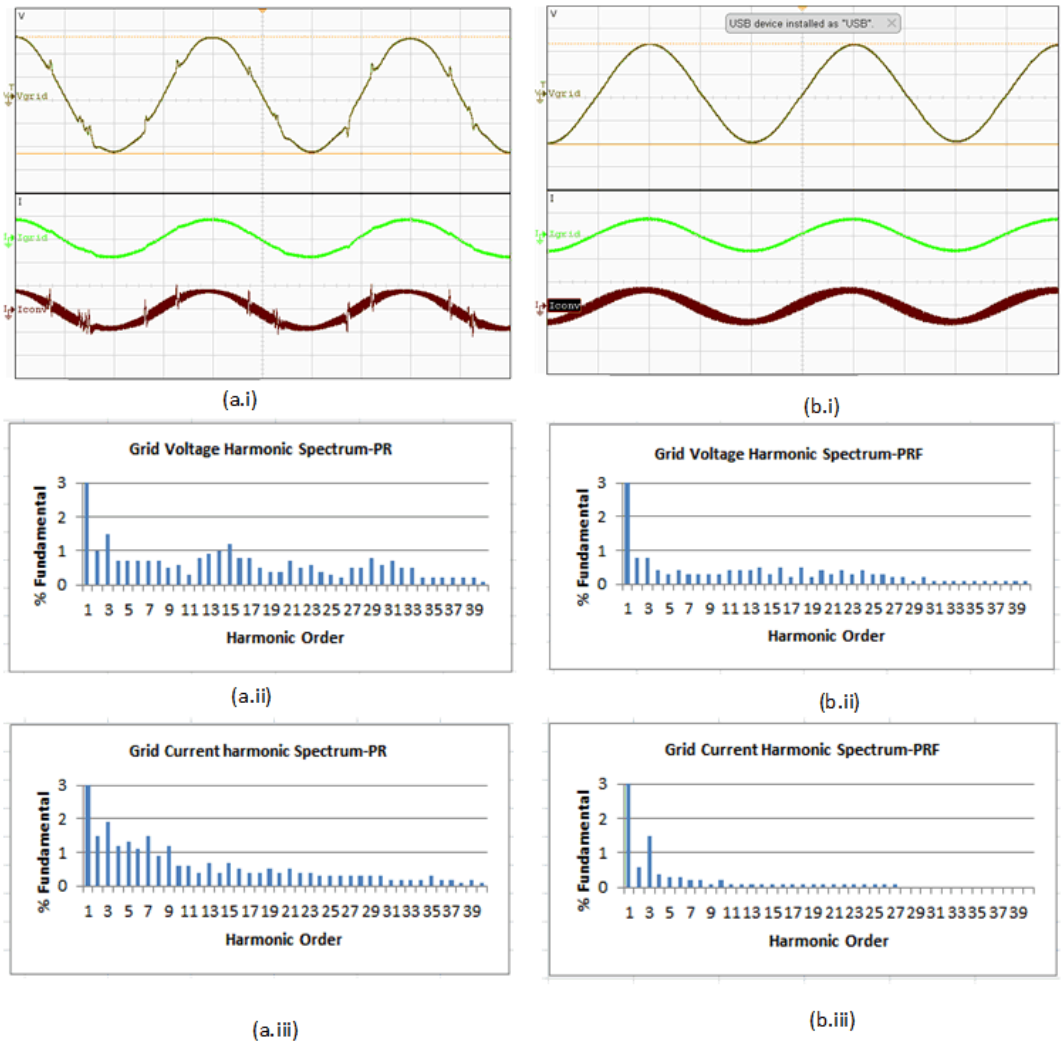


Figure 3.43: Converter current regulated system - output voltage - waveform (yellow - 20 V/div) and harmonic spectrum, converter current (red - 0.5 A/div), grid current - waveform (green - 0.5 A/div) and harmonic spectrum, time 5 ms/div (a) PR control (b) PRF control

3.4.4 Filter Requirements in High Frequency Grid Connected Converters

Single Phase H-Bridge Converter using Analytical Model of SiC Devices

A single phase H bridge converter is simulated in LTspice using the spice model of C2M0080120D and C4D20120D [152], which are available from Cree website. The spice simulation helps to analyze the effectiveness of different filter configurations in high frequency converter interfaced systems. The circuit shown in Figure 3.44 is assumed as an islanded grid and DC source considered as power from either battery source or from renewable energy source like PV. The switching pulses are generated using carrier based asynchronous PWM.

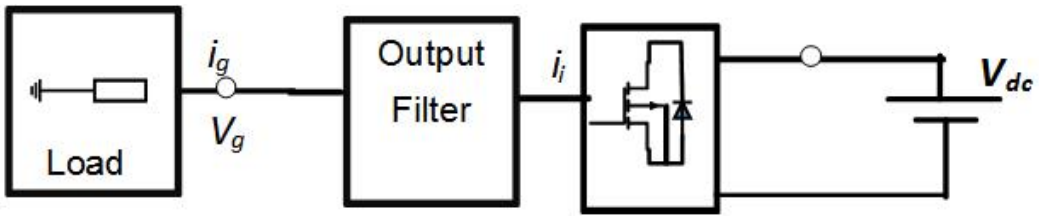


Figure 3.44: Single phase grid converter in islanded mode

A comparative study is performed at two different frequencies with LCL and L type filters. Initially, SiC MOSFETS are operated at 10 kHz switching frequency with LCL filter configuration. The filter parameters are L_i = L_g = 12 mH, C_f = 2 μF. Following, the switching frequency has increased to 50 kHz with reduced filter values of L_i = L_g = 2.3 mH, C_f = 1 μF. Then the filter capacitor is disconnected from the circuit to verify the effectiveness of L type filter at higher switching frequencies. Figure 3.45 represents the grid voltage and current waveforms obtained from LTspice simulation. It is evident from the results that, the L filter can sufficiently eliminate the switching frequency related harmonics, but the ripple contents in grid voltage and current waveforms are higher compared to LCL filter type. Even

though in stiff grids, the grid will keep the voltage distortion in acceptable limits, but a small value filter capacitor can only provide further ripple attenuation in weak grids and islanded grids.

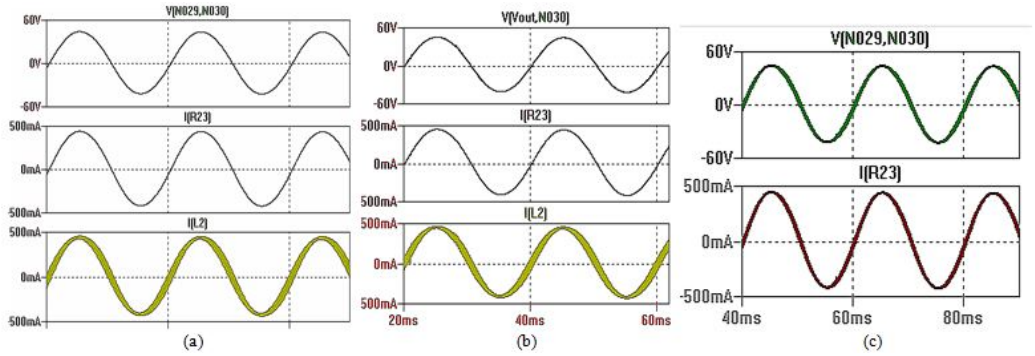


Figure 3.45: LTspice simulation of single phase converter - PCC voltage, grid current and converter current waveforms (red) (a) at 15 kHz with LCL filter (b) 50 kHz with LCL filter, (c) 50 kHz with L filter

Experimental Evaluation of Wide Band Gap Single Phase H-Bridge Converter

To compare and verify the effectiveness of LTspice simulation results with the practical conditions, an experimental prototype is implemented with SIC MOSFETs are Diodes. Figure 3.46 depicts the experimental results for grid voltage and current of a single phase H-bridge converter.

The results verify the efficient operation of high frequency single phase converter with reduced passive components. As evident from Figure 3.46.c that, the ripple percentage is more in grid voltage and current waveforms due to the lower attenuation capability of L filter. An increased value of inverter side inductor can further reduce the voltage ripple content in islanded grids, but a small value of filter capacitor is better considering the effective attenuation capability in LCL filters. Polypropylene film type capacitors (MKP62 275 AC) are used for filter

capacitance [153].

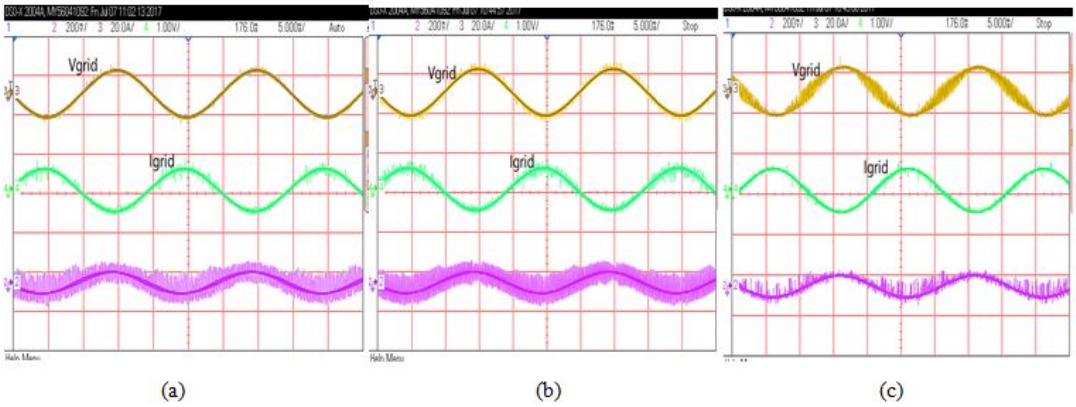
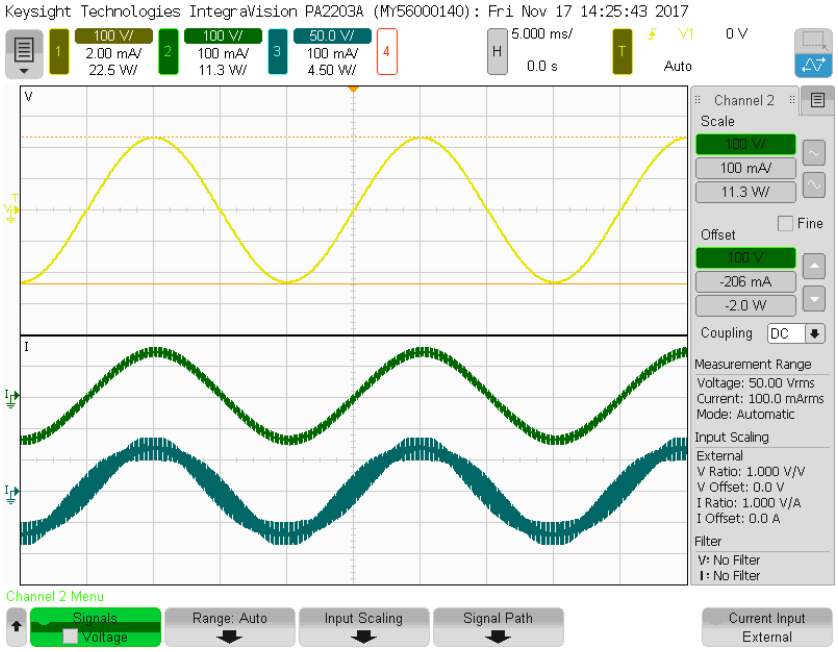


Figure 3.46: Experimental evaluation of single phase converter - PCC voltage - 50 V/div (blue) and grid current - 1 A/div(red) waveforms (a) at 15 kHz with filter values L_g = L_i = 7.8 mH, C_f = 2 μF (b) at 50 kHz with L_g = L_i = 2.2 mH, C_f = 1 μF (c) at 50 kHz with L_g = L_i = 2.2 mH

In order to evaluate the performance of SiC semiconductor based power converters at a relatively higher power rating and voltages, the input DC voltage and current is increased to 250 V and 1 A. The prototype is tested with LCL and L filter types at two different switching frequencies 10 kHz and 50 kHz. Higher order harmonics are analysed with a power system analyser, which is able to provide the harmonic distortion till order 40. Figure 3.47 shows the grid voltage, current and converter current at switching frequency 10 kHz. In this case, the filter values are L_i = L_g = 12 mH and C_f = 2 μF are chosen to effectively eliminate the ripples in grid side voltage and current.



(a)

(b)

Figure 3.47: Converter fed with LCL filter at 10 kHz switching frequency (a) PCC voltage, grid current and converter current, (b) grid current harmonic spectrum

As evident from the filter design, a reduced value of filter parameters L_i = L_g = 2.3 mH and C_f = 1 μF can be chosen with the increased switching frequency of 50 kHz. Figure 3.48 shows the obtained waveforms at grid and converter side. The harmonic spectrum for grid voltage and current are illustrated in Figure 3.49. Note that the power system analyser is capable of analysing the individual harmonics upto 40^{th} order. But at higher switching frequencies, the higher order harmonics may shift to high frequency range 2 - 150 kHz. This necessitates the need for high bandwidth power system analysers for measuring these harmonics. The major challenge in adopting high frequency converters are the unavailability of measurement devices and non-existence of standards in the above specified range. The increased high frequency oscillations in the power network will introduce EMI and communication issues.

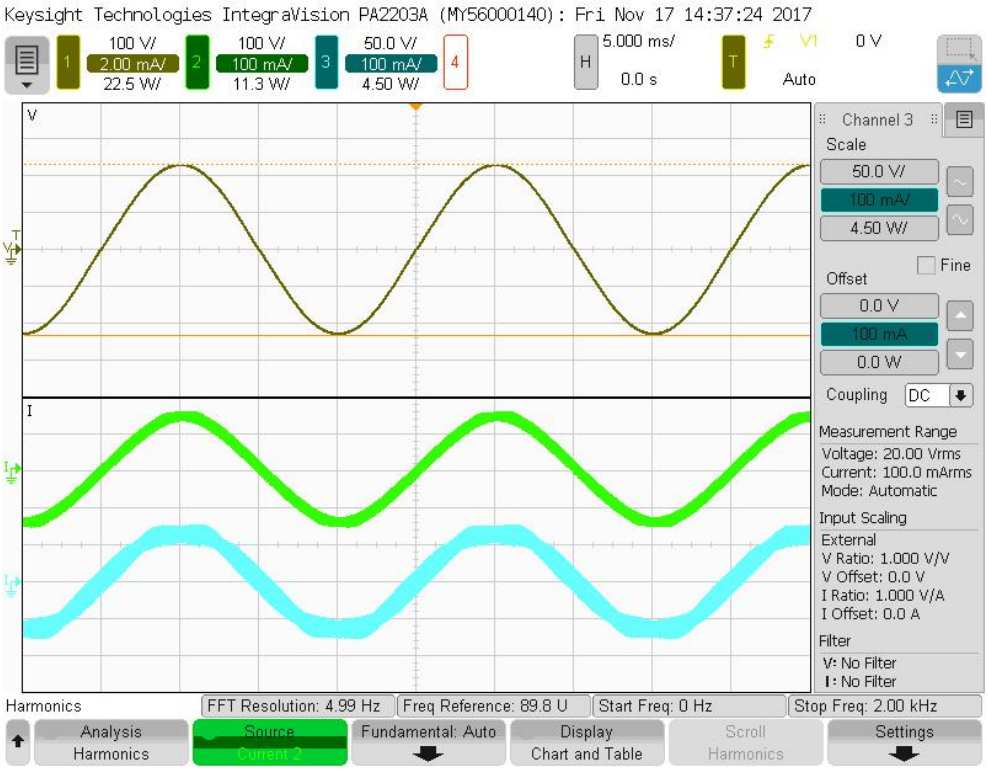
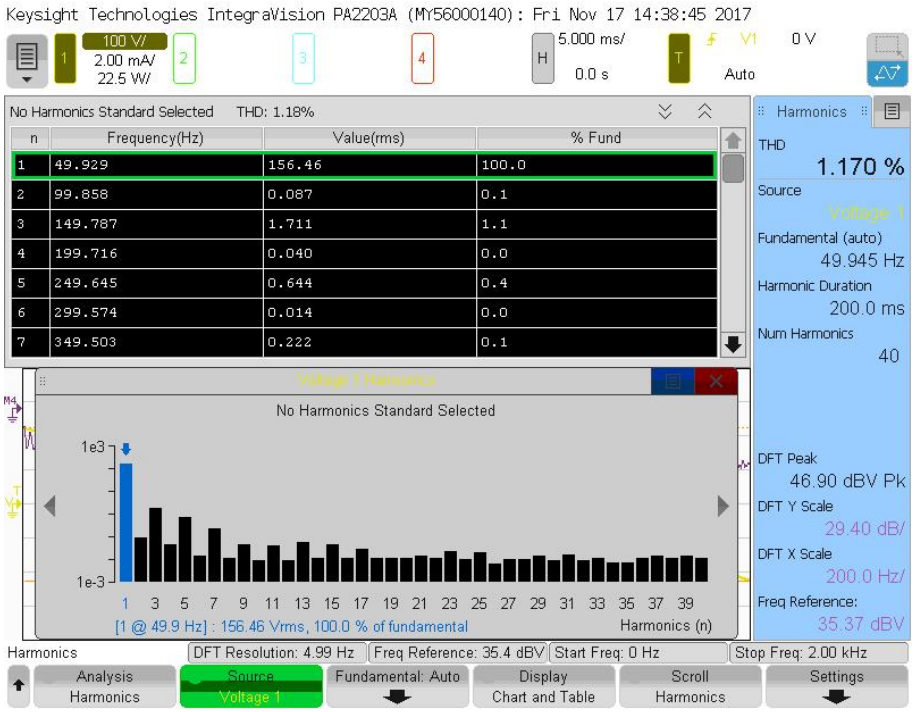


Figure 3.48: Testing with LCL filter at 50 kHz PCC voltage(brown), grid current (green) and converter current (blue)

(a)

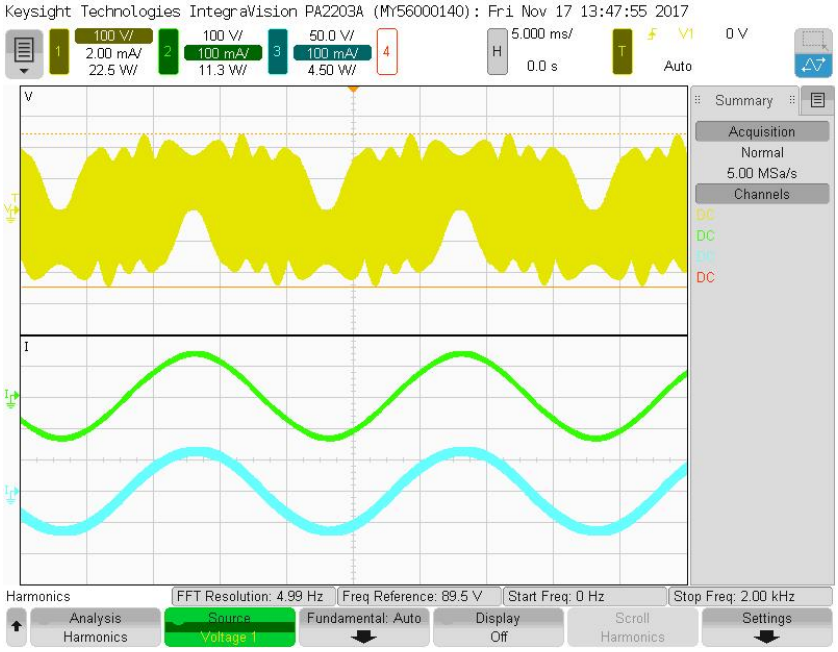


(b)

Figure 3.49: Harmonic spectrum - (a) grid current, (b) PCC voltage

But in this case, a simple L filter is found to be ineffective at 50 kHz with the same filter inductor values. The converter side filter value is now increased to 4.2 mH to analyse the effectiveness of L filter, and the obtained results are shown in Figure 3.50.

The ripple content in grid current is now reduced, but the voltage ripple content remains the same. This verifies the need for LCL filters in islanded grids or weak grids. In such cases, a small value of filter capacitor can effectively reduce the higher order harmonics as the capacitor provides low impedance path to higher order harmonics.



(a)

(b)

Figure 3.50: Testing with L filter at 50 kHz - (a) PCC voltage (yellow), grid current (green) and converter current (blue) (b) PCC voltage harmonic spectrum

3.5 Conclusion

This chapter presents the design and control implications of current controlled AFE operating at different frequency ranges. The comparative stability analysis of grid and converter current regulated grid connected AFE verifies that grid current regulated AFE is unstable unless otherwise incorporated any passive or active damping techniques. Even though narrowing the bandwidth of controller by reducing proportional coefficients or shifting resonant frequency to high frequency region can make the system stable, the individual harmonic distortion of higher order harmonics usually exceeds allowed limits. On the other hand, converter current regulated systems have inherent damping capability in all frequency regions due to resonant zeros; still, the higher order harmonics near resonant frequencies have to be kept within defined standards. Furthermore, the system delay has a negative impact on stability. These drawbacks have been overcome by the proposed PRF controller, where converter current negative feedback ensures adequate damping to resonant oscillations. The total harmonic distortion in grid current has significantly reduced to 1.8 %, whereas it was 4.51 % with PR regulated converter. This implies the delay effects are also nullified without any additional control or sensors. Simulation and experimental results validate the advantage of converter current regulation over grid current regulated AFE and verify the efficacy of proposed controller for converter current regulated systems. The latter section of this chapter dealt with the wide bandgap high frequency AFEs, its design, control challenges and stability issues. Increasing the switching frequency will reduce the filter requirements. The nature of higher order harmonics may differ in high frequency converters, where the resonant region will fall in the 2 - 150 kHz range. As the existing measurement devices are not sufficient to accurately record the data in this range, experimental analysis of individual harmonics is not possible. The harmonic and stability issues in high frequency converters are analysed using

computer simulation platform such as MATLAB and PSCAD [154], [155]. Grid current regulated PR controller with passive damping technique is found to be most effective under high frequency switching as the losses due to damping resistor is inversely proportional to the switching frequency. Thus the accumulated losses of SiC device based high frequency converters are comparatively lower than usual IGBT based converters. A physical prototype of single phase SiC MOSFET based converter is used to study the filter requirements under different frequency ranges.

Chapter 4

Improved Control Strategy for Accurate Load Power Sharing in an Autonomous Microgrid

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In Australia, the majority of the population is centered on urban areas. However, there are several remote communities dispersed throughout the land, which are supplied mainly by diesel generators or connected to the network through long distance transmission lines. However, the cost of network upgrade or transporting fuel to these areas is huge. State government and Transmission Network Providers (TNP) are aiming to invest in renewable energy sources like solar and wind along with battery storage units and interfacing converters [116] - [119]. These converter interfaced DGs, are the best candidates for angle droop control, which has a superior transient response and no steady-state frequency deviation. However, such a controller suffers from the effect of having the output inductance dictating the power sharing [30].

In this chapter, a new angle droop method is proposed to eliminate the dependence of the output inductance in angle droop control of an autonomous MG [156]. This is achieved by considering the magnitude and angle of the bus voltage

to which the DER is connected and it is downstream from the LCL filter. Real and reactive power sharing is achieved by modified angle droop and voltage droop respectively. A global clock signal is used to synchronise all DGs, which eliminate the necessity of costlier GPS communications. Furthermore, it eliminates the interactions between the decentralised droop control and the individual converter control. Stationary axis based non-ideal PR controller is used for bus voltage and converter current control due to its superior performance over synchronous axis-based PI control. The filter parameter and the inner current controller design discussed in Chapter 3 is followed in this chapter. The resonant frequency of each converter falls in the high-frequency region, which obviates the necessity of additional damping. Moreover, the choice of the converter current as feedback variable can be helpful in protecting the converter switches. The current controller reference is obtained from the voltage controller by exploiting the concept of similarity in the fundamental component of grid and converter currents. In addition, converter current control improves the reactive sharing among the DERs. Therefore, the new strategy is designed to eliminate the dependence of the output inductance on power sharing and also provide more accurate reactive power sharing. The accurate reactive power distribution is important in converter interfaced DGs since the converter output current depends on the square root of the sum of the active power squared and reactive power squared. Most of the materials of this chapter are taken from our published papers [156], [158].

4.1 Load Power Sharing by DGs in an Autonomous MG

Consider a simple islanded microgrid shown in Figure 4.1. In this, DG_1 and DG_2 are assumed to be voltage source converters fed by constant DC sources and the direction of power flow is as indicated in the figure. Here P_L, Q_L are the real and reactive load demand, P_{D1}, Q_{D1} and P_{D2}, Q_{D2} represent the active and imaginary

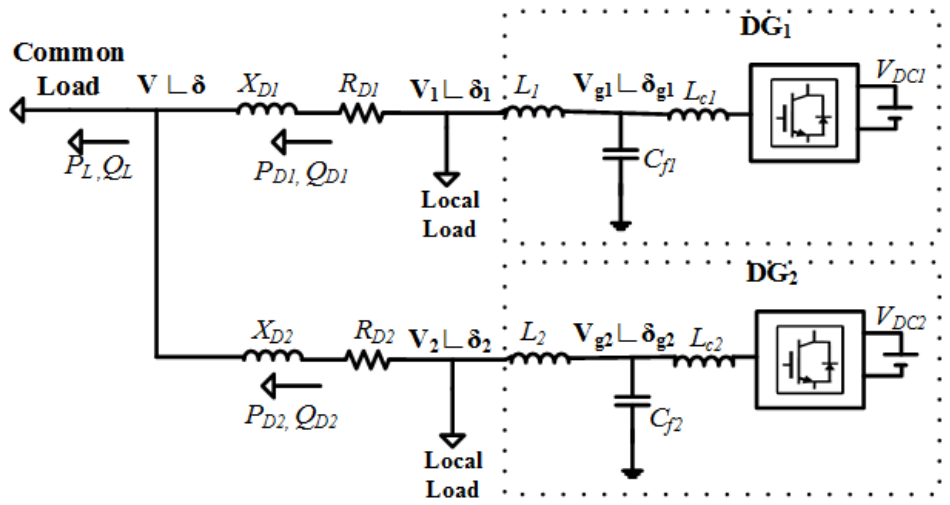


Figure 4.1: Schematic diagram of a simple islanded microgrid.

power delivered by DG_1 and DG_2 respectively to the common load, which is assumed to have inertial, passive (impedance) and non-linear characteristics. Bus voltages are denoted by $V_i\angle\delta_i$, while the voltage at output capacitor is denoted by $V_{gi}\angle\delta_{gi}$, i = 1, 2 for DG_1 and DG_2 respectively. The feeder impedance of DG_1 and DG_2 are defined as $R_{D1} + jX_{D1}$ and $R_{D2} + jX_{D2}$, L_1 and L_2 denote the output inductance. Here L_1, C_{f1} and L_{c1} constitute the LCL filter.

Considering power flow equation of DG_1, power flow to common load by DG_1 at PCC is given in (4.1).

$$P_{D1} + jQ_{D1} = V_1\angle\delta_1 \times \left\{ \frac{(V_1\angle\delta_1 - V\angle\delta)}{R_{D1} + jX_{D1}} \right\}^* \tag{4.1}$$

Upon simplification, P_{D1} and Q_{D1} can be expressed as

$$\begin{aligned} P_{D1} &= \frac{V_1[R_{D1}(V_1 - Vcos(\delta_1 - \delta)) + X_{D1}Vsin(\delta_1 - \delta)]}{{R_{D1}}^2 + {X_{D1}}^2} \\ Q_{D1} &= \frac{V_1[-R_{D1}Vsin(\delta_1 - \delta) + X_{D1}(V_1 - Vcos(\delta_1 - \delta))]}{{R_{D1}}^2 + {X_{D1}}^2} \end{aligned} \tag{4.2}$$

In order to simplify (4.2), we assume that the angle difference is relatively small, i.e.,

$$sin(\delta_1 - \delta) = \delta_1 - \delta,\ cos(\delta_1 - \delta)) = 1$$

Therefore, (4.2) can be rewritten as

$$P_{D1} = \frac{V_1}{{R_{D1}}^2 + {X_{D1}}^2}[R_{D1} \times (V_1 - V) + X_{D1} \times V \times (\delta_1 - \delta)]$$

$$Q_{D1} = \frac{V_1}{{R_{D1}}^2 + {X_{D1}}^2}[-R_{D1} \times V \times (\delta_1 - \delta) + X_{D1} \times (V_1 - V)] \tag{4.3}$$

In case of high X/R ratio feeder lines, R_{D1} can be assumed to be zero. Then, for small angle difference, (4.3) becomes

$$P_{D1} = \frac{V_1 V X_{D1}(\delta_1 - \delta)}{{Z_{D1}}^2} \Rightarrow P_{D1} \propto (\delta_1 - \delta)$$

$$Q_{D1} = \frac{V_1 X_{D1}(V_1 - V)}{{Z_{D1}}^2} \Rightarrow Q_{D1} \propto (V_1 - V) \tag{4.4}$$

It is clear from equation (4.4) that the active and reactive power requirements of the microgrid can be achieved by an outer loop controller, which droops the network voltage magnitude and angle on the basis of reactive and real control commands. Thus the decentralised voltage and angle droop for these two DGs, are defined as given in equations (4.5) and (4.6) respectively.

$$V_1 = V_{1rated} - n_1[Q_{D1rated} - Q_{D1}],$$

$$V_2 = V_{2rated} - n_2[Q_{D2rated} - Q_{D2}] \tag{4.5}$$

$$\delta_1 = \delta_{1rated} - m_1[P_{D1rated} - P_{D1}],$$

$$\delta_2 = \delta_{2rated} - m_2[P_{D2rated} - P_{D2}] \tag{4.6}$$

where $V_{1rated}\angle\delta_{1rated}$, $V_{2rated}\angle\delta_{2rated}$, and $V_1\angle\delta_1$, $V_2\angle\delta_2$ are the reference and measured values of DG_1 and DG_2 bus voltage magnitude and angle respectively, $P_{D1rated} + jQ_{D1rated}, P_{D2rated} + jQ_{D2rated}$, and $P_{D1} + jQ_{D1}, P_{D2} + jQ_{D2}$ are the real and reactive power rated and measured value of the two DGs; m_1, m_2 and n_1, n_2 are the angle and voltage droop control coefficients of the DGs. These are calculated as,

$$m_i = \frac{\Delta\delta_i}{\Delta P_i}, n_i = \frac{\Delta V_i}{\Delta Q_i}, i = 1, 2 \tag{4.7}$$

where Δ denotes the difference between the rated and measured values. It has been shown in [30] - [31] that by applying DC load flow with essential assumptions, the following equations can be obtained.

$$\delta_1 - \delta = \lambda_{D1} P_{D1}$$

$$\delta_2 - \delta = \lambda_{D2} P_{D2} \tag{4.8}$$

where $\lambda_{D1} = \frac{X_{D1}}{VV_1}, \lambda_{D2} = \frac{X_{D2}}{VV_2}$. The following assumptions are made,

$$m_1 \times P_{D1rated} = m_2 \times P_{D2rated}, \delta_{1rated} = \delta_{2rated} \tag{4.9}$$

Substituting aforementioned assumptions in (4.6) and (4.8) results in (4.10) and (4.11) respectively,

$$\delta_1 - \delta_2 = -m_1 P_{D1} + m_2 P_{D2} \tag{4.10}$$

$$\delta_1 - \delta_2 = \lambda_{D1} P_{D1} - \lambda_{D2} P_{D2} \tag{4.11}$$

Combining (4.10) and (4.11), the following equation is obtained.

$$\frac{P_{D1}}{P_{D2}} = \frac{\lambda_{D2} + m_2}{\lambda_{D1} + m_1} \tag{4.12}$$

It is clear from (4.12) that the real power sharing does not depend on output inductances of converter interfaced sources. In case of inductive lines, prior knowledge of line parameters will ensure proper load power sharing. But in case of MG placed in a small geographical area, line inductance values are negligibly small. Since $m_1 >> \lambda_{D1}$ and $m_2 >> \lambda_{D2}$, (4.12) can be rewritten as

$$\frac{P_{D1}}{P_{D2}} = \frac{m_2}{m_1} \tag{4.13}$$

The magnitude of the reference voltage can be obtained from voltage droop equation given in (4.5) and the corresponding droop coefficients are defined as mentioned in (4.14) .

$$\frac{Q_{D1}}{Q_{D2}} = \frac{n_2}{n_1} \tag{4.14}$$

Thus, the modified droop controllers $P - \delta$ and $Q - V$ can control the output voltage fundamental frequency and magnitude so that the real and reactive power sharing can be achieved without the knowledge of output impedance of individual converter and without the requirement of any communication medium to improve the sharing accuracy.

The schematic diagram of the control of an individual DG connected to the islanded MG is shown in Figure 4.2. The converter fed DER is connected to the PCC through an output LCL filter (shown inside the dotted rectangle). The control loop has three distinct components - the droop control, outer DG voltage control and the inner current control. These are discussed below:

Droop Control: The instantaneous values of active and reactive power at the PCC are measured. These measured values are passed through two Low Pass Filters (LPFs) to eliminate any ripple. These are then used in the droop control of (4.5) and (4.6) to produce δ_i and V_i. After determining the magnitude and angle of DG_1 output voltage, the reference voltage to the outer voltage control loop of

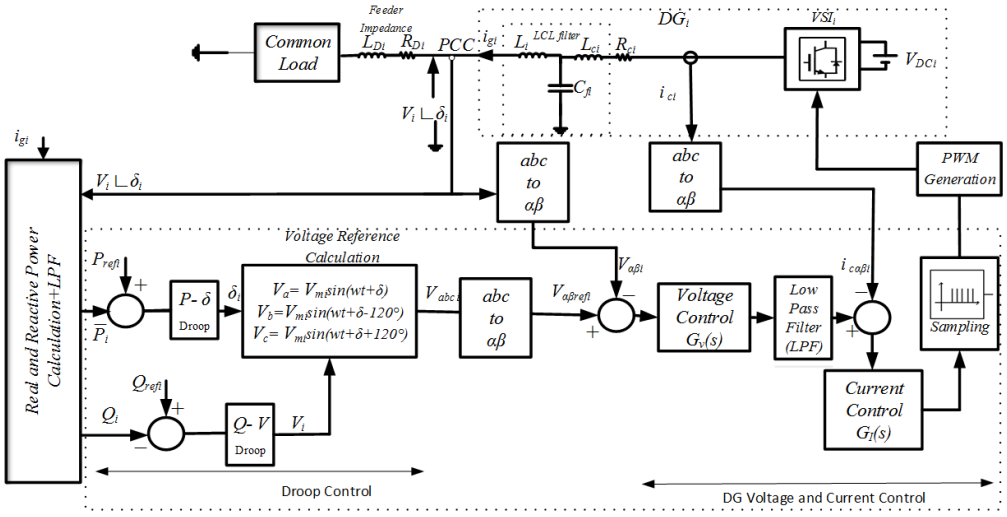


Figure 4.2: Control algorithm for an individual DG in islanded microgrid

DG_1 can be defined as given in (4.15),

$$V_{arefi} = |V_i|sin(\omega t + \delta_i)$$

$$V_{brefi} = |V_i|sin(\omega t - 120^o + \delta_i)$$

$$V_{crefi} = |V_i|sin(\omega t + 120^o + \delta_i) \tag{4.15}$$

where, ω is rated frequency in rad/s.

Voltage Control: The three-phase reference voltages are then converted into $\alpha\beta$ frame from their abc frame. The three-phase instantaneous measured voltages are also converted into $\alpha\beta$ frame. These are then compared and the error is given to the voltage controller, the transfer function of which is given by $G_v(s)$. A PR controller is utilized to implement voltage control and a harmonic term has been added to the voltage loop to enable more accurate reactive power sharing. This is discussed in the next section.

Current Control: The output of the voltage controller is then passed through a

low pass filter to obtain the reference for the inner converter current loop. This is then compared with the measured value of converter side current in the $\alpha\beta$ frame. The obtained error is fed to PR controller ($G_I(s)$) which outputs the modulation reference signal for PWM generation. The detailed analysis and design on voltage and current control for individual DGs are described in Section 4.2.

In a frequency droop control, the power generation depends on the frequency and hence if the droop gains are chosen properly, the frequency of the entire system remains the same. However, in an angle based control, the power flow depends on the relative angle difference between the DGs and hence they must be synchronized to a common reference frame. One of the options is the use of GPS signals, but it may be expensive. Assuming that a microgrid spans a smaller area, a simpler solution is to use a global clock that gets transmitted through fibre optic cables to each DG. The global signal can be transmitted at a slower rate in seconds or tens of seconds.

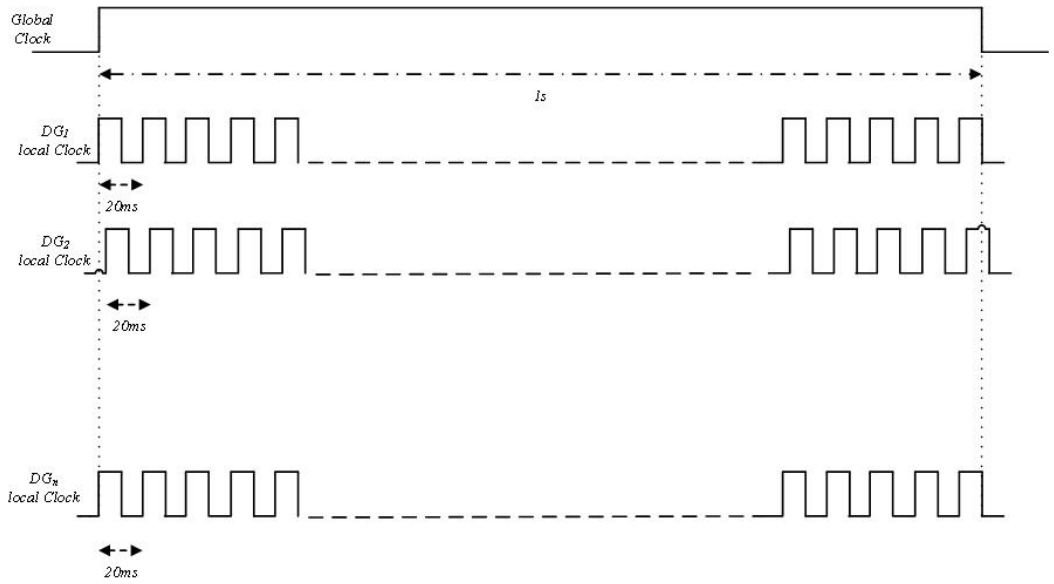


Figure 4.3: Synchronisation process in an islanded MG using global clock

Each DG is equipped with a local clock that generates 50 pulses every second as shown in Figure 4.3, assuming a fundamental frequency of 50 Hz. The angles are then calculated based on this local clock. Since angle droop method does not experience any frequency deviation and the microgrid operates at 50 Hz, the synchronization based on global and local clocks will be effective.

4.2 Voltage and Current Control of DGs in Islanded MGs

The voltage and current controller blocks are shown in Figure 4.4, where the transfer function of each block is also given. This figure illustrates the converter switching pulse generation scheme. Also included in this scheme is a Butter worth low pass filter and a PWM block. The functionality and design of each block are discussed below.

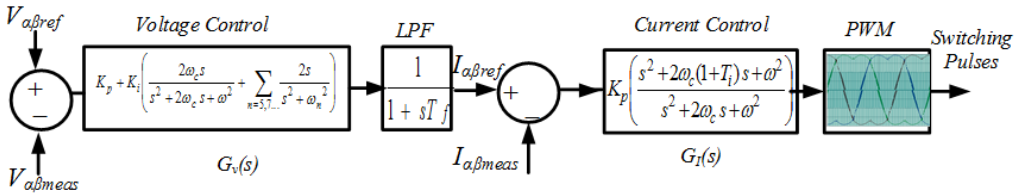


Figure 4.4: Voltage and current control of a DG in an islanded microgrid

The effectiveness of an ideal PR control for grid connected converters was discussed in Chapter 3. In the islanded mode of operation, a non-ideal PR controller is utilized for voltage and current control which is given by

$$G_c(s) = K_p + K_i\left\{\frac{2\omega_c s}{s^2+2\omega_c s+\omega^2} + \sum_{n=5,7..}\frac{2s}{s^2+\omega_n^2}\right\} \tag{4.16}$$

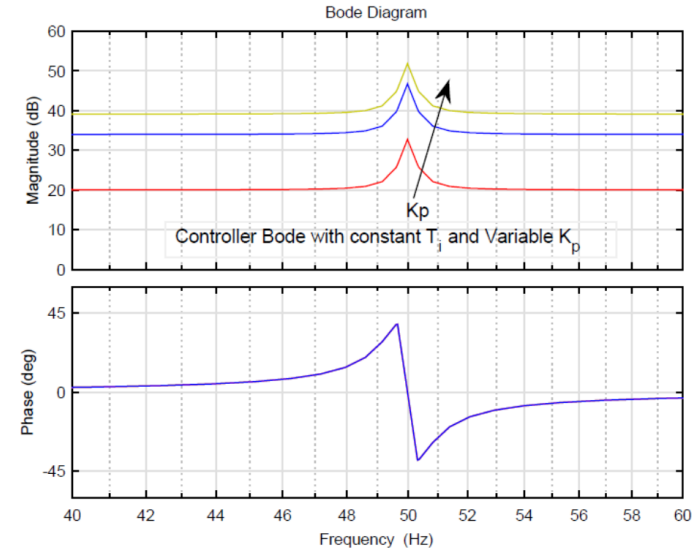
where, K_p and K_i respectively are the proportional and integral gains of the PR

controller and ω is the fundamental frequency. This control structure provides an infinite gain at the base frequency [19]. In voltage control, additional control for dominant odd order harmonics is provided to ensure the adequate harmonic control at PCC. Since the third order harmonics are eliminated by suitable PWM method, triplen harmonics are not included in the resonant controller.

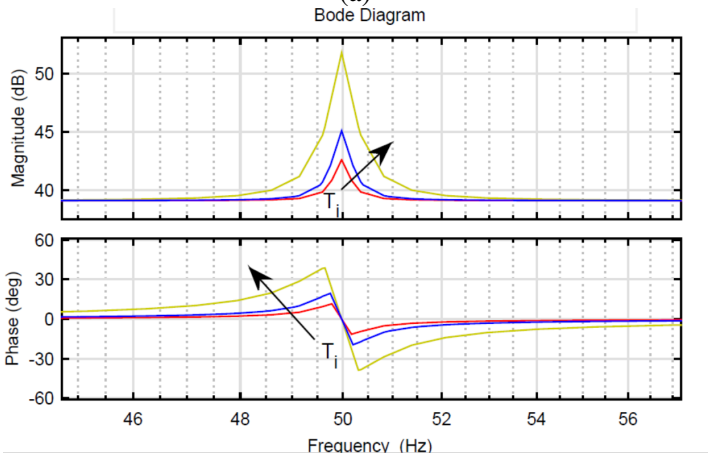
The output of voltage controller provides the reference for the grid side current. However, the aim is to control the converter current as it has the added advantage on the protection of converter module besides the inherent damping capability. Converter current is considered as the sum of the fundamental component and the switching frequency components and the LCL filter is designed in such a way that it can eliminate high frequency switching components from the converter current by passing the high frequency components through the filter capacitor. Thus the fundamental component of grid current is treated as converter current reference and it is obtained by passing the voltage controller output signal through a low pass filter which can reject high frequency signals and passes only the fundamental component. A first order Butterworth filter with a cut-off frequency equal to the fundamental frequency is used to separate the fundamental component and this method provides control over harmonic components as the high frequency signals are eliminated from converter current reference. The reference and measured quantities are converted into $\alpha\beta$ frame and the error is passed to the current controller. For the analysis purpose, the current controller transfer function can be rewritten as given in (4.17),

$$G_I(s) = K_p\left\{\frac{s^2 + 2\omega_c(1+T_i)s + \omega^2}{s^2 + 2\omega_c s + \omega^2}\right\} \tag{4.17}$$

where T_i is considered as the time constant and it is defined as $T_i = \frac{K_i}{K_p}$. Effect of control variables K_p, T_i and ω_c on the controller transfer function is analysed in the frequency domain as depicted in Figure 4.5.



(a)



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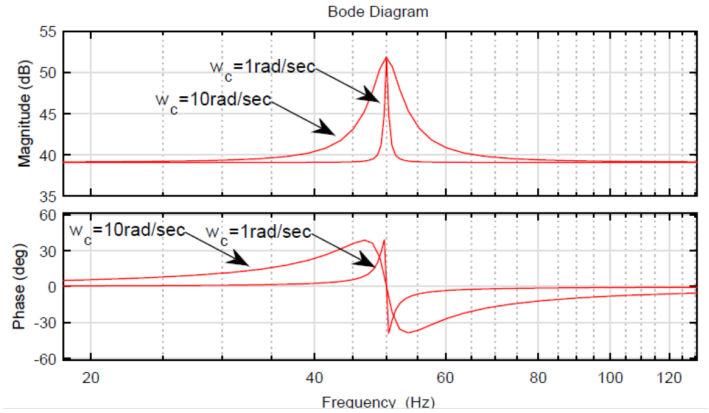


(c)

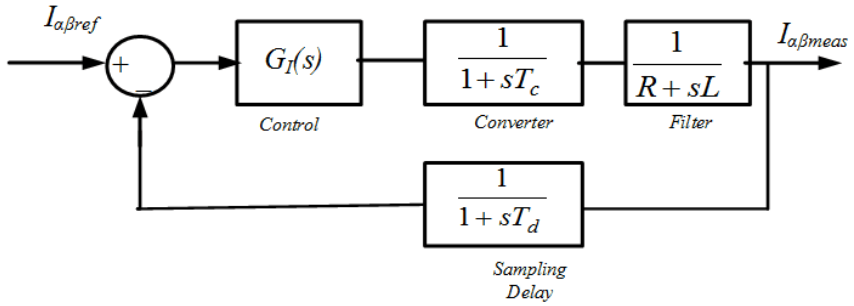
Figure 4.5: Controller Bode plots - effect of parameter variation (a)with constant T_i and variable K_p (b)with constant K_p and variable T_i (c)effect of ω_c

Conceptually, the procedure for obtaining K_p and T_i values are same as mentioned in Chapter 3, [20] and [23]. A more detailed analysis is performed here to find the optimum values of these parameters. The proportional gain K_p is taken as 10, 50 and 90, while keeping the resonant coefficient constant. The magnitude and the phase plots are shown in Figure 4.5(a). It is clear that with the increasing gain, the magnitude plot is shifted vertically upwards. This implies that the gain margin of the system increases with increase in K_p. Also, note that K_p has no impact on the phase plot. In contrast, T_i is taken as 0.6, 1, 10 for a constant value of K_p, has a direct impact on the magnitude and phase plots, as can be seen from Figure 4.5(b). Thus T_i has to be selected with a compromise between higher phase margins and steady state error. Therefore K_p is used to determine the gain margin of the system and T_i to eliminate the steady state error. The Bode plot of Figure 4.5(c) clearly illustrates the effect of ω_c on controller resonant part, where two value of ω_c are chosen (1 and 10 rad/s). As per the IEEE standards, grid frequency variation is restricted to 50 $\pm$ 0.5 Hz and ω_c is selected as π rad/s to achieve it.

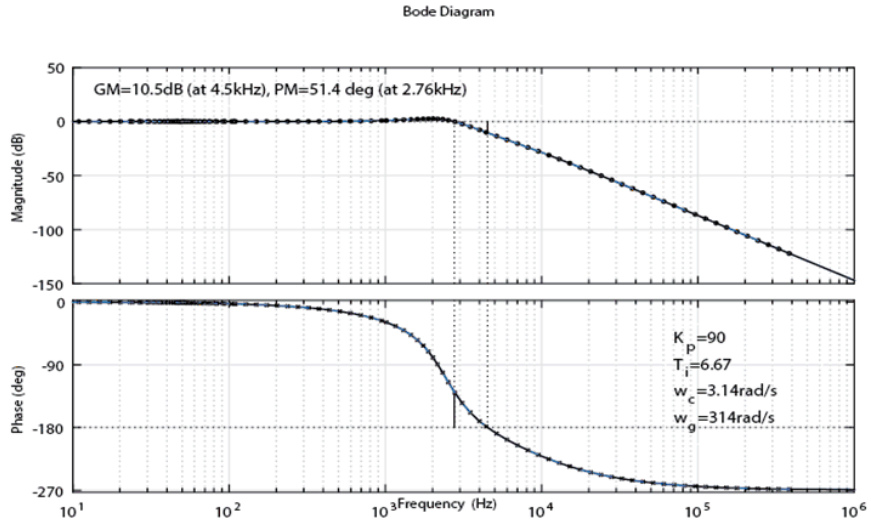
The details of the current control loop chosen in this study is shown in Figure 4.6(a). From control design point of view, the equivalent transfer functions of the LCL filter, converter and total delay can each be represented by first order systems [23]. Here the sampling time is taken as T_s = 0.5 T_{sw} , i.e., twice in a switching cycle, which has a time period of T_{sw} and a switching frequency of $f_{sw} = \frac{1}{T_{sw}}$. Even though, converter current feedback possesses an inherent damping capability, the delay in the system can affect this characteristic and can make the system unstable [78]. In order to overcome the stability issues from the delay, the total delay in system is taken as T_d = 0.5 T_s. For obtaining K_p and T_i values, classical control analysis is utilized [23], [157], where it is desired that the system will have a phase margin of at least 50° and a minimum gain margin of 10 dB. Closed loop Bode plot of the current control loop shown in Figure 4.6(a) is illustrated in Figure 4.6(b). With K_p = 90, T_i = 6.67 and ω_c = π rad/s, a phase and gain margin of 51.4° and

10.5 dB respectively are obtained.

Outer voltage control loop is slow compared to inner current control loop and the identical design procedure is followed to determine K_p and T_i (K_p = 0.79, T_i = 0.75) and the cut-off frequency is chosen as 0.2 Hz. The inner current loop should need higher bandwidth compared to outer voltage control loop. The resonant frequency f_{res} is selected inside the region $\frac{f_{sw}}{6} < f_{res} < \frac{f_{sw}}{2}$, so that the resonant frequency is outside the system bandwidth [21]. Filter parameters are designed to meet the above requirements as well as grid voltage and current standards. Modulation reference signal generated by the current controller is sampled with twice the switching frequency and carrier based asynchronous PWM is utilized for generating the switching signals for the IGBTs. A common mode third harmonic signal is superimposed with the sinusoidal modulation signal to effectively utilize the DC link voltage near rated operating conditions.



a



b

Figure 4.6: Current control loop design in discrete domain (a) equivalent circuit of current control loop (b) closed loop bode response

4.3 Simulation Studies

The proposed algorithm is validated using simulation studies on PSCAD/EMTDC. For simplicity, initial study is based on two DG system fed by constant DC sources. The system parameters under nominal operating conditions are listed in Table 4.1. Both DGs assumed to be of equal rating and expected to share the common load equally. To show the effect of output impedance on droop control, feeder

impedance of DG_1 and DG_2 are assumed as equal. PWM scheme chosen for DG_1 is third harmonic injected PWM, whereas sinusoidal PWM concept is utilized in DG_2. Accordingly, the output impedance of DG_1 and DG_2 is taken as 3.3 mH and 4.5 mH respectively.

Table 4.1: System under simulation study

System Parameters	**Values**
PCC Line to Line Voltage	1.1 kV
System Frequency	50 Hz
DG_1 Feeder Impedance	0.01+j1 Ω
DG_2 Feeder Impedance	0.015+j0.15 Ω
X/R Ratio	10
Load	P + jQ (P-kW, Q-kVAR)
Impedance Load	22.45 + j2.9 Ω
Nonlinear Load	9.4 + j0.7 Ω
Inertial Load	30 HP Induction Motor
Converter and Filter	
Filter Capacitor	5 μF
Converter Side Filter Inductor	DG_1-3.2 mH, DG_2-4.3 mH
Grid Side Filter Inductor	DG_1-3.3 mH, DG_2-4.5 mH
Switching Frequency	10 kHz

Angle and voltage droop coefficients are designed based on DG rating and droop control output voltage is taken as the bus voltage of DGs. Real, reactive and harmonic power sharing among DG_1 and DG_2 is shown in Figure 4.7. Different

types of loads are applied at different time instants to validate the performance of the proposed algorithm. At the beginning the system operates only with a passive impedance load. Then at 1 s, the nonlinear load is switched on, following which, the inertial load is switched on at 2 s. Due to similar angle and voltage droop characteristics and rating, DG_1 and DG_2 share the real and imaginary power equally and the difference in output impedance of VSCs has no impact on power sharing. It is interesting to note that the harmonic power is shared equally without any additional control loops.

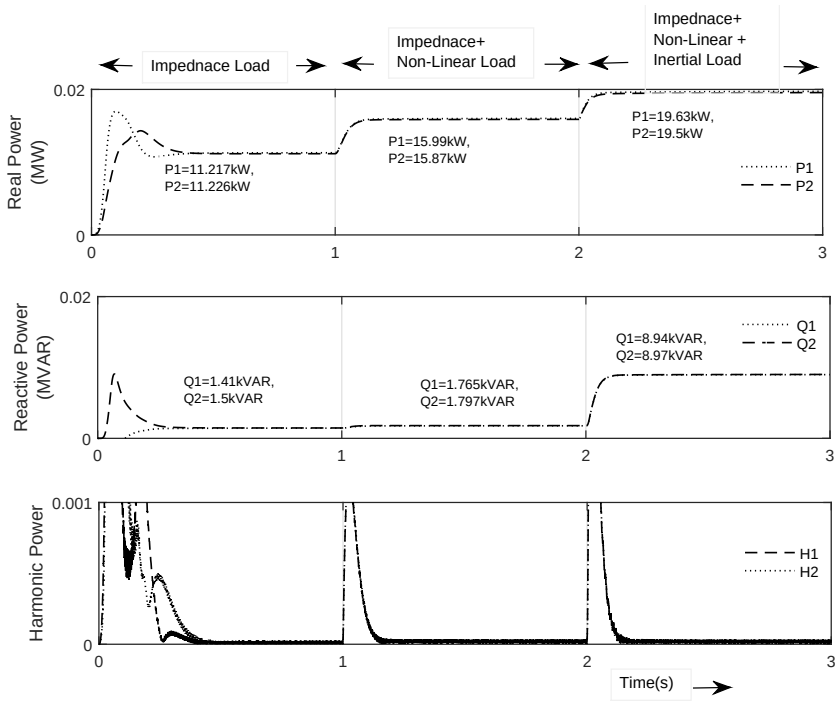


Figure 4.7: Load power sharing among DG_1 and DG_2 with the proposed control

In order to compare the results with a conventional angle droop, the same load pattern and the output inductance as the previous example are chosen. Also, the same droop coefficients are chosen as in the previous example. Note that for this case, the voltage of the filter capacitor is taken as the droop control variable. The

results are depicted in Figure 4.8. It is evident that the power sharing, in this case, is

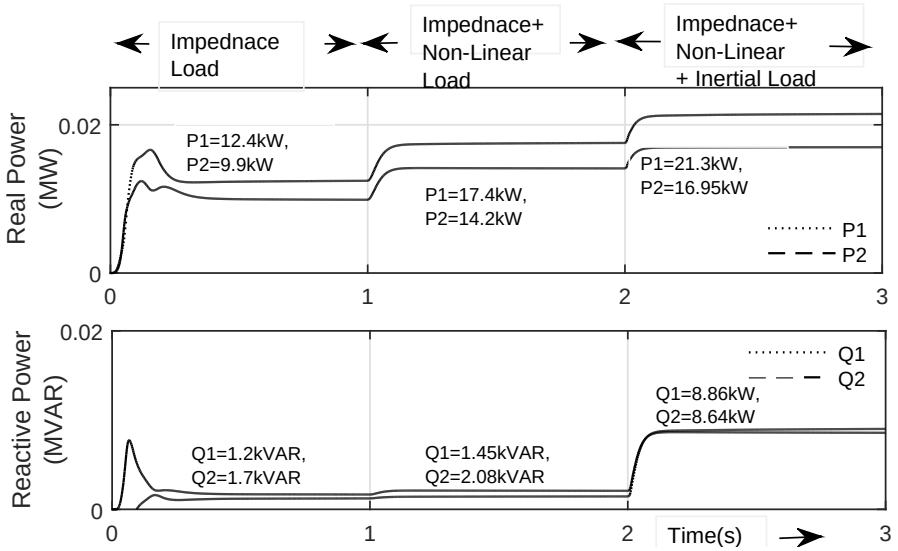


Figure 4.8: Load power sharing with conventional angle droop control

poor as the droop gains chosen cannot overcome the effect of the output inductance.

The results of the previous two simulation studies (Figure 4.7 and Figure 4.8) are listed as Case I in Table 4.2. Now to examine the impact of feeder impedance on the angle droop control, the feeder impedance of DG_1 is taken as twice that of DG_2. Again the performance of the proposed method ($V_{ref} = V_i \angle \delta_i$) is compared with that of the conventional droop control ($V_{ref} = V_{gi} \angle \delta_{gi}$).

For Case II in Table 4.2, the low angle droop coefficients are considered ($m_1 = m_2 = 0.057$). It can be seen that the load power sharing is slightly degraded in the proposed method. However, in the conventional method, a change in feeder impedance does not show strong impact, since the feeder impedance is much higher than the output impedance.

The accuracy of power sharing with both these methods improves with higher droop gains ($m_1 = m_2 = 0.57$) (Case III). Even though, higher droop gains can improve the load sharing accuracy, it can have an impact of the system stability, as has been mentioned before. The average percentage deviation in rating based

Table 4.2: Real power sharing among DG_1 and DG_2 under different scenarios

	Time	Case I		Case II		Case III	
Feeder Impedance		DG_1 Z_{D1}	DG_2 Z_{D1}	DG_1 Z_{D1}	DG_2 $2\times Z_{D1}$	DG_1 Z_{D1}	DG_2 $2\times Z_{D1}$
Droop Coefficient		m_1 0.057	m_2 0.057	m_1 0.057	m_2 0.057	m_1 0.57	m_2 0.57
Real Power (kW)		P_1	P_2	P_1	P_2	P_1	P_2
Proposed Method	0-1s	11.217	11.226	10.96	11.4	11.02	11.47
	1-2s	15.99	15.87	15.5	16.3	15.65	16.23
	2-3s	19.63	19.5	18.92	20.26	19.13	20.04
Conventional Method	0-1s	12.4	9.9	12.1	10.2	11.8	10.4
	1-2s	17.4	14.2	17	14.6	16.7	14.8
	2-3s	21.3	16.95	20.64	17.51	20.3	17.8

active power sharing under aforementioned conditions are depicted graphically in Figure 4.9, from it can be seen that the deviations with the proposed method are much smaller compared to those with the conventional method.

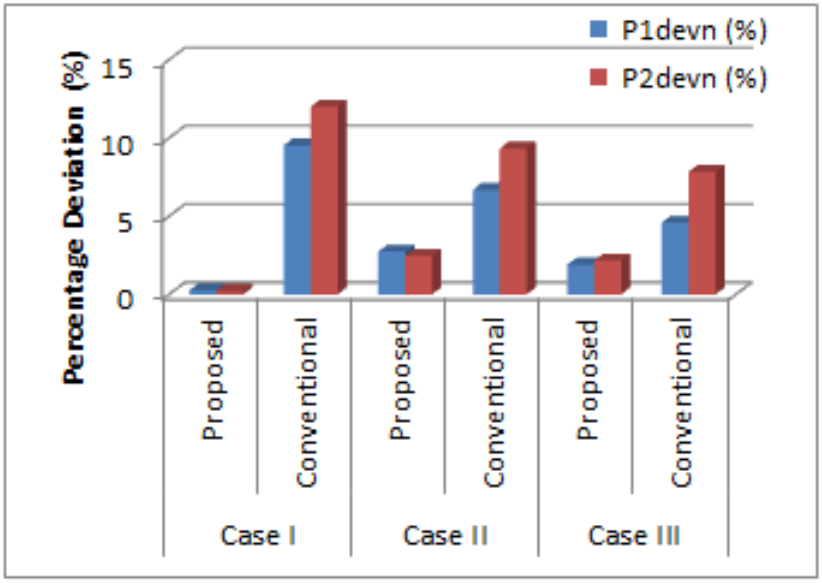


Figure 4.9: Comparative study between proposed and conventional method

Frequency deviation is found to be within the acceptable limits (Figure 4.10), as ω_c for the voltage control loop is chosen as 50 ± 0.2 Hz. Significant frequency excursions occur during load changes and the steady state frequency deviation is negligible.

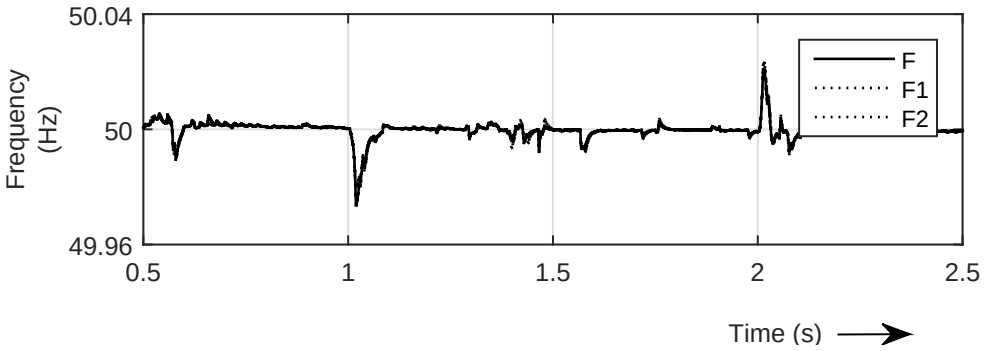


Figure 4.10: Grid and DG frequency variations

The results for load voltages, currents and phase - a DG currents with the proposed control of Figure 4.7 are shown in Figure 4.11(a). The circulating current between DGs is found to be negligible. The load voltage THD is obtained as 1.49% whereas DG_1 and DG_2 current distortions are 4.3 % and 4.89 % respectively. Individual converter current and bus voltage control are shown in Figure 4.11 (b), in which the three phase measured quantities exactly follow the reference values. Furthermore, the control of harmonic components by the DG voltage control algorithm results in lesser voltage distortion in addition to the effective sharing of reactive and harmonic power.

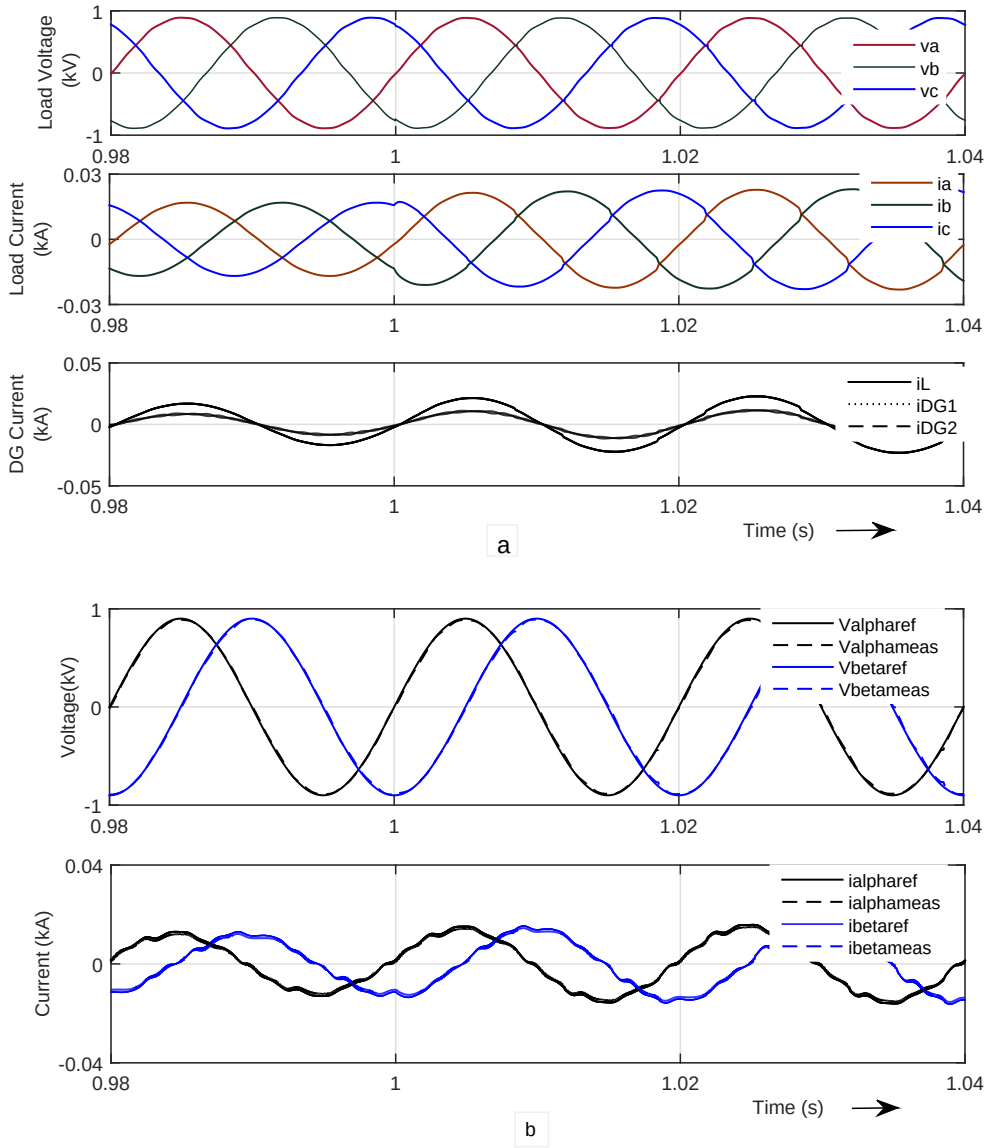


Figure 4.11: Voltage and current waveforms using proposed method (Case I) (a) Load voltage, load current and DG currents (b) DG voltage and current control

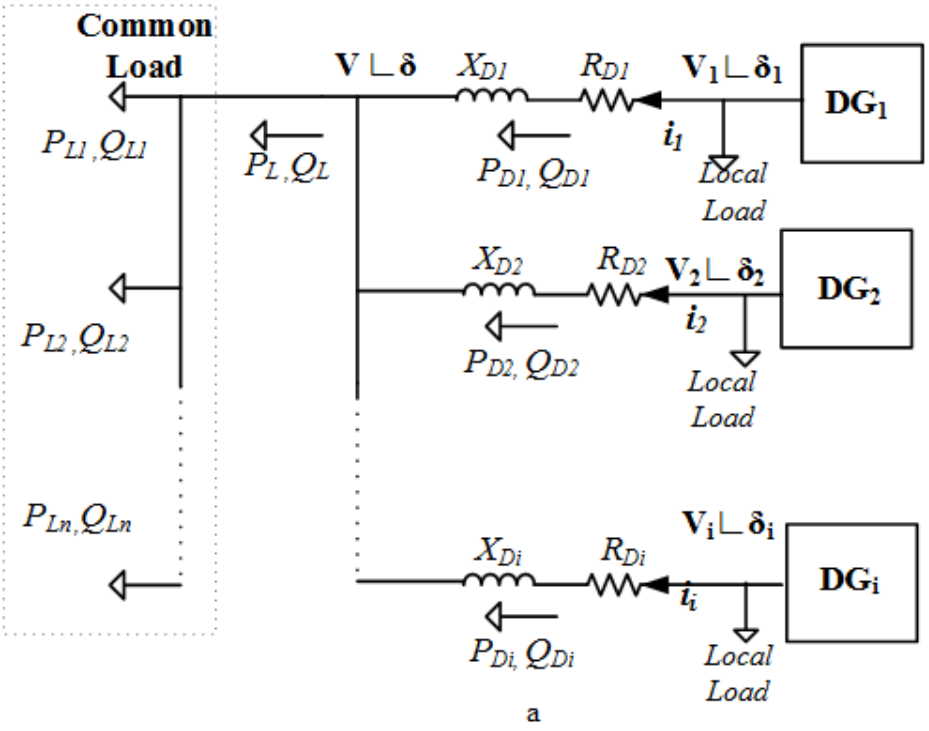
To illustrate the proposed concept on a larger microgrid, the system of Figure 4.12 (a) is now considered. Assuming that there are a total of i number DGs in a microgrid, the droop coefficients can be written as

$$m_1 \times P_{D1rated} = m_2 \times P_{D2rated} = ...m_i \times P_{Dirated},$$

$$n_1 \times Q_{D1rated} = n_2 \times Q_{D2rated} = ...n_i \times Q_{Dirated}, \tag{4.18}$$

The droop coefficients for this example are chosen as per the above two equations, where the ratings of the four DGs are taken in the ratio of DG_1:DG_2:DG_3:DG_4 = 1:1.1:1.2:1.3. With the system operating in the steady state, the load demand is reduced by 50 % at time instant t = 1 s.

Figure 4.12 (b) shows the active power distribution between DGs, and the load power is found to be shared based on the desired ratio mentioned above. Figure 4.12 (b) also shows phase - a of DG output current waveforms. It is evident that the DGs deliver currents based on their ratings.



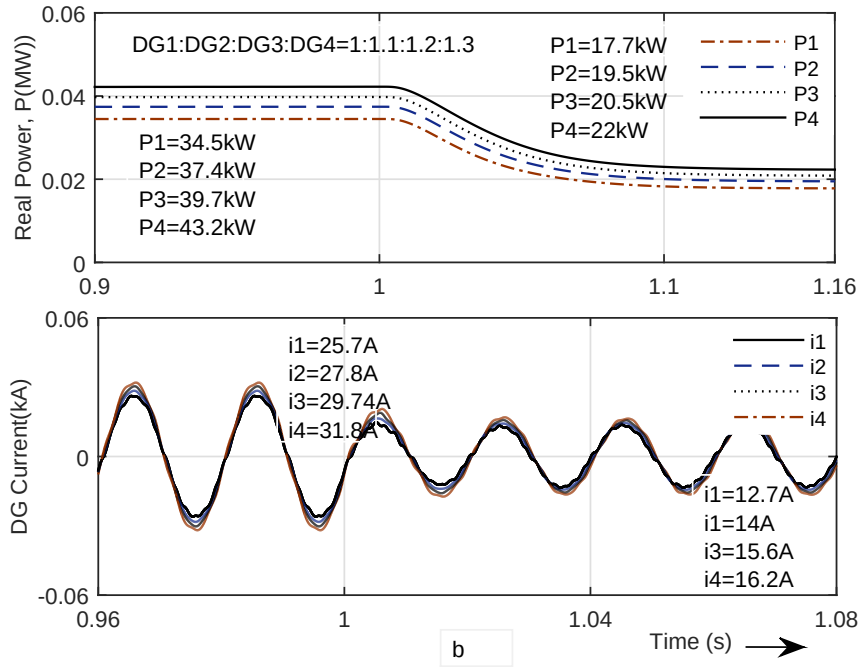


Figure 4.12: Microgrid with multi - number of DGs (a) single line diagram of large scale microgrid (b) real power sharing and current distribution among DGs

The percentage deviations in the real power sharing for this case are listed in Table 4.3.

Table 4.3: Large scale microgrid-percentage deviation in real power sharing

Percentage Error in Real Power Sharing (%)		
	Time Instant (0 - 1 s)	Time Instant (1 - 2 s)
DG_1	2.5	2.19
DG_2	1	2.3
DG_3	1.68	1.4
DG_4	1.26	2.3

4.4 Conclusion

In this chapter, a decentralized droop control method has been proposed for converter interfaced DGs in an islanded microgrid. It has been shown that the proposed modified angle droop is independent of the output inductance, and therefore it enables improved power sharing even with low droop gains. Voltage reference generated by angle droop method is taken as the bus voltage instead of three phase voltage measured across output capacitor. A proportional resonant controller is employed for the outer voltage and inner current loop. Furthermore, a harmonic voltage control has been added to the voltage controller resonant term to facilitate effective reactive power distribution among DGs. Indeed, this chapter addresses both the real and reactive power sharing between independently controlled DGs, where only a common clock is required for DG synchronization. Moreover, the advantage of inherent damping capability of converter current feedback along with advantages in high frequency resonant region of LCL filter is utilized. Simulation study and analysis are conducted for different feeder and output impedances. The results shown verifies that the suggested method successfully attain the desired

load real and reactive power sharing without the requirement of any supplementary control.

Chapter 5

Load Sharing in Medium and Low Voltage Islanded Microgrids

Traditional droop methods are based on the assumption of dominant inductive nature of feeder lines. The effect of output impedance in LCL filter fed converter interfaced DERs and a mitigating solution to nullify its adverse effect is investigated in Chapter 4. This method is applicable to medium voltage MGs with same converter and filter structure. But in DERs with voltage controlled converters, an LC filter can satisfactorily eliminate the switching frequency harmonics as discussed in Chapter 2. But there are other serious concerns to investigate in weak medium and low voltage MGs to achieve accurate load power sharing. In low voltage dominant resistive lines, the conventional droop law is usually reversed. But the line inductance value is small compared to cable resistance in medium voltage MGs and therefore normally possess unity or low X/R ratio. Due to strong coupling among real and reactive power, load distribution cannot be effectively attained with conventional voltage and angle droop methods. since decoupling between real and imaginary load demand cannot be possible in this scenario, a transformation matrix is used to modify droop equations to account for the coupling effects and therefore, the percentage deviation in real power sharing is much improved [32]. But the need

for intercommunication channel between converters still remains as a drawback due to distance.

This chapter proposes advanced decentralised droop control methods for medium voltage strong coupled lines and low voltage resistive lines. Initially, a modified angle droop control for strong coupled lines is discussed. A power decoupling term has been added to the network reference voltage, to effectively eliminate the coupling between real and reactive power, and thereby achieve accurate load sharing in islanded microgrids with feeder lines having low or unity X/R ratio. In addition, harmonic power sharing among DERs can also be achieved. The proposed scheme overcomes the drawbacks of conventional angle droop method without compromising its advantages such as constant frequency regulation and no communication medium between DERs. Secondly, a new droop control strategy which incorporate the concept of angle droop control along with virtual impedance concept is introduced for low voltage resistive MGs, where real and reactive power sharing among DGs are achieved by drooping voltage and angle of DG output voltage. The added virtual resistor with droop characteristics will improve the accuracy in load power distribution among converter interfaced DGs. Since the resistor is virtual, the power loss is nullified. However, it improve damping characteristics to harmonics generated by filter capacitor with line impedance and thus will improve overall system response. Fundamental component of DG current is filtered out using first order filters, which avoids any complexity or cumbersome computations.

The proposed methods uses the DLQR based converter inner loop control method for individual converter control, which provides robustness to the individual DERs under various loading conditions. A third harmonic injection based PWM is chosen to generate switching signals, which possess the added benefit of effective DC link voltage utilization. The advanced decentralised control schemes are demonstrated through computer simulation studies in PSCAD/EMTDC to verify its effectiveness.

The core content of this work has been published in two papers [158, 159].

5.1 Load Power Sharing by DGs in Strong Coupled Lines

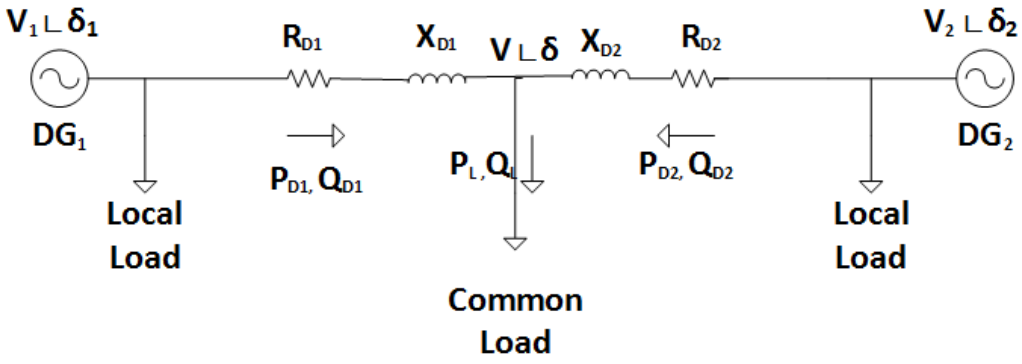


Figure 5.1: Power sharing in droop control

The single-line diagram of an islanded microgrid feeding local and common loads is illustrated in Figure 5.1, where $V_1\angle\delta_1$ and $V_2\angle\delta_2$ are DG_1 and DG_2 output voltage, $R_{D1} + jX_{D1}$ and $R_{D2} + jX_{D2}$ are DG_1 and DG_2 feeder impedances. Both DGs are loaded with local as well as common loads and the common load is assumed to be shared among them in islanded operating mode where droop control is the key factor in load sharing. Common loads can be linear, non-linear, frequency dependent or unbalanced in nature and it is shared by DGs based on their ratings.

Real and imaginary load power (P_L, Q_L) supplied by both DG_1 and DG_2 are defined as

$$P_L = \sum(P_{Di}) - \sum(P_{Didrop})$$
$$Q_L = \sum(Q_{Di}) - \sum(Q_{Didrop}), \quad (i = 1, 2) \tag{5.1}$$

where, P_{Di} and Q_{Di} are real and reactive power delivered by each DGs, P_{Didrop} and Q_{Didrop} are corresponding drop across feeder impedance of respective DGs.

Medium or low voltage lines with $\frac{X}{R} = 1$ have strong coupling between real and reactive power. In such cases, the power flow equation for i^{th} DG can be written as

$$P_{Di} = \frac{V_i}{{R_{Di}}^2 + {X_{Di}}^2}[R_{Di}(V_i - Vcos(\delta_i - \delta)) + X_{Di}Vsin(\delta_i - \delta)]$$

$$Q_{Di} = \frac{V_i}{{R_{Di}}^2 + {X_{Di}}^2}[-R_{Di}Vsin(\delta_i - \delta) + X_{Di}(V_i - Vcos(\delta_i - \delta))] \quad (5.2)$$

It has been clear from (5.2) that the strong coupling between real and reactive power does not allow the DGs to share common loads using conventional droop control. Accuracy in load sharing can be obtained by incorporating the effect of coupling in power balance equation. One of the method is to use a transformation matrix for modifying the droop coefficients as mentioned in [32]. Another method proposed in this chapter is to use a power decoupling factor to nullify the coupling effects. These two methods are explained below.

5.1.1 Decoupling using Power Decoupling Factor

In this method, decoupling between real and reactive power can be achieved by adding a power decoupling term with the reference voltage. Rewriting (5.2) for DG_1 gives

$$P_{D1} = \frac{V_1 X_{D1} Vsin(\delta_1 - \delta)}{{Z_{D1}}^2} + P_{dec1}$$

$$Q_{D1} = \frac{V_1 X_{D1}[V_1 - Vcos(\delta_1 - \delta)]}{{Z_{D1}}^2} + Q_{dec1} \quad (5.3)$$

where, P_{dec1} and Q_{dec1} are the real and reactive power decoupling factors of DG_1, given by

$$P_{dec1} = \frac{V_1 R_{D1}[V_1 - V cos(\delta_1 - \delta)]}{{Z_{D1}}^2}$$
$$Q_{dec1} = \frac{-V_1 R_{D1} V sin(\delta_1 - \delta)}{{Z_{D1}}^2} \tag{5.4}$$

In feeder lines with low X/R ratio, the decoupling factors P_{dec1} and Q_{dec1} cannot be neglected. Let us define $\Delta\delta_1 = \delta_1 - \delta$. Then from (5.4), the complex decoupling power can be written as

$$P_{dec1} + jQ_{dec1} = \frac{V_1 R_{D1}(V_1 - V(cos(\Delta\delta_1) + jsin(\Delta\delta_1))}{{Z_{D1}}^2}$$
$$= \frac{V_1 R_{D1}}{Z_{D1}} \frac{[V_1 - V\angle(\Delta\delta_1)]}{Z_{D1}} \tag{5.5}$$

Dividing both sides by V_1, we get

$$\frac{P_{dec1}}{V_1} + j\frac{Q_{dec1}}{V_1} = \frac{R_{D1}}{Z_{D1}} \frac{[V_1 - V\angle(\Delta\delta_1)]}{Z_{D1}} = \frac{R_{D1}}{Z_{D1}} \hat{I} \tag{5.6}$$

(5.6) is modified by multiplying both sides with a proportional constant K and converting the three phase currents into equivalent two phase orthogonal quantities as,

$$\frac{KP_{dec1}}{V_1} + j\frac{KQ_{dec1}}{V_1} = \frac{KR_{D1}}{Z_{D1}}(I_{D\alpha 1} + jI_{D\beta 1})$$
$$= K_{D\alpha 1} I_{D\alpha 1} + jK_{D\beta 1} I_{D\beta 1} \tag{5.7}$$

where, $\frac{KP_{dec1}}{V_1} = V_{Pdec1}$ and $\frac{KQ_{dec1}}{V_1} = V_{Qdec1}$ represent the α-β axis voltage decoupling terms resulting from P_{dec1} and Q_{dec1}, and $K_{D\alpha 1} = K_{D\beta 1}$ is the resistive factor used in calculating the voltage drop. $I_{D\alpha 1}$ and $I_{D\beta 1}$ are stationary axis components of current through feeder lines and $K_{D\alpha 1}$ and $K_{D\beta 1}$ are considered as additional control variables in droop control which will improve the load sharing. The resultant stationary frame decoupling voltages are converted back to

three phase abc frame using inverse Clarke transform and then subtracted from the voltage reference obtained from droop control as illustrated in Figure 5.2. This form simplifies the decoupling factor and by subtracting it from three phase reference voltage obtained from droop control, makes it possible to achieve better decoupling effect between real and imaginary power. The angle droop and voltage droop controller and the selection of droop coefficients are explained in Chapter 4. Nevertheless, the compensation for the resistive drop in power sharing accuracy is achieved, as the feeder resistor is not incorporated in droop coefficient calculation. Once the instantaneous equation for $V_{abcref1}{}^{*}$ is obtained as depicted in Figure 5.2, these signals are used for converter tracking, which will be explained in later section.

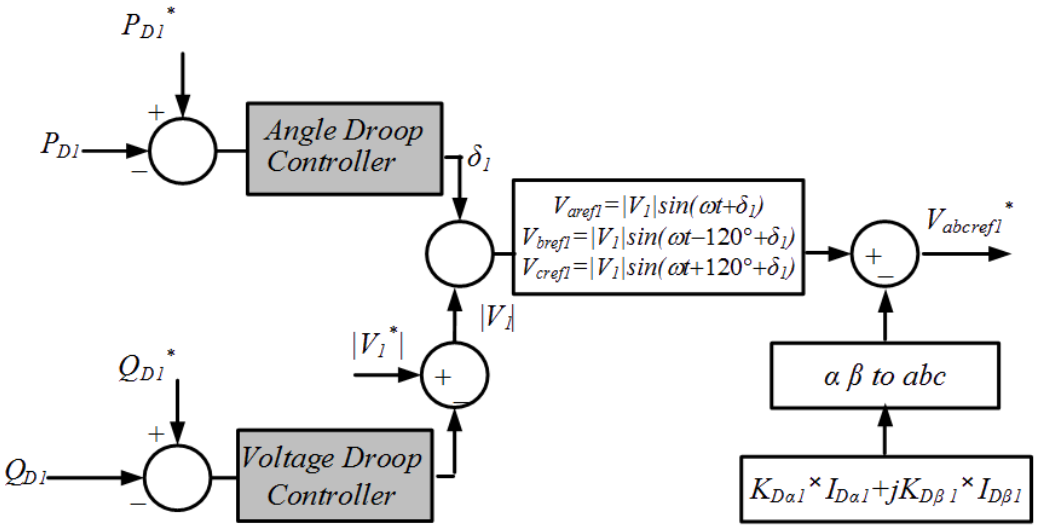


Figure 5.2: Modified angle droop control

5.1.2 Decoupling using Transformation Matrix [32]

A transformation matrix is derived after few manipulation of (5.2) and these has been utilized for achieving the decoupling of real and reactive power. This is done

by modifying droop equation as

$$\begin{bmatrix} \delta_1 \\ |V_1| \end{bmatrix} = \begin{bmatrix} \delta_1^* \\ |V_1|^* \end{bmatrix} - T \begin{bmatrix} m_1 \\ n_1 \end{bmatrix} \times T \begin{bmatrix} {P_{D1}}^* - P_{D1} \\ {Q_{D1}}^* - Q_{D1} \end{bmatrix} \tag{5.8}$$

where, transformation matrix T is defined as

$$T = \begin{bmatrix} \frac{X_{D1}}{Z_{D1}} & \frac{-R_{D1}}{Z_{D1}} \\ \frac{R_{D1}}{Z_{D1}} & \frac{X_{D1}}{Z_{D1}} \end{bmatrix}$$

While rewriting the modified pseudo power and droop coefficients as given below, final angle and voltage droop equations can be defined as given in (5.9).

$$\begin{bmatrix} {P'}_{D1}{}^* - {P'}_{D1} \\ {Q'}_{D1}{}^* - {Q'}_{D1} \end{bmatrix} = T \times \begin{bmatrix} {P_{D1}}^* - P_{D1} \\ {Q_{D1}}^* - Q_{D1} \end{bmatrix}, \begin{bmatrix} m_1' \\ n_1' \end{bmatrix} = T \times \begin{bmatrix} m_1 \\ n_1 \end{bmatrix}$$

$$\delta_1 = \delta_1^* - m_1'[{P'}_{D1}{}^* - {P'}_{D1}],$$

$$|V_1| = |V_1|^* - n_1[{Q'}_{D1}{}^* - {Q'}_{D1}] \tag{5.9}$$

5.2 Load Power Sharing in High R/X Ratio-Resistive Lines

Considering the nature of low voltage lines below 600 V, feeders are assumed to be resistive and inductance factor is negligible. Substituting X_{D1} = 0 in equation (4.3) the real and reactive power supplied by DG_1 can be defined as

$$P_{D1} = \frac{V_1}{R_{D1}}(V_1 - V) \Rightarrow P_{D1} \propto (V_1 - V)$$

$$Q_{D1} = -\frac{V_1}{R_{D1}} V(\delta_1 - \delta) \Rightarrow Q_{D1} \propto -(\delta_1 - \delta) \tag{5.10}$$

It is clear from (5.10) that active and reactive power requirements of microgrid can be achieved by drooping network voltage magnitude and angle respectively. Thus, droop control for DG_1 is defined as

$$|V_1| = |V_1|^* - m_1[P_{D1} - {P_{D1}}^*],$$

$$\delta_1 = \delta_1^* - n_1[{Q_{D1}}^* - Q_{D1}] \tag{5.11}$$

where, $|V_1|^*$ and δ_1^* are the rated magnitude and angle of DG voltage, which can deliver the rated real and reactive power of ${P_{D1}}^*$ and ${Q_{D1}}^*$ respectively. m_1 and n_1 are real and reactive power droop coefficients and it is defined as

$$m_1 = \frac{\Delta V_1}{\Delta P_1}, \;\; n_1 = \frac{\Delta \delta_1}{\Delta Q_1}$$

Droop coefficients depends on the power rating of each DG as well as the voltage regulation requirement at point of common coupling. Similarly, for DG_2, droop control is defined as

$$|V_2| = |V_2|^* - m_2[P_{D2} - {P_{D2}}^*],$$

$$\delta_2 = \delta_2^* - n_2[{Q_{D2}}^* - Q_{D2}] \tag{5.12}$$

The above assumptions will work for resistive lines, but a slight error in power sharing cannot be avoided in dominant resistive lines and medium voltage lines. In either case, complete decoupling between real and reactive power is possible by adding a virtual impedance to the reference voltage. Virtual impedance will be resistive in nature in dominant resistive lines and combination of inductive and resistive behavior in medium voltage lines. Thus by virtually including the resistive

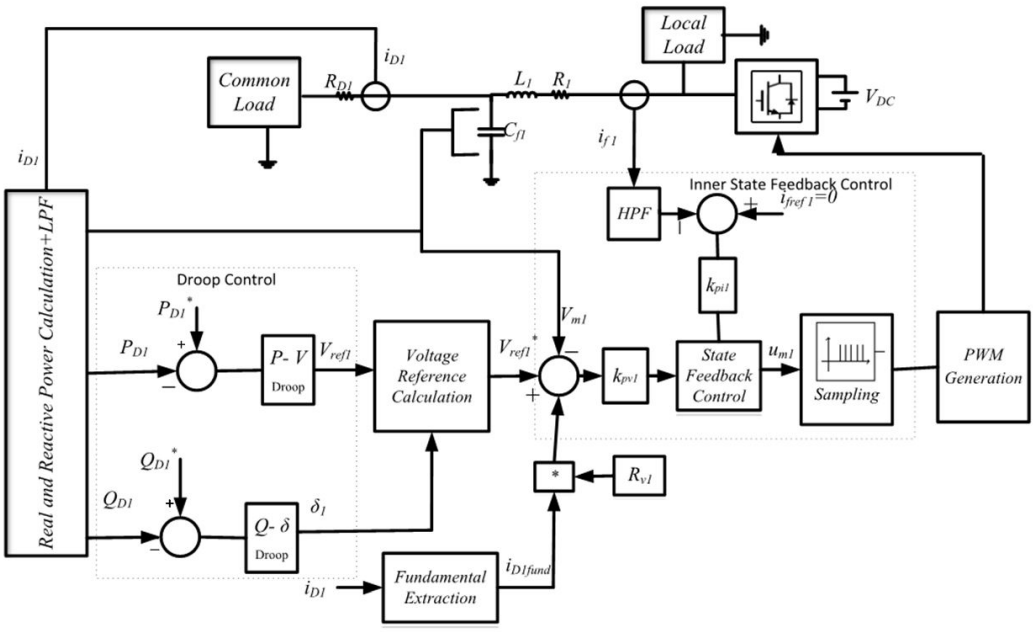


Figure 5.3: Block diagram of modified droop control and inner state feedback control for resistive MGs

drop across feeder lines, the reference voltage for i^{th} DG can be written as

$$V_{refi}{}^* = V_{refi} - I_{Difund} * Z_{vi} \tag{5.13}$$

where, Z_{vi} is the virtual impedance and I_{Difund} is the fundamental of current through feeder lines. Virtual Impedance is chosen based on the relation given below.

$$\frac{Z_{v1}}{Z_{v2}} \propto \frac{Z_{L1}}{Z_{L2}}$$

The value of virtual impedance also depends on the voltage drop in load voltage. The virtual impedance should be selected to keep the deviation in load voltage within acceptable limits. Figure 5.3 represents the block diagram representation of overall control for DG_1. Instantaneous real and reactive power are calculated from DG_1 output current and voltage. It is then passed through a low pass filter to obtain the average value. Measured values are applied to inverse angle and

voltage droop control and a voltage factor corresponding to virtual impedance term is then subtracted from the output of droop controller as shown in Figure 5.3. Since the feeder has resistive nature, virtual impedance term is taken as virtual resistance. The fundamental term of DG output current is extracted by filtering method, in which harmonic components are separated using high pass filter and the resultant is subtracted from total current to obtain the fundamental component. Since this method utilizes only first order filters, the extensive calculation can be avoided compared to other techniques. In feeder lines with strong coupling between real and reactive power, virtual inductance needs to be considered in addition to resistance. The obtained reference voltage is used as a reference for inner state feedback control. The desired three phase reference voltages across output capacitor of DG_1 can be defined as,

$$V_{aref}{}^{*} = |V_p|sin(\omega t + \delta) - I_{D1funda} \times R_{v1}$$

$$V_{bref}{}^{*} = |V_p|sin(\omega t - 120^o + \delta) - I_{D1fundb} \times R_{v1}$$

$$V_{cref}{}^{*} = |V_p|sin(\omega t + 120^o + \delta) - I_{D1fundc} \times R_{v1} \tag{5.14}$$

where, $|V_p|$ is the voltage magnitude obtained from P - V droop, δ is the angle that maintains the power flow from DG to load and ω is rated frequency.

5.3 Voltage Control of DGs

Structure of three phase converter interfaced source with an output LC filter is described in Figure 2.7 (a) and its equivalent circuit is redrawn as shown in Figure 5.4. A discrete linear quadratic regulator based state feedback control which considers equivalent model of converter and filter is chosen to develop a controller for each converter. Robustness of this control algorithm helps to compensate for any

external disturbances in the system.

The state space equation of converter and output filter obtained from its single phase equivalent circuit is given in (5.15). The voltage across the capacitor and the filter inductor current are chosen as states.

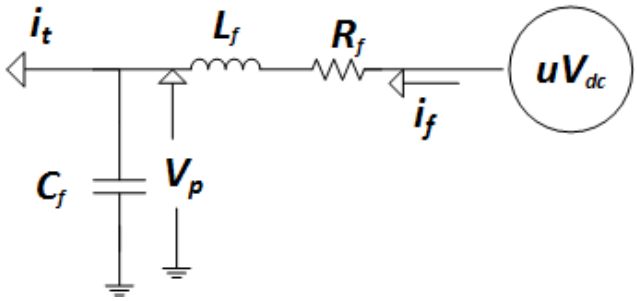


Figure 5.4: Single phase equivalent of the converter with LC filter

$$\dot{x} = Ax + Bu + Ci_t, \tag{5.15}$$

where state vector X is defined as $X^T = [i_f \;\; V_p]$ and i_t is the current being fed to the microgrid network. i_t is assumed to be a disturbance input and is not considered in the control design. One of the major advantages of discrete quadratic regulator based control is its robustness to any external disturbance or parameter variations. Filter inductor is designed to keep the current ripple within 10 - 20 % so that it has the capability of eliminating high frequency signals. Considering this, the reference for filter inductor current is taken as zero, and the measured current signal is passed through a high pass filter to obtain only the high frequency components. In addition, the error in capacitor voltage reference and actual voltage is passed through a proportional controller, and sum of these two controller output signal is sampled with two fold switching frequency to obtain a discretized modulation signal. The control law is given by

$$u_c = k(x_{ref} - x) \tag{5.16}$$

where, k_1 and k_2 are proportional gains calculated using discrete time quadratic regulator. The block diagram representation of control law is given in Figure 5.5 and it is same as the DLQR based state feedback control described in Chapter 2.

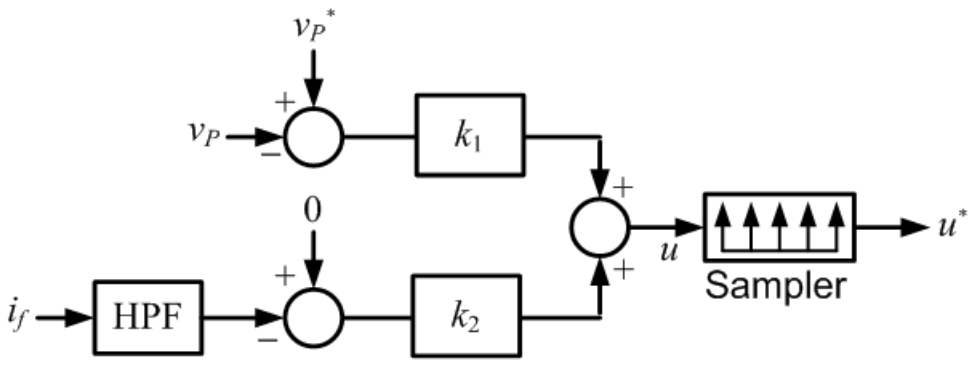


Figure 5.5: LQR based state feedback control

The discretized modulating signal is then added to a third harmonic signal which is derived by maximum and minimum values of three phases and the sum is compared with the triangular carrier to generate switching signals for upper and lower switches in each leg. This method is a replica of conventional space vector modulation scheme and has similar advantages such as effective DC link voltage utilization, constant switching frequency. In addition, it avoids complex calculations and delays, which are undesirable for high frequency switching applications. The LC filter is designed for eliminating switching harmonics produced by high frequency switching.

5.4 Simulation Studies

A study is conducted using PSCAD/EMTDC to analyze the efficacy of above methods under different loading conditions. Initially, case scenarios with strong coupled MG are carried out to validate the proposed power decoupling algorithm.

Subsequently, the proposed algorithm for the resistive MG is validated using simulation studies.

5.4.1 Strong Coupled lines with X/R Ratio = 1

The design specifications used in simulation study are listed in Table 5.1.

Table 5.1: System parameters for strongly coupled microgrid

Parameters	Details
Source Voltage	1100 V (L-L)
Source Frequency	50 Hz
DG_1 Line Impedance DG_2 Line Impedance	$R_{D1} + jX_{D1}$ = 1 + j1 Ω $R_{D2} + jX_{D2}$ = 3 + j3 Ω
DG_1 Local Load = DG_2 Local Load	$R_{La} = R_{Lb} = R_{Lc}$ = 325 Ω, $L_{La} = L_{Lb} = L_{Lc}$ = 0.419 H
Common Load_A and Load_B Impedance Load Non-linear Load	 2* $R_{La} = R_{Lb} = R_{Lc}$=225 Ω, $L_{La} = L_{Lb} = L_{Lc}$ = 61 mH 2* Three Phase Diode Rectifier with an RL load R_L = 110 Ω, L_L = 5 H
Common Unbalanced Load	R_{La} = 300 Ω, R_{Lb} = 100 Ω, R_{Lc} = 425 Ω $R_a + jX_a = 225 + j6.594$, $R_b + jX_b = 105 + j19.15$, $R_c + jX_c = 55 + j12.87$
Frequency Dependant Load	30 HP Induction Motor
Filter Inductance	0.003 H
Filter Capacitor	10 μH
Converter Losses	0.001 Ω
Switching Frequency	15 kHz
Angle Droop Gain (rad/MVAr)	m_1 = 0.057, m_2 = 0.114
Voltage Droop Gain	n_1 = 0.22, n_2 = 0.44
Decoupling Coefficients	$K_{D\alpha1} = K_{D\beta1}$ = 0.33, $K_{D\alpha2} = K_{D\beta2}$ = 0.11

All loads connected at PCC are represented in Figure 5.6 and common Load_A

and Load$_B$ are assumed to be a combination of non-linear and impedance load. Examples I-IV represent different loading scenarios and example V illustrates a faulty condition under impedance and inertial loading. A comparative analysis is performed with the three different decentralized droop methods namely conventional angle droop, transformation matrix angle droop and the proposed method.

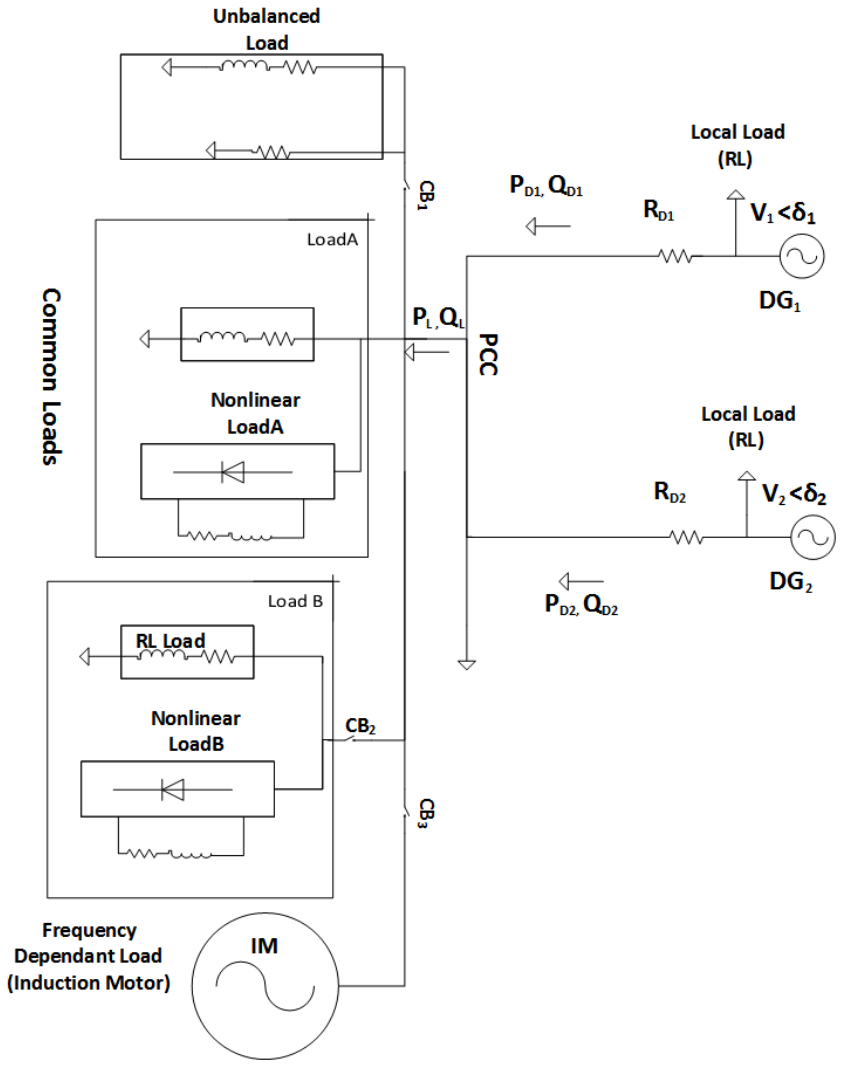


Figure 5.6: Microgrid under consideration

Example I

In a standalone operation of converter interfaced sources, common loads are shared by DGs based on their ratings. Rating of DG_2 is half of DG_1 and droop coefficients have been chosen accordingly. Initially common $Load_A$ and $Load_B$ are connected to the microgrid and together they need $80 + j14$ kVA power from the DGs. Based on rating of the DGs, DG_1 and DG_2 have to supply $\frac{2}{3}$ and $\frac{1}{3}$ of load power respectively. Figure 5.7 illustrates real and reactive power sharing, corresponding to above loading scenario. The power sharing ratio of 0.487 clearly validates the effectiveness of proposed method where DG_1 is supplying almost 2 times power to the loads compared to DG_2. The main advantage of angle droop, which is the

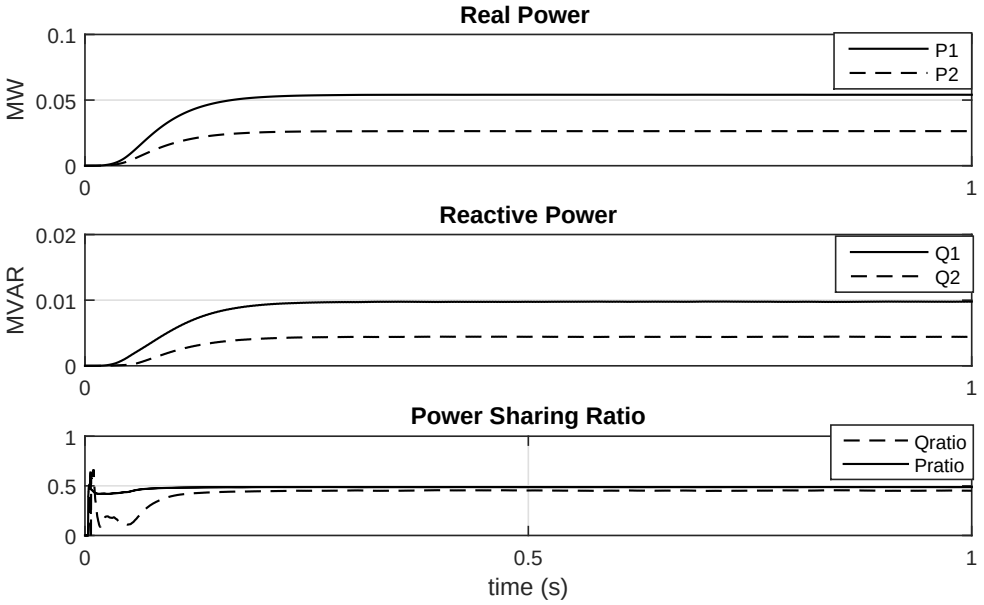


Figure 5.7: Power sharing under nonlinear loads

lesser frequency variation under steady state is illustrated in Figure 5.8 and it is found to be less than 1 %. Load currents and voltages are shown in Figure 5.9 and the harmonic content of load power is found to be shared based on DG rating. It is clear from Figure 5.10 that converter currents are almost equally shared based on

rating and corresponding total harmonic distortion is found to be 17 % and 16 % in DG_1 and DG_2 respectively.

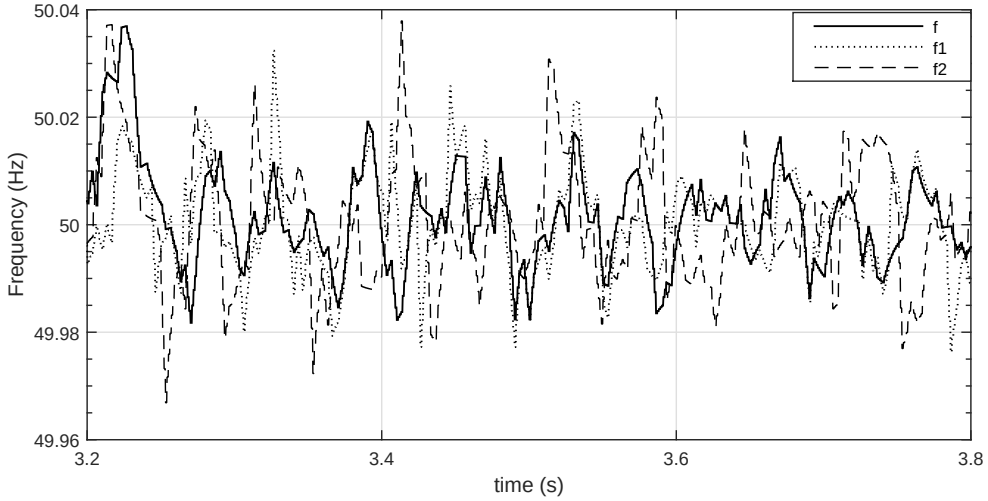


Figure 5.8: Converter and network frequency under non-linear loads

Example II

A study of the system behaviour during load change is conducted on this section and corresponding results on power sharing and system frequency under transient and steady state are illustrated in Figure 5.11 and Figure 5.12. A step change of $40 + j7$ kVA is made at load side at time t = 1 s by opening the circuit breaker CB_2 and $Load_B$ is disconnected from the circuit. This is to illustrate the transient behaviour of the system during a load change. Also, Figure 5.12 shows frequency deviation during load change is within 50 $\pm$ 0.3 Hz range and this transient lasts only for 150 milliseconds before reaching the steady state value of 50 Hz.

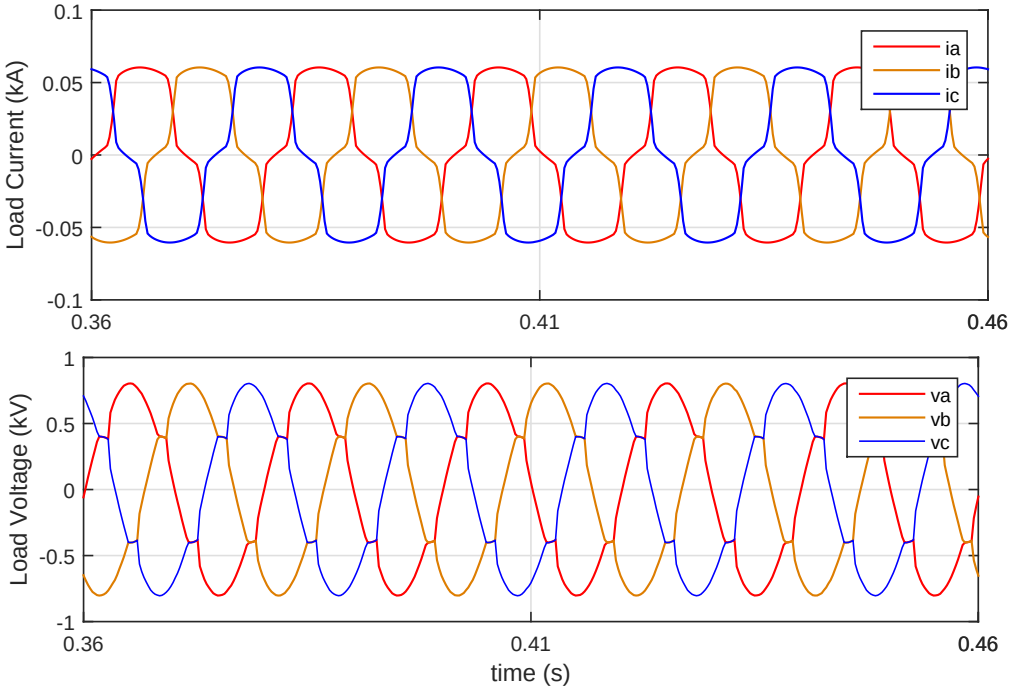


Figure 5.9: Load voltage and current under non-linear loads

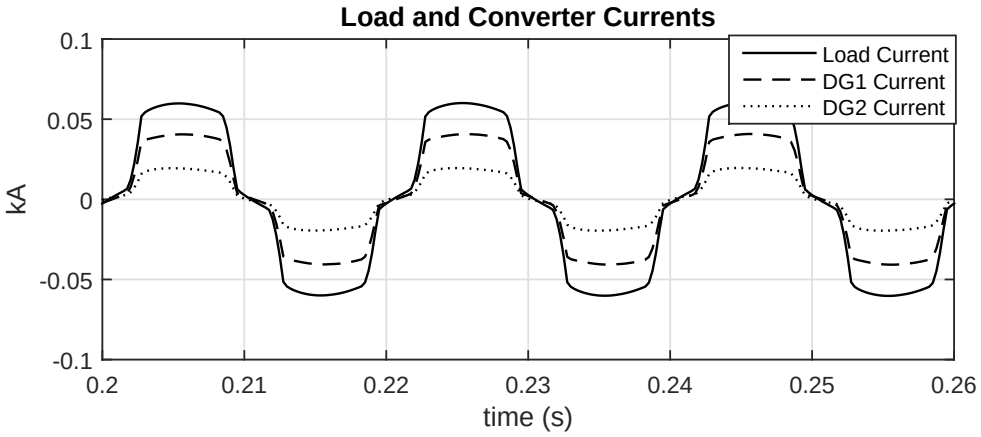


Figure 5.10: Load current sharing under non-linear loads

Example III

An unbalanced loading scenario is explained in this part by introducing a resistive-inductive load at t = 3 s. Load voltage and current waveforms, illustrated in Figure

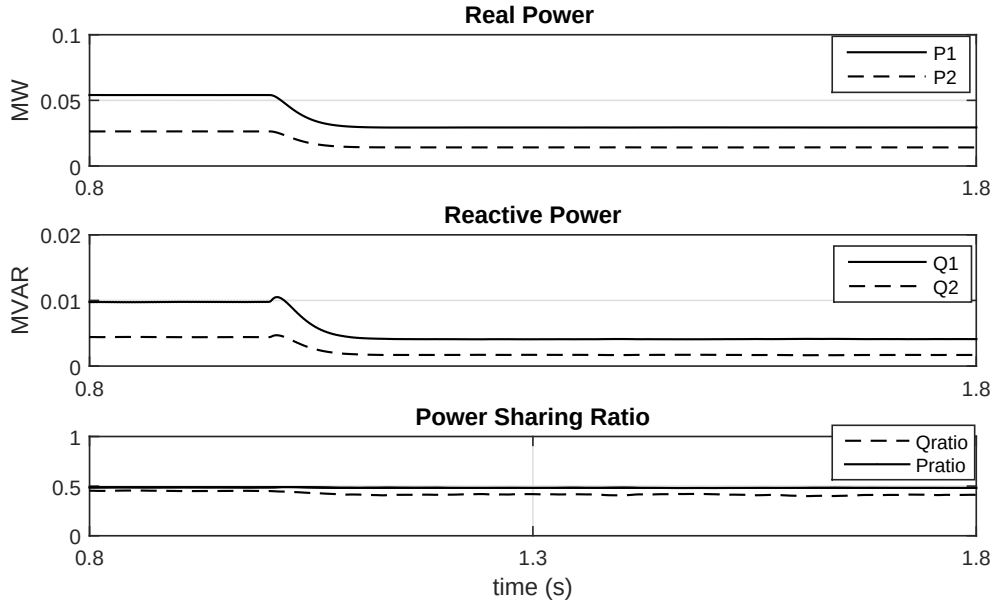


Figure 5.11: Power sharing during load change

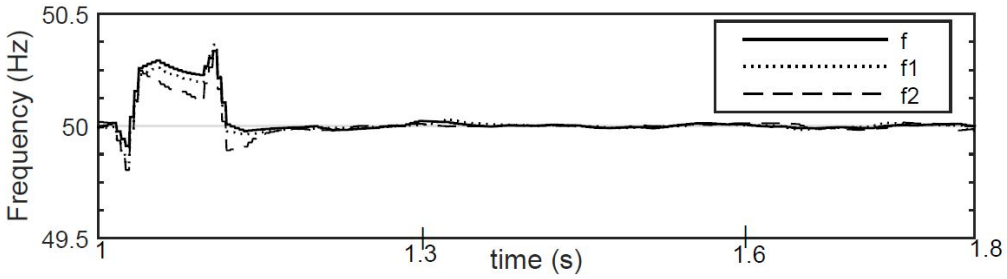


Figure 5.12: Transient analysis of frequency during load change

5.13, show the stable unbalanced operation at PCC. Real and reactive power sharing accuracy is improved even under this load change (Figure 5.14) and indicated reactive power sharing ratio of 0.465 from the expected value of 0.5 clearly verifies better reactive and harmonic power sharing in addition to active power proportional distribution. Harmonic power is shared among two DGs based on converter rating as illustrated in Figure 5.14. The load current is found to be the sum of converter currents which are based on droop control design and effect of circulating currents are not observed (Figure 5.15).

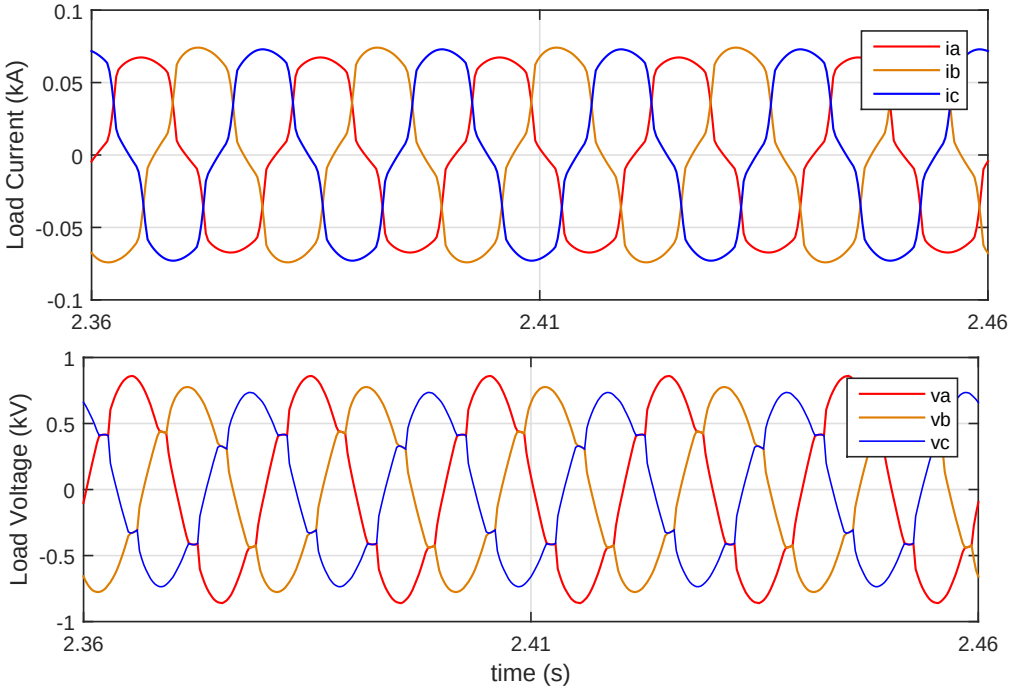


Figure 5.13: Load current and voltage under unbalanced loads

Example IV

A frequency dependent induction motor load of 30 HP is applied at the PCC at t = 3.25 s to analyze the effectiveness of advanced angle droop control. Real and reactive power sharing accuracy is surprisingly improved to 2 % and 7.2 % in this scenario as shown in Figure 5.16. Interestingly, the system frequency settles down with a steady state error well below $\pm$ 0.2 Hz in addition to negligible overshoot in the transient region as illustrated in Figure 5.17. Above results clearly validate the most accurate load sharing and negligible frequency deviation by the modified angle droop algorithm under frequency dependent loading.

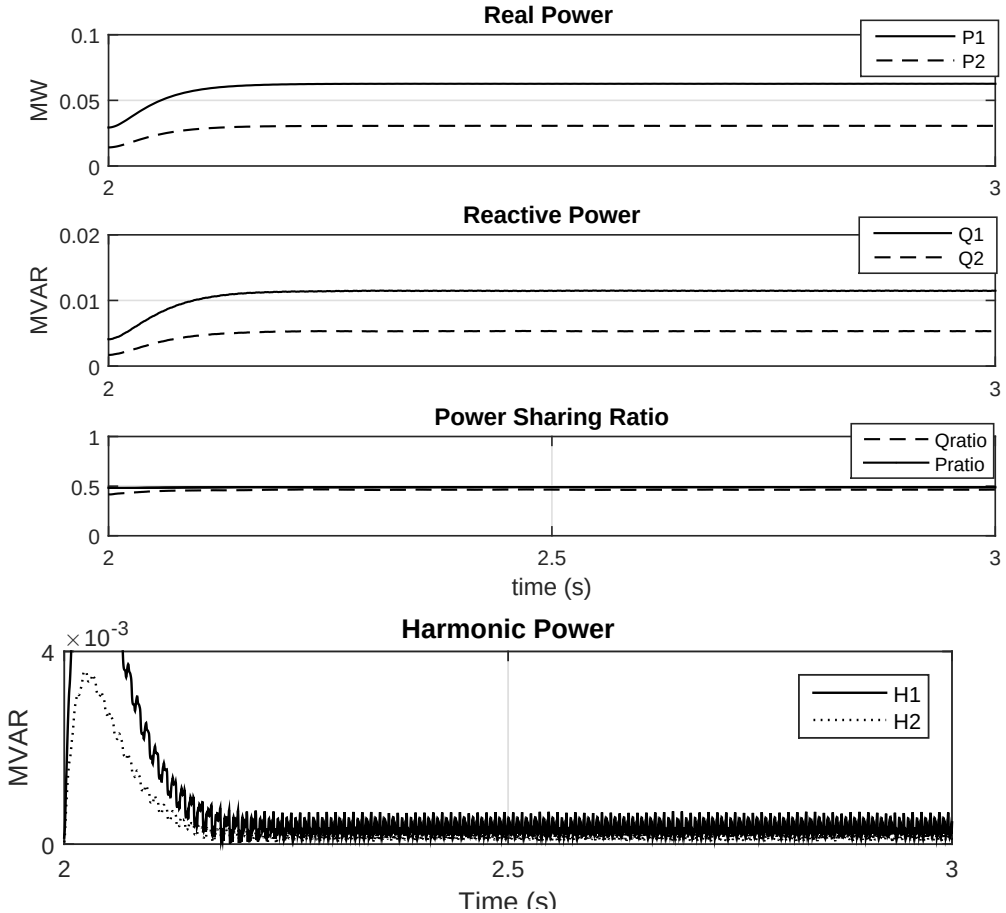


Figure 5.14: Power sharing under unbalanced loads

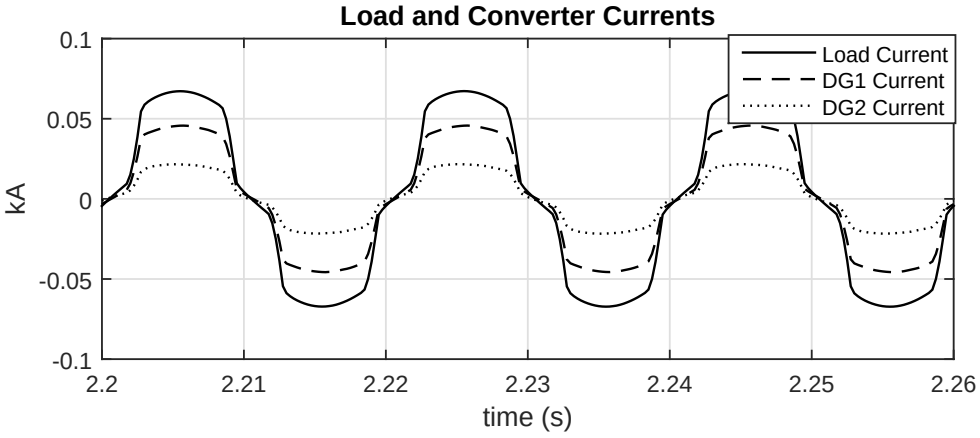


Figure 5.15: Load and converter currents under unbalanced loads

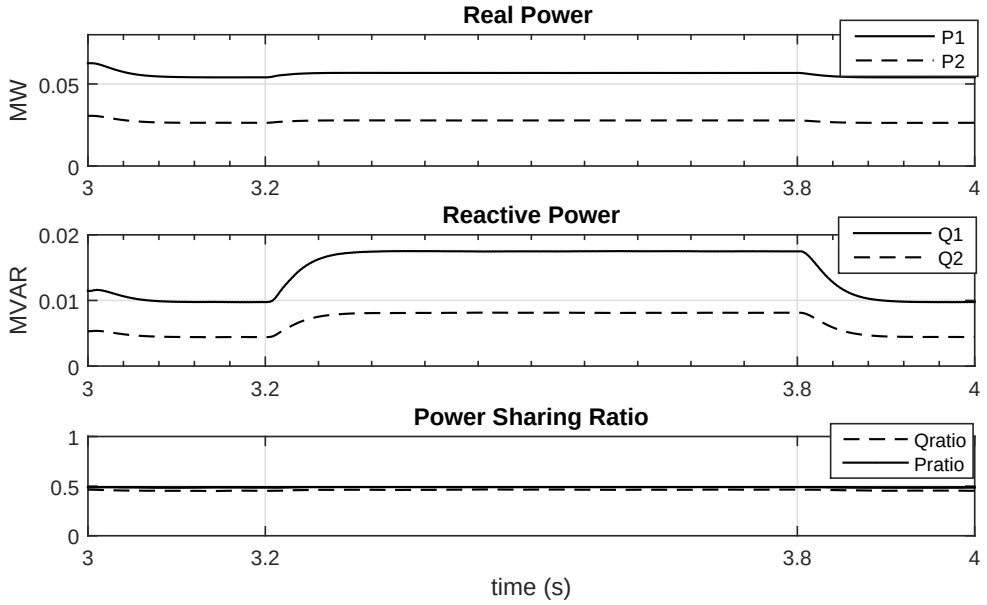


Figure 5.16: Power sharing under inertial loading

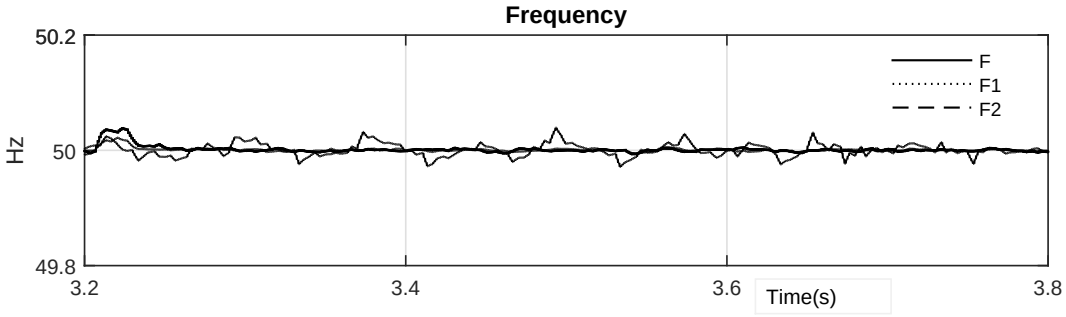


Figure 5.17: Load and converter frequency under inertial loading

Example V

In this case, only inertial and impedance loads are considered. Load voltage and current waveforms are illustrated in Figure 5.18.a, which verifies that voltage THD is well below 1 % under these kinds of loads. DG_2 is disconnected at t = 4.2 s and is reconnected at t = 4.4 s. During this period, DG_1 supplies the entire load as shown in Figure 5.18.b. This condition may occur when one of the DGs are under fault or

maintenance and only critical loads are allowed to connect to the microgrid.

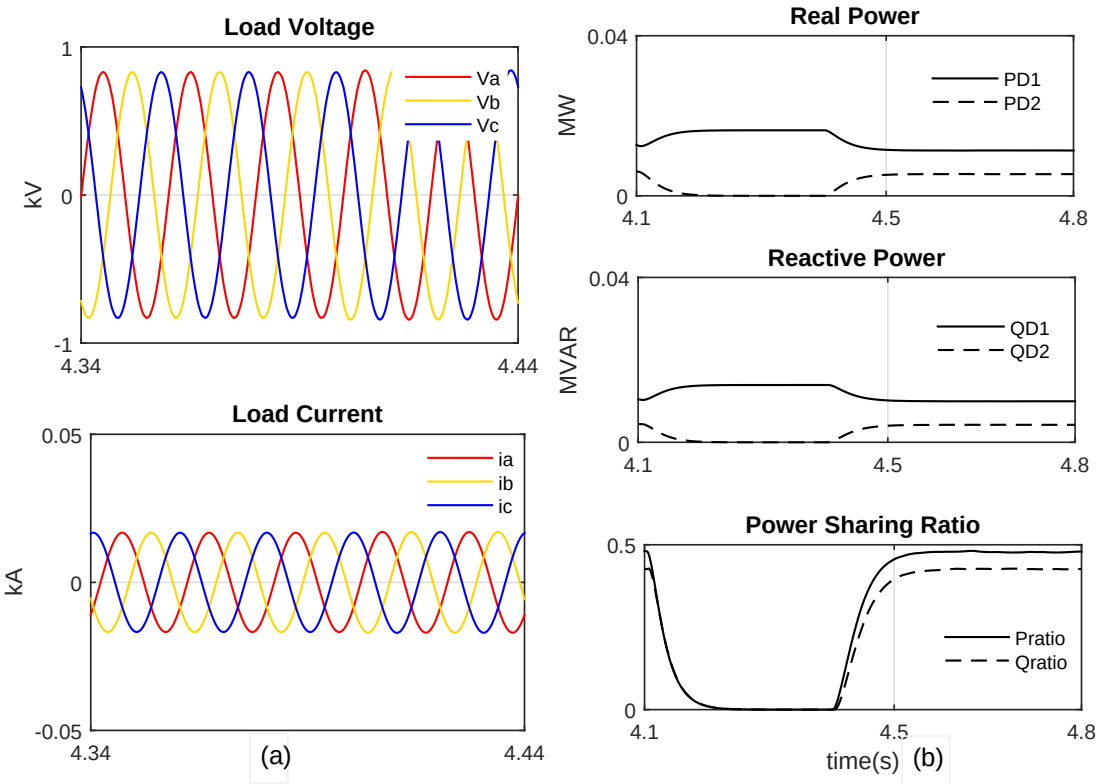


Figure 5.18: Example V: (a) load voltage and current under impedance and inertial loading (b) load power distribution under faulty condition

Performance of Conventional and Transformation Matrix based Methods

Examples I to IV show the efficacy of the proposed method. To observe and compare the performance of the proposed method with the conventional and transformation matrix method, two more simulation studies are performed and are shown in Figure 5.19 and Figure 5.20. Note that Examples I to IV each run for 1 s (Example I between 0 and 1 s, Example II between 1 and 2 s and so on). Each of the plots in Figure 5.19 and Figure 5.20 captures all the four different cases in a single frame. Since the DG_1 rating is double that of DG_2 rating, expected value in all cases is

0.5. As expected the conventional angle droop possess more deviation in the real power sharing whereas, the ratio is improved by 1 % by introducing transformation matrix and the value clearly matches with percentage deviation in [32]. In case of frequency dependent loads, all three methods show an improved power sharing which clarifies the suitability of angle droop control designs.

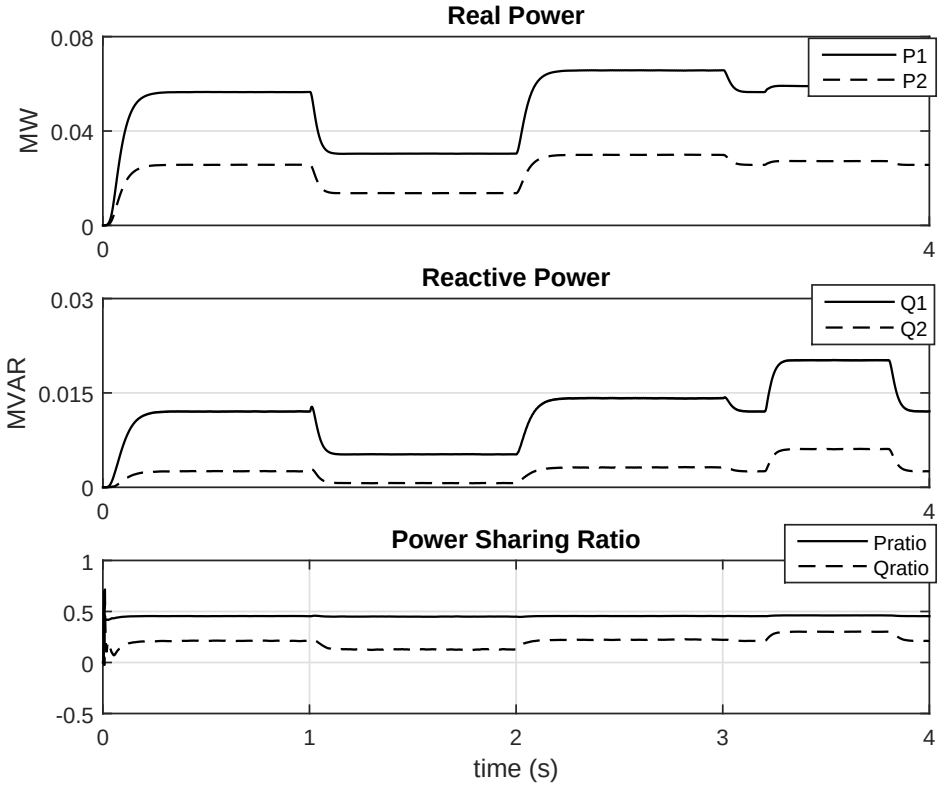


Figure 5.19: Power sharing with conventional angle droop

Comparison between Conventional, Transformation Matrix and Modified Angle Droop Method

In this subsection, the performance of the three methods (e.g., the conventional angle droop, the transformation matrix method and the proposed method) is compared. Again the four different time instants mentioned in the previous subsection

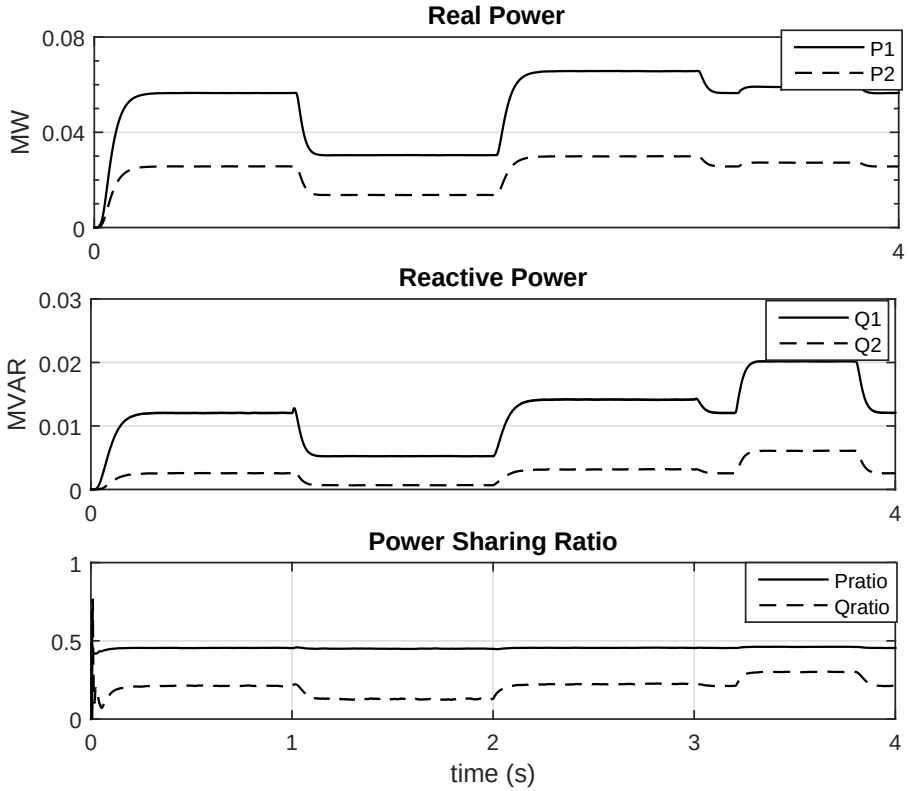


Figure 5.20: Power sharing using droop control with the transformation matrix

is considered. The real and reactive power sharing ratios are listed respectively in Table 5.2 and Table 5.3. It can be seen that the sharing ratio improves with the proposed method. The improvement is especially significant for the reactive power.

Figure 5.21 and Figure 5.22 graphically depict the percentage deviations in the real and reactive powers respectively for the three methods in the four different time instants.

Table 5.2: Real power sharing ratio

Time Interval (s)	0 - 1	1 - 2	2 - 3	3.2 - 3.8
Conventional Angle Droop	0.45	0.445	0.45	0.457
Angle Droop with Transformation Matrix	0.4543	0.451	0.4554	0.462
Proposed Angle Droop	0.487	0.4834	0.4882	0.49

Table 5.3: Reactive power sharing ratio

Time Interval (s)	0 - 1	1 - 2	2 - 3	3.2 - 3.8
Conventional Angle Droop	0.207	0.124	0.22	0.296
Angle Droop with Transformation Matrix	0.212	0.13	0.2234	0.3
Proposed Angle Droop	0.451	0.4074	0.465	0.464

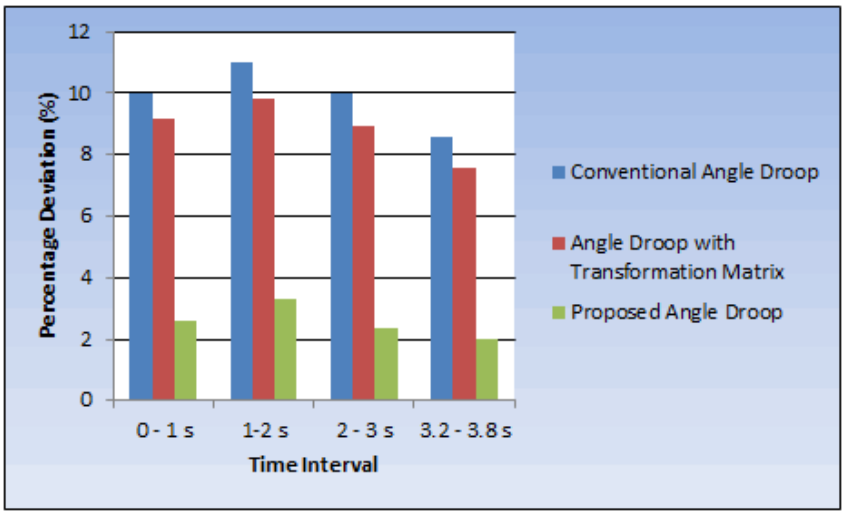


Figure 5.21: Percentage deviation in real power

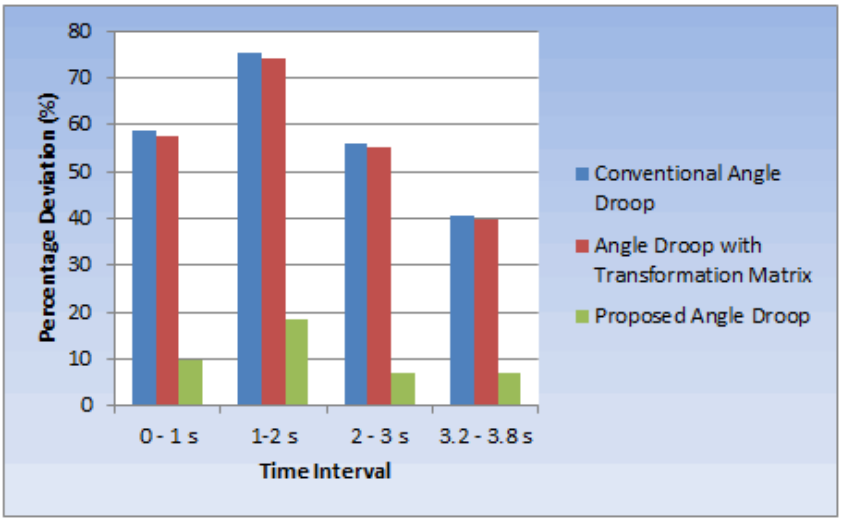


Figure 5.22: Percentage deviation in reactive power

Table 5.4 lists the average values of percentage deviation for the four cases considered. In the proposed method, the percentage deviation in active power is reduced to 2.56 %, which clearly validates the more efficient decoupling between active and reactive power terms. Reactive power sharing is very poor in conventional and transformation matrix based angle droop. But, it is found to be much effective in the proposed method, where average percentage deviation is 10 % compared to the huge deviation of 57.65 % and 56.6 % by the first two methods. Percentage deviation in reactive power can be further reduced by increasing the decoupling coefficient.

Table 5.4: Percentage deviation in real and imaginary power

Method	Real Power	Reactive Power
Conventional Angle Droop	9.9 %	57.65 %
Angle Droop with Transformation Matrix	8.8 %	56.6 %
Proposed Angle Droop	2.56 %	10 %

Table 5.5 explains the effect of decoupling coefficient on drop in load voltage

and power sharing accuracy. In this table, the decoupling coefficient is considered as a per unit value with respect to the base value of parameters given Table 5.1, while the load voltage obtained from conventional angle droop is taken as 1 pu. As the inclusion of the decoupling coefficient causes a slight voltage drop at the load side, choice of these parameters is a compromise between the accuracy in (mainly) the reactive power sharing and the voltage drop.

Table 5.5: Dependency of decoupling coefficient in power sharing and load voltage

Decoupling Coefficient $K_{D\alpha i} = K_{D\beta i}, i = 1, 2$	Error in Real Power Sharing	Error in Reactive Power Sharing	Load Voltage (pu)
0	9.9 %	57.65 %	1
0.72 pu	4.8 %	24.74 %	0.992
1 pu	2.6 %	10 %	0.989
1.18 pu	1.19 %	0.315 %	0.9868

It can be seen that maximum load voltage is obtained when the coefficient is zero, where the error in sharing is the maximum. Also, the voltage drop increases as the coefficient increases. However, the drop is negligible compared to the advantage obtained in power sharing. Improved reactive power sharing implies that both the converters are supplying current in proportion to their rating, and none of them is left with the burden of supplying excessive current.

5.4.2 Load Power Sharing in Resistive Microgrids (X/R $<$ 1)

The proposed controller was simulated using PSCAD/EMTDC software to analyse and verify proposed method under different loading conditions. Microgrid system data under study are listed in Table 5.6. Local loads are supplied by their local DGs and the common load is shared among two DGs and it may be balanced, linear, non-linear or unbalanced. Results obtained are redrawn using MATLAB for better clarity.

Table 5.6: System parameters for resistive microgrid

System Variables	Values
Source Voltage	440 V (L-L)
Source Frequency	50 Hz
DG_1 Line Impedance	1 Ω
DG_2 Line Impedance	3 Ω
DG_1 and DG_2 Local Load	$R_{La} = R_{Lb} = R_{Lc}$ = 325 Ω, $L_{La} = L_{Lb} = L_{Lc}$ = 0.419 H
Common Impedance $Load_A$ and $Load_B$	$R_{Lma} = R_{Lmb} = R_{Lmc}$ = 225 Ω, $L_{Lma} = L_{Lmb} = L_{Lmc}$ = 61 mH
Common Nonlinear $Load_A$ and $Load_B$	Three Phase Diode Rectifier with an RL load R_{Lm} = 110 Ω, L_{Lm} = 5 H
Common Unbalanced Load	R_{Lma} = 300 Ω, R_{Lmb} = 100 Ω, R_{Lmc} = 425 Ω
Frequency Dependant Load	30 HP Three Phase Induction Motor
Filter Inductance	0.002 H
Filter Capacitor	5 μH
Converter Losses	0.001 Ω
Switching Frequency	25 kHz

Case I

In the islanded mode, the common loads are shared by DGs based on their ratings. Rating of DG_2 is half the rating of DG_1 and droop coefficients have been chosen

accordingly. Initially, Load A and B, which is a combination of a three phase rectifier feeding an RL load and a constant impedance RL load, are connected to the microgrid. Based on rating of DGs, DG_1 and DG_2 has to supply $\frac{2}{3}$ and $\frac{1}{3}$ of load power respectively. Figure 5.23 illustrates real power sharing using voltage droop. Corresponding to the above condition, DG_1 is supplying twice the power to loads compared to DG_2. Transient and steady-state behavior of load and DG frequency is illustrated in Figure 5.23. The frequency variation is negligibly small during steady state with an acceptable deviation in the transient region.

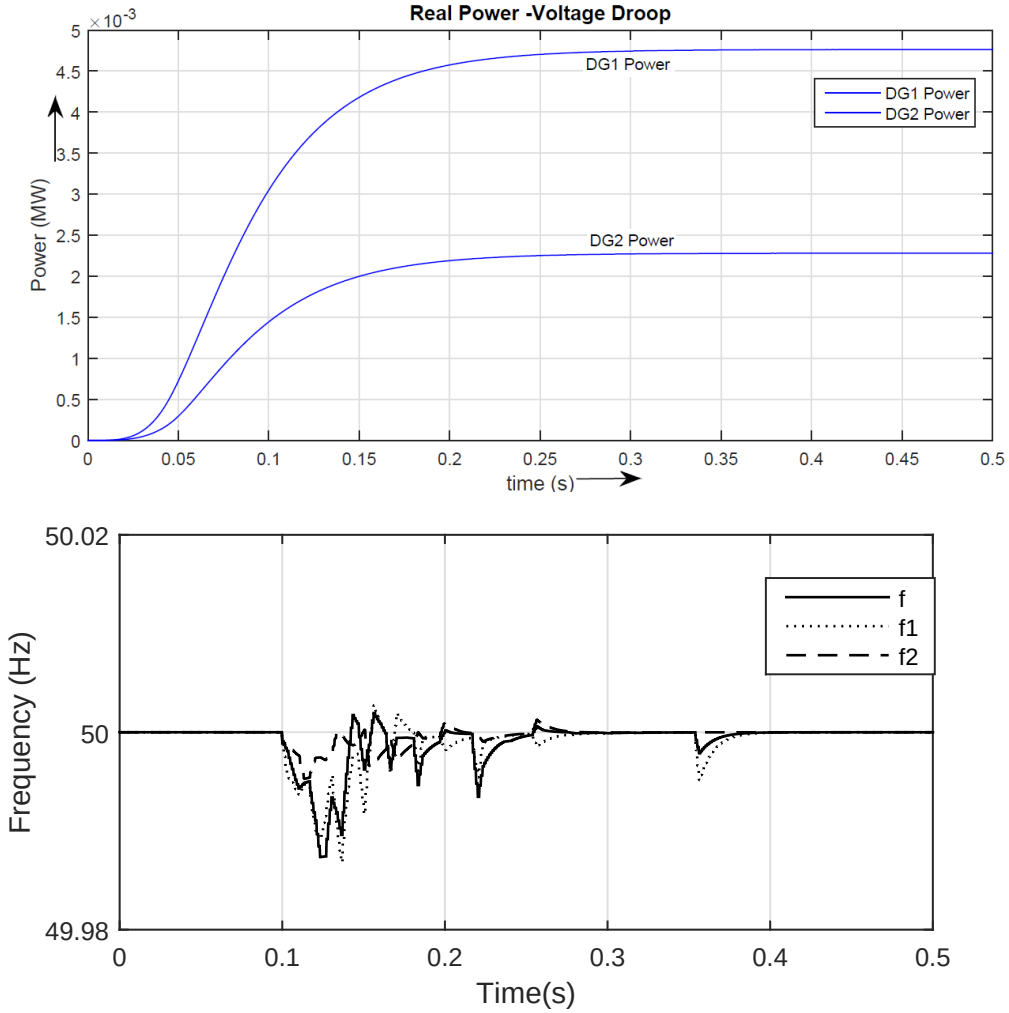


Figure 5.23: Real power sharing and frequency deviation in resistive lines

State feedback voltage control for phase - a is depicted in Figure 5.24, where the measured voltage follows the reference voltage without much deviation. Harmonic studies conducted on DG currents shows that all triplen harmonics are eliminated from DG output current. This clarifies the elimination of harmonic resistance term in the virtual resistance factor.

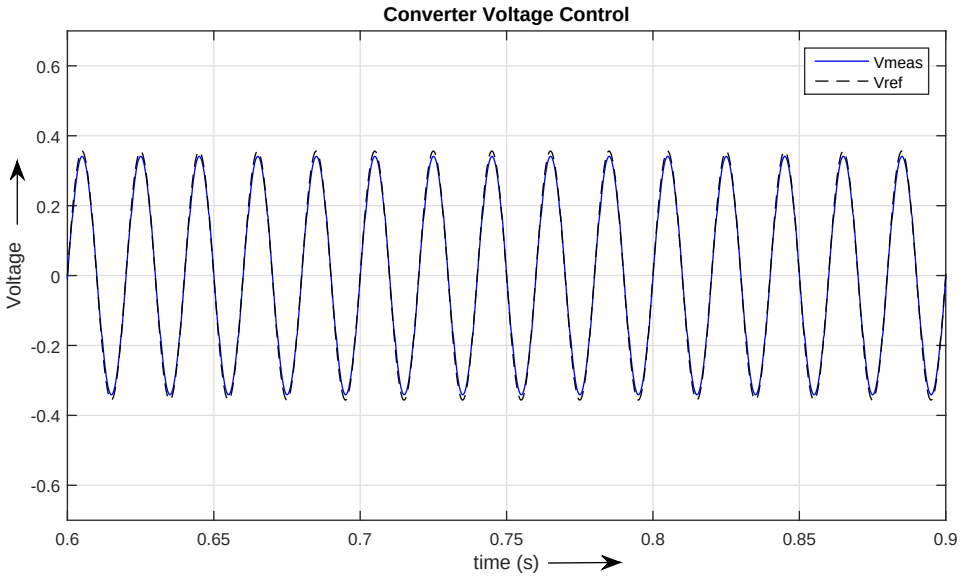


Figure 5.24: State feedback voltage control

Case II

An unbalanced resistive load is introduced at instant t = 3 s, in addition to impedance and non-linear load. Load sharing (Figure 5.25) is found to be comparatively accurate even under unbalanced conditions and variation in frequency is within acceptable limits and attains a steady-state value of 50 Hz at time, t = 3.06 s.

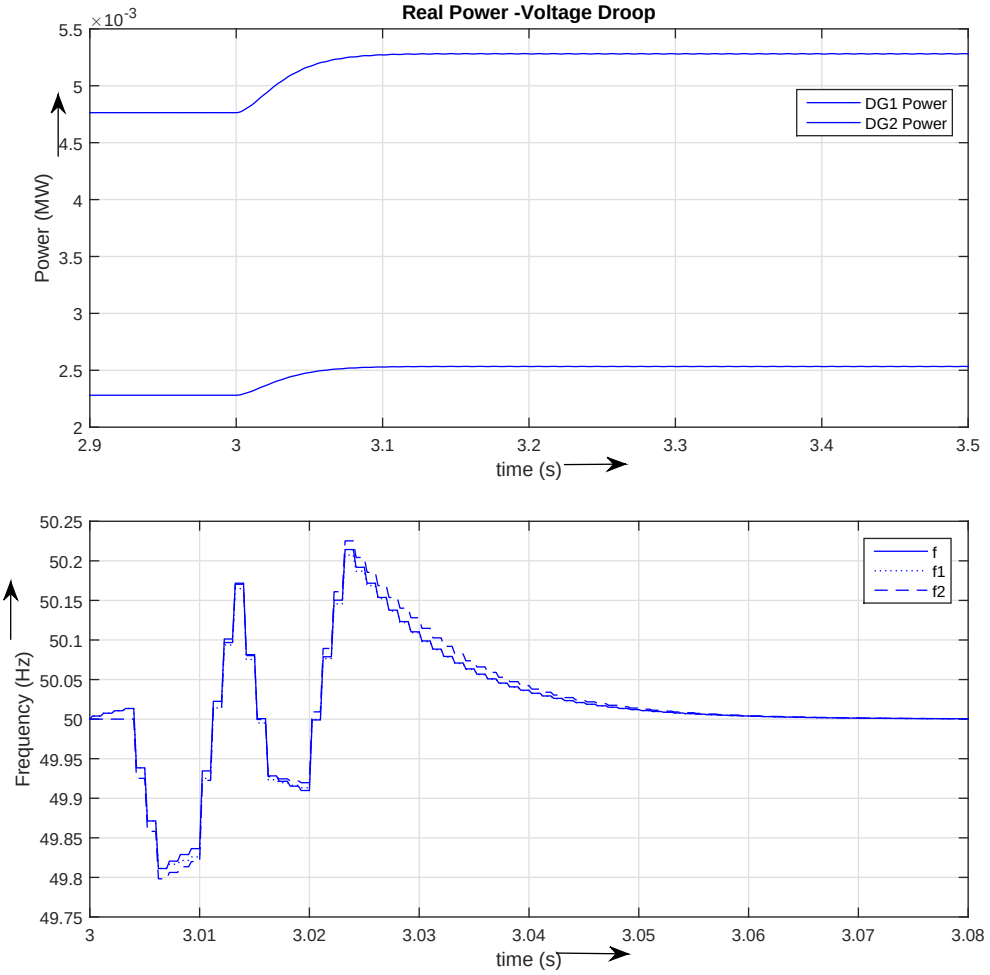


Figure 5.25: Real power sharing and frequency deviation with unbalanced load

Figure 5.26 illustrates the load current distribution among DGs, which is based on converter rating and load power requirements.

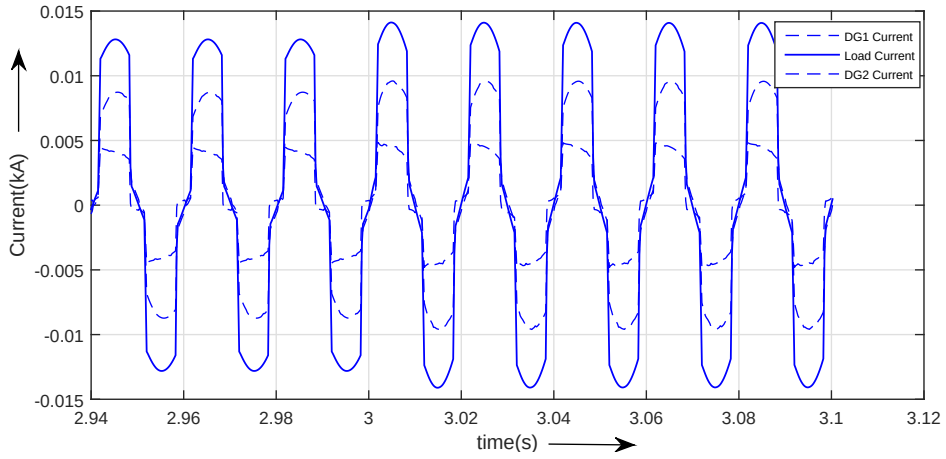


Figure 5.26: Load current sharing among DGs

Case III

In this case, a frequency dependent induction motor of 30 HP rating is connected along with load A at time t = 4.2 s to 4.5 s, to analyze the effectiveness of inverse angle droop control. Interestingly, DG and load frequency settles with negligible steady-state error in addition to acceptable overshoot in the transient region as illustrated in Figure 5.27.

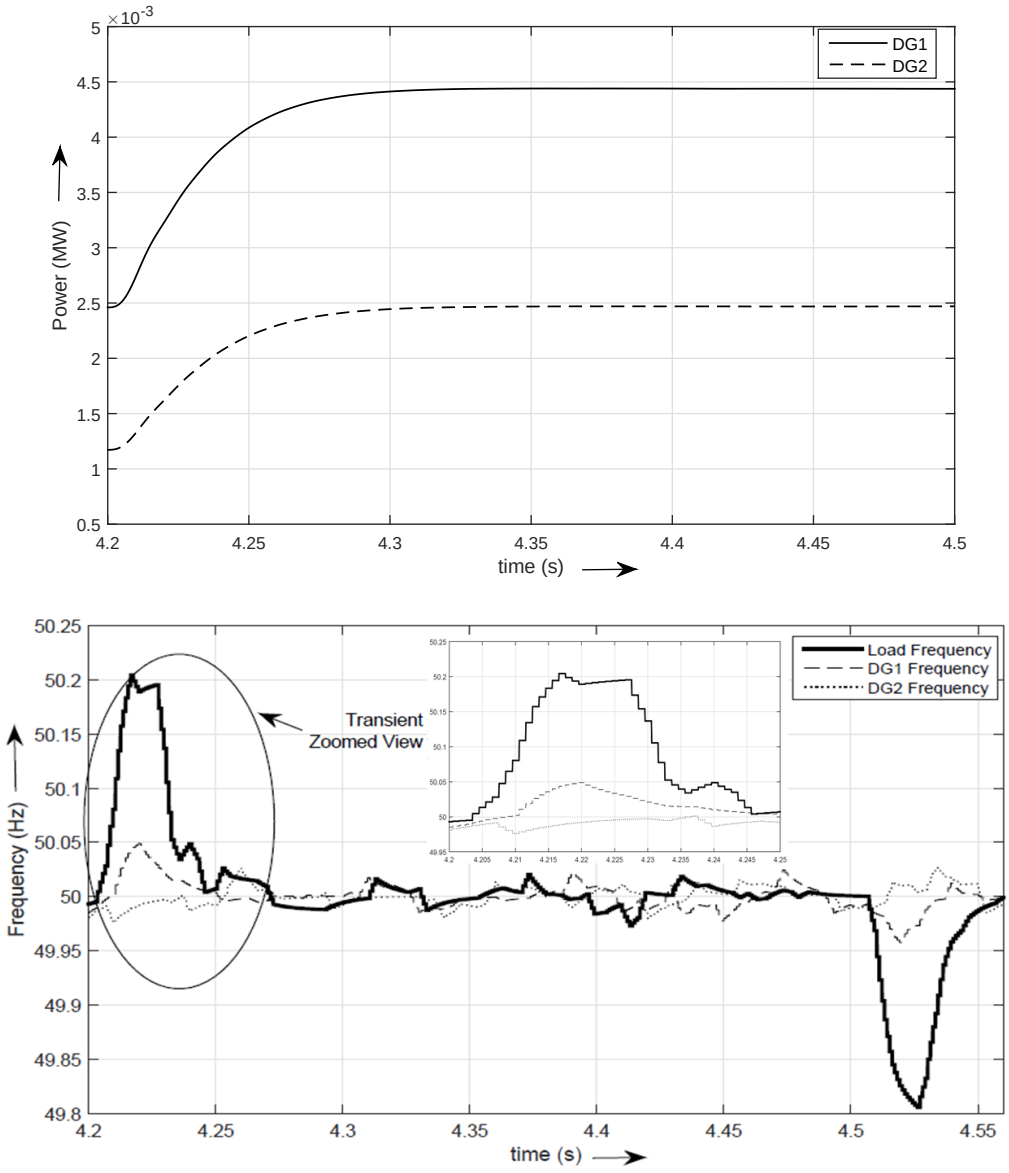


Figure 5.27: Real power and frequency under frequency dependent loads

Even though real power sharing among two DGs differs slightly from the expected value, it is more accurate than neglecting the virtual resistive term (Figure 5.27). In addition, modified PWM scheme effectively eliminates multiple of third order harmonics, an attractive feature needed in frequency dependent loads.

Table 5.7 gives the summary of real power sharing and the percentage deviation from expected value of real power in all the above case studies.

Table 5.7: Real power sharing among DGs

Case	P_L kW	P_{DG1} kW	P_{DG1} kW Deviation	P_{DG_2} kW	P_{DG_2} kW Deviation
I	7.02	4.74	-0.073	2.28	0.053
II	7.73	5.2	-0.046	2.53	0.046
III	6.83	4.43	0.12	2.4	0.12

Effect of Virtual Impedance on Angle Droop Control

This section illustrates the effect of virtual resistance in inverse angle droop control for low voltage resistive lines. It is clear from Table 5.8 that with the addition of virtual resistance to inverse angle droop control, total load power is accurately shared based on their power rating, but percentage error in power sharing is more in without using virtual resistance. The average percentage deviation in inverse angle droop and proposed control are 7.1 % and 1.2 % respectively, which implies that the real power distribution is improved by 5.9 % in proposed control. Frequency deviation is acceptable and falls in 50 $\pm$ 0.2 Hz range, which is considered as an added advantage of angle droop over frequency droop control.

Table 5.8: Effect of virtual resistance on droop control

Method	P_{DG_1} kW	P_{DG_2} kW	(P_{DG_1}/P_L)	(P_{DG_2}/P_L)
Inverse Angle Droop Control	4.96	2.15	0.709	0.307
Proposed Control	4.74	2.29	0.677	0.327

The virtual impedance cause a voltage drop in load voltage and this voltage

drop increases as the virtual impedance increases. However, the drop is negligible compared to the accuracy achieved in power sharing.

5.5 Conclusions

An effective droop control strategy for sharing common loads in converter interfaced parallel connected distributed generators fed islanded microgrid has been presented in this chapter. The proposed method utilizes the concept of conventional angle droop with an additional decoupling approach which can accurately share the non-linear, unbalanced or frequency dependent loads in medium voltage lines, where feeder line resistance are not negligible. In fact, compared to conventional angle droop and angle droop with transformation matrix methods, this method has improved real and reactive power sharing and the real power sharing is increased by 6 - 7 %. Simulation results and analysis verify the efficacy of proposed algorithm under different operating conditions. Moreover, this method offers better harmonic power sharing and avoids the use of additional secondary loops for voltage and frequency deviations. In addition, state feedback control with third harmonic injection PWM method offers better DC link utilization and lesser harmonic distortion in converter interfaced sources. Since the tests are conducted under highly non-linear loads, total harmonic distortion of load voltage was found to be 8 % under worst case, but THD is improved to 0.25 % under impedance and inertial loads.

Furthermore, a new control strategy for sharing load requirements in low voltage islanded microgrid with converter interfaced parallel connected distributed generators is described in the later section of this chapter. Since conventional angle droop control strategy cannot be applicable in dominant resistive networks where, X/R ratio is very small, an inverse angle droop with added virtual resistive impedance control is utilized for highly resistive rural distributed lines. Thus, the load sharing is achieved by controlling voltage and reactive power by angle droop

method. By subtracting a resistive drop proportional to DG output current, which has the effect of decoupling between active and reactive power, a more accurate rating based power sharing is ensured. In addition, the resistive term has an added advantage of effective system damping and inclusion of line impedance effect in load power sharing. Third harmonic injection based pulse width modulation scheme suppresses the effects of triplen harmonics during unbalanced condition, in addition to the effective DC link utilization under different load conditions. Moreover, lesser deviation in the network, as well as DG frequency, are attractive features of this method.

Chapter 6

Stability and Harmonic Issues in Converter Interfaced DERs

The nature of harmonics and the stability issues may be different in parallel connected converter interfaced DERs. Even though the harmonic distortion in individual converter is within the limits specified by IEEE 519 and IEC 61000.3.2, the interconnection may introduce stability issues. Although the resonance due to feeder impedance and the output filter capacitance can create stability issues in parallel connected converters, these effects can be eliminated to an extent by increasing the switching frequency of converter switches. This is because, switching at higher frequencies will reduce the output filter requirements drastically. With the reduced value of filter capacitor, the resonance area will shift to high frequency regions, where the magnitudes of individual harmonics are negligibly small. Even though the traditional Si IGBTs can switch up to a maximum of 15 kHz, recently introduced wide bandgap SiC devices can operate at 100 kHz and can have lower switching and conduction losses at such a high frequency. These characteristics allow the usage of high frequency semiconductors in grid connected converters. Section 6.1 explains the prime contribution of this chapter, i.e. the stability issues due to the controller interaction in grid interfaced parallel connected converters.

The controller interaction among outer power control loops is explained with the help of stability studies in MATLAB and a mitigating solution to eliminate the circulating currents is proposed [131]. Section 6.2 describes the second contribution of this chapter, where the suitability of closed loop SVPWM technique is tested with a DSTATCOM which is used to mitigate the harmonics produced by non-linear or unbalanced loads in a converter dominated islanded microgrid. In autonomous operation of a microgrid, the parallel connected converter fed DERs are expected to share the real and reactive load power requirement at the PCC. Common loads may have non-linear and/or unbalance behavior. The DSTATCOM can not only mitigate harmonics, but also satisfy the reactive power requirement in common loads and rectify unbalance problems. In [160], a control strategy is discussed to limit the flow of DSTATCOM surplus reactive power feeding back to distributed sources. In this chapter, a coordinated control strategy is proposed for DERs and DSTATCOM in an autonomous MG to provide adequate reactive demand management.

6.1 Controller Interaction in Grid Connected Converters

In this section, harmonics and stability issues in parallel grid connected converters in grid connected mode are analysed by connecting two voltage controlled DERs to the PCC. The significant reduction in output capacitor size in high frequency converters can reduce the harmonic interaction between filter capacitor and feeder cables. Controller interaction is still present in high frequency converters, where a PI regulated real power control loop of one converter interacts with the outer loop of other converters. The circulating currents in parallel converters destabilize the system and result in sustained oscillation in power. As the dynamic interaction between real power loops in both converters results in unnecessary oscillations in grid connected systems, a damping factor is essential in the real power loop to

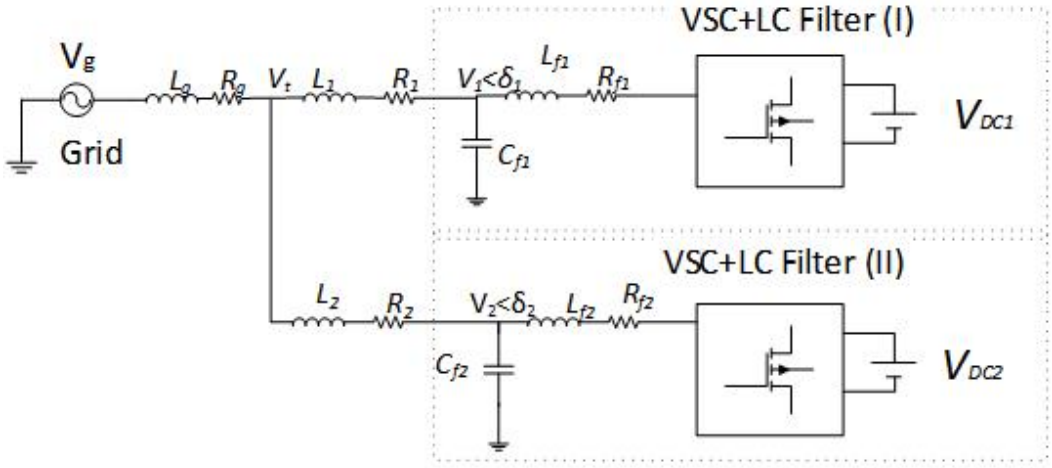


Figure 6.1: One line diagram of grid connected VSCs

eradicate sustained oscillations present in the active power feeding to the grid.

6.1.1 Stability Analysis of Grid Interfaced Parallel Connected VSCs

A three phase network, where two parallel voltage controlled converters are connected to the grid through feeder is depicted in Figure 6.1. A constant DC Link voltage is assumed for converters. L_g and R_g correspond to grid inductance and resistance. L_1, R_1 and L_2, R_2 represent the feeder impedance for converter 1 and 2 respectively. An LC type filter is utilized at the output of the converter to eliminate switching frequency harmonics, where L_f and C_f correspond to filter inductance and capacitance for different converters and R_f represents the converter losses.

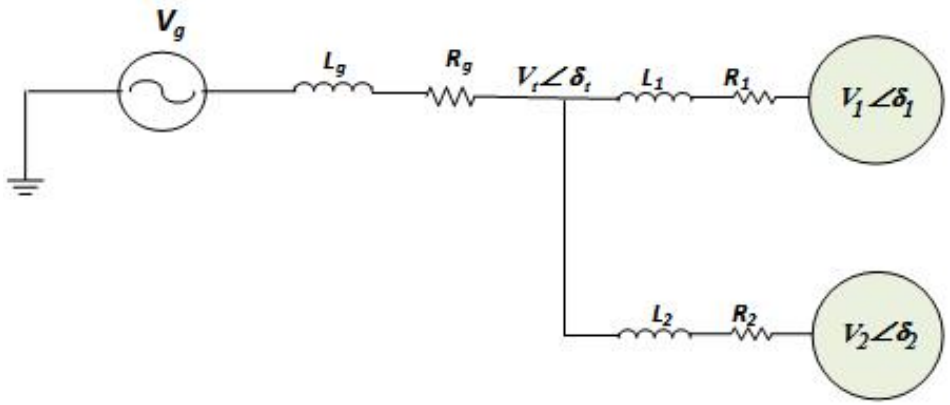


Figure 6.2: Single phase equivalent circuit of parallel connected VSCs

From the single line diagram shown in Figure 6.2, the real power delivered by the converters to grid can be written as mentioned in (6.1).

$$P_1 = \frac{V_1 V_t X_1 sin(\delta_1 - \delta_t)}{{R_1}^2 + {X_1}^2}$$

$$P_2 = \frac{V_2 V_t X_2 sin(\delta_2 - \delta_t)}{{R_2}^2 + {X_2}^2} \tag{6.1}$$

A system transfer function and controller transfer function are necessary to analyse the time domain response of individual converters and the controller interaction among them. The outer loop system transfer function can be written as

$$\frac{k}{s + \alpha} = \frac{k}{s + \frac{R_1}{L_1}} \tag{6.2}$$

Step response of an individual system with PI and PID controller is shown in Figure 6.3.

Results verify that both PI and PID controller have a satisfactory response for outer loop control of a VSC. Note that the effect of controller interaction is not incorporated in this case.

The interaction between the controllers can be modelled by feeding back a part

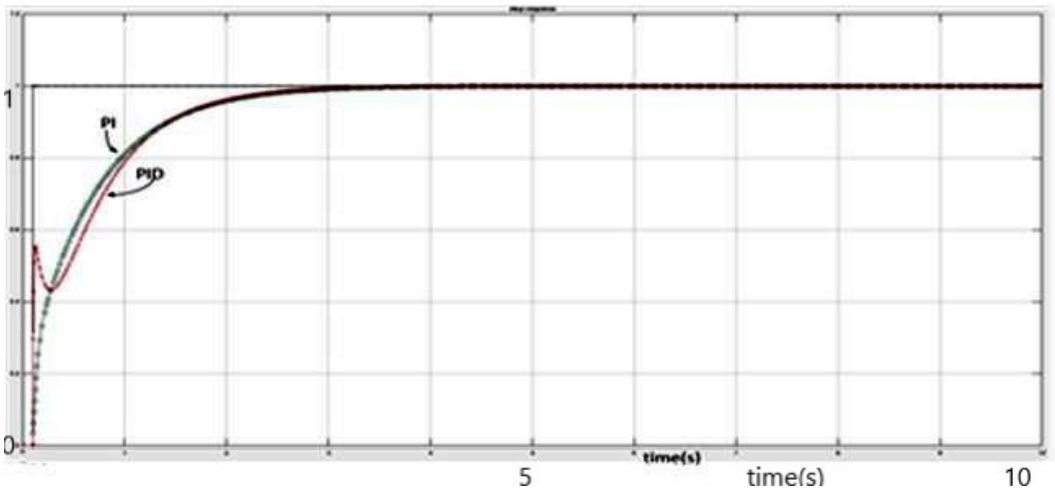


Figure 6.3: Step response of VSC real power with PI and PID controller

of converter 1 real power to converter 2 and vice versa as given in (6.3). In reality, the interconnection of controller algorithm is difficult due to excessive communication requirements. In addition, it creates a delay in converter fast switching operation. During parallel operation, this may lead to sustained oscillations which cause unstable condition.

$$P_1 + x_2 P_2 = \frac{V_1 V_t X_1 sin(\delta_1 - \delta_t)}{{R_1}^2 + {X_1}^2}$$

$$P_2 + x_1 P_1 = \frac{V_2 V_t X_2 sin(\delta_2 - \delta_t)}{{R_2}^2 + {X_2}^2} \tag{6.3}$$

Since the angle difference $\delta_1 - \delta_t$ and $\delta_2 - \delta_t$ are very small, $sin(\delta_1 - \delta_t) \approx \delta_1 - \delta_t$, $sin(\delta_2 - \delta_t) \approx \delta_2 - \delta_t$. Furthermore, in case of feeder lines with high X/R ratio, R_1 and R_2 can be assumed as 0. Also assuming the angle at PCC $\delta_t \approx 0$, real power can be rewritten as

$$P_1 \propto (\delta_1 - x_2 P_2)$$

$$P_2 \propto (\delta_2 - x_1 P_1) \tag{6.4}$$

This strategy is explained in Figure 6.4, where $\frac{k}{s+\alpha}$ is the system transfer function.

A part of converter 2 real power is fed back to converter 1 real power. As the controller is the mirror image of the system, the same factor is subtracted inside the controller. This factor is treated as a disturbance signal inside the controller. PI or PID control can be used as real power control as shown in Figure 6.5. A similar strategy has been applied to converter 2, where a part of converter 1 power is used as disturbance signal. The step response of the above mentioned system with PI and PID control is illustrated in Figure 6.6.

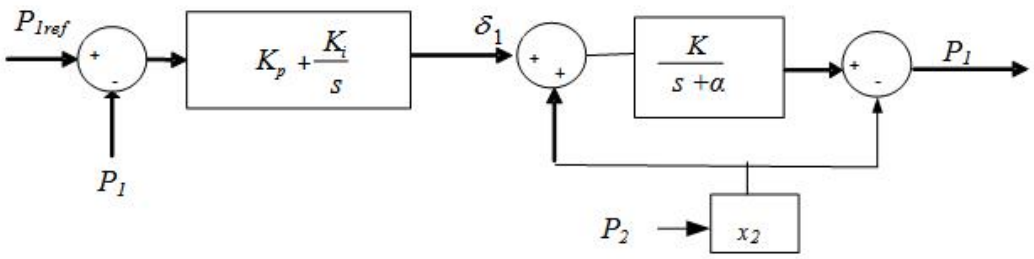


Figure 6.4: Outer loop real power- closed loop operation

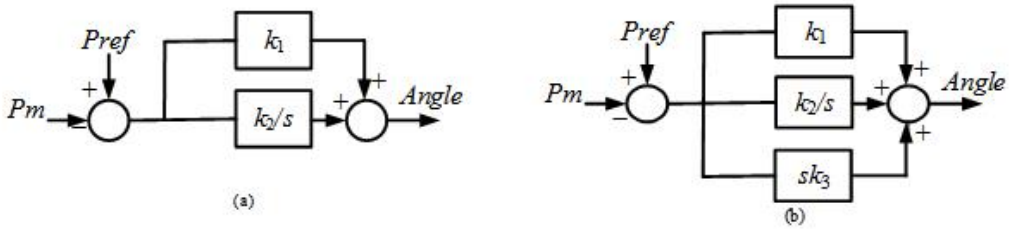


Figure 6.5: Outer real power loop with (a) PI control (b) PID control

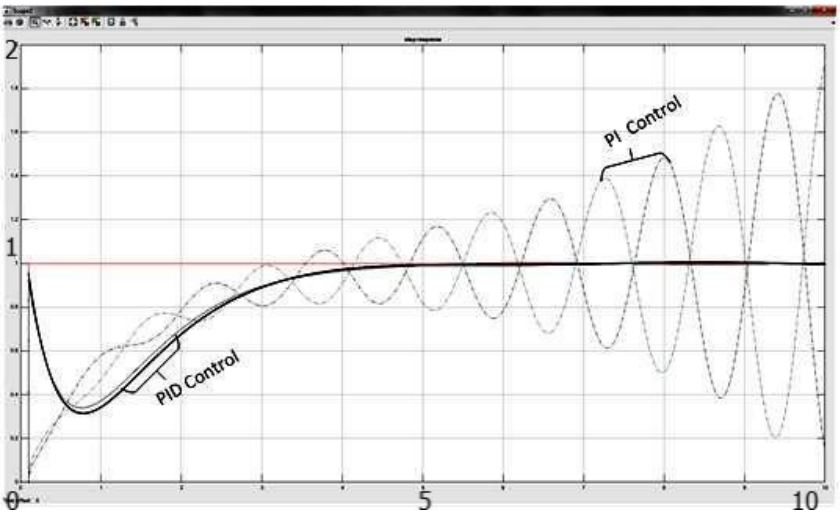


Figure 6.6: Step response of parallel connected VSC real power with PI and PID

As seen from the response with PI control, P_1 and P_2 become unstable. Even though the PI control work for an individual converter operation, the interaction between the control loops may lead to unstable operation. These unnecessary oscillations can be damped out by introducing a damping factor to the system. Here a PID control is proposed to damp down the resonance oscillation caused by the interaction of the parallel converter. Moreover, it limits the peak overshoot and steady state error to an acceptable range. A compromise between peak overshoot and settling time is inevitable for active power loop in parallel operation of the converter.

6.2 Reactive Power Management in an Islanded MG

Consider an islanded MG dominated by converter interfaced DERs as shown in Figure 6.7, where $R_{fi} + jL_{fi}$ is the feeder impedance for i^{th} DER. It has been assumed that n number of DERs are connected at the PCC and each DER is a power electronic converter interfaced RES. A DSTATCOM is connected at the PCC

to achieve reactive power support for loads in addition to harmonic compensation. A DSTATCOM consists of a three phase VSI and a passive LC (L_f, C_f) filter is connected at the output side of VSC to suppress the harmonics generated by the high frequency switching of semiconductor switches. $P_G + jQ_G$, $P_L + jQ_L$ and $P_D + jQ_D$ are the real and reactive power of MG, load and DSTATCOM respectively. Common load can be linear, non-linear or inertial.

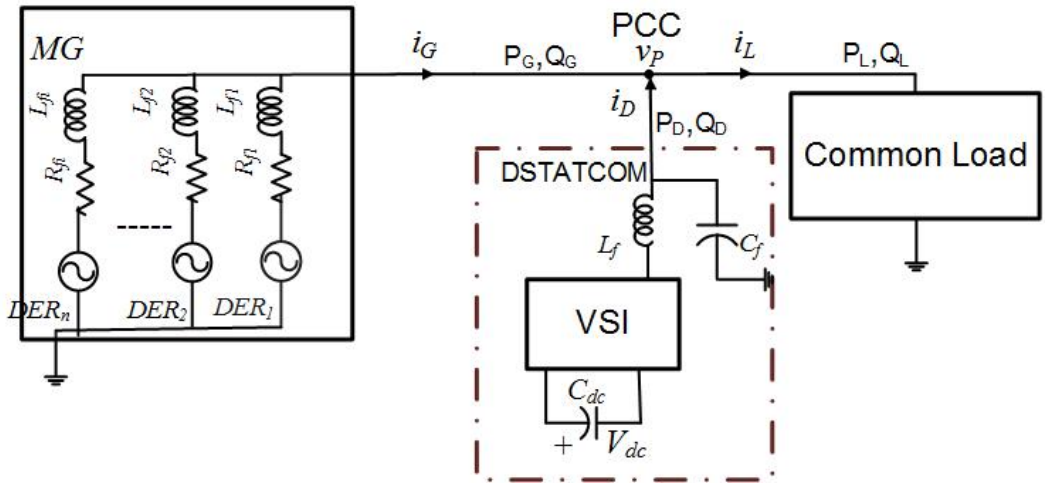


Figure 6.7: Single line diagram of DSTATCOM connected to an islanded microgrid

In an islanded mode, the DERs share the common load demand using angle and voltage droop control as given in (4.5). The real and reactive power droop will determine the angle and magnitude of reference voltage respectively, where, $V_i \angle \delta_i$ is the reference angle, $P^*_{Gi} + jQ^*_{Gi}$ and $P_{Gi} + jQ_{Gi}$ are the reference and measured quantities of MG power respectively and i represents the i^{th} DER. Each DER is assumed as a controllable DC source fed through a three phase AFE converter. A DLQR based state feedback control is used for the individual converter control as described in Chapter 5. In an islanded microgrid, the voltage droop control is used to share the common load reactive power demand and the DERs can share a specified amount of reactive demand based on its rating. But this will cause PCC

voltage to drop below permissible voltage standards. Thus a reactive power management strategy is necessary for converter fed DER dominated MGs to mitigate the PCC voltage stability issues [161]. In a strongly coupled microgrid, the PCC voltage drop also depends on power decoupling factor as mentioned in Chapter 5. Therefore, the voltage drop at PCC has to be limited to maintain the voltage stability in autonomous MGs.

6.2.1 Role of DSTATCOM in an Islanded MG

In an islanded microgrid, the purpose of a DSTATCOM is twofold. Firstly it can mitigate the harmonics produced by the common non-linear loads. In addition, DSTATCOM plays an important role in voltage regulation at PCC by controlling the reactive power flow in the MG. The DSTATCOM draws a small amount of power from the grid to compensate for the internal losses. The capacitor is able to supply the reactive power and the harmonic components to compensate for the distorted waveform due to non-linear loads based on DSTATCOM rating. In this subsection, three case studies are considered. In the first case, the DSTATCOM is providing harmonic compensation for an autonomous MG and satisfies the entire reactive load demand. The controller is designed such that, the DSTATCOM is supposed to satisfy the entire reactive power demand of common loads and the DERs are designed to meet the active power demand. In the second case, the DSTATCOM provides reactive power support to DERs using the coordinated control strategy in addition to harmonic mitigation. Reactive load demand is shared among DERs and DSTATCOM, but the real power demand is distributed among DERs. In the third case, DSTATCOM is expected to provide only harmonic mitigation functionality to an islanded MG without any reactive power support.

Case I: DSTATCOM Provides Harmonic Mitigation and Satisfies the entire Reactive Power Demand in an Islanded MG

Let us assume that, the DERs are solely responsible for meeting the real power common load demand of an autonomous MG. Then, the DERs are expected to share the common load real power demand using decentralised angle droop method. The reactive power demand of local loads is satisfied by individual DERs. In some cases, the DSTATCOM is expected to satisfy entire reactive common load demand, in addition, to providing harmonic compensation at the PCC of a MG. Harmonic mitigation capability is achieved by eliminating the unwanted dominant higher order harmonics from the DER currents such that the fundamental component of the load current is supplied by DERs and the harmonic components due to non-linear loads are supplied by DSTATCOM. In order to satisfy the entire reactive common load demand, the DSTATCOM voltage reference is calculated with the help of a PI controller, which regulate the effective reactive power demand from DERs to zero as given below.

$$V_p = K_{pD}(0 - Q_G) + \frac{K_{iD}}{s}(0 - Q_G) \tag{6.5}$$

where Q_G is the reactive power requirement from DERs, K_{pD} and K_{iD} are the proportional and integral coefficients of the controller. In this case, the reference value of reactive power demand from DERs is zero since the DERs are expected to meet local load reactive demand.

Case II: DSTATCOM Provides Harmonic Compensation and Satisfies a Portion of Reactive Power Demand

Assume that, the DERs can supply a specified amount of load reactive power based on their ratings and the DSTATCOM will supply the reactive power shortfall of

the common loads connected to the PCC. This can be achieved by regulating the reactive power supplied by DERs to a pre-specified value. This value depends on DERs reactive power rating and the permissible drop in PCC voltage. Again a PI controller is used, the output of which is the DSTATCOM reference voltage magnitude (V_p). This is given by

$$V_p = K_p(Q_{Gref} - Q_G) + \frac{K_i}{s}(Q_{Gref} - Q_G) \tag{6.6}$$

where Q_{Gref} is pre-specified portion of Q_G (see Figure 6.7). Now the V-Q droop for i^{th} DER is given by

$$V_{refi} - V_i = n_i \times Q_{Gi}$$

Now if, $V_{refi} - V_i$ = 0.95 $\times V_{refi}$,

$$Q_{Gi} = \frac{0.95 \times V_{refi}}{n_i}$$

Then the pre-specified reference value for reactive power requirement from DERs is given by

$$Q_{Gref} = \sum_{i=1}^{n} Q_{Gi}$$

In Cases I and II mentioned above, the DSTATCOM regulates the PCC voltage to a set of balanced sinusoidal voltages. Since the DERs also produce balanced sinusoidal voltages, the current flowing though the DERs and PCC will also be balanced sinusoids. This means that the harmonic and unbalanced currents will be circulated by the DSTATCOM. Additionally, it can successfully meet the necessary reactive power requirements without exceeding the permissible PCC voltage drop.

Case III: DSTATCOM Provides only Harmonic Mitigation Capability to an Islanded MG

In this case, it has been assumed that, DSTATCOM is capable of providing only harmonic compensation to an islanded MG and it is not responsible for supplying any portion of the load reactive power. Therefore, the reference voltage magnitude V_p can be set as 1 pu as given in [43].

6.2.2 Closed Loop Space Vector Modulated Voltage Control for DSTATCOM

The overall control for DSTATCOM is illustrated in Figure 6.8. The reference voltage magnitude V_p is obtained from reactive power control as discussed in previous section. Moreover, the DSTATCOM draws a small amount of power from the grid to compensate for the internal losses. The voltage across DC capacitor is regulated using a PI controller to maintain the required power flow to the PCC. The capacitor will now be able to supply the harmonic components to compensate for the distorted waveform due to non-linear loads. The output of this PI controller gives the desired angle to generate the reference voltage at PCC.

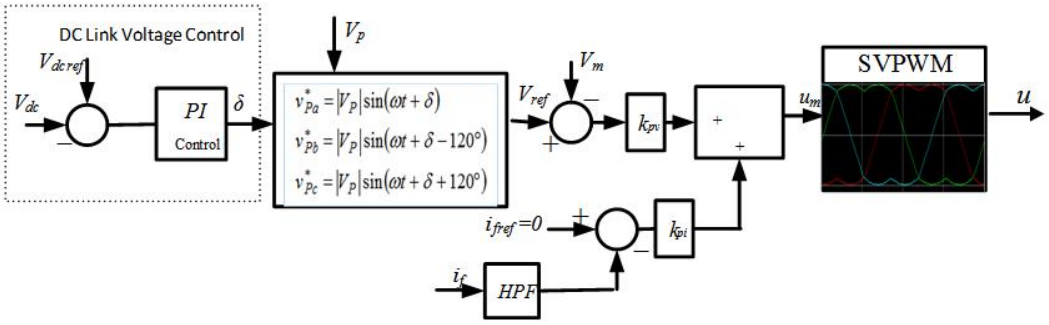


Figure 6.8: Control algorithm for DSTATCOM

$$\delta = K_p(V_{dcref} - V_{dc}) + \frac{K_i}{s}(V_{dcref} - V_{dc}) \tag{6.7}$$

where,V_{dcref} and V_{dc} are the reference and measured voltage across DC capacitor, K_p and K_i are the proportional and integral gains of PI controller respectively. The desired three phase reference voltages at the PCC can be defined as,

$$\begin{aligned} v_{Pa}* &= |V_p|sin(\omega t + \delta) \\ v_{Pb}* &= |V_p|sin(\omega t + \delta - 120^\circ), \\ v_{Pc}* &= |V_p|sin(\omega t + \delta + 120^\circ) \end{aligned} \tag{6.8}$$

where, V_p is the magnitude and ω is a fixed frequency of 50 Hz. Note that in grid connected applications, the variation in ω is negligible as the frequency is synchronised to grid frequency. But in islanded grids, the variation in network frequency with conventional frequency droop control necessitates additional controller to regulate the frequency to 50 Hz. One such control is an isochronous controller, which consists of a derivative factor sensitive to system disturbances [43]. As discussed earlier, angle droop control has an attractive feature of negligible frequency variations, the necessity of additional controller for eliminating the network frequency variations can be avoided. The obtained voltage magnitude and angle are considered as the reference voltage for inner loop voltage control. DSTATCOM is operating in voltage control mode and the state feedback regulator based CLSVPWM is chosen as the controller. The CLSVPWM controller is discussed in Chapter 2. It is clear from [43] that, more effective DC link voltage utilization is possible in a DSTATCOM, by adopting the closed loop space vector modulation based voltage control. Furthermore, the total harmonic distortion is low due to the symmetrical sequencing of switching vectors. In addition, the reduced peak to peak converter current ripple results in a lower value of converter side filter inductance L_f which in turn leads to reduced losses.

6.3 Simulation Study

6.3.1 Controller Interaction in Grid Interfaced Parallel Converters

In this section, simulation studies are conducted using PSCAD for grid connected converters to demonstrate the interaction between control loops of each converter when connected in parallel. The data chosen for grid and converters are given in Table 6.1.

Table 6.1: System under simulation study

System Quantities	Values
PCC Voltage	11 kV (L-L)
Grid Impedance	R_g = 1.21 Ω, L_g = 38.5 mH
Feeder Impedance	
Converter 1	R_{f1} = 0.25 Ω, L_{f1} = 12 mH
Converter 2	R_{f1} = 0.21 Ω, L_{f1} = 10 mH
Converter 1 Rating	500 kW
Converter 2 Rating	250 kW
Load	R_g = 1.21 Ω, L_g = 38.5 mH
Switching Frequency f_{sw}	100 kHz
State Feedback Control	
Converter 1 - Voltage Gain	93 kV/MVAr
Converter 1 - Current Gain	150.5 rad/kWs
Converter 2 - Voltage Gain	93 kV/MVAr
Converter 2 - Current Gain	150.5 rad/kWs

Each converter is switched at a high frequency of 100 kHz to analyse the harmonic effects at parallel connected converters at the high frequency range. Due to the decreased value of 2 μF filter capacitor, the interaction with cable inductance is found to be negligible in high frequency converters. Two different case studies and corresponding results are presented.

Case-1: Converter 1 and 2 with the independent PI controller

Each converter is controlled by an independent controller. The outer real power control loop utilizes PI control to regulate the active power delivered to the grid. Even though, the controller follows the reference value until steady state, the circulating current produces oscillations in converter currents, which in turn results in oscillating real power. These oscillations lead the system to instability as depicted in Figure 6.9(a).

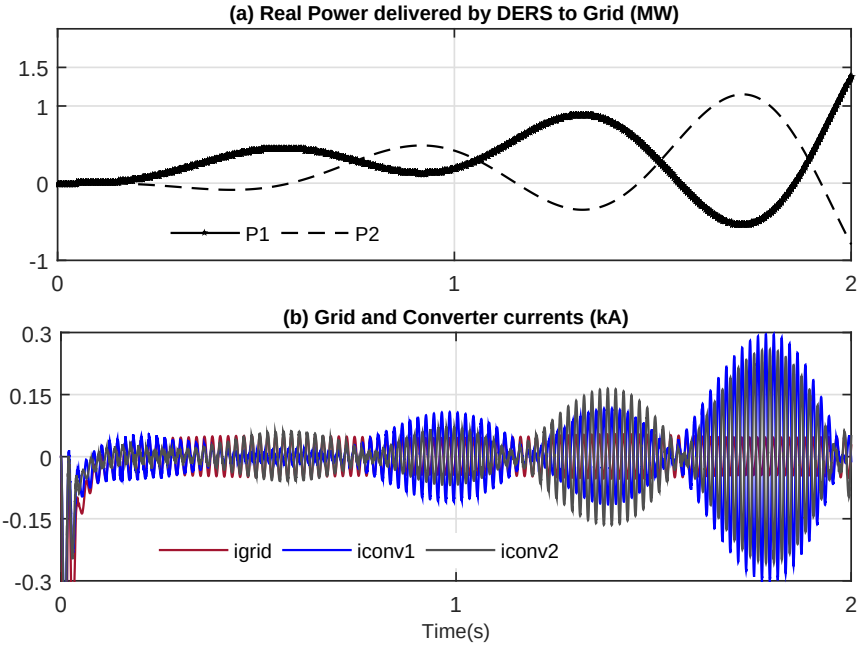


Figure 6.9: Converter 1 and 2 with real power - PI control (a) real power (b) grid and converter currents

Due to filters used for measuring real power, the system order and delay have been increased, which in turn make the closed loop complex and uncontrollable by PI. The grid and converter circulating currents are shown in Figure 6.9(b), clearly reveal that a constant current flowing to the grid, but the current circulating through converters eventually adds up in grid current. Since the integrator part adds

this circulating current over a period which results in sustained oscillations in the parallel system. Even though the resonance frequency is falling in the range of 2 - 9 kHz, the harmonics are not dominant in this range, giving a grid voltage and current THD of 0.56 % and 2.5 % respectively.

Case-2: Converter 1 and 2 with independent PID controller

As clear from the previous subsection that, the sustained oscillations in parallel connected converters lead to an unstable integrated system. Therefore, a damping must be incorporated in the controller for ensuring stability. Hence, a damping factor is introduced in the active power control loop to mitigate the unnecessary oscillations in the real power, which in turn controls the circulating currents. Converter 1 and 2 are supplying 400 W and 200 W to the grid respectively as depicted in Figure 6.10 (a).

The resulting voltage reference angle is depicted in Figure 6.10 (b), which follows the same trend as the real power. Furthermore, phase - a grid and converter currents verify that the oscillations in converter currents are damped out, which results in a stabilized system. The maximum overshoot and the steady state error lies within the limits as per grid requirements. Moreover, grid voltage and current THD is found to be 0.45 % and 3.6 % respectively. The amplitude of harmonics present around the resonant frequency is very small and thus eliminates the necessity of individual passive or active damping methods. This, in turn, reduces the loss in overall system, in addition to reduced losses in highly efficient fast switching wide bandgap power converters.

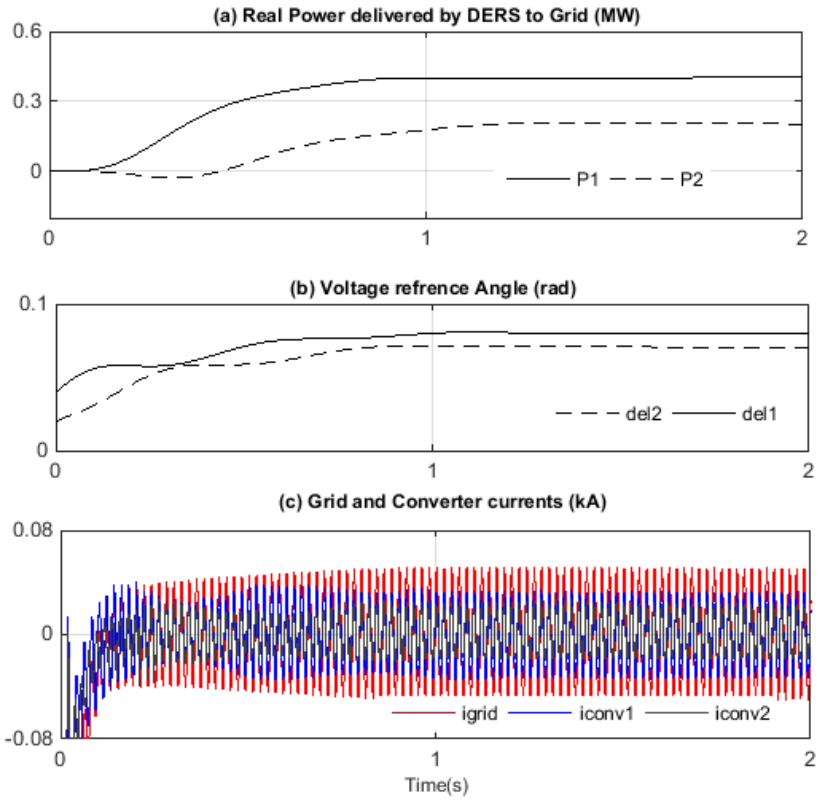


Figure 6.10: Converter 1 and 2 with independent PID control (a) active power feeding to grid (b) voltage angle reference (c) grid and converter currents

6.3.2 DSTATCOM Operation in an Islanded MG

A simulation study is carried out in PSCAD/EMTDC software to validate the effectiveness of DSTATCOM in an islanded MG. The real and reactive power sharing among DERs are achieved by angle and voltage droop respectively. The system parameters under simulation study are given in Table 6.2. Two cases have been considered as described below.

Table 6.2: System under simulation study-DSTATCOM in an islanded microgrid

System Quantities	Values
PCC Voltage	11 kV (L-L)
Switching Frequency	50 Hz
Feeder Impedance DER 1 DER 2	 R_{f1} = 0.1 Ω, L_{f1} = 3.18 mH R_{f2} = 0.1 Ω, L_{f2} =9.5 mH
DER 1 Rating	2 MVA
DER 2 Rating	1 MVA
DSTATCOM	
Converter Losses R_f	0.001 Ω
Filter Capacitor C_f	50 μF
Filter Inductor	33 mH
DC Link Voltage V_{dc}	14 kV
Switching Frequency f_{sw}	2.5 kHz

Case I: DSTATCOM Provides Harmonic Mitigation and Satisfies the Entire Load Reactive Power Demand

In this case study, the harmonic mitigation and VAR capability of DSTATCOM in an islanded microgrid are evaluated. Let us assume that, the DSTATCOM is supplying the entire reactive load demand and the DERs are only responsible for satisfying the real power demand of the common load. The MG includes two converter interfaced DERs and they are expected to share the real power in a ratio 2:1. The entire reactive power requirement of the common load is supplied by DSTATCOM and it is achieved by setting the MG reactive power reference Q_{Gref} = 0. Initially, the load power is assumed to be 1.2 + j0.26 (MW, MVAr) and the load is changed to 2.15 + j0.43 (MW, MVAr) at 1 s. The results are shown in Figures 6.11 - 6.14.

.1

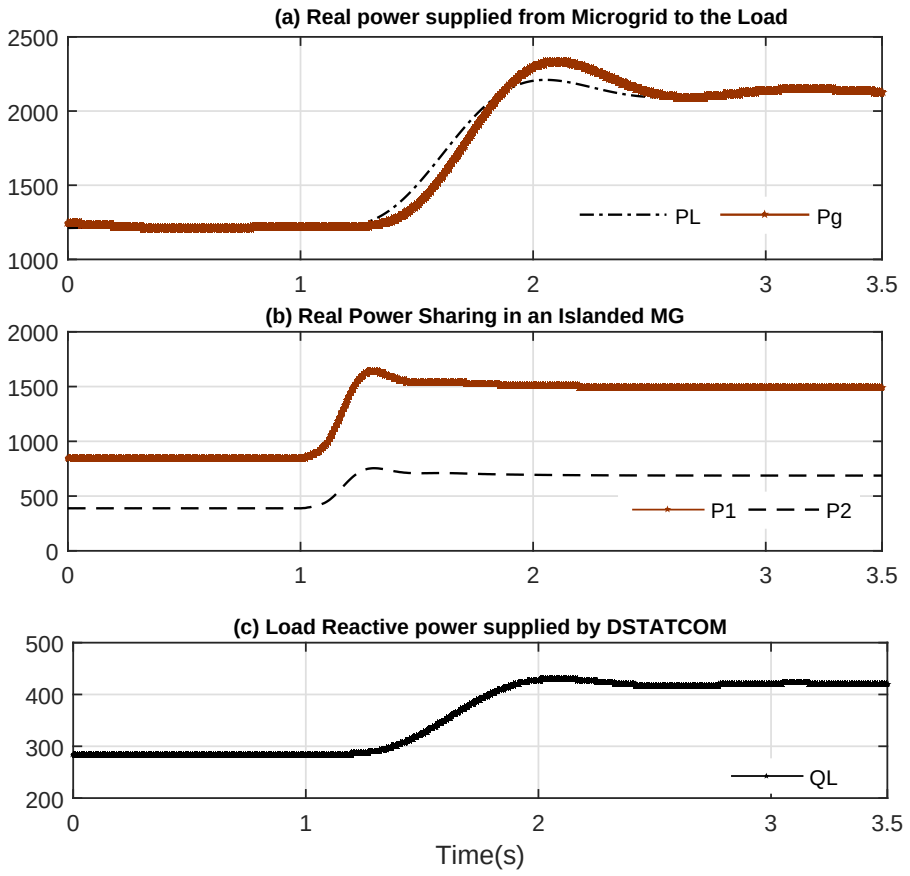


Figure 6.11: Real and reactive power flow in an islanded microgrid

It is clear from Figure 6.11 that the load real power demand is shared by DERs in the expected ratio of 2:1. Therefore, the entire real power demand of common load is supplied by DERs. Also the load reactive power demand is 260 kVAr before the load change and 430 kVAr after load change is supplied by the DSTATCOM in its entirety.

Figure 6.12 depicts the phase - a MG, load and DSTATCOM currents respectively.

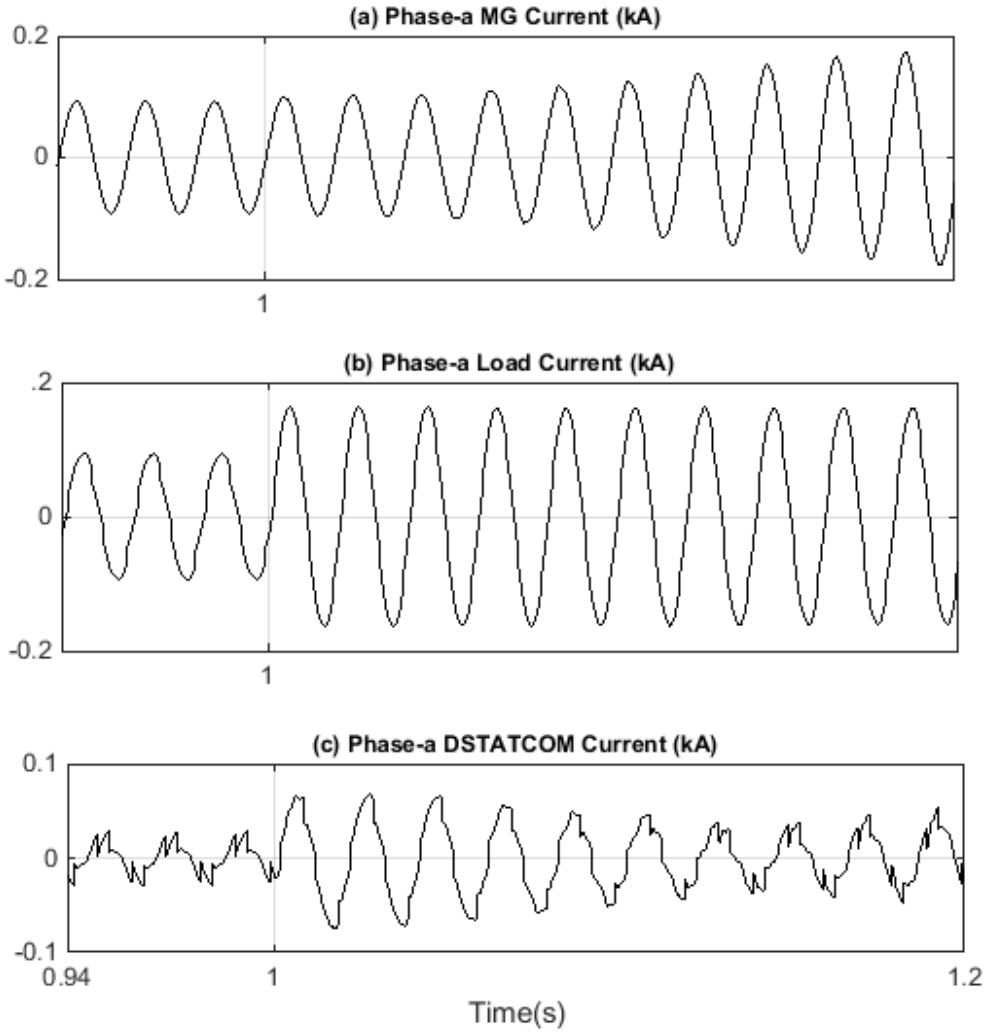


Figure 6.12: Phase - a (a) MG current (b) load current (c) DSTATCOM current

It is evident that DERs are supplying only the fundamental component of load current and the harmonic elements are supplied by the DSTATCOM. Figure 6.13 shows that, DC link voltage controller follows its reference value of 14 kV and delivers the required voltage angle reference value for state feedback voltage controller. PCC voltage is regulated using DLQR as depicted in Figure 6.13 (c) and

the voltage is regulated to approximately 1 pu (9 kV).

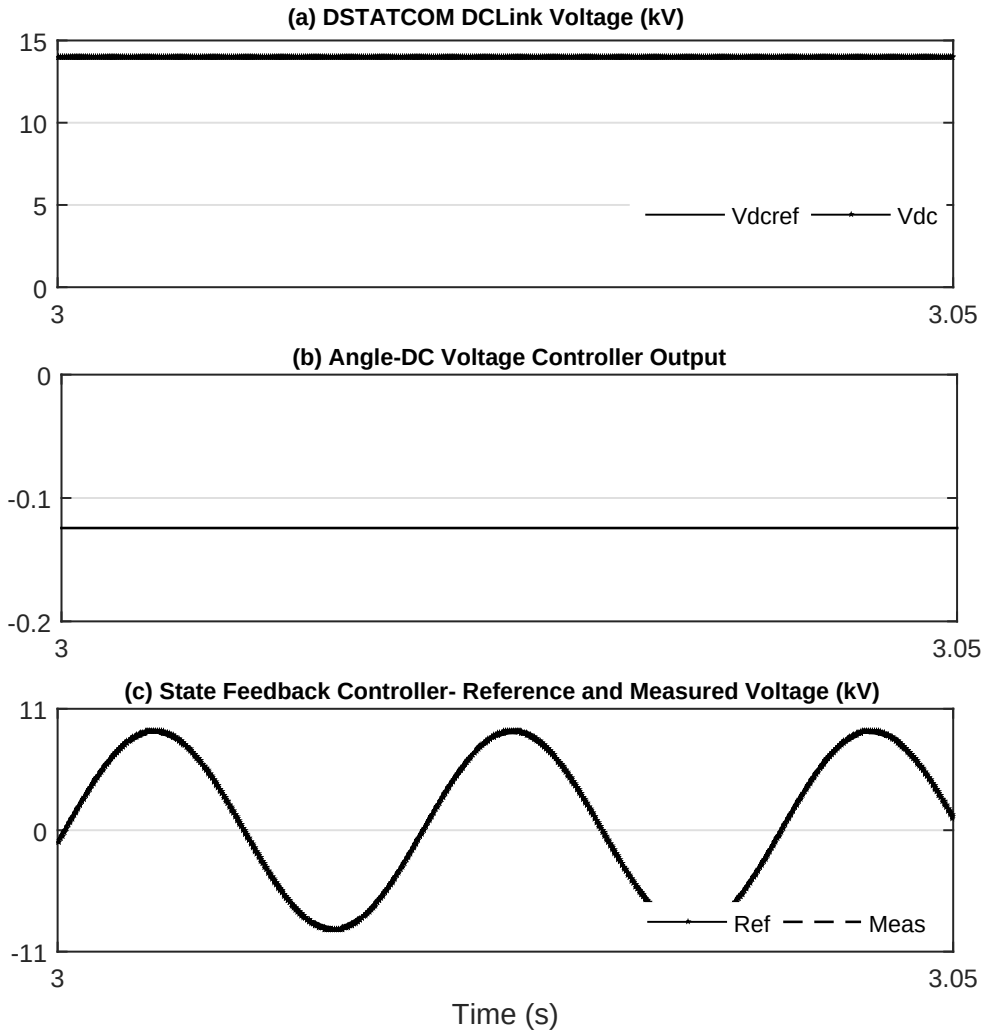


Figure 6.13: Controller operation in DSTATCOM (a) DC link voltage (b) angle obtained from DC link controller (c) state feedback control

The switching signal generated from CLSVPWM block is illustrated in Figure 6.14. Although the reference input signal miss the triangular carrier around the peak values, the modulation signal generated from SVPWM block scarcely miss

the carrier signal. Thus, a 15 % more DC link voltage utilization has been obtained from CLSVPWM.

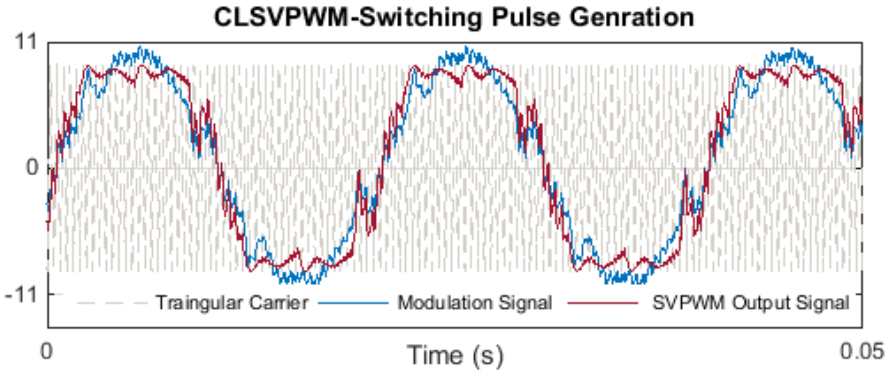


Figure 6.14: Modulation signal generation from CLSVPWM block

Case II: Coordinated control Strategy among DSTATCOM and DERs for meeting the reactive power load demand of Islanded MG

In this case, the coordinated control strategy for effectively meeting reactive power demand in an MG is evaluated under different loading conditions. Initially, let us assume that the total reactive power demand in an MG is satisfied by DSTATCOM by setting Q_{Gref} as zero. The voltage at PCC is shown in Figure 6.15 (a), which verifies that the drop in terminal voltage is only 2.2 %.

At time t = 3 s, the MG reference reactive power, Q_{Gref} is set as 0.26 MVAr. Accordingly, the PCC voltage has dropped to 8.55 kV. The active and reactive power flow in the MG is shown in Figure 6.16, which clearly shows that the real and reactive power load demand is shared among DER_1 and DER_2 in 2:1 ratio. In this case, the main functionality of DSTATCOM is to provide harmonic mitigation capability to islanded MG. Therefore, the DERs satisfy the entire the real demand and the reactive power demand is hared between the DERs since the DSTATCOM

supply any, as illustrated in Figure 6.16.

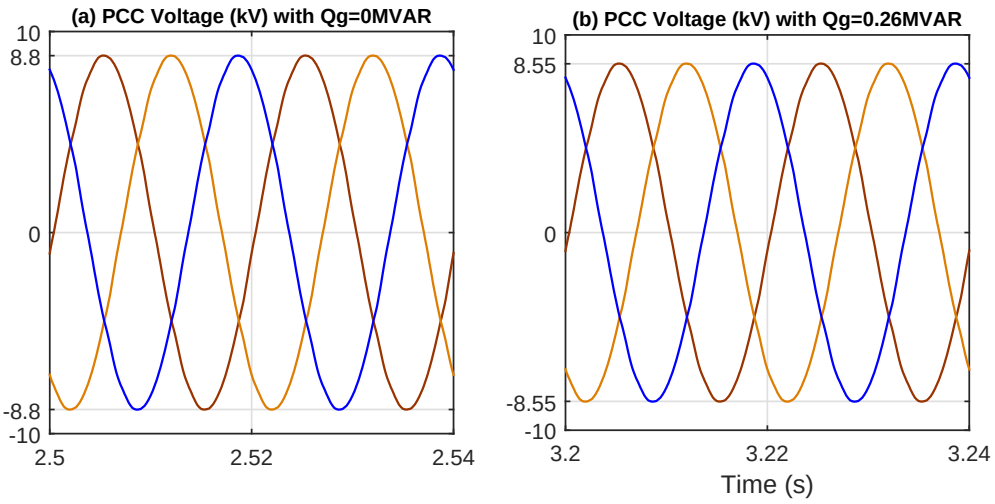


Figure 6.15: PCC voltage (a) with no reactive power supply from MG (b) coordinated reactive power supply from MG and DSTATCOM

At time t = 3.5 s, the reactive load demand is increased above MG VAR rating. The maximum reactive power can be supplied by an MG with a permissible PCC voltage drop of 5 % is considered as MG VAR rating. Since Q_{Gref} remains unchanged, the DSTATCOM starts supplying DERs reactive power shortfall. Thus, DERs and the DSTATCOM supply a reactive power of Q_G = 0.26 MVAr and Q_D = 0.23 MVAr respectively.

Note that the DSTATCOM reactive power is nil till time t = 3.5 s. At time t = 3.5 s, the load demand is increased such that, the DSTATCOM starts supplying the additional reactive load power requirement. Thus, a pre-specified amount of total reactive power can be supplied by DERs and the power shortfall in reactive load demand is satisfied by the DSTATCOM. The percentage voltage drop has been calculated from the PCC voltage as shown in Figure 6.15. It remains same as 5 %, even during a load change.

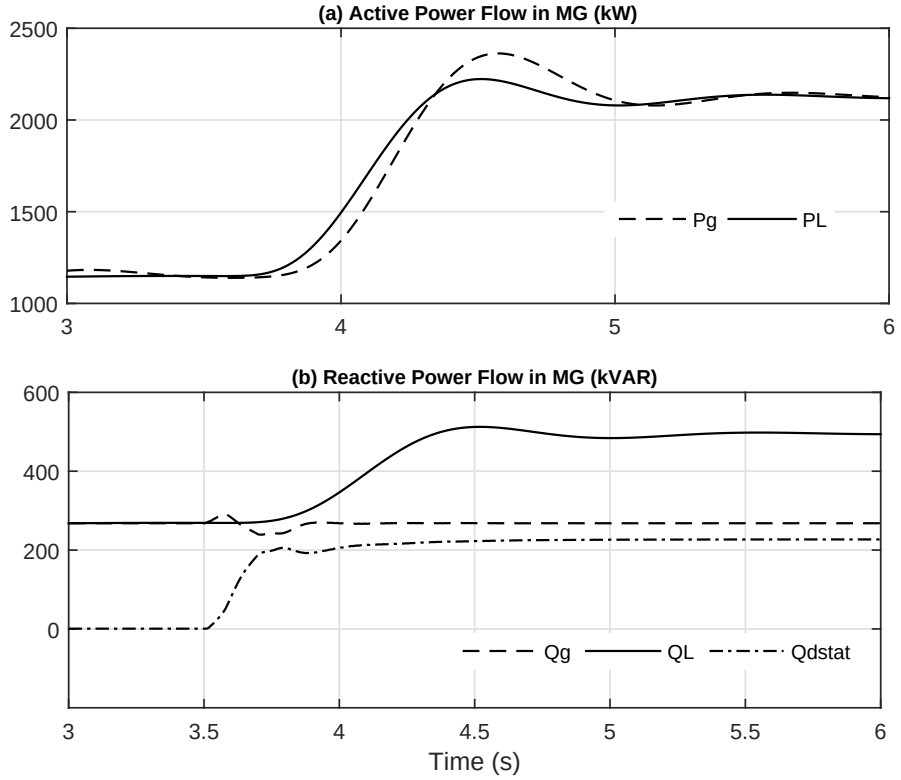


Figure 6.16: Power flow in MG (a) active power (b) reactive power

Figure 6.17 depicts the MG, load and DSTATCOM phase a current under these two conditions, wherein the first case, DSTATCOM current supplies only the harmonic compensating components, but in the latter case it also contributes to reactive load demand in addition to harmonic compensation.

Performance Comparison of the System with and without Connecting DSTATCOM at PCC

In this comparative case study, the effect of reactive load demand on the PCC voltage magnitude is illustrated. At time t = 3.46 s, the reactive load demand is 0.26 MVAr and it is changed to 0.49 MVAr at t = 3.5 s.

Initially, it has been assumed that DSTATCOM is not connected at the PCC and the DERs are responsible for entire real and reactive load demand. Real and reactive power distribution among DER_1 and DER_2 is depicted in Figure 6.18.

The DERs share the load demand in 2:1 ratio. Figure 6.19 depicts the three phase voltage at PCC at this two different time instants. It is clear that the voltage drop at PCC is 5 % with Q_L = 0.26 MVAr, but it has been increased to 8.56 % with an increased load demand of Q_L = 0.49 MVAr.

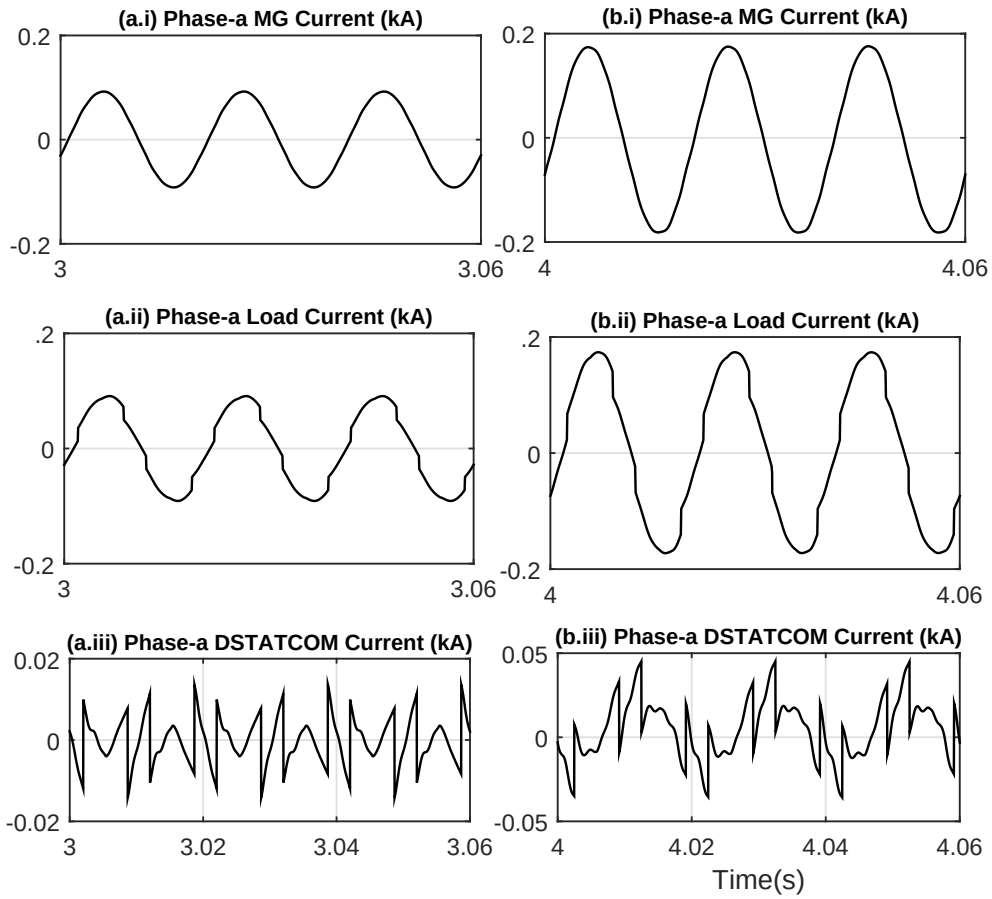


Figure 6.17: Phase-a MG, load and DSTATCOM currents (a) with no reactive power supply from MG (b) coordinated reactive power supply from MG and DSTATCOM

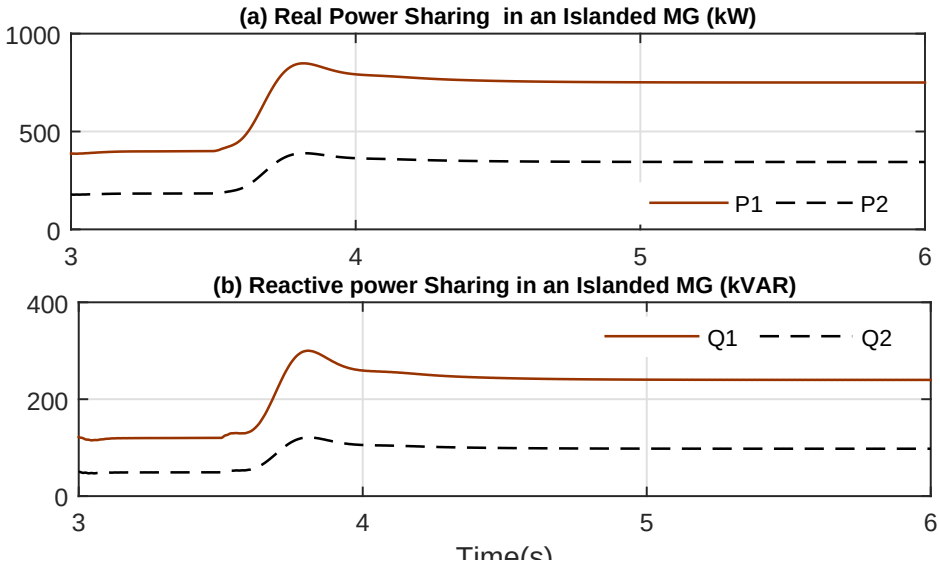


Figure 6.18: Load power distribution among DERs in an MG (a) real power (b) reactive power

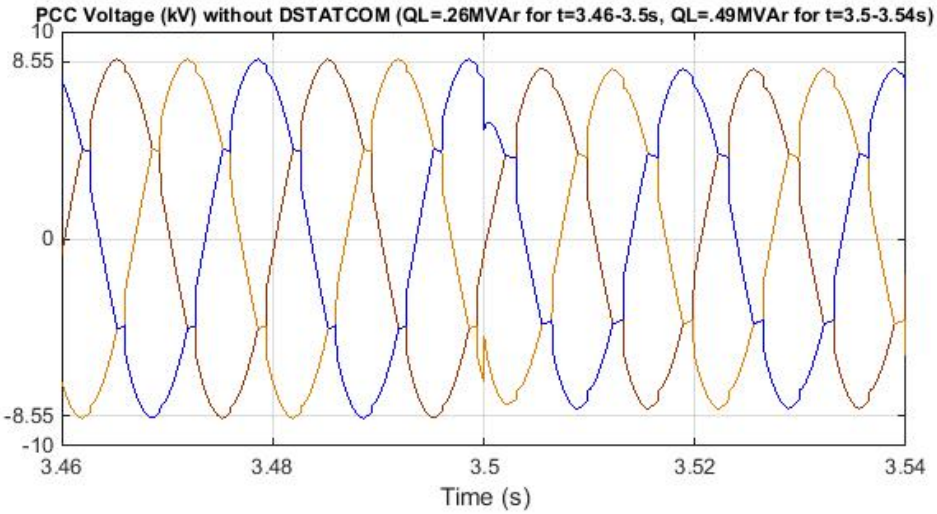


Figure 6.19: PCC voltage without DSTATCOM (Q_L = 0.26 MVAr for t = 3.46 - 3.5 s, Q_L = 0.49 MVAr for t = 3.5 - 3.54 s)

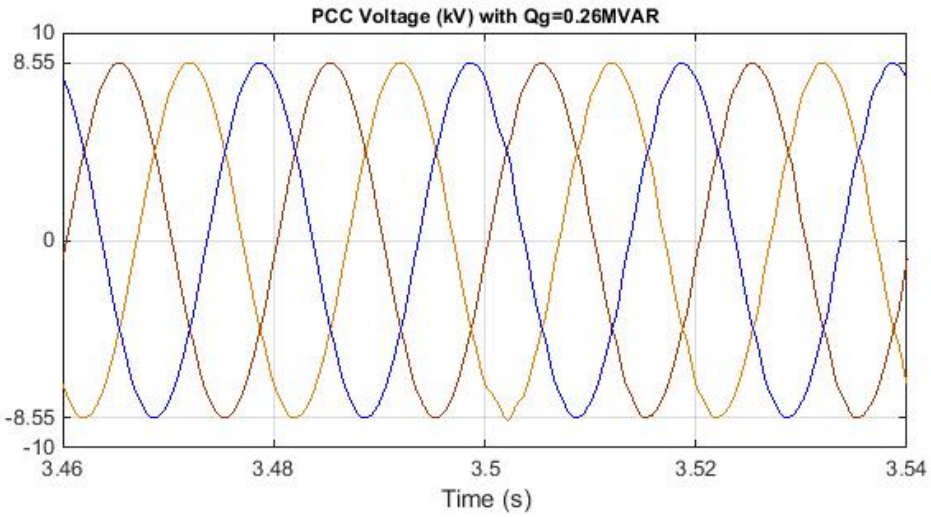


Figure 6.20: PCC voltage with integrated DSTATCOM (Q_L = 0.26 MVAr for t = 3.46 - 3.5 s, Q_L = 0.49 MVAr for t = 3.5 - 3.54 s)

Now, a DSTATCOM is assumed to be connected at the PCC as illustrated in case II, so that the two DERs together are expected to supply Q_G = 0.26 MVAr to a common load and the remaining load reactive demand is satisfied by the DSTATCOM. Three phase voltage waveform at PCC is shown in Figure 6.20, clearly verifies that the magnitude of PCC voltage remains the same at two different time instants and the variation in reactive load demand no longer affects the PCC voltage magnitude. The percentage voltage drop at PCC is limited to 5 % even with an increased reactive load demand.

6.4 Conclusion

This chapter investigates the stability and power quality issues in converter fed DERs. Initially, a closed loop SVPWM based voltage controller is proposed for an LC filter fed converter interfaced DER, which possesses attractive features such

as, effective DC link voltage utilization, constant and reduced switching frequency compared to traditionally used PWM schemes. Also, the phase shift due to the output filter is eliminated in this control. Since the proposed controller is based on state feedback DLQR, it is not sensitive to the parameter variations and other disturbances. Assuming the converter is stable in distinct operating mode, the stability issues in parallel connected DERs are discussed in the following section. Operating at higher switching frequencies reduces the output filter requirements significantly, which reduce the resonance and stability issues due to the output capacitor and feeder impedance. But the interaction between outer power loop controllers in different converters connected to PCC is still a concern. A damping method is introduced in this chapter to effectively eliminate the stability issues in parallel converter due to controller interaction. The nature of stability issues in islanded mode is different than the grid connected mode. The harmonic issues in an islanded MG can be mitigated by connecting a DSTATCOM at the PCC. In a later section of this chapter, a coordinated control strategy is proposed to share the reactive power demand among DSTATCOM and DERs of an MG in addition to the harmonic mitigation functionality. The stability analysis and computer simulation study conducted in PSCAD and MATLAB verify the findings and proposed solutions.

Chapter 7

Power Flow Management in Interconnected Microgrids

Microgrid concept is becoming popular in remote communities, where it can reduce the network expansion/upgrade costs, minimizing the power losses in long feeders and therefore increase the reliability of the grid. The power flow in an islanded MG can be managed as discussed in Chapter 4, 5, and 6. But the contingent power shortfall in an autonomous MG under maintenance or fault conditions can adversely affect the essential and non-essential loads, therefore negatively impact the stability of the integrated system. In such context, interconnecting MG clusters will be a viable solution in future, since an individual MG can send and receive power from neighboring MGs and it will improve the resiliency and reliability of power networks [48], [130].

This chapter proposes a direct current power exchange highway to interconnect neighboring MGs and DC droop control strategy is utilized to manage the power flow in DCPEH. In addition, a sophisticated power flow controller (PFC) is developed for DCPEH connected MG cluster to meet the necessary functionalities such as overload prevention, distribution of surplus power to other MGs with power shortfall and islanding of an MG from DCPEH under adverse conditions. A

computer based simulation study is conducted on PSCAD/EMTDC to verify the proposed DCPEH concept and its superior functionalities.

7.1 Overall System Structure

The system under study is shown in Figure 7.1. In this, a total number of n microgrids are connected together through a DC link, which exchanges power between the microgrids. Therefore, the DC link is termed as the DC power exchange highway. No load is assumed to be connected to the DCPEH. Each microgrid is connected to the DCPEH through a voltage source converter. The DC link of each VSC is connected to a storage capacitor. The capacitors are connected in parallel through the DCPEH, which is represented by line resistances and smoothing reactors. This configuration contains a power flow controller for each MG and a Master Controller (MC) that is used as a supervisory control.

Nominally each microgrid supplies its local load. It holds the voltage across the DC capacitor connected to the VSC constant at a pre-defined level. However,

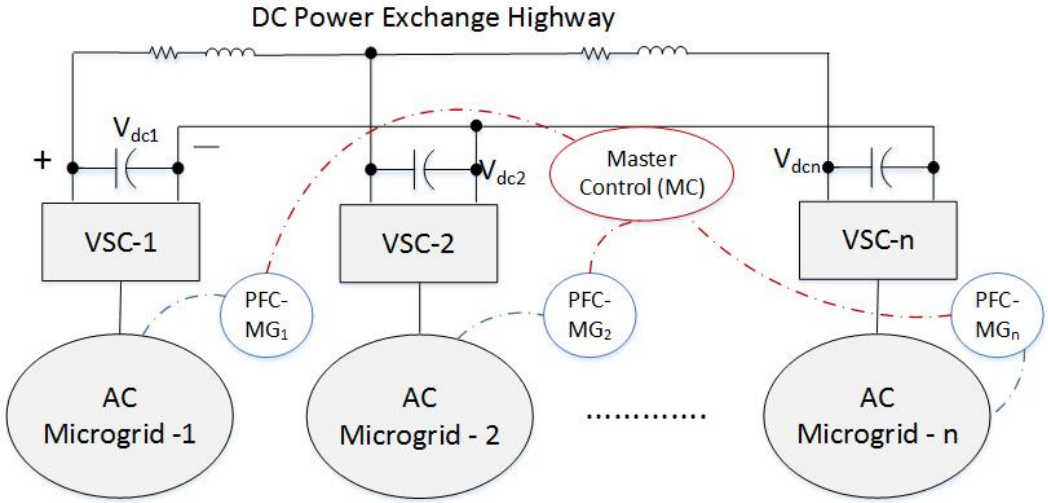


Figure 7.1: Microgrid cluster connected by a DCPEH

when a power shortfall occurs in one (or more) microgrid, the other microgrids supply a part of their excess available power to support it. The excess power available in a microgrid can vary depending on the consumption of its local load. Hence it is not possible to determine a priori how much support, in terms of real power, a microgrid can provide to others. Therefore the surplus available power in a microgrid has to be continually updated based on which the microgrid with excess available power will support the microgrids with power shortfall. The power exchange between the microgrids is facilitated by the DCPEH.

7.2 Microgrid Structure and Control

The microgrid structure under study is shown in Figure 7.2.

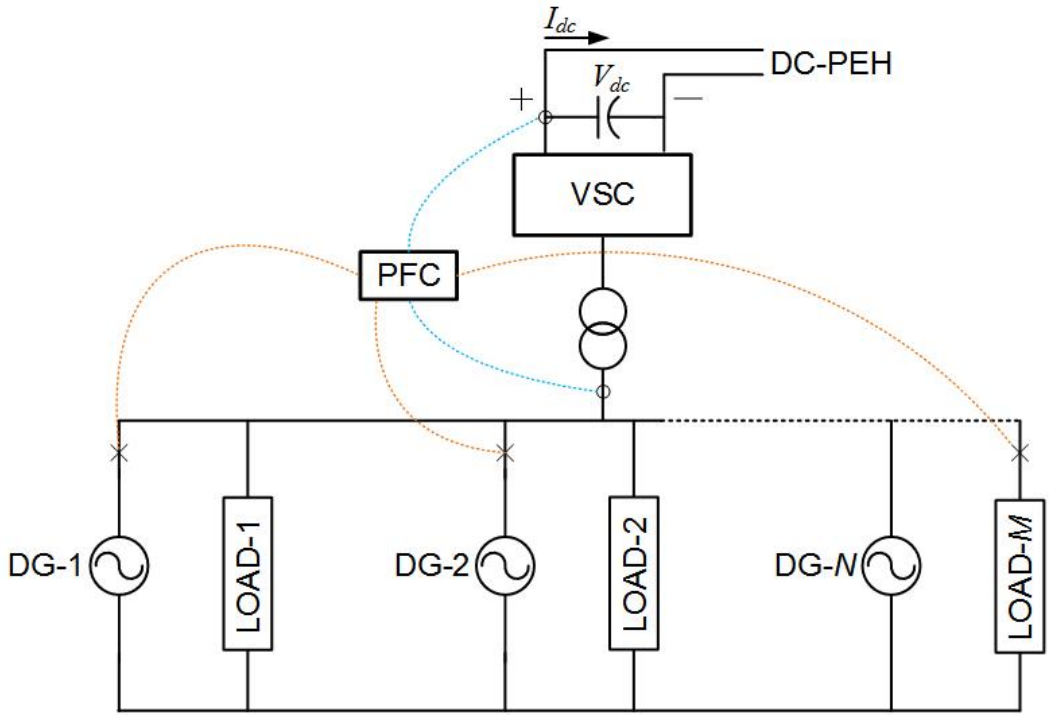


Figure 7.2: AC microgrid structure

It contains several DGs and loads. As mentioned before, each microgrid is connected thorough a VSC to the DCPEH. The VSC is connected to the microgrid bus through a transformer. A PFC controls the bidirectional power flow between the microgrid and DCPEH, by determining either the available excess power that can be supplied to DCPEH or the exact amount of power shortfall that is required for the safe operation of the microgrid. As shown in Figure 7.2, the PFC needs information about breaker status, voltage angles and DC power to send requisite control signals. This is discussed later.

7.2.1 Droop Control

All the DGs in the microgrid are assumed to operate in real power-angle and voltage magnitude-reactive power droop control. For the i^{th} DG, this is given by

$$\delta_i = \delta_i^* - m_i[P_i^* - P_i], \tag{7.1}$$

$$|V_i| = |V_i|^* - n_i[Q_i^* - Q_i] \tag{7.2}$$

where δ and δ^* respectively are the actual and the rated voltage angle of the DG, V and V^* are the actual and the rated DG voltage magnitude respectively, m and n are the droop gains. The rated and measured real powers are denoted by P^* and P respectively, while the rated and measured reactive power are denoted by Q^* and Q respectively. Note that in (7.1), the rated power (P^*) has been used and δ^* is considered as zero as this global reference angle is used to synchronize all DERs connected to each MG as well as the interconnected MGs. This implies that when δ = 0 ^{o}, the DG is required to supply its rated power. The droop gain of the i^{th} DG is calculated based on its power rating from (7.1) as

$$m_i = \frac{\delta_i^* - \delta_i}{P_i^* - P_i} = \frac{\Delta\delta}{\Delta P} \tag{7.3}$$

In case of a microgrid with two DGs, the droop gain m can be selected as,

$$\frac{m_1}{m_2} = \frac{P_2}{P_1} \tag{7.4}$$

Note that, in angle droop control, the relative angle difference will determine the power flow between individual DGs. A global clock signal is used to synchronize DGs as well as the interconnected MGs and this signal is transmitted at a comparatively slower speed through fibre optic cables as described in Chapter 4.

7.2.2 Overload Prevention Scheme

Let us assume that a microgrid has a total number of n DGs. It has been assumed that when a microgrid is overloaded, it should draw the exact amount of power that will maintain the stability in the system. For example, let us assume that the i^{th} DG in a microgrid has a total generation capacity of P_i^*, while at some instant it is supplying a total demand (load plus losses) of P_{Li}. Let us define the generation surplus capacity of a microgrid as $\Delta P_i = P_i^* - P_{Li}$. If the droop gains of the DG is chosen as per (7.3), the angle will be 0 when the total demand is P_i^*, i.e., when $\Delta P_i = 0$. However when $\Delta P_i < 0$, the angle of the DG will drop below 0.

Now if the droop gains of all the DGs are chosen as per (7.4), one DG gets overloaded implies that all the DGs are overloaded where their angles are all negative. If this condition is allowed to persist, a system collapse will occur.

To prevent this, the microgrid will be allowed to draw $\Delta P = \sum_{i=1}^{n}(\Delta P_i)$ amount of power from the other microgrids through the DCPEH. The drawing of this exact amount of power is tantamount to a reduction of load such that ΔP becomes 0. At this point, the angles of all the DGs will also become 0. Thus the basic aim is to get the angles back to 0 by drawing power from the other microgrids through the DCPEH. Note that if the angle δ_i of the i^{th} DG is brought to zero, the angles of

all other DGs will also become zero. Based on this argument, the PI controller is designed that set the reference P^*_{dc} for the amount of power to be drawn from the DCPEH as

$$e_{\delta_i} = 0 - \delta_i$$

$$P^*_{dc} = K_{p\delta}\, e_{\delta_i} + K_{I\delta} \int e_{\delta_i} dt \tag{7.5}$$

The block diagram of the overload prevention scheme is shown in Figure 7.3. The angle δ_i is compared with a fixed number 0. If the error is greater than 0, then a trigger signal (T_{rg}) is activated. Otherwise, the trigger signal remains zero. If T_{rg} = 1, then the input to the PI controller is invoked as in (7.5). When the T_{rg} changes from 1 to 0, a one-shot Schmitt trigger is used to generate a pulse that will reset the integrator. The input to the PI controller is then changed to 0 such that P^*_{dc} is zero as no power is required from DCPEH.

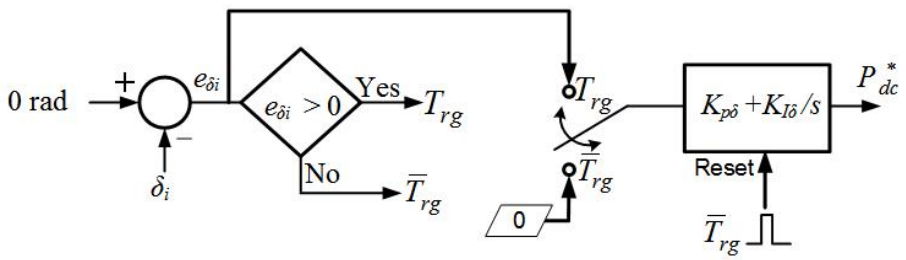


Figure 7.3: Schematic diagram of the overload prevention scheme

7.2.3 Power Surplus Calculation

The power surplus capacity (P_{SC}) that a microgrid has is defined as the difference between the total generation capacity that the microgrid has at a given instant of time minus the total local load that it is supplying at that instant. Let us assume that, at a particular time, the angle of the i^{th} DG is δ, while its total power generation capacity of a DG is P^*_i. The surplus power of this DG in an MG is defined as

$$\Delta P_i = P_i^* - P_i = \frac{\delta_i}{m_i}$$

Thus, for all the DGs in an MG, we have an individual MG surplus capacity,

$$P_{MG} = \sum_{i=1}^{n} \Delta P_i = \sum_{i=1}^{n} \frac{\delta_i}{m_i} \tag{7.6}$$

Note that P_{MG} includes the power that is supplied to the local load plus the power supplied to other microgrids through the DCPEH. Therefore the power consumed by the microgrid local loads and losses is the difference between P_{MG} and the dc power flowing to the DCPEH through the interlinking converter. The surplus capacity is calculated based on the microgrid local load (and losses) only. Therefore this is defined as

$$P_{SC} = P_{MG} - V_{dc} \times I_{dc} = \sum_{i=1}^{n} \frac{\delta_i}{m_i} - V_{dc} \times I_{dc} \tag{7.7}$$

It is interesting to note that the PFC of Figure 7.2 does not need to know about the status of each DG for overload prevention - it just draws power from DCPEH to stabilize the angle to 0 irrespective of how many DGs are connected to the system. On the other hand, the PFC needs the DG status for surplus power calculation. This is because of the maximum generation capacity of microgrid changes with the availability of the DGs. It might so happen that one of the DGs is out of commission due to required maintenance work. Also, the microgrid generation capacity can vary when the plug and play type DGs are included. Therefore, a communication link between the DGs and the PFC will be required to update the DG status. Note that the link is used only for a status update, a low bandwidth communication channel is sufficient.

7.2.4 VSC Structure and Operation

The VSC structure used in this study is shown in Figure 7.4. It is supplied from a dc storage capacitor (C_{dc}). The capacitor is connected to the DCPEH, as shown in Figure 7.1. An LC filter (L_fC_f) is connected at the output of the VSC to suppress high frequency switching harmonics. The resistance R_f represents the converter losses. The VSC is connected to the microgrid phases A, B and C through a transformer, as shown.

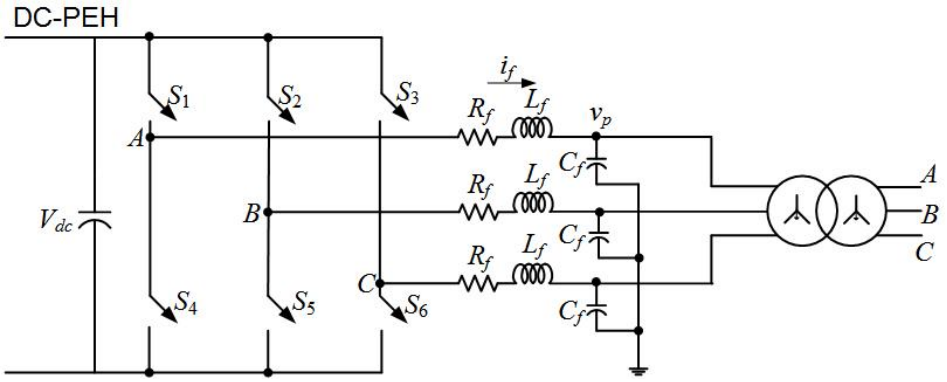


Figure 7.4: Interlinking voltage source converter structure

Each phase of the VSC is controlled individually through a state feedback controller that is designed taking into account the filter characteristics. Thereafter, the switching signals are generated using closed loop SVPWM. The first step in the process is to generate instantaneous reference voltages (v^*_{pa}, v^*_{pb} and v^*_{pc}) for the three phases. The VSC switching control then has to synthesize these voltages across the filter capacitors (C_f). The reference voltages are given by

$$v^*_{pa} = |V|sin(\omega t + \phi)$$

$$v^*_{pb} = |V|sin(\omega t + \phi - 120^0)$$

$$v^*_{pc} = |V|sin(\omega t + \phi + 120^0) \tag{7.8}$$

where $|V|$ is a pre-specified voltage magnitude, ϕ is the desired angle and ω is the microgrid frequency. The switching control law that is used to synthesize these voltages is discussed in Chapter 2. The angle ϕ should be such that the required amount of power flows from a microgrid to or from the DCPEH. Also, the VSC needs some amount of power from the microgrid to compensate for its switching and internal losses. The VSC can regulate the voltage across its dc capacitor (i.e., at its point of connection with DCPEH) if the angle ϕ is able to force a power balance through a feedback mechanism. For the j^{th} microgrid, the dc capacitor control equation is given by,

$$\phi_j = K_{P\phi}(V^*_{dcj} - V_{dcj}) + K_{I\phi}\int (V^*_{dcj} - V_{dcj})dt \tag{7.9}$$

where V_{dcj} is the voltage across the dc capacitor of the VSC connecting the j^{th} microgrid with the DCPEH and V^*_{dcj} is its reference. This reference computation is discussed in the next section.

7.3 Operation of DCPEH

The operation of a DCPEH is analogous to that of a dc microgrid. In this section, first, we shall discuss the droop sharing in a dc microgrid, which will then be generalized for a DCPEH.

7.3.1 DC Microgrid Operation

Consider a simple DC MG circuit that is shown in Figure 7.5. It contains two DC sources with voltages of V_{dc1} and V_{dc2}. These two sources are supplying a resistive load R_L. The resistances R_{f1} and R_{f2} denote the feeder resistances. The droop

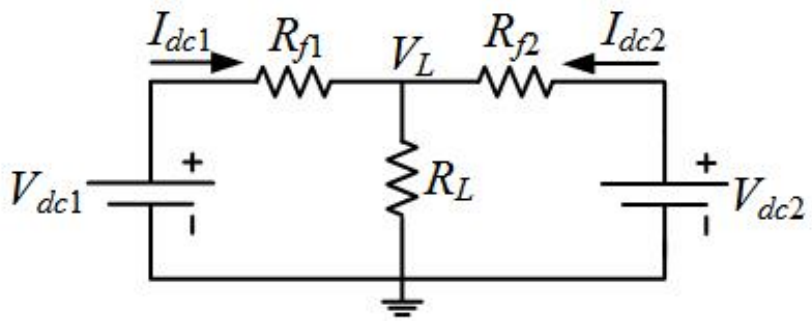


Figure 7.5: Schematic diagram of a DC MG

equations for a DC microgrid are given by [162]

$$V_{dc1} = V_{dc}^{ref} - n_1 I_{dc1}$$

$$V_{dc2} = V_{dc}^{ref} - n_2 I_{dc2} \tag{7.10}$$

where V_{dc}^{ref} is the reference DCPEH operating voltage, n_1 and n_2 are the droop gains. From Figure 7.5, the voltage across the load is given by

$$V_L = V_{dc1} - R_{f1} I_{dc1} = V_{dc2} - R_{f2} I_{dc2} \tag{7.11}$$

Combining (7.10) and (7.11), the following equation is obtained

$$\frac{I_{dc1}}{I_{dc2}} = \frac{n_2 + R_{f2}}{n_1 + R_{f1}} \tag{7.12}$$

Now the powers generated by the two sources are given by

$$P_{dc1} = V_{dc1} I_{dc1}, P_{dc2} = V_{dc2} I_{dc2} \tag{7.13}$$

Therefore the power ratio is given by

$$\frac{P_{dc1}}{P_{dc2}} = \frac{V_{dc1} I_{dc1}}{V_{dc2} I_{dc2}} \tag{7.14}$$

Let us now assume that the voltage across the dc microgrid is roughly constant. Then

$$V_{dc1} \approx V_{dc2} \tag{7.15}$$

Substituting (7.15) into (7.14), the following expression is obtained

$$\frac{P_{dc1}}{P_{dc2}} \approx \frac{I_{dc1}}{I_{dc2}} \tag{7.16}$$

Comparing (7.16) with (7.12), we get

$$\frac{P_{dc1}}{P_{dc2}} \approx \frac{n_2 + R_{f2}}{n_1 + R_{f1}} \tag{7.17}$$

Now if $n_1 >> R_{f1}$ and $n_2 >> R_{f2}$, the power sharing will be governed by the droop gains, i.e.,

$$\frac{P_{dc1}}{P_{dc2}} \approx \frac{n_2}{n_1} \tag{7.18}$$

From (7.17) and (7.18) it can be surmised that if the droop gains are much larger than the line resistance, the power sharing is more accurate. However, from (7.10) it can also be surmised that high droop gains can also cause a voltage drop in the line.

As per [163], the maximum conductor resistance, dc at 20 °C for a single core heavy duty screened unarmored Copper wire with voltage rating 1.9 - 3.3 kV (MV) falls in the range 0.124 to 0.0283 Ω/km. The resistance value differs with different manufacturers, conductor material etc. and it is selected based on the nominal cross sectional area and rated current, which can be obtained from ABB switchgear manual [164]. Since the obtained resistance value is comparatively lesser than the designed dynamic droop gains, the approximation $n_1 >> R_{f1}$ and $n_2 >> R_{f2}$ in (7.18), is acceptable. In MVDC system with comparatively short connections, the losses in DC transmission lines mainly depend on the voltage drop and admittance between two nodes [165]. Here, the study is based on the MG clusters placed in

a small geographical area and thus the connections are not so long. In addition, the advanced voltage control in interlinking converter minimizes the voltage drop between two nodes.

7.3.2 DCPEH Operation

Nominal Operation

Let us now consider Figure 7.6, where the three voltage sources represent the dc capacitors of three microgrids and they are connected through the DCPEH.

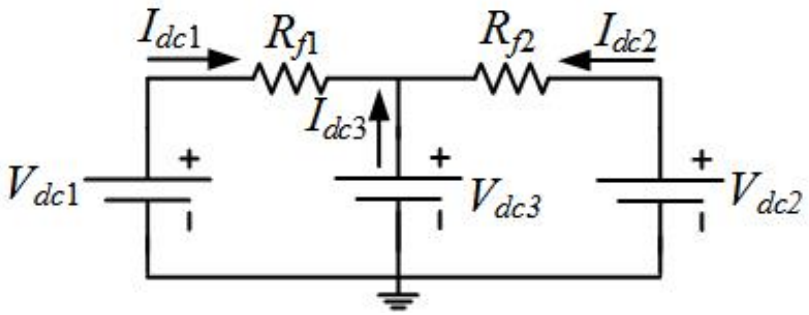


Figure 7.6: Schematic diagram of the DCPEH

The MGs are numbered according to their voltage sources, i.e., V_{dc1} represents MG_1 etc. Nominally all the microgrids supply their local demand and no power exchange is required through DCPEH. Therefore the droop gains of all the MGs are set as per (7.10) as

$$V^*_{dc1} = V^{ref}_{dc} - n_1 I_{dc1}$$

$$V^*_{dc2} = V^{ref}_{dc} - n_2 I_{dc2}$$

$$V^*_{dc3} = V^{ref}_{dc} - n_3 I_{dc3} \tag{7.19}$$

Since there is no power flow in the PEH, all the dc capacitor voltage references are equal to V^{ref}_{dc}.

Overload Prevention

Now assume that MG_3 needs power from the DCPEH. The power requirement (P^*_{dc3}) is obtained from the control logic of Figure 7.3. We then set the dc capacitor voltage reference for MG_3 such that this amount of power is drawn from the DCPEH. This is accomplished through another PI controller, given by

$$e_{d3} = P^*_{dc3} - P_{dc3}$$

$$V^*_{dc3} = V^{ref}_{dc} - K_{Pd}e_{d3} - K_{Id}\int e_{d3}dt \tag{7.20}$$

where $P_{dc3} = -V_{dc3} \times I_{dc3}$. The reference voltages of the other two MGs in (7.19) remain unaltered. The overall dc capacitor voltage reference selection scheme is shown in Figure 7.7, where the signal T_{rg} is obtained from Figure 7.3. The signal T_{rg} dictates the selection between (7.19) and (7.20).

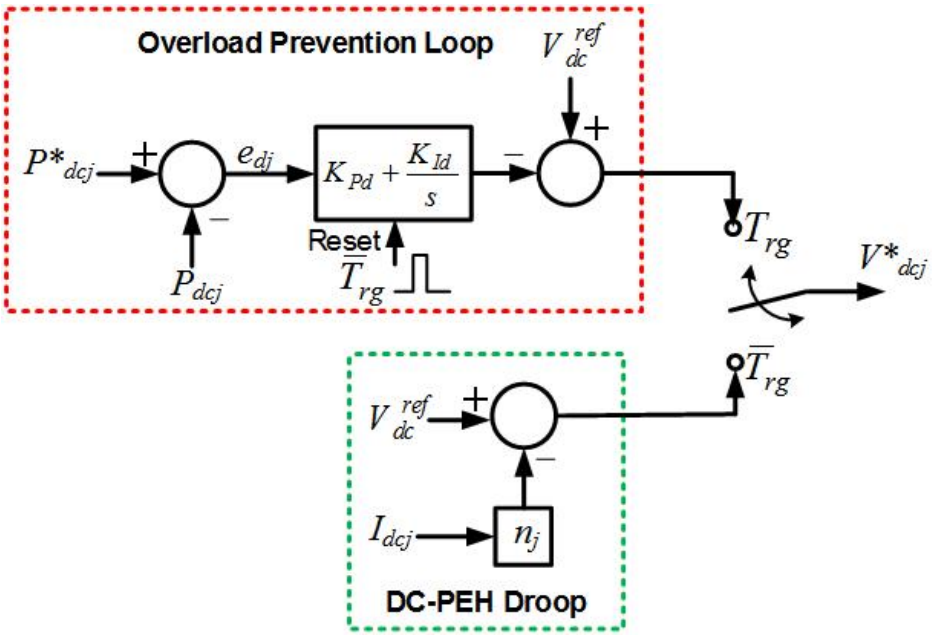


Figure 7.7: DC capacitor voltage reference generation scheme

Dynamic Droop Gain Selection

The surplus capacity that a microgrid has can be estimated from (7.7). It might not however be necessary that the microgrid schedules the entire amount for dispatch through DCPEH. Let us assume that the maximum power that the microgrid schedules for dispatch is P_{ref}. Notice that this quantity can change depending on the local load of each microgrid. Therefore the droop gains may need to be adjusted dynamically.

From (7.19), it can be surmised that large droop gains can cause large voltage drops. Since these voltages are used to set the references for the dc capacitors, a large voltage drop might lead to a tracking failure in the VSCs, thereby distorting the microgrid voltages. It may even lead to voltage collapse in the microgrids. In order to restrict the voltage drop, let us assume that the microgrids together will supply a maximum of P_{max} power to all the overloaded microgrids. A limit of ΔV_{max} has been set for the maximum allowable voltage drop. Then from (7.10), we get

$$\Delta V_{max} = V_{dc}^{ref} - V_{dc} = nI_{dc} = n\frac{P_{max}}{V_{dc}} \tag{7.21}$$

The above equation can be rewritten as

$$n = \frac{V_{dc}\Delta V_{max}}{P_{max}} \tag{7.22}$$

Since the quantities of the right-hand side of (7.22) are known, the droop gain n can be calculated. Then from (7.18), we get the following expression for a total number of N microgrids

$$n_1 P_{ref1} = n_2 P_{ref2} = ... = n_N P_{refN} = nP_{max} = \alpha \tag{7.23}$$

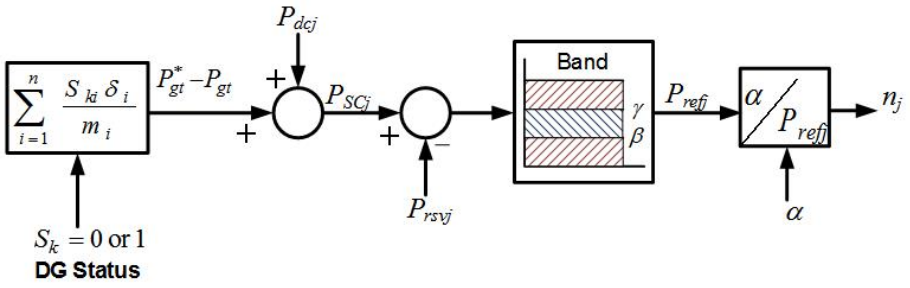


Figure 7.8: The scheme to select the droop gains dynamically

The quantity α sets the reference for all microgrids to follow. The schematic diagram of the dynamic droop gain selection scheme is shown in Figure 7.8. Based on the angle and the status of the DGs in a microgrid, its surplus capacity is calculated from (7.7). A certain amount of power (P_{rsv}) is kept as reserve in the microgrid to cater for a sudden change in its local load. Thereafter P_{ref} is selected based on ($P_{SC} - P_{rsv}$). Note that P_{SC} changes for every change in the microgrid local load. This will cause a continuous fluctuation in n if P_{ref} is chosen as ($P_{SC} - P_{rsv}$). In order to prevent this, P_{ref} is changed in discrete steps of ($P_{SC} - P_{rsv}$) in a band that is given by

$$if \quad \beta \leq P_{SC} - P_{rsv} < \gamma, \quad then \quad P_{ref} = \beta \tag{7.24}$$

where β is lower limit and γ is the upper limit of the band and the bandwidth is selected as

$$\gamma - \beta = \lambda \times P_{MG} \tag{7.25}$$

where λ is a constant that defines a percentage of the total generation capacity of the microgrid. Once P_{ref} is obtained, the droop gain of the microgrid is computed from the preset value of α, as given in 7.23. The power flow control scheme is shown in Figure 7.9. This is a combination of Figure 7.3, Figure 7.7, Figure 7.8 and the dc capacitor control of (7.9). This figure shows how the different components interlink together for the bidirectional power flow control between a microgrid and DCPEH.

If all the microgrids are overloaded, the load shedding will be unavoidable, where

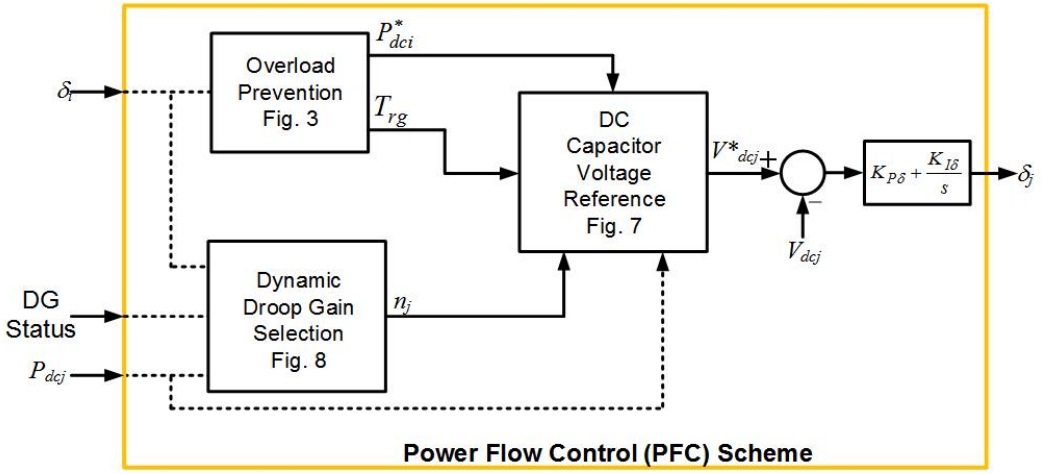


Figure 7.9: The overall power flow control scheme

no essential loads must be shed. Now there can be two different scenarios.

In the first scenario, the power reserves of all the microgrids are nearly zero. The MC, getting the angle information from all PFCs, can then issue a command to all the microgrids that no support will be available in case of overload and the MGs will have to load shed if the angle becomes negative.

In the second scenario, the reserves in all the microgrids are not significant when a microgrid gets overloaded. It can so happen that the overloaded MG will not have sufficient support from the PEH. Now the PFC of this microgrid checks the angle status of the MG continuously. If the angle is not brought back to zero within say 10 s, it implies that the PEH cannot provide the required power support. The PFC will then issue a command to switch off the non-essential loads so that the angle becomes positive.

Islanding Process

Islanding is a process to disconnect the individual MGs from DCPEH, when there is no power reserve in an individual MG to supply to DCPEH or the DCPEH has any excess power to satisfy the increased load demand of an MG. The MC has necessary angle information of all MGs and it will determine and send the islanding signal to individual MGs. Upon receiving this signal, PFC will initiate the islanding process by setting the individual MG dynamic droop gain to a high value, as disconnecting the MG with minimum power will limit the transient oscillations and ensure the system stability. This high droop gain value is calculated based on (7.22) and (7.23). The maximum dispatchable power of an individual MG, P_{ref} is assumed as 1 % of P_{max} to find out the upper limit of droop gain. MG will wait in this status for 10 seconds to damp out the transient oscillations and then open the circuit breaker to disconnect the MG from DCPEH.

7.4 Simulation Results

In this section, simulation results with three microgrids connected to a DCPEH are discussed. Several case studies are presented below, starting with the selection of droop gains dynamically. It has been assumed that each microgrid contains two DGs. The data used are given in Table 7.1.

7.4.1 Dynamic Droop Gain Selection

In the system of Figure 7.6, the line resistances are $R_{f1} = 0.01\ \Omega$ and $R_{f2} = 0.06\ \Omega$, while the dc voltage reference is V_{dc}^{ref} = 2.5 kV. We stipulate that the maximum power that can flow through the DCPEH is P_{max} = 250 kW and the maximum allowable voltage drop ΔV_{max} = 100 V. Then V_{dc} in (7.21) is equal to 2.4 kV.

Table 7.1: System parameters

System Parameters	Values
DCPEH	
DCPEH Voltage	2.5 kV
MG_1 Line Impedance	$R_{f1} = 0.01\ \Omega$, L_{f1}=1 mH
MG_2 Line Impedance	$R_{f1} = 0.06\ \Omega$, L_{f1}=1 mH
MG_1, MG_2, MG_3	
Generation Capacity	1 MW
Rated Voltage	11 kV
Transformer Rating	1 MVA, 11/1.72 kV
DG_1 Rating	0.667 MW
DG_1 Feeder Impedance	0.1+j1 Ω
DG_1 Angle Droop Gain	0.04 rad/MW
DG_2 Rating	0.333 MW
DG_2 Feeder Impedance	0.15+j1.5 Ω
DG_2 Angle Droop Gain	0.08 rad/MW

Therefore from (7.22), we get

$$n = \frac{2.4 \times 10^3 \times 100}{250 \times 10^3} = 0.96\ \Omega$$

Hence α from (7.22) is computed as

$$\alpha = n \times P_{max} = 2.4 \times 10^5$$

Assume that, MG_1 and MG_2, at any given time, have the surplus power of 200 kW and 100 kW, respectively. Then their droop gains will be

$$n_1 = \frac{\alpha}{P_{ref1}} = 1.2\ \Omega, n_2 = \frac{\alpha}{P_{ref2}} = 2.4\ \Omega$$

7.4.2 Overload in MG_3

At the beginning, the entire system is in steady state, where the local load in MG_3 is 833 kW. The surplus power and droop gains of the other two MGs are those given in the previous sub-section. At time 2 s, the load in MG_3 increases to 1.1 MW, which is beyond its total generation capacity of 1 MW. This causes the MG_3 DGs voltage angle to drop below 0 and hence the activation of the overload prevention scheme of Figure 7.3. The output (P^*_{dc}) of the PI controller (7.5) and the angle of MG_3 - DG_1 are shown in Figure 7.10. It can be seen that the angle reaches the desired value of 0 rad at around 12 s.

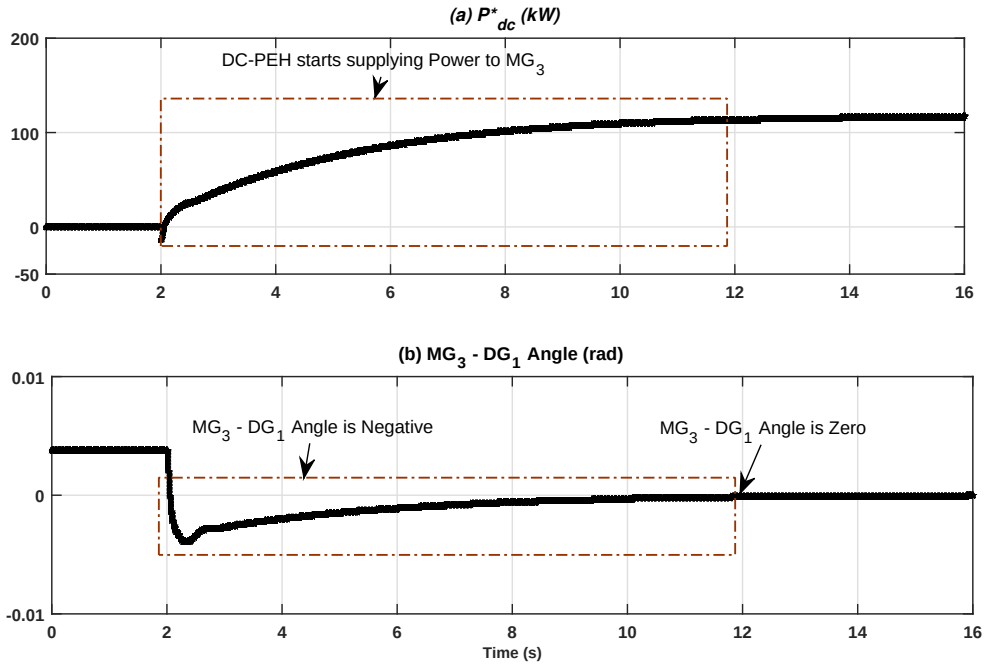


Figure 7.10: Overload prevention scheme; (a) required power to be drawn from DCPEH and (b) MG_3 - DG_1 Angle

The power flow through MG_3 is shown in Figure 7.11 (a). It can be seen that the total generation saturates at 1 MW, while the demand is 1.1 MW. This excess

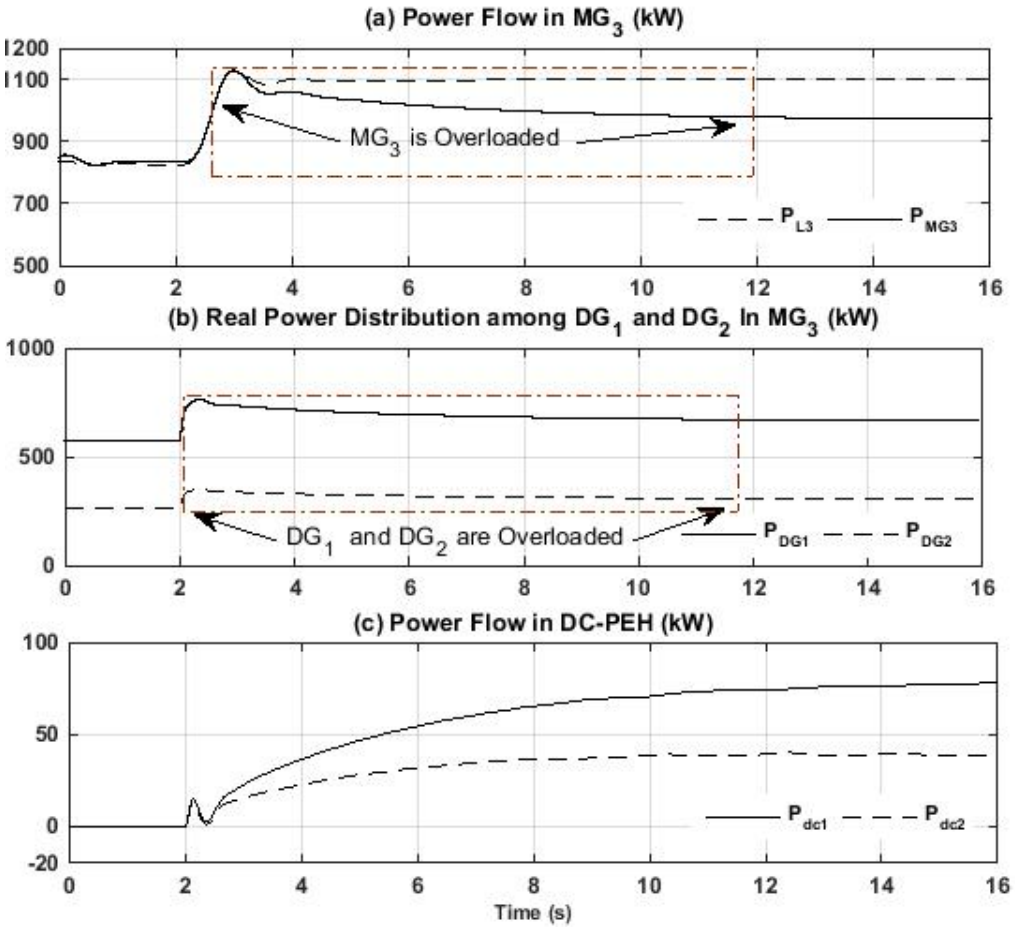


Figure 7.11: Power flow through (a) MG_3, (b) individual DGs in MG_3 and (c) DCPEH

amount of power flows from DCPEH as shown in Figure 7.11 (b), where the share of power between MG_1 and MG_2 remains in the ratio of 2:1. The dc capacitor voltage of MG_3 and the output of its angle controller are shown in Figure 7.12. The dc capacitor voltages of the other two MGs are shown in Figure 7.13. It is evident from Figures 7.12 and 7.13 that none of the DC voltages violate the minimum limit of 2.4 kV. Under the transient condition, the maximum overshoot falls within 10 % of the final steady-state value and the undershoot percentage deviation is limited to 1.25 % of minimum DC link voltage limits. Since the settling time is within few

seconds, overshoot and undershoot deviation is acceptable.

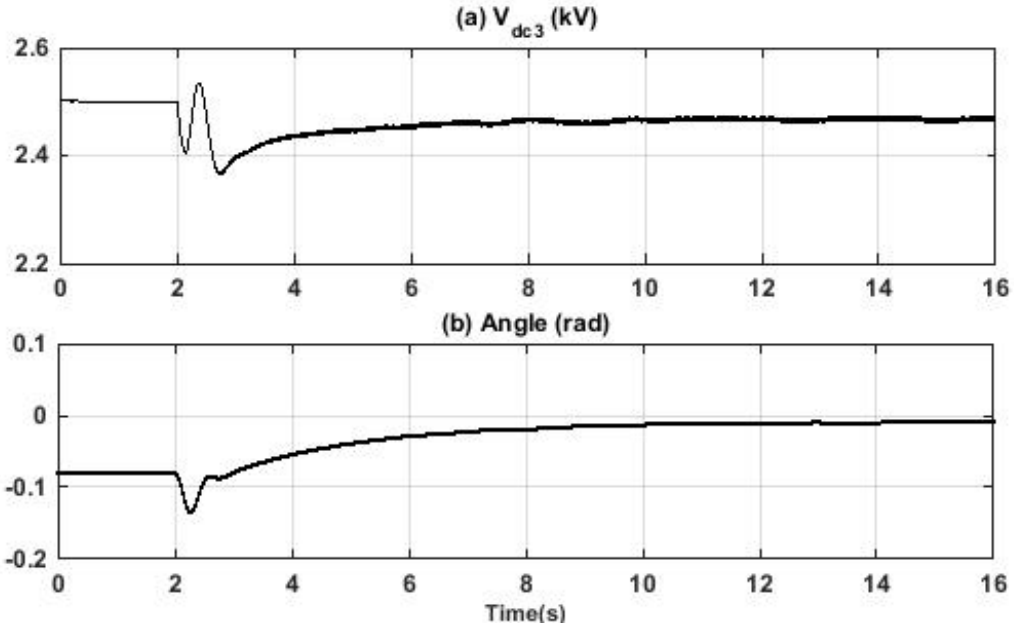


Figure 7.12: DC capacitor voltage control in MG_3

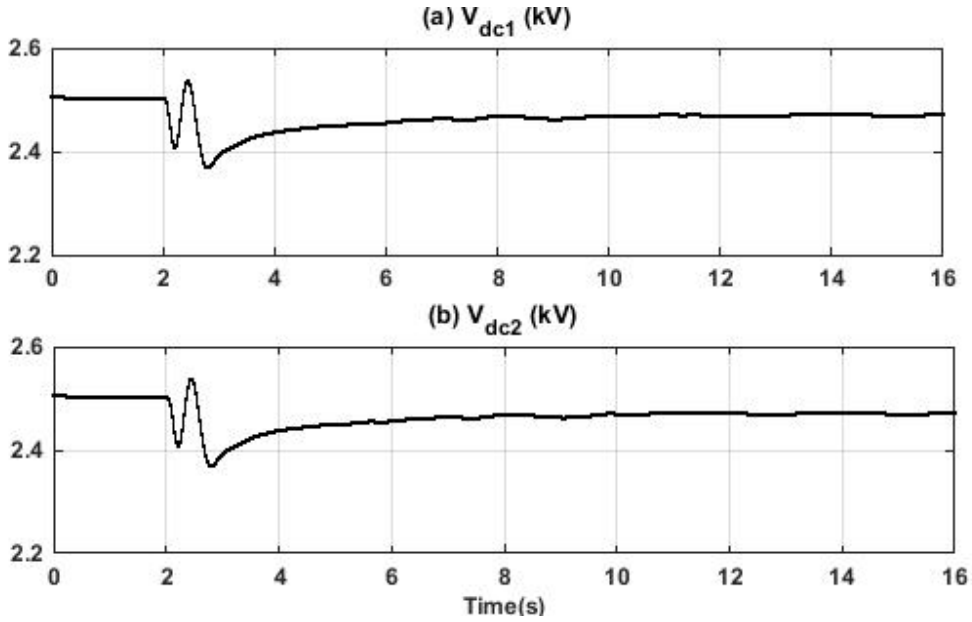


Figure 7.13: DC capacitor voltages of MG_1 and MG_2

7.4.3 Surplus Power Supply by MG_3

In this example, it is assumed that MG_2 requires a total power of 200 kW. MG_1 has a surplus capacity of 200 kW and hence its droop gain is chosen as 1.2 Ω. To select the droop gain of MG_3, λ in (7.25) is chosen as 0.05 and P_{rsv} is chosen as 50 kW, while the total generation capacity of the microgrid is 1 MW. This implies that the dynamic droop remains constant for less than 50 kW change in the local load. The droop gain selection is given in Table 7.2, for α of 2.4×10^5.

Table 7.2: Dynamic droop gains of MG_3

Range	P_{ref3}	n_3
kW	kW	Ω
$0< (P_{SC} - P_{rsv}) \leq 50$	0	∞
$50< (P_{SC} - P_{rsv}) \leq 100$	50	4.8
$100< (P_{SC} - P_{rsv}) \leq 150$	100	2.4
$150< (P_{SC} - P_{rsv}) \leq 200$	150	1.6
$200< (P_{SC} - P_{rsv}) \leq 250$	200	1.2
$250< (P_{SC} - P_{rsv})$	250	0.96

At the beginning MG_3 is in steady state supplying 760 kW of local load plus system losses of around 8 kW. Then $(P_{SC} - P_{rsv})$ is equal to 182 kW. The n_3 is chosen as 1.6 Ω from Table 7.2. The MG_3 local load changes to 780 kW at 1 s. This implies that $(P_{SC} - P_{rsv})$ is equal to 162 kW, including losses. Therefore the droop gain should not change and the power supplied by MG_3 to DCPEH should remain unchanged. Thereafter at 6 s, the MG_3 local load changes to 830 kW, which reduces P_{ref} to 112 kW and n_3 changes to 2.4 Ω. The power flow through MG_3 is shown in Figure 7.14 (a), while the power supplied to DCPEH by MG_1 is shown in Figure 7.14 (b). It can be seen that this remains (almost) constant when MG_3 local load changes to 780 kW, but increases when the load increases to 830 kW. $(P_{SC} - P_{rsv})$ of MG_3 is shown in Figure 7.15 (a), while its droop gain is shown in Figure 7.15 (b). It can be seen that they follow the data given in Table 7.2.

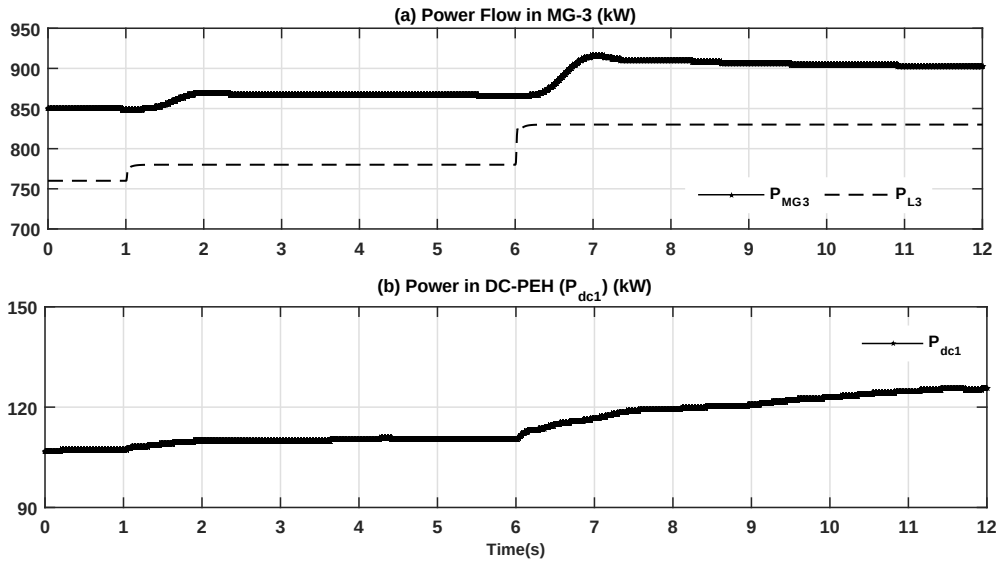


Figure 7.14: Power flow through MG_3 and supplied by MG_1 to DCPEH

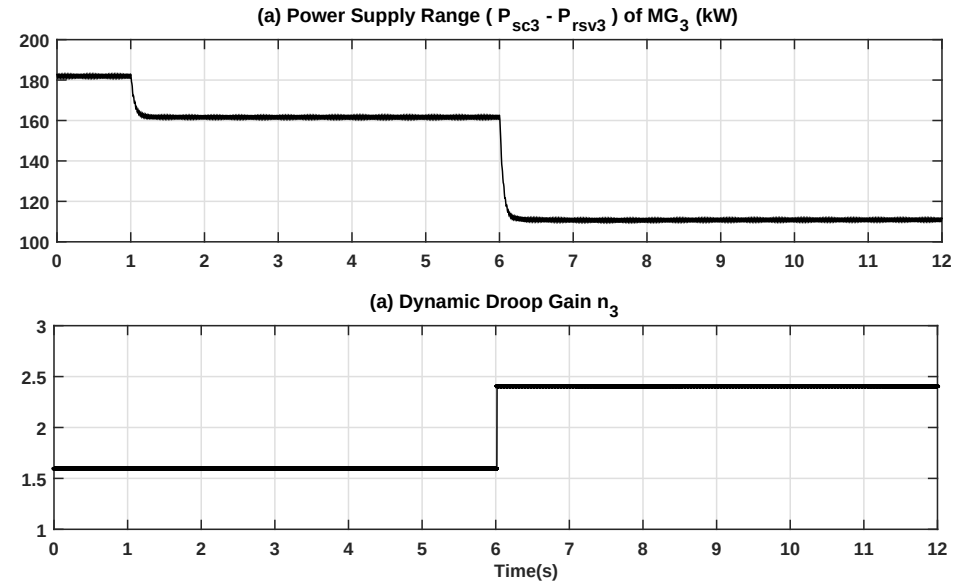


Figure 7.15: Power supply range and droop gain of MG_3

7.4.4 Power Sharing among MG_1 and MG_2 and Islanding of MG_2 in Contingency

In this case, it has been assumed that MG_3 has power shortfall and it is supplied by the other two MGs under dynamic droop control strategy. The excess power available from MG_2 is changed in different time intervals to verify the effectiveness of droop control and its transient response. An islanding procedure is also illustrated here to isolate an individual MG, based on the increase in local load demand and scarcity of supplying excess power to other MGs.

Initially, MG_3 is assumed to be running under steady-state and it is supplying its local load of 833 kW. At 4.5 s, the local load of MG_3 is increased to 1.1 MW which is beyond its generation capacity of 1 MW. The power flow in MG_3 is shown in Figure 7.16(a). MG_1 and MG_2 start supplying the power shortage of 100 kW through DCPEH. The maximum dispatchable power of MG_1 and MG_2 are found to be 200 kW and 50 kW respectively and the dynamic droop gains are chosen as per MG rating. It is evident from Figure 7.16 (b) that, the power is shared among MG_1 and MG_2 in the ratio 4:1.

Thereafter at t=15 s, MG_2 local load is increased by 50 kW so that it cannot supply power to DCPEH. At this condition, MG_1 is responsible for supplying the entire power shortage of MG_3. Once the PFC of MG_2 receives the islanding command from MC, MG_2 kick-starts the islanding process. In order to obtain a smooth transition, the droop gain of MG_2 is increased to a high value of $n_2 = 96$, whereas n_1 remains unchanged. The high droop gain will force power flow from MG_2 to DCPEH to a negligibly small value with damped oscillations.

The transient oscillations with high droop gain are noticeable (15 s - 20 s) as illustrated in Figure 7.16 (b), but these oscillations are damped out within 5 s. Increasing the droop gain above this value will lead the system to unstable mode. It is visible from Figure 7.16 (b) that, the MG_2 surplus power is a negligibly small value, with a percentage deviation of 1 % (7.3).

With this minimal percentage error, opening circuit breaker cannot result in high transients, which otherwise will lead the system to instability. Thus, MG_2 is disconnected from DCPEH using hard switching at time, t = 25 s. It is clear from Figure 7.16 (b) that MG_1 is alone supplying the excess power of 100 kW through DCPEH.

Subsequently, MG_2 surplus power is increased to 100 kW at t = 35 s. In order to achieve smooth transient performance, the dynamic droop gain n_2 is kept unchanged during circuit breaker closure. Thereafter at t = 40 s, n_2 is changed to 2.4 and the power is expected to share between MG_1 and MG_2 in the ratio 2:1.

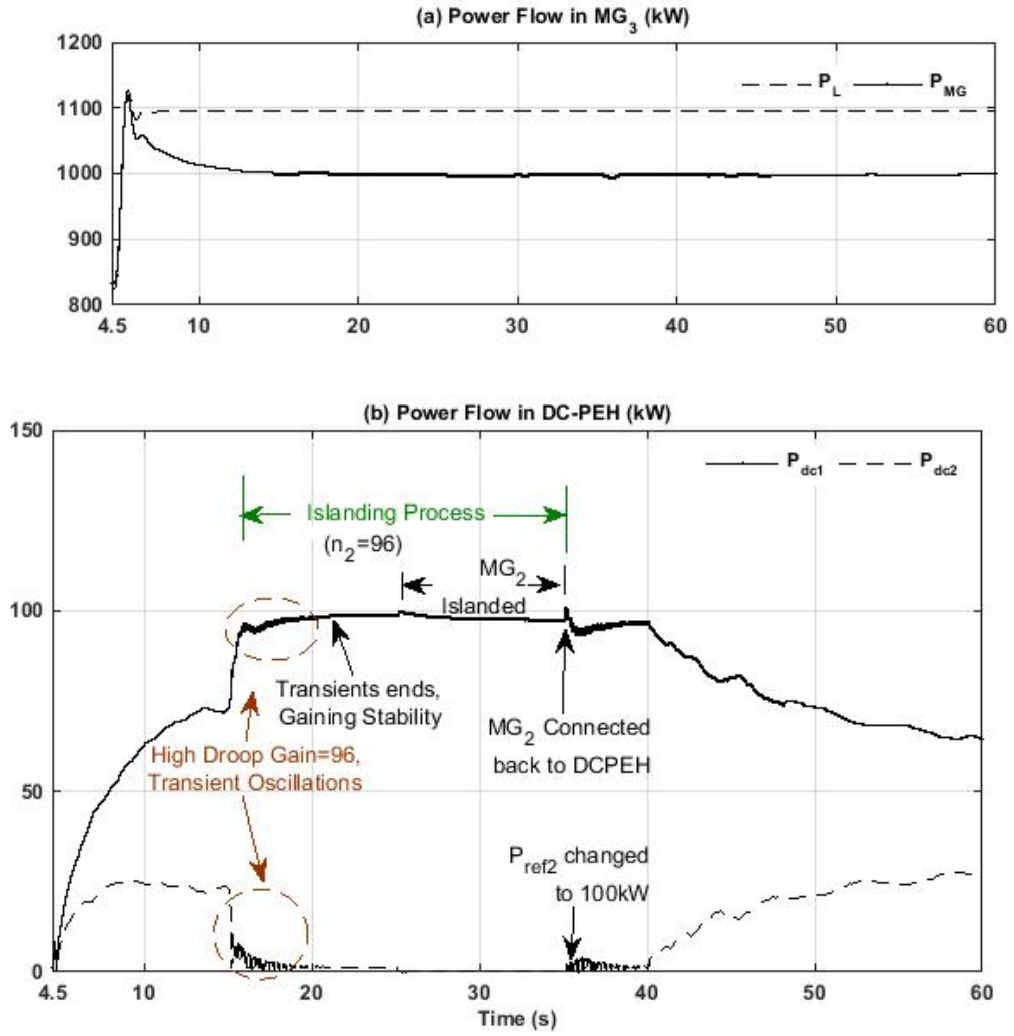


Figure 7.16: Power flow through (a) MG_3 and (b) DCPEH

The percentage deviation in power sharing between MG_1 and MG_2 during different time intervals is tabulated in Table 7.3 and the average deviation is found to be 2.06 % and 5.46 % respectively for MG_1 and MG_2.

Table 7.3: Power distribution among MG_1 and MG_2 in DCPEH

Time Interval	P_{sc1}	n_1	Deviation	P_{sc2}	n_2	Deviation
(s)	kW	Ω	%	kW	Ω	%
4.5-15	200	1.2	2.6	50	4.8	4
15-40	200	1.2	1	0	96	1
40-60	200	1.2	1.6	100	2.4	11.4

Figure 7.17 shows the dynamic droop gains of MG_1 and MG_2. The dc capacitor voltage of MG_1, MG_2 and MG_3 are shown in Figure 7.18. It can be seen that, MG_2 DC link voltage is 2.5 kV for the duration time between 25 s and 35 s and none of the capacitor voltages violate the minimum limit of 2.4 kV under steady-state conditions.

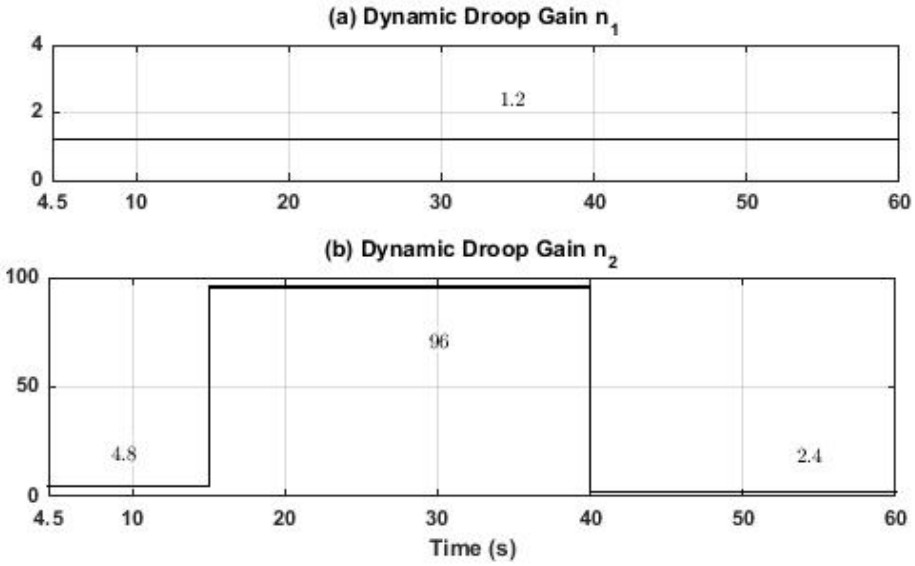


Figure 7.17: Dynamic droop gain (a) MG_1, (b) MG_2

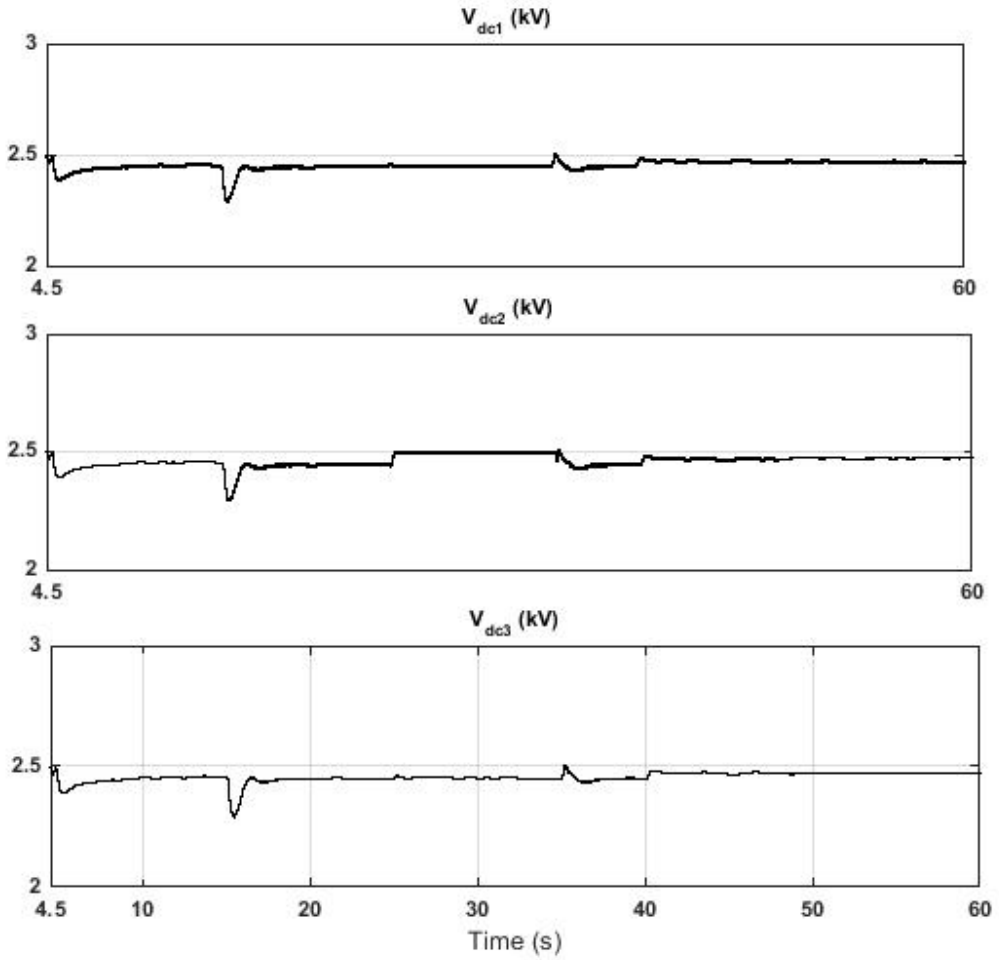


Figure 7.18: DC capacitor voltages of MG_1, MG_2 and MG_3

7.4.5 Power Flow in DCPEH with Multiple MGs

In this case study, 10 number of MGs are assumed to be connected to DCPEH. The maximum dispatchable power of each MG is calculated based on the surplus power and minimum power reserve. Accordingly, the dynamic droop gains are selected as per Table 7.2. Table 7.4 summarises the individual MG rating and the local load demand at different time instants. The results are shown in Figure 7.19.

The power flow in DCPEH is calculated using algorithm describes in Section 4. It has been assumed that, at time instant 1, maximum dispatchable power in DCPEH is greater than the total power shortfall in MGs. MG_1, MG_2, MG_3 and MG_7 can supply a power reserve of 100 kW, 200 kW, 150 kW and 50 kW respectively and the dynamic droop gains are calculated accordingly. In the interim, MG_8, MG_9 and MG_{10} have a power shortfall of 100 kW, 200 kW and 150kW respectively. Thus the DCPEH supplies a total power of 450 kW to the MGs with power short fall.

At time instant 2, the MG_2 local load is increased by 100 kW, and MG_{10} local load demand is reduced by 50 kW. The load demand in other MGs remains unchanged. Thus, the total power shortfall and the power reserve in DCPEH becomes 400 kW. At this condition, the additional power requirement by overloaded MGs (400 kW) can be satisfied by DCPEH.

At time instant 3, MG_1 local load is increased to its maximum capacity, and it cannot supply any excess power to DCPEH. This leads the aggregated power shortfall in all MGs to exceed the maximum dispatchable power in DCPEH. Load shedding is unavoidable at this instant, where the non-critical loads should be disconnected from overloaded MGs - MG_8, MG_9 and MG_{10}.

At time instant 4, the local loads of MG_2 and MG_3 are also increased to its rated capacity, but the power shortfall in MG_8, MG_9 and MG_{10} remains unchanged. Now DCPEH cannot supply power to MGs with power short fall and load shedding is the only measure to prevent system collapse. In short, when the maximum dispatchable power in DCPEH is less than the total power shortfall in microgrid cluster or when there is no surplus power available in DCPEH, load shedding should be initiated in the overloaded MGs.

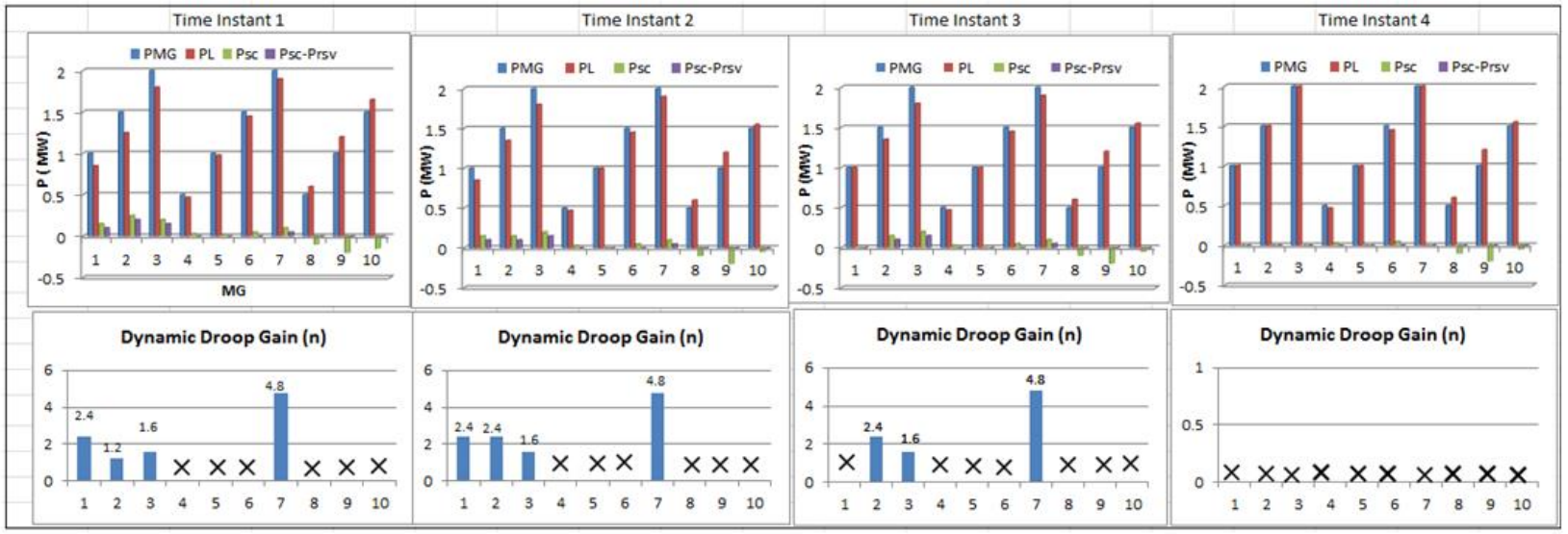


Figure 7.19: Power flow and dynamic droop gain selection in DCPEH with multiple MGs

Table 7.4: Power flow in DCPEH with multiple MGs

Time Instant	1				2				3				4			
	P_{MG}	P_L	P_{ref}	n	P_{MG}	P_L	P_{ref}	n	P_{MG}	P_L	P_{ref}	n	P_{MG}	P_L	P_{ref}	n
	MW	MW	MW		MW	MW	MW		MW	MW	MW		MW	MW	MW	
MG_1	1	0.85	0.1	2.4	1	0.85	0.1	2.4	1	1	0	×	1	1	0	×
MG_2	1.5	1.25	0.2	1.2	1.5	1.35	0.1	2.4	1.5	1.35	0.1	2.4	1.5	1.5	0	×
MG_3	2	1.8	0.15	1.6	2	1.8	0.15	1.6	2	1.8	0.15	1.6	2	2	0	×
MG_4	0.5	0.47	0	×	0.5	0.47	0	×	0.5	0.47	0	×	0.5	0.47	0	×
MG_5	1	1	0	×	1	1	0	×	1	1	0	×	1	1	0	×
MG_6	1.5	1.45	0	×	1.5	1.45	0	×	1.5	1.45	0	×	1.5	1.45	0	×
MG_7	2	1.9	0.05	4.8	2	1.9	0.05	4.8	2	1.9	0.05	4.8	2	2	0	×
MG_8	0.5	0.6	0	×	0.5	0.6	0	×	0.5	0.6	0	×	0.5	0.6	0	×
MG_9	1	1.2	0	×	1	1.2	0	×	1	1.2	0	×	1	1.2	0	×
MG_{10}	1.5	1.65	0	×	1.5	1.6	0	×	1.5	1.65	0	×	1.5	1.55	0	×

7.5 Conclusions

The interconnection of multiple MGs dominated by converter interfaced DERs through DCPEH is introduced in this chapter. The PFC integrated with individual MG establishes the coordinated power flow management by importing the surplus power of an MG to other interconnected MGs during power shortfall. In addition, the controller prevents overloading of any MGs under all operating conditions. Interconnection of MGs allows not only the maximum utilization of the generation capacity of individual DERs integrated in an MG, but also supports other MGs in case of any emergencies or faulty conditions. Furthermore, it reduces the power requirement from the grid at the point of common coupling. The improved resiliency and enhanced operational reliability of microgrid clusters during unpredictable conditions underpin its practice in future smart grids.

Chapter 8

Conclusions and Recommendations

The general conclusions of this thesis, as well as the scope for future research, are presented in this chapter.

8.1 Conclusions

The significant conclusions of this thesis are described as follows.

- The closed loop space vector pulse width modulation scheme can facilitate more effective DC link voltage utilization in LC filter fed voltage controlled grid converters in addition to the constant and reduced switching frequency operation. Filter characteristics incorporated design of CLSVPWM leads to a stable VSC operation, whereas the reduced switching frequency operation in traditional converters helps to decrease the total losses in the system.

- An accurate design of LCL filter parameters is crucial in grid converters to maintain the system stability in current controlled converters. Study on grid current regulated and converter current regulated systems show the impact of filter and controller parameters on overall system stability. Damping is

necessary for grid current regulated systems, whereas the proposed PRF controller can effectively eliminate the stability and delay effects in converter current regulated systems.

- High frequency SiC based converters are capable of overcoming the switching frequency limitation of traditional converters with reduced losses and power density. Output filter requirements can be drastically reduced in wide bandgap converters and even L filter can satisfy the filtering needs of VSC. But the analysis verifies the need for a small value filter capacitor to limit the voltage ripple in weak grid systems and grid converters with strict regulatory needs.

- In highly inductive MGs, eliminating output impedance effect from angle droop control helps to achieve the stability even with lower droop gains. In addition, an accurate reactive power distribution among DGs can also be achieved with the proposed droop control strategy, which is an unavoidable feature in converter dominated MGs.

- In strongly coupled remote microgrids, the introduction of power decoupling factor in droop control can facilitate the effective decoupling and distribution of real and reactive power demand among DERs. Since this strategy does not require additional communication needs and additional control loops for stability, complexity in droop mechanism is also avoided. The percentage error is significantly reduced in proposed scheme in comparison with existing schemes for strong coupled MGs.

- A virtual impedance scheme along with inverse angle droop control can effectively meet the active and imaginary power demand in resistive MGs, where feeding back an additional control variable can help to eliminate the error in real and reactive power sharing between DGs.

- Although harmonic interaction effects can be neglected in high frequency parallel connected converters, further measures are necessary to eliminate the controller interaction among them. Proposed control strategy helps to eliminate controller interaction in parallel grid converters and thereby eliminates circulating currents among VSCs and related stability issues.

- A small power rated DSTATCOM is preferred in islanded converter dominated MGs to maintain the voltage stability by providing the ancillary services such as reactive power support. A coordinated reactive power control algorithm can help a DSTATCOM to share the reactive power demand among other DGs so that the percentage drop in PCC voltage can be kept within certain limits specified by IEEE/IEC.

- Interconnecting neighbouring MGs is vital in future grid systems, where the resiliency of a remote MG can be achieved with suitable power management from other interconnected MGs. Proposed DCPEH concept along with advanced power flow controller can facilitate the bidirectional power flow in DCPEH to /satisfy/utilize the power shortfall/power surplus in interconnected MGs.

8.2 Future Research Scope

The recommendations for future research are described below.

- The stability issues and performance analysis of high frequency SiC based converters are analysed using computer simulations and a low power rated experimental prototype in this thesis. A DSP based processor has few performance limitations in analysing the attractive capabilities of wide bandgap converters. A high performance FPGA based processor can be considered

for implementing the fast acting control systems and the performance can be explored at high power ranges.

- In this thesis, microgrid consists of converter interfaced DERs are discussed. But in present MGs, a synchronous generator based DERs together with converter interfaced DERs form the power generation systems. This asymmetrical DER structure can be taken into account for power sharing strategy in remote microgrids.

- The advancement in battery energy storage and its management systems can provide necessary ancillary services to converter interfaced solar and wind energy systems. Although DSTATCOM can provide the ancillary services such as voltage stability and reactive power support to an MG as discussed in Chapter 6, the capability of DS to provide such services can be explored.

- Interconnecting AC microgrids with a DCPEH is discussed in this thesis. In current scenarios, the DC sources (solar) and DS are penetrating into markets which lead to AC-DC hybrid MGs. The possibility of directly connecting the DC energy sources to power exchange highway can be explored.

- Interconnecting multiple MGs is necessary for future to maintain the power system resiliency and efficiency. Individual MGs configuration may be different and similar MGs are considered in this thesis for verifying the power management strategy through DCPEH. Dissimilar MGs can be taken into account in future and the power system stability studies can also be considered to analyse the stability issues under steady state and transient conditions.

Appendix A

Publications from This Thesis

J1 B. John, A. Ghosh and F. Zare, *Load Sharing in Medium Voltage Islanded Microgrids with Advanced Angle Droop Control*, DOI 10.1109/TSG.2017.2713452, IEEE Trans. on Smart Grid.

J2 B. John, A. Ghosh, F. Zare and S. Rajakaruna, *Improved Control Strategy for Accurate Load Power Sharing in an Autonomous Microgrid*, DOI 10.1049/iet.gtd.2017.0499, Issue. 17, Vol. 11, pp. 4384-4390, IET Generation, Distribution and Transmission, Nov. 2017.

J3 B. John, A. Ghosh and F. Zare, *An Investigation on Filter Requirements and Stability Effects of Silicon Carbide MOSFET based High Frequency Grid Connected Converters*, Accepted for publication in The Journal of Engineering, 2018.

C1 M. Goyal, B. John, A. Ghosh, *Harmonic Mitigation in an Islanded Microgrid using a DSTATCOM*, IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Brisbane, Australia, Nov. 2015.

C2 B. John and A. Ghosh, *Control Loop Interaction in Parallel Connected High Frequency Grid Converters*, Australian Universities Power Engineering

Conference (AUPEC), Sep. 2016.

C3 B. John, A. Ghosh and F. Zare, *Droop Control in Low Voltage Islanded Microgrids for Sharing Nonlinear and Unbalanced Loads*, IEEE Region 10, TENSYMP, July. 2017.

C4 B. John, A. Ghosh and F. Zare, *An Investigation on Filter Requirements and Stability Effects of Silicon Carbide MOSFET based High Frequency Grid Connected Converters*, PEMD Conference, Liverpool, UK, April. 2018.

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